SCRETE SEMICONDUCTORS

PowerMOS Transistors

Data Handbook SC13
CD-ROM included
1999

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QUALITY ASSURED

Our quality system focuses on the continuing high quality of our components and the best possible service for our customers. We have a three-sided quality strategy: we apply a system of total quality control and assurance; we operate customer-oriented dynamic improvement programmes; and we promote a partnering relationship with our customers and suppliers.

PRODUCT SAFETY

In striving for state-of-the-art perfection, we continuously improve components and processes with respect to environmental demands. Our components offer no hazard to the environment in normal use when operated or stored within the limits specified in the data sheet.

Some components unavoidably contain substances that, if exposed by accident or misuse, are potentially hazardous to health. Users of these components are informed of the danger by warning notices in the data sheets supporting the components. Where necessary the warning notices also indicate safety precautions to be taken and disposal instructions to be followed. Obviously users of these components, in general the set-making industry, assume responsibility towards the consumer with respect to safety matters and environmental demands.

All used or obsolete components should be disposed of according to the regulations applying at the disposal location. Depending on the location, electronic components are considered to be 'chemical', 'special' or sometimes 'industrial' waste. Disposal as domestic waste is usually not permitted.

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PREFACE

Dear Customer

We are pleased to introduce this new Philips Semiconductors data handbook SC13. This data book contains a complete overview of the Philips Semiconductor product offering in small-signal, medium and high power MOS transistors for switching applications.

We would like to draw your attention to our extensive range of TrenchMOS products, setting new standards for low $R_{DS(ON)}$ performance and cost-effectiveness. Also of note are

- N- and P-Channel MOS transistors in a wide choice of surface mount and through-hole packages ranging from SOT323 and TSOP6 to SOT429 (TO247) and SO24.
- TOPFET, self protected power MOSFETs
- IGBT's

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POWERMOS SELECTION GUIDE

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25	0.01	25	75	142	PHB87N03LT	L2 TrenchMOS N	SOT404	1656
25	0.01	25	75	142	PHP87N03LT	L2 TrenchMOS N	SOT78	1656
25	0.014	25	69	125	PHB69N03LT	L2 TrenchMOS N	SOT404	1644
25	0.014	25	69	125	PHD69N03LT	L2 TrenchMOS N	SOT428	1644
25	0.014	25	69	125	PHP69N03LT	L2 TrenchMOS N	SOT78	1644
25	0.018	25	55	103	PHB55N03LT	L2 TrenchMOS N	SOT404	1626
25	0.018	25	55	103	PHD55N03LT	L2 TrenchMOS N	SOT428	1626
25	0.018	25	55	103	PHP55N03LT	L2 TrenchMOS N	SOT78	1626
25	0.021	25	48	86	PHB50N03LT	L2 TrenchMOS N	SOT404	1614
25	0.021	25	48	86	PHP50N03LT	L2 TrenchMOS N	SOT78	1614
25	0.021	25	48	86	PHD50N03LT	L2 TrenchMOS N	SOT428	1614
30	0.006	25	75	187	BUK7506-30	TrenchMOS N	SOT78	906
30	0.006	25	75	187	BUK7606-30	TrenchMOS N	SOT404	978
30	0.006	25	75	187	BUK9506-30	L2 TrenchMOS N	SOT78	1079
30	0.006	25	75	187	BUK9606-30	L2 TrenchMOS N	SOT404	1151
30	0.006	25	75	187	PHB130N03LT	L2 TrenchMOS N	SOT404	1682
30	0.006	25	75	187	PHP130N03LT	L2 TrenchMOS N	SOT78	1682
30	0.01	25	75	142	BUK7510-30	TrenchMOS N	SOT78	918
30	0.01	25	75	142	BUK7610-30	TrenchMOS N	SOT404	990
30	0.01	25	75	142	BUK9510-30	L2 TrenchMOS N	SOT78	1091
30	0.01	25	75	142	BUK9610-30	L2 TrenchMOS N	SOT404	1163
30	0.014	25	69	125	BUK7514-30	TrenchMOS N	SOT78	924
30	0.014	25	69	125	BUK7614-30	TrenchMOS N	SOT404	996
30	0.014	25	69	125	BUK9514-30	L2 TrenchMOS N	SOT78	1097
30	0.014	25	69	125	BUK9614-30	L2 TrenchMOS N	SOT404	1169
30	0.018	25	55	103	BUK7518-30	TrenchMOS N	SOT78	936
30	0.018	25	55	103	BUK7618-30	TrenchMOS N	SOT404	1008
30	0.018	25	55	103	BUK9518-30	L2 TrenchMOS N	SOT78	1109
30	0.018	25	55	103	BUK9618-30	L2 TrenchMOS N	SOT404	1181
30	0.024	25	45	86	PHB45N03LT	L2 TrenchMOS N	SOT404	1608
30	0.024	25	45	86	PHD45N03LT	L2 TrenchMOS N	SOT428	1608
30	0.024	25	45	86	PHP45N03LT	L2 TrenchMOS N	SOT78	1608
30	0.026	25	42	86	PHB42N03LT	L2 TrenchMOS N	SOT404	1596
30	0.026	25	42	86	PHP42N03LT	L2 TrenchMOS N	SOT78	1596
30	0.03	3.2	6	1.8	BUK7830-30	TrenchMOS N	SOT223	1050
30	0.03	3.2	6	1.8	BUK9830-30	L2 TrenchMOS N	SOT223	1229

V_{DS} (V)	$R_{DS(on)}$ (Ohm)	@I_D (A)	I_{Dmax} (A)	P_{Dmax} (W)	TYPE NUMBER	TECHNOLOGY	PACKAGE	PAGE
30	0.03	3.2	6	1.8	PHT6N03LT	L2 TrenchMOS N	SOT223	1725
30	0.056	25	24	60	PHB24N03LT	L2 TrenchMOS N	SOT404	1574
30	0.056	25	24	60	PHP24N03LT	L2 TrenchMOS N	SOT78	1574
48	0.02	20	52	116	BUK9120-48TC	Protected L2 TrenchMOS N	SOT426	1072
50	0.028	25	50	125	BUK106-50L	TOPFET	SOT263	447
50	0.028	25	50	125	BUK106-50LP	TOPFET	SOT263-01	447
50	0.028	25	50	125	BUK116-50L	TOPFET	SOT426	535
50	0.035	25	45	125	BUK102-50DL	TOPFET	TO220AB	419
50	0.035	25	45	125	BUK110-50DL	TOPFET	SOT404	507
50	0.035	25	45	125	BUK102-50GL	TOPFET	TO220AB	427
50	0.035	25	45	125	BUK110-50GL	TOPFET	SOT404	515
50	0.06	13	26	75	BUK101-50DL	TOPFET	TO220AB	402
50	0.06	13	26	75	BUK109-50DL	TOPFET	SOT404	490
50	0.06	13	26	75	BUK101-50GL	TOPFET	TO220AB	410
50	0.06	13	26	75	BUK109-50GL	TOPFET	SOT404	498
50	0.1	7.5	15	40	BUK104-50L	TOPFET	SOT263	436
50	0.1	7.5	15	40	BUK104-50LP	TOPFET	SOT263-01	436
50	0.1	7.5	15	40	BUK114-50L	TOPFET	SOT426	524
50	0.125	7.5	13.5	40	BUK100-50DL	TOPFET	TO220AB	385
50	0.125	7.5	13.5	40	BUK108-50DL	TOPFET	SOT404	473
50	0.125	7.5	13.5	40	BUK100-50GL	TOPFET	TO220AB	393
50	0.125	7.5	13.5	40	BUK108-50GL	TOPFET	SOT404	481
50	0.2	0.1	0.7	1.8	BUK107-50DL	TOPFET	SOT223	458
50	0.2	0.1	0.5	1.8	BUK107-50GL	TOPFET	SOT223	465
50	0.038	10	20	125	BUK202-50Y	TOPFET High side switch	SOT263-01	568
50	0.038	10	20	125	BUK206-50Y	TOPFET High side switch	SOT426	612
50	0.06	7.5	15	83.3	BUK201-50Y	TOPFET High side switch	SOT263-01	557
50	0.06	7.5	15	83.3	BUK205-50Y	TOPFET High side switch	SOT426	601
50	0.1	5	10	62.5	BUK200-50Y	TOPFET High side switch	SOT263-01	546
50	0.1	5	10	62.5	BUK204-50Y	TOPFET High side switch	SOT426	590
50	0.22	2	4	50	BUK203-50Y	TOPFET High side switch	SOT263-01	579

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50	0.22	2	4	50	BUK207-50Y	TOPFET High side switch	SOT426	623
55	0.008	25	75	187	BUK7508-55	TrenchMOS N	SOT78	912
55	0.008	25	75	187	BUK7608-55	TrenchMOS N	SOT404	984
55	0.008	25	75	187	BUK9508-55	L2 TrenchMOS N	SOT78	1085
55	0.008	25	75	187	BUK9608-55	L2 TrenchMOS N	SOT404	1157
55	0.008	25	75	250	PHB125N06LT	L2 TrenchMOS N	SOT404	1676
55	0.008	25	75	250	PHP125N06LT	L2 TrenchMOS N	SOT78	1676
55	0.014	25	68	142	BUK7514-55	TrenchMOS N	SOT78	930
55	0.014	25	68	142	BUK7614-55	TrenchMOS N	SOT404	1002
55	0.014	25	68	142	BUK9514-55	L2 TrenchMOS N	SOT78	1103
55	0.014	25	68	142	BUK9614-55	L2 TrenchMOS N	SOT404	1175
55	0.014	25	75	178	PHB80N06LT	L2 TrenchMOS N	SOT404	1650
55	0.014	25	75	178	PHP80N06LT	L2 TrenchMOS N	SOT78	1650
55	0.018	25	57	125	BUK7518-55	TrenchMOS N	SOT78	942
55	0.018	25	57	125	BUK7618-55	TrenchMOS N	SOT404	1014
55	0.018	25	57	125	BUK9518-55	L2 TrenchMOS N	SOT78	1115
55	0.018	25	57	125	BUK9618-55	L2 TrenchMOS N	SOT404	1187
55	0.018	25	63	150	PHB65N06LT	L2 TrenchMOS N	SOT404	1638
55	0.018	25	63	150	PHP65N06LT	L2 TrenchMOS N	SOT78	1638
55	0.02	25	52	116	BUK7520-55	TrenchMOS N	SOT78	948
55	0.02	25	52	116	BUK7620-55	TrenchMOS N	SOT404	1020
55	0.02	25	52	116	BUK9520-55	L2 TrenchMOS N	SOT78	1121
55	0.02	25	52	116	BUK9620-55	L2 TrenchMOS N	SOT404	1193
55	0.02	25	58	150	PHB60N06LT	L2 TrenchMOS N	SOT404	1632
55	0.02	25	58	150	PHP60N06LT	L2 TrenchMOS N	SOT78	1632
55	0.024	25	45	103	BUK7524-55	TrenchMOS N	SOT78	954
55	0.024	25	45	103	BUK7624-55	TrenchMOS N	SOT404	1026
55	0.024	25	45	103	BUK9524-55	L2 TrenchMOS N	SOT78	1127
55	0.024	25	45	103	BUK9624-55	L2 TrenchMOS N	SOT404	1199
55	0.024	25	50	125	PHB50N06LT	L2 TrenchMOS N	SOT404	1620
55	0.024	25	50	125	PHP50N06LT	L2 TrenchMOS N	SOT78	1620
55	0.028	20	40	96	BUK7528-55	TrenchMOS N	SOT78	960
55	0.028	20	40	96	BUK7628-55	TrenchMOS N	SOT404	1032
55	0.028	20	40	96	BUK9528-55	L2 TrenchMOS N	SOT78	1133
55	0.028	20	40	96	BUK9628-55	L2 TrenchMOS N	SOT404	1205
55	0.028	20	44	114	PHB44N06LT	L2 TrenchMOS N	SOT404	1602
55	0.028	20	44	114	PHP44N06LT	L2 TrenchMOS N	SOT78	1602
55	0.035	17	34	85	BUK7535-55	TrenchMOS N	SOT78	966

V_{DS} (V)	$R_{DS(on)}$ (Ohm)	@I_D (A)	I_{Dmax} (A)	P_{Dmax} (W)	TYPE NUMBER	TECHNOLOGY	PACKAGE	PAGE
55	0.035	17	34	85	BUK7635-55	TrenchMOS N	SOT404	1038
55	0.035	17	34	85	BUK9535-55	L2 TrenchMOS N	SOT78	1139
55	0.035	17	34	85	BUK9635-55	L2 TrenchMOS N	SOT404	1211
55	0.035	17	37	100	PHB37N06LT	L2 TrenchMOS N	SOT404	1590
55	0.035	17	37	100	PHP37N06LT	L2 TrenchMOS N	SOT78	1590
55	0.04	5	10.7	1.8	BUK7840-55	TrenchMOS N	SOT223	1058
55	0.04	5	10.7	1.8	BUK9840-55	L2 TrenchMOS N	SOT223	1237
55	0.04	5	10.7	1.8	PHT11N06LT	L2 TrenchMOS N	SOT223	1745
55	0.075	10	19.7	61	BUK7575-55	TrenchMOS N	SOT78	972
55	0.075	10	19.7	61	BUK7675-55	TrenchMOS N	SOT404	1044
55	0.075	10	19.7	61	BUK9575-55	L2 TrenchMOS N	SOT78	1145
55	0.075	10	19.7	61	BUK9675-55	L2 TrenchMOS N	SOT404	1217
55	0.075	7	11.7	19	BUK9775-55	L2 TrenchMOS N	SOT186A	1223
55	0.075	10	21	69	PHB21N06LT	L2 TrenchMOS N	SOT404	1568
55	0.075	10	21	69	PHP21N06LT	L2 TrenchMOS N	SOT78	1568
55	0.08	5	7.5	1.8	BUK7880-55	TrenchMOS N	SOT223	1065
55	0.08	5	7.5	1.8	BUK9880-55	L2 TrenchMOS N	SOT223	1244
55	0.08	5	7.5	1.8	PHT8N06LT	L2 TrenchMOS N	SOT223	1738
55	0.15	5	5.5	1.8	BUK78150-55	TrenchMOS N	SOT223	1251
55	0.15	5	5.5	1.8	BUK98150-55	L2 TrenchMOS N	SOT223	1258
55	0.15	5	5.5	1.8	PHT6N06LT	L2 TrenchMOS N	SOT223	1731
60	0.15	6	12	50	PHD3055E	MOSFET N	SOT428	1333
60	0.15	6	12	50	PHP3055E	MOSFET N	SOT78	1715
60	0.18	6	12	50	PHD3055L	L2FET N	SOT428	1338
60	0.18	6	12	50	PHP3055L	L2FET N	SOT78	1720
100	0.057	15	34	150	BUK456-100A	MOSFET N	SOT78	709
100	0.057	15	34	150	BUK466-100A	MOSFET N	SOT404	754
100	0.057	17	34	175	PHP33N10	MOSFET N	SOT78	1585
100	0.08	13	26	125	BUK455-100A	MOSFET N	SOT78	699
100	0.08	13	26	125	BUK465-100A	MOSFET N	SOT404	744
100	0.08	17	26	125	PHP26N10E	MOSFET N	SOT78	1580
100	0.085	13	13	30	BUK545-100A	L2FET N	SOT186	807
100	0.085	13	25	125	BUK555-100A	L2FET N	SOT78	837
100	0.085	13	25	125	BUK565-100A	L2FET N	SOT404	862
100	0.1	13	23	125	BUK455-100B	MOSFET N	SOT78	699
100	0.11	13	12	30	BUK545-100B	L2FET N	SOT186	807
100	0.11	13	22	125	BUK555-100B	L2FET N	SOT78	837

V_{DS} (V)	$R_{DS(on)}$ (Ohm)	@I_D (A)	I_{Dmax} (A)	P_{Dmax} (W)	TYPE NUMBER	TECHNOLOGY	PACKAGE	PAGE
100	0.16	5	14	75	BUK453-100A	MOSFET N	SOT78	684
100	0.16	5	14	75	BUK463-100A	MOSFET N	SOT404	734
100	0.16	5	9	25	BUK473-100A	MOSFET N	SOT186A	769
100	0.16	5	14	75	PHD12N10E	MOSFET N	SOT428	1328
100	0.16	5	14	75	PHP12N10E	MOSFET N	SOT78	1555
100	0.18	5	8.3	25	BUK543-100A	L2FET N	SOT186	802
100	0.18	6.5	13	75	BUK553-100A	L2FET N	SOT78	827
100	0.18	6.5	13	75	BUK563-100A	L2FET N	SOT404	852
100	0.2	5	13	75	BUK453-100B	MOSFET N	SOT78	684
100	0.2	5	8	25	BUK473-100B	MOSFET N	SOT186A	769
100	0.22	6.5	12	75	BUK553-100B	L2FET N	SOT78	827
100	0.25	5.5	11	60	BUK462-100A	MOSFET N	SOT404	729
100	0.25	5.5	11	60	BUK452-100A	MOSFET N	SOT78	679
100	0.25	5.5	6.6	22	BUK472-100A	MOSFET N	SOT186A	764
100	0.25	5.5	11	60	PHD10N10E	MOSFET N	SOT428	1323
100	0.25	5.5	11	60	PHP10N10E	MOSFET N	SOT78	1539
100	0.28	1.8	1.8	1.8	BUK482-100A	MOSFET N	SOT223	790
100	0.28	5.5	10	60	BUK552-100A	L2FET N	SOT78	822
100	0.3	5.5	10	60	BUK452-100B	MOSFET N	SOT78	679
100	0.3	5.5	6.1	22	BUK472-100B	MOSFET N	SOT186A	764
100	0.31	1.7	1.7	1.8	BUK582-100A	L2FET N	SOT223	878
100	0.35	5.5	8.5	60	BUK552-100B	L2FET N	SOT78	822
100	0.54	3.4	6.3	50	PHD6N10E	MOSFET N	SOT428	1318
100	0.54	3.4	6.3	50	PHP6N10E	MOSFET N	SOT78	1481
100	0.8	1	1	1.5	BUK481-100A	MOSFET N	SOT223	784
100	0.9	0.9	0.9	1.5	BUK581-100A	L2FET N	SOT223	872
200	0.16	10	19	125	BUK436W-200A	MOSFET N	SOT429	634
200	0.16	10	19	150	BUK456-200A	MOSFET N	SOT78	714
200	0.16	10	19	150	BUK466-200A	MOSFET N	SOT404	759
200	0.18	11	18	150	PHP18N20E	MOSFET N	SOT78	1563
200	0.2	10	17	125	BUK436W-200B	MOSFET N	SOT429	634
200	0.2	10	17	150	BUK456-200B	MOSFET N	SOT78	714
200	0.23	7	7.6	30	BUK445-200A	MOSFET N	SOT186	664
200	0.23	7	14	125	BUK455-200A	MOSFET N	SOT78	704
200	0.23	7	14	125	BUK465-200A	MOSFET N	SOT404	749
200	0.23	7	7.6	30	BUK475-200A	MOSFET N	SOT186A	779
200	0.23	7	7.6	30	BUK545-200A	L2FET N	SOT186	812
200	0.23	7	14	125	BUK555-200A	L2FET N	SOT78	842

V_{DS} (V)	$R_{DS(on)}$ (Ohm)	@I_D (A)	I_{Dmax} (A)	P_{Dmax} (W)	TYPE NUMBER	TECHNOLOGY	PACKAGE	PAGE
200	0.23	7	14	125	BUK565-200A	L2FET N	SOT404	867
200	0.28	7	7	30	BUK445-200B	MOSFET N	SOT186	664
200	0.28	7	13	125	BUK455-200B	MOSFET N	SOT78	704
200	0.28	7	7	30	BUK475-200B	MOSFET N	SOT186A	779
200	0.28	7	7	30	BUK545-200B	L2FET N	SOT186	812
200	0.28	7	13	125	BUK555-200B	L2FET N	SOT78	842
200	0.4	3.5	5.3	25	BUK444-200A	MOSFET N	SOT186	654
200	0.4	3.5	9.2	90	BUK454-200A	MOSFET N	SOT78	689
200	0.4	3.5	9.2	90	BUK464-200A	MOSFET N	SOT404	739
200	0.4	3.5	5.3	25	BUK474-200A	MOSFET N	SOT186A	774
200	0.4	3.5	9.2	90	BUK554-200A	L2FET N	SOT78	832
200	0.4	3.5	9.2	90	BUK564-200A	L2FET N	SOT404	857
200	0.4	6.4	9.2	90	PHP8N20E	MOSFET N	SOT78	1518
200	0.5	3.5	4.7	25	BUK444-200B	MOSFET N	SOT186	654
200	0.5	3.5	8.2	90	BUK454-200B	MOSFET N	SOT78	689
200	0.5	3.5	4.7	25	BUK474-200B	MOSFET N	SOT186A	774
200	0.5	3.5	8.2	90	BUK554-200B	L2FET N	SOT78	832
200	0.9	2	2	8.3	BUK482-200A	MOSFET N	SOT223	796
200	0.9	2.5	5	60	PHD5N20E	MOSFET N	SOT428	1313
200	0.9	2.5	5	60	PHP5N20E	MOSFET N	SOT78	1313
200	1.5	2	3.5	50	PHD3N20E	MOSFET N	SOT428	1303
200	1.5	2	3.5	50	PHD3N20L	L2FET N	SOT428	1308
200	1.5	2	3.5	50	PHP3N20E	MOSFET N	SOT78	1303
200	1.5	2	3.5	50	PHP3N20L	L2FET N	SOT78	1308
400	0.4	6.4	12.8	156	PHB13N40E	MOSFET N	SOT404	1560
400	0.4	6.4	12.8	156	PHP13N40E	MOSFET N	SOT78	1560
400	0.4	6.4	12.8	156	PHW13N40E	MOSFET N	SOT429	1560
400	0.55	5.3	10.6	147	PHB10N40E	MOSFET N	SOT404	1544
400	0.55	5.3	10.6	147	PHP10N40E	MOSFET N	SOT78	1544
400	0.55	5.3	10.6	147	PHW10N40E	MOSFET N	SOT429	1544
400	0.55	5.3	5.3	37	PHX10N40E	MOSFET N	SOT186A	1854
400	1	3.6	7.2	125	PHB7N40E	MOSFET N	SOT404	1506
400	1	3.6	7.2	125	PHP7N40E	MOSFET N	SOT78	1506
400	1	3.6	3.8	35	PHX7N40E	MOSFET N	SOT186A	1830
400	1.8	2.2	4.4	83	PHB4N40E	MOSFET N	SOT404	1458
400	1.8	2.2	4.4	83	PHP4N40E	MOSFET N	SOT78	1458
400	1.8	2.2	2.7	30	PHX4N40E	MOSFET N	SOT186A	1791
400	1.8	2.2	4.4	83	PHB4ND40E	MOSFET N	SOT404	1470

V_{DS} (V)	$R_{DS(on)}$ (Ohm)	@I_D (A)	I_{Dmax} (A)	P_{Dmax} (W)	TYPE NUMBER	TECHNOLOGY	PACKAGE	PAGE
400	1.8	2.2	4.4	83	PHP4ND40E	MOSFET N	SOT78	1470
400	1.8	2.2	2.7	30	PHX4ND40E	MOSFET N	SOT186A	1803
400	3.5	1.25	2.5	50	PHB3N40E	MOSFET N	SOT404	1440
400	3.5	1.25	2.5	50	PHD3N40E	MOSFET N	SOT428	1440
400	3.5	1.25	2.5	50	PHP3N40E	MOSFET N	SOT78	1440
400	3.5	1.25	1.7	25	PHX3N40E	MOSFET N	SOT186A	1473
500	0.27	10	20	250	PHW20N50E	MOSFET N	SOT429	1759
500	0.4	7	14	192	PHW14N50E	MOSFET N	SOT429	1757
500	0.6	5.2	10.4	156	PHB11N50E	MOSFET N	SOT404	1552
500	0.6	5.2	10.4	156	PHP11N50E	MOSFET N	SOT78	1552
500	0.6	5.2	10.4	156	PHW11N50E	MOSFET N	SOT429	1552
500	0.85	4.8	8.5	147	PHB8N50E	MOSFET N	SOT404	1523
500	0.85	4.8	8.5	147	PHP8N50E	MOSFET N	SOT78	1523
500	0.85	4.8	8.5	147	PHW8N50E	MOSFET N	SOT429	1523
500	0.85	4.8	4.2	37	PHX8N50E	MOSFET N	SOT186A	1842
500	0.85	4.8	8.5	147	PHB8ND50E	MOSFET N	SOT404	1529
500	0.85	4.8	8.5	147	PHP8ND50E	MOSFET N	SOT78	1529
500	0.85	4.8	8.5	147	PHW8ND50E	MOSFET N	SOT429	1529
500	0.85	4.8	4.2	37	PHX8ND50E	MOSFET N	SOT186A	1848
500	1.5	3	5.9	125	PHB6N50E	MOSFET N	SOT404	1486
500	1.5	3	5.9	125	PHP6N50E	MOSFET N	SOT78	1486
500	1.5	3	3.1	35	PHX6N50E	MOSFET N	SOT186A	1809
500	1.5	3	5.9	125	PHB6ND50E	MOSFET N	SOT404	1492
500	1.5	3	5.9	125	PHP6ND50E	MOSFET N	SOT78	1492
500	1.5	3	3.1	35	PHX6ND50E	MOSFET N	SOT186A	1824
500	3	1.7	3.4	83	PHB3N50E	MOSFET N	SOT404	1446
500	3	1.7	3.4	83	PHP3N50E	MOSFET N	SOT78	1446
500	3	1.7	2.1	30	PHX3N50E	MOSFET N	SOT186A	1779
500	5	1	2	50	PHB2N50E	MOSFET N	SOT404	1418
500	5	1	2	50	PHD2N50E	MOSFET N	SOT428	1418
500	5	1	2	50	PHP2N50E	MOSFET N	SOT78	1418
500	5	1	1.4	25	PHX2N50E	MOSFET N	SOT186A	1761
600	0.75	4.4	10	156	PHP10N60E	MOSFET N	SOT78	1550
600	0.85	4.4	8.7	156	PHB9N60E	MOSFET N	SOT404	1512
600	0.85	4.4	8.7	156	PHW9N60E	MOSFET N	SOT429	1535
600	1.2	3.25	6.5	125	PHP6NA60E	Low Capacitance MOSFET N	SOT78	1504

V_{DS} (V)	$R_{DS(on)}$ (Ohm)	@I_D (A)	I_{Dmax} (A)	P_{Dmax} (W)	TYPE NUMBER	TECHNOLOGY	PACKAGE	PAGE
600	1.2	3.25	3.9	45	PHX6NA60E	Low Capacitance MOSFET N	SOT186A	1821
600	1.2	3.5	7	147	PHB7N60E	MOSFET N	SOT404	1512
600	1.2	3.5	7	147	PHP7N60E	MOSFET N	SOT78	1512
600	1.2	3.5	7	147	PHW7N60	MOSFET N	SOT429	1752
600	1.2	3.5	3.6	37	PHX7N60E	MOSFET N	SOT186A	1836
600	1.8	2.7	5.4	125	PHB6N60E	MOSFET N	SOT404	1498
600	1.8	2.7	5.4	125	PHP6N60E	MOSFET N	SOT78	1498
600	1.8	2.7	2.8	35	PHX6N60E	MOSFET N	SOT186A	1815
600	2.5	2.25	4.5	125	PHB4N60E	MOSFET N	SOT404	1464
600	2.5	2.25	4.5	125	PHP4N60E	MOSFET N	SOT78	1464
600	2.5	2.25	2.4	35	PHX4N60E	MOSFET N	SOT186A	1797
600	4.4	1.4	2.8	83	PHB3N60E	MOSFET N	SOT404	1452
600	4.4	1.4	2.8	83	PHP3N60E	MOSFET N	SOT78	1452
600	4.4	1.4	1.7	30	PHX3N60E	MOSFET N	SOT186A	1785
600	6	1	1.9	50	PHB2N60E	MOSFET N	SOT404	1424
600	6	1	1.9	50	PHD2N60E	MOSFET N	SOT428	1424
600	6	1	1.9	50	PHP2N60E	MOSFET N	SOT78	1424
600	6	1	1.3	25	PHX2N60E	MOSFET N	SOT186A	1767
800	1.5	4	7.6	220	BUK438W-800A	MOSFET N	SOT429	649
800	2	4	6.6	220	BUK438W-800B	MOSFET N	SOT429	649
800	3	1.5	4	125	BUK436W-800A	MOSFET N	SOT429	639
800	3	1.5	2	30	BUK446-800A	MOSFET N	SOT186	669
800	3	1.5	4	125	BUK456-800A	MOSFET N	SOT78	719
800	4	1.5	3.5	125	BUK436W-800B	MOSFET N	SOT429	649
800	4	1.5	1.7	30	BUK446-800B	MOSFET N	SOT186	669
800	4	1.5	3.5	125	BUK456-800B	MOSFET N	SOT78	719
800	6	1	1.4	30	BUK444-800A	MOSFET N	SOT186	659
800	6	1	2.4	100	BUK454-800A	MOSFET N	SOT78	694
800	8	1	1.2	30	BUK444-800B	MOSFET N	SOT186	659
800	8	1	2	100	BUK454-800B	MOSFET N	SOT78	694
1000	5	1.5	3.1	125	BUK436W-1000B	MOSFET N	SOT429	644
1000	5	1.5	1.5	30	BUK446-1000B	MOSFET N	SOT186	674
1000	5	1.5	3.1	125	BUK456-1000B	MOSFET N	SOT78	724

N-CHANNEL MOS-FETS

TYPE NUMBER	PACKAGE	RATINGS			CHARACTERISTICS						PAGE
		V_{DS} (V)	I_D (mA)	P_{tot} (mW)	V_{GSth} (V)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	at I_D (mA)	at V_{GS} (V)	t_{on}/t_{off} max. (ns)	
BS107	SOT54/TO-92var	200	150	830	0.8 to 2.4	20	28	20	2.6	10/20	60
BS107A[1]	SOT54/TO-92	200	250	600	1 to 3	4.5	6.4	250	10	5/15	66
BS108	SOT54/TO-92	200	250	1000	0.4 to 1.8	5	8	100	2.8	10/30	70
BS170[1]	SOT54/TO-92var	60	500	830	0.8 to 3	2.5	5	200	10	10/10	73
BSH101[1]	SOT23	60	700	500	1[2]	–	0.6	350	10	7/13.5[3]	79
BSH102[1]	SOT23	30	850	500	1[2]	–	0.4	500	10	7.5/11[3]	86
BSH103[1]	SOT23	30	850	500	0.4[2]	–	0.5	500	2.5	6/27[3]	93
BSH105[1]	SOT23	20	1210	500	0.4[2]	–	0.25	600	2.5	6.5/65[3]	100
BSH106[1]	SOT363	20	1430	700	0.4[2]	–	0.25	700	2.5	6.5/65[3]	103
BSH107	SOT457 (TSOP6)	20	2500	800	0.4[2]	–	0.09	1200	2.5	–	106
BSN10[1]	SOT54/TO-92	50	175	830	0.4 to 1.8	8	15	100	10	5/10	137
BSN10A[1]	SOT54/TO-92	50	175	830	0.4 to 1.8	8	15	100	10	5/10	137
BSN20[1]	SOT23	50	100	250	0.4 to 1.8	8	15	100	10	5/10	141
BSN20W[1]	SOT323	50	80	200	0.4 to 1.8	8	15	80	10	5/10	148
BSN205[1]	SOT54/TO-92var	200	300	1000	0.8 to 2.8	4	6	400	10	10/20	145
BSN205A[1]	SOT54/TO-92var	200	300	1000	0.8 to 2.8	4	6	400	10	10/20	145
BSN254[1]	SOT54/TO-92var	250	300	1000	0.8 to 2	5	10	20	2.4	10/30	152
BSN254A[1]	SOT54/TO-92var	250	300	1000	0.8 to 2	5	10	20	2.4	10/30	152
BSN274	SOT54/TO-92var	270	250	1000	0.8 to 2	9	14	20	2.4	10/30	157
BSN274A	SOT54/TO-92var	270	250	1000	0.8 to 2	9	14	20	2.4	10/30	157
BSN304[1]	SOT54/TO-92var	300	250	1000	0.8 to 2	7.9	14	20	2.4	10/30	160
BSN304A[1]	SOT54/TO-92var	300	250	1000	0.8 to 2	7.9	14	20	2.4	10/30	160
BSP030	SOT223	30	10000	5000	1 to 2.8	–	0.03	5000	10	60/150	166
BSP89	SOT223	240	350	1500	0.8 to 2	4	6	340	10	10/30	295
BSP100[1]	SOT223	30	3500	5000	1 to 2.8	0.08	0.1	2200	10	40/75	180
BSP106	SOT223	60	425	1500	0.8 to 3	2.5	4	200	10	5/15	186
BSP107	SOT223	200	200	1500	0.8 to 2.4	20	28	20	2.6	10/20	192
BSP108	SOT223	80	500	1500	1.5 to 3.5	2	3	500	10	8/15	198
BSP110[1]	SOT223	80	325	1500	0.8 to 2.8	7	10	150	5	5/10	203
BSP120	SOT223	200	250	1500	0.8 to 2.8	7	12	250	10	6/20	208
BSP121[1]	SOT223	200	350	1500	0.8 to 2.8	4.5	6	400	10	10/20	213
BSP122	SOT223	200	550	1500	0.4 to 2	1.6	2.5	750	10	35/50	219
BSP126[1]	SOT223	250	350	1500	0.8 to 2	5	10	20	2.4	10/30	221
BSP127	SOT223	270	350	1500	0.8 to 2	6.5	8	250	10	10/30	226
BSP128	SOT223	200	350	1500	0.4 to 1.8	5	8	100	2.8	10/30	228
BSP130[1]	SOT223	300	300	1500	0.8 to 2	6.7	8	250	10	10/30	230

TYPE NUMBER	PACKAGE	RATINGS			CHARACTERISTICS						PAGE
		V_{DS} (V)	I_D (mA)	P_{tot} (mW)	V_{GSth} (V)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	at I_D (mA)	at V_{GS} (V)	t_{on}/t_{off} max. (ns)	
BSS87[1]	SOT89	200	280	1000	0.8 to 2.8	4.5	6	400	10	10/25	306
BSS89[1]	SOT54/TO-92var	200	300	1000	0.8 to 2.8	4.5	6	400	10	5/15[3]	309
BSS123[1]	SOT23	100	150	250	0.8 to 2.8	3	6	120	10	10/20	315
BST70A	SOT54/TO-92var	80	500	1000	1.5 to 3.5	2	4	500	10	10/15	324
BST72A[1]	SOT54/TO-92var	80	300	830	1.5 to 3.5	7	10	150	5	10/10	330
BST74A	SOT54/TO-92var	200	250	1000	0.8 to 2.8	6	12	250	10	10/25	336
BST76A	SOT54/TO-92var	180	300	1000	0.7 to 2.4	7	10	15	3	10/15	342
BST80	SOT89	80	500	1000	1.5 to 3.5	2	3	500	10	10/15	347
BST82[1]	SOT23	80	175	300	1.5 to 3.5	7	10	150	5	10/10	352
BST84	SOT89	200	250	1000	0.8 to 2.8	6	12	250	10	10/25	358
BST86	SOT89	180	300	1000	0.7 to 2.7	7	10	15	3	10/15	364
PHN103	SOT96-1 (SO8)	30	8500	4000	1 to 2.8	–	0.03	5500	10	35/150	1343
PHN110[1]	SOT96-1 (SO8)	30	4000	2800	1 to 2.8	0.08	0.1	2000	10	16/50	1351
PHN203[4]	SOT96-1 (SO8)	30	8200	3500	1[2]	–	0.03	4000	10	25/60	1358
PHN205[1][4]	SOT96-1 (SO8)	30	6400	3500	1 to 2.8	–	0.05	3200	10	15/32[3]	1361
PHN210[1][4]	SOT96-1 (SO8)	30	3500	2000	1 to 2.8	0.08	0.1	2200	10	40/140	1368
PHN405[5]	SOT338-1 (SSOP16)	30	3700	1400	1 to 2.8	–	0.06	2000	10	10/30	1375
PHN603S[6]	SOT137-1 (SO24)	30	5000	2000	1[2]	–	0.03	5000	10	25/60	1383
PHN708[7]	SOT340-1 (SSOP24)	30	3100	1300	1 to 2.8	–	0.08	1500	10	10/25	1390
PHN1011	SOT96-1 (SO8)	25	11000	2500	1 to 2[8]	0.009	0.011	5000	5	82/230[3]	1398
PHN1013	SOT96-1 (SO8)	30	11000	2500	2.1 to 4[8]	0.011	0.0135	10000	10	165/180[3]	1403
PHN1015	SOT96-1 (SO8)	25	9000	1600	1 to 2	0.009	0.013	10000	10	120/200	1408
PHN1018	SOT96-1 (SO8)	25	8700	1600	1 to 2	0.013	0.018	10000	10	95/120	1413
PMBF107	SOT23	200	100	250	0.8 to 2.4	20	28	20	2.6	10/20	1860
PMBF170[1]	SOT23	60	250	300	0.8 to 3	2.5	5	200	10	10/15	1865
2N7000[1]	SOT54/TO-92var	60	280	830	0.8 to 3	3.5	5.3	75	4.5	10/10	48
2N7002[1]	SOT23	60	180	300	0.8 to 3	3.5	5.3	75	4.5	10/15	54

Notes

1. Data on spice parameters is available on SC13 CD-ROM.
2. Minimum value.
3. Typical values.
4. Dual FET.
5. 4 - FET array.
6. 6 - FET/Schottky array.
7. 7 - FET array.
8. V_{GSth} at I_D = 250 μA instead of 1 mA.

P-CHANNEL MOS-FETS

TYPE NUMBER	PACKAGE	RATINGS			CHARACTERISTICS						PAGE
		V_{DS} (V)	I_D (mA)	P_{tot} (mW)	V_{GSth} (V)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	at I_D (mA)	at V_{GS} (V)	t_{on}/t_{off} max. (ns)	
BS250[1]	SOT54/TO-92var	45	250	830	1 to 3.5	9	14	200	10	4/10	76
BSH201	SOT23	60	340	500	1[2]	–	2.5	160	10	–	109
BSH202	SOT23	30	570	500	1[2]	–	0.9	280	10	5/29[3]	112
BSH203	SOT23	30	570	500	0.4[2]	–	1.1	280	2.5	4.5/45[3]	119
BSH205	SOT23	12	860	500	0.4[2]	–	0.5	430	2.5	5/170[3]	122
BSH206	SOT363	12	1000	700	0.4[2]	–	0.5	500	2.5	5/170[3]	125
BSH207	SOT457(TSOP6)	12	2000	800	0.4[2]	–	0.15	1000	2.5	–	128
BSH299[1]	SOT363	50	200	700	0.8 to 2	–	10	130	10	3/7[3]	131
BSP090	SOT223	30	5700	5000	1 to 2.8	–	0.09	2800	10	25/190	173
BSP92[1]	SOT223	240	180	1500	0.8 to 2	10	20	180	10	10/30	298
BSP204[1]	SOT54/TO-92var	200	250	1000	0.8 to 2.8	10	15	200	10	10/30	236
BSP204A[1]	SOT54/TO-92var	200	250	1000	0.8 to 2.8	10	15	200	10	10/30	236
BSP205[1]	SOT223	60	275	1500	1.5 to 3.5	7.5	10	200	10	6/15	242
BSP206[1]	SOT223	60	350	1500	1.5 to 3.5	4.5	6	200	10	8/25	248
BSP220	SOT223	200	225	1500	0.8 to 2.8	10	12	200	10	20/30	253
BSP225[1]	SOT223	250	225	1500	0.8 to 2.8	10	15	200	10	10/30	259
BSP230[1]	SOT223	300	210	1500	1.95 to 2.8	–	17	170	10	10/30	265
BSP250[1]	SOT223	30	3000	5000	1 to 2.8	0.22	0.25	1000	10	80/140	271
BSP254[1]	SOT54/TO-92var	250	200	1000	0.8 to 2.8	10	15	200	10	10/30	277
BSP254A[1]	SOT54/TO-92var	250	200	1000	0.8 to 2.8	10	15	200	10	10/30	27
BSP255	SOT223	300	325	4000	0.8 to 2	–	17	160	10	4/25[3]	282
BSP304[1]	SOT54/TO-92var	300	170	1000	1.95 to 2.8	–	17	170	10	10/30	289
BSP304A[1]	SOT54/TO-92var	300	170	1000	1.95 to 2.8	–	17	170	10	10/30	289
BSS84[1]	SOT23	50	130	250	0.8 to 2	–	10	130	10	3/7[3]	301
BSS92[1]	SOT54/TO-92var	240	150	1000	0.8 to 2.8	10	20	100	10	5/20[3]	312
BSS192[1]	SOT89	240	150	1000	0.8 to 2.8	10	20	100	10	10/30	319
BST100[1]	SOT54/TO-92var	60	300	1000	1.5 to 3.5	4.5	6	200	10	4/20[3]	370
BST120[1]	SOT89	60	300	1000	1.5 to 3.5	4.5	6	200	10	4/20[3]	375
BST122[1]	SOT89	60	250	1000	1.5 to 3.5	7.5	10	200	10	4/10[3]	380
PHP109[1]	SOT96-1 (SO8)	30	5000	4000	1 to 2.8	–	0.09	2500	10	35/200	1662
PHP125[1]	SOT96-1 (SO8)	30	2500	2800	1 to 2.8	0.22	0.25	1000	10	16/80	1669
PHP206[4]	SOT96-1 (SO8)	30	5600	3500	1[2]	–	0.065	2800	10	–	1688
PHP212[1][4]	SOT96-1 (SO8)	30	4000	3500	1 to 2.8	–	0.12	2000	10	10/45[3]	1691
PHP222[4]	SOT96-1 (SO8)	30	3200	3500	0.4[2]	–	0.22	1600	2.5	7.5/125[3]	1691

TYPE NUMBER	PACKAGE	RATINGS			CHARACTERISTICS						PAGE
		V_{DS} (V)	I_D (mA)	P_{tot} (mW)	V_{GSth} (V)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	at I_D (mA)	at V_{GS} (V)	t_{on}/t_{off} max. (ns)	
PHP225[1][4]	SOT96-1 (SO8)	30	2300	2000	1 to 2.8	0.22	0.25	1000	10	80/140	1702
PHP1025	SOT96-1 (SO8)	12	10000	4000	0.4[2]	–	0.025	5000	2.5	–	1709
PHP1035	SOT96-1 (SO8)	30	8000	4000	1[2]	–	0.035	4000	10	–	1712

Notes

1. Data on spice parameters is available on SC13 CD-ROM.
2. Minimum value.
3. Typical values.
4. Dual FET.

N-CHANNEL / P-CHANNEL / COMPLEMENTARY MULTI-CHIP POWERMOS

TYPE NUMBER	PACKAGE	CHANNEL	RATINGS			CHARACTERISTICS						PAGE
			V_{DS} (V)	I_D (mA)	P_{tot} (mW)	V_{GSth} (V)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	at I_D (mA)	at V_{GS} (V)	t_{on}/t_{off} max. (ns)	
PHC2300	SOT96-1 (SO8)	N[1]	300	340	1600	0.8 to 2	–	8	175	10	10/30	1265
		P	300	235	1600	0.8 to 2	–	17	115	10	10/35	1265
PHC20306	SOT96-1 (SO8)	N	30	8200	3500	1[2]	–	0.03	4000	10	25/60	1276
		P	30	5600	3500	1[2]	–	0.065	2800	10	–	1276
PHC20512[1]	SOT96-1 (SO8)	N	30	6400	3500	1 to 2.8	–	0.05	3200	10	15/32[3]	1280
		P	30	4000	3500	1 to 2.8	–	0.12	2000	10	10/45[3]	1280
PHC21025[1]	SOT96-1 (SO8)	N	30	3500	2000	1 to 2.8	0.08	0.1	2200	10	40/140	1293
		P	30	2300	2000	1 to 2.8	0.22	0.25	1000	10	80/140	1293

Notes

1. Data on spice parameters is available on SC13 CD-ROM.
2. Minimum values.
3. Typical values.

Types in SOT23, SOT89, and SOT323 packages are marked with a code as listed in the following table.

TYPE NUMBER	MARKING CODE
BSN20	M8p
BSN20W	M8t
BSS84	SP
BSS87	KA
BSS123	SA
BSS192	KB
BST80	KM
BST82	02p
BST84	KN
BST86	KO
BST120	LM
BST122	LN
PMBF107	pKz
PMBF170	pKX
2N7002	702

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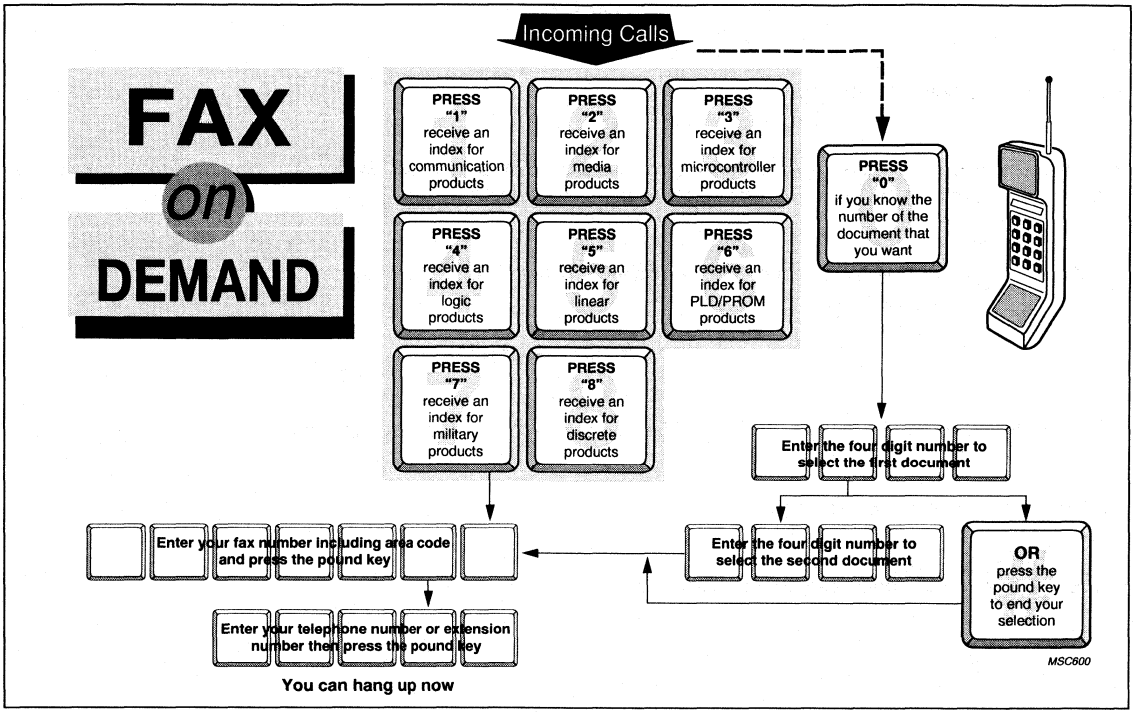

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United Kingdom, Ireland, Benelux & Scandinavia	44-181-730-5020
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REPLACED/WITHDRAWN TYPES

The following type numbers were included in the previous issue of this data handbook, but are not in the current edition.

TYPE NUMBER	REASON FOR DELETION	BUK REPLACEMENT	PH REPLACEMENT
BUK100-50GS	Discontinued		
BUK101-50GS	Discontinued		
BUK102-50GS	Discontinued		
BUK106-50SP	Discontinued		
BUK107-50DS	Discontinued		
BUK111-50GL	Discontinued		
BUK112-50GL	Discontinued		
BUK113-50GL		BUK127-50GL AVAILABLE Q3 1998	
BUK200-50X	Discontinued		
BUK201-50X	Discontinued		
BUK202-50X	Discontinued		
BUK203-50X	Discontinued		
BUK204-50X	Discontinued		
BUK205-50X	Discontinued		
BUK206-50X	Discontinued		
BUK207-50X	Discontinued		
BUK452-60A		BUK7575-55	PHP21N06T
BUK452-60B		BUK7575-55	PHP21N06T
BUK474-60H		BUK7735-55	
BUK475-60A		BUK7735-55	
BUK475-60B		BUK7735-55	
BUK475-60H	Discontinued		
BUK481-60A		BUK78150-55	PHT6N06T
BUK475-100B	Discontinued		
BUK542-60A		BUK9775-55	
BUK542-60B		BUK9775-55	
BUK545-60A		BUK9735-55	
BUK545-60B		BUK9735-55	
BUK545-60H	Discontinued		
BUK552-60A		BUK9575-55	PHP21N06LT
BUK553-48C	Discontinued		
BUK563-48C	Discontinued		
BUK573-48C	Discontinued		
BUK573-60B		BUK9775-55	
PHB36N06E	Discontinued		
PHP15N06E	Discontinued		
PHP20N06E	Discontinued		
PHP36N06E	Discontinued		

Power Diodes — Replacement list

TYPE NUMBER	REASON FOR DELETION	BUK REPLACEMENT	PH REPLACEMENT
PHP50N06	Discontinued		
PHX15N06E	Discontinued		
BUK453-60A	BUK7575-55		
BUK453-60B	BUK7575-55		
BUK454-60H	BUK7535-55		
BUK455-60A	BUK7535-55		
BUK455-60B	BUK7535-55		
BUK455-60H	BUK7528-55		
BUK456-60A	BUK7524-55		
BUK456-60B	BUK7524-55		
BUK456-60H	BUK7518-55		
BUK463-60A	BUK7675-55		
BUK464-60H	BUK7635-55		
BUK465-60A	BUK7635-55		
BUK465-60H	BUK7628-55		
BUK466-60A	BUK7624-55		
BUK482-60A	BUK78150-55		
BUK483-60A	BUK7880-55		
BUK543-60A	BUK573-60A		
BUK543-60B	BUK573-60A		
BUK553-60A	BUK9575-55		PHP21N06LT
BUK553-60B	BUK9575-55		PHP21N06LT
BUK554-60H	BUK9535-55		PHP37N06LT
BUK555-60A	BUK9535-55		PHP37N06LT
BUK555-60B	BUK9535-55		PHP37N06LT
BUK555-60H	BUK9535-55		PHP37N06LT
BUK556-60A	BUK9520-55		PHP60N06LT
BUK556-60H	BUK9520-55		PHP60N06LT
BUK563-60A	BUK9675-55		PHB21N06LT
BUK564-60H	BUK9635-55		PHB37N06LT
BUK565-60A	BUK9635-55		PHB37N06LT
BUK565-60H	BUK9635-55		PHB37N06LT
BUK566-60A	BUK9620-55		PHB60N06LT
BUK566-60H	BUK9620-55		PHB60N06LT
BUK582-60A	BUK98150-55		PHT6N06LT
BUK583-60A	BUK9880-55		PHT8N06LT
BUK444-400B			PHX4N40E
BUK444-500B			PHX3N50E
BUK444-600B			PHX3N60E
BUK445-400B			PHX7N40E
BUK445-500B			PHX6N50E

Power Diodes — Replacement list

TYPE NUMBER	REASON FOR DELETION	BUK REPLACEMENT	PH REPLACEMENT
BUK445-600B			PHX4N60E
BUK454-400B			PHP4N40E
BUK454-500B			PHP3N50E
BUK454-600B			PHP3N60E
BUK455-400B			PHP7N40E
BUK455-500B			PHP6N50E
BUK455-600B			PHP4N60E
BUK457-400B			PHP10N40E
BUK457-500B			PHP8N50E
BUK457-600B			PHP7N60E
BS208	Discontinued		
PHP212L			PHP222

GENERAL

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TOTAL QUALITY MANAGEMENT

Philips Semiconductors is a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is described in the following paragraphs.

Quality assurance

Based on ISO 9000 standards, customer standards such as Ford TQE and IBM MDQ. Our factories are certified to ISO 9000 by external inspectorates.

Partnerships with customers

PPM co-operations, design-in agreements, ship-to-stock, just-in-time and self-qualification programmes, and application support.

Partnerships with suppliers

Ship-to-stock, statistical process control and ISO 9000 audits.

Quality improvement programme

Continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

ADVANCED QUALITY PLANNING

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase.

PRODUCT CONFORMANCE

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- Incoming material management through partnerships with suppliers.
- In-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control.
- Acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications.
- Periodic inspections to monitor and measure the conformance of products.

PRODUCT RELIABILITY

With the increasing complexity of Original Equipment Manufacturer (OEM) equipment, component reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies result in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the products reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

CUSTOMER RESPONSES

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

RECOGNITION

The high quality of our products and services is demonstrated by many Quality Awards granted by major customers and international organizations.

RATING SYSTEMS

The rating systems described are those recommended by the IEC in its publication number 134.

Definitions of terms used

ELECTRONIC DEVICE

An electronic tube or valve, transistor or other semiconductor device. This definition excludes inductors, capacitors, resistors and similar components.

CHARACTERISTIC

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

BOGEY ELECTRONIC DEVICE

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics that are directly related to the application.

RATING

A value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

RATING SYSTEM

The set of principles upon which ratings are established and which determine their interpretation. The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

Absolute maximum rating system

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type, as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value for the intended service is exceeded with any device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

Design maximum rating system

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout the life of the device, no design maximum value for the intended service is exceeded with a bogey electronic device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

Design centre rating system

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

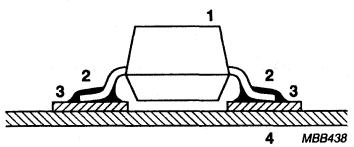
THERMAL CONSIDERATIONS

Thermal resistance

Circuit performance and long-term reliability are affected by the temperature of the transistor die. Normally, both are improved by keeping the die temperature (junction temperature) low.

Electrical power dissipated in any semiconductor device is a source of heat. This increases the temperature of the die about some reference point, normally an ambient temperature of 25 °C in still air. The size of the increase in temperature depends on the amount of power dissipated in the circuit and the net thermal resistance between the heat source and the reference point.

Devices lose most of their heat by conduction when mounted on a a printed board, a substrate or heatsink. Referring to Fig.1 (for surface mounted devices mounted on a substrate), heat conducts from its source (the junction) via the package leads and soldered connections to the substrate. Some heat radiates from the package into the surrounding air where it is dispersed by convection or by forced cooling air. Heat that radiates from the substrate is dispersed in the same way.



Heat radiates from the package '1' to ambient.
Heat conducts via leads '2', solder joints '3' to the substrate '4'.

Fig.1 Heat losses.

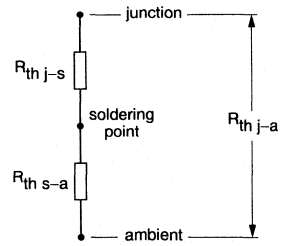


Fig.2 Representation of thermal resistance paths of a device mounted on a substrate or printed circuit board.

The elements of thermal resistance shown in Fig.2 are defined as follows:

$R_{th\ j-mb}$	thermal resistance from junction to mounting base
$R_{th\ j-c}$	thermal resistance from junction to case
$R_{th\ j-s}$	thermal resistance from junction to soldering point
$R_{th\ s-a}$	thermal resistance from soldering point to ambient
$R_{th\ c-a}$	thermal resistance from case to ambient ($R_{th\ s-a}$ and $R_{th\ c-a}$ are the same for most packages)
$R_{th\ j-a}$	thermal resistance from junction to ambient.

The temperature at the junction depends on the ability of the package and its mounting to transfer heat from the junction region to the ambient environment. The basic relationship between junction temperature and power dissipation is:

$$T_{j\ max} = T_{amb} + P_{tot\ max}\ (R_{th\ j-s} + R_{th\ s-a})$$
$$= T_{amb} + P_{tot\ max}\ (R_{th\ j-a})$$

where:

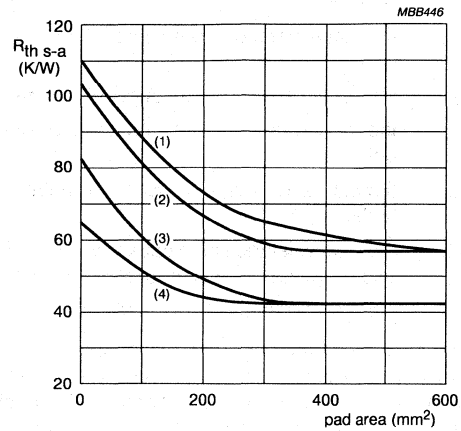
$T_{j\ max}$	is the maximum junction temperature
T_{amb}	is the ambient temperature
$P_{tot\ max}$	is the maximum power handling capability of the device, including the effects of external loads when applicable.

In the expression for $T_{j\ max}$, only T_{amb} and $R_{th\ s-a}$ can be varied by the user. The package mounting technique and the flow of cooling air are factors that affect $R_{th\ s-a}$. The device power dissipation can be controlled to a limited extent but under recommended usage, the supply voltage and circuit loading dictate a fixed power maximum. The $R_{th\ j-s}$ value is essentially independent of external mounting method and cooling air; but is sensitive to the materials used in the package construction, the die bonding method and the die area, all of which are fixed.

Values of $T_{j\ max}$ and $R_{th\ j-s}$, or $R_{th\ j-c}$ or $R_{th\ j-a}$ are given in the device data sheets. For applications where the temperature of the case is stabilized by a large or temperature-controlled heatsink, the junction temperature can be calculated from:

$T_j = T_{case} + P_{tot} \times R_{th\ j-c}$ or, using the soldering point (T_s) definition, from $T_j = T_s + P_{tot} \times R_{th\ j-s}$.

The thermal resistance from soldering point to ambient, and that from case to ambient depends on the substrate or PCB material used. Refer to figures 3 and 4 for R_{th} versus mounting substrate area.



(1) Single-sided, unplated.
(2) Single-sided, plated.
(3) Double-sided, unplated.
(4) Double-sided, plated.

Fig.3 Thermal resistance ($R_{th\ s\text{-}a}$) as a function of pad area on different configurations of FR4 epoxy fibre-glass circuit board.

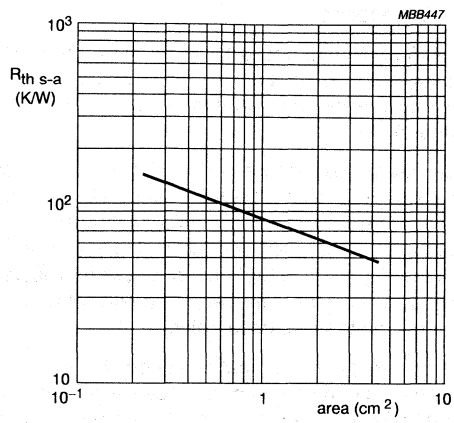


Fig.4 Thermal resistance ($R_{th\ s\text{-}a}$) as a function of area of ceramic substrate.

ELECTROSTATIC CHARGES

Electrostatic charges can exist in many things; for example, man-made-fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All of our MOS devices are internally protected against electrostatic discharge but they **can** be damaged if the following precautions are not taken.

WORK STATION

Figure 5 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is between 1 and 500 kΩ per cm^2. The floor should also be covered with antistatic material. The following precautions should be observed:

- Persons at a work bench should be earthed via a wrist strap and a resistor.
- All mains-powered electrical equipment should be connected via an earth leakage switch.
- Equipment cases should be earthed.
- Relative humidity should be maintained between 50 and 65%.
- An ionizer should be used to neutralize objects with immobile static charges.

RECEIPT AND STORAGE

MOS devices are packed for dispatch in antistatic/conductive containers, usually boxes, tubes or blister tape. The fact that the contents are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be performed at a protected work station. Any MOS devices that are stored temporarily should be packed in conductive or antistatic packing or carriers.

ASSEMBLY

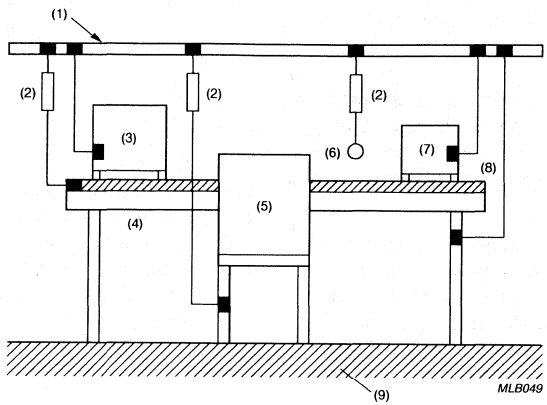
MOS devices must be removed from their protective packing with earthed component pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Do not remove more devices from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

During assembly, ensure that the MOS devices are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand tools should be of conductive or antistatic material and, where possible, should not be insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Assembled circuit boards containing MOS devices should be handled in the same way as unmounted MOS devices. They should also carry warning labels and be packed in conductive or antistatic packing.



(1) Earthing rail.
(2) Resistor (500 kΩ ± 10%, 0.5 W).
(3) Ionizer.
(4) Work bench.
(5) Chair.
(6) Wrist strap.
(7) Electrical equipment.
(8) Conductive surface/antistatic sheet.
(9) Antistatic floor.

Fig.5 Protected work station.

l manufacturers of power MOSFETs provide a data ıeet for every type produced. The purpose of the data ıeet is primarily to give an indication as to the capabilities a particular product. It is also useful for the purpose of ılecting device equivalents between different anufacturers. In some cases however data on a number parameters may be quoted under subtly different ınditions by different manufacturers, particularly on ıcond order parameters such as switching times. In ıdition the information contained within the data sheet ıes not always appear relevant for the application. Using ıta sheets and selecting device equivalents therefore quires caution and an understanding of exactly what the ıta means and how it can be interpreted. Throughout is chapter the BUK553-100A is used as an example, is device is a 100 V logic level MOSFET.

ıformation contained in the Philips data sheet

ıe data sheet is divided into 8 sections as follows:

Quick reference data

Limiting values

Thermal resistances

Static characteristics

Dynamic characteristics

Reverse diode limiting values and characteristics

Avalanche limiting value

Graphical data

he information contained within each of these sections now described.

ıuick reference data

his data is presented for the purpose of quick selection. lists what is considered to be the key parameters of the evice such that a designer can decide at a glance 'hether the device is likely to be the correct one for the pplication or not. Five parameters are listed, the two most nportant are the drain-source voltage V_{DS} and rain-source on-state resistance, $R_{DS(ON)}$. V_{DS} is the ıaximum voltage the device will support between drain nd source terminals in the off-state. $R_{DS(ON)}$ is the ıaximum on-state resistance at the quoted gate voltage, $_{GS}$, and a junction temperature of 25 °C. (NB $R_{DS(ON)}$ is ɜmperature dependent, see static characteristics). It is ıese two parameters which provide a first order indication f the devices capability.

ı drain current value (I_D) and a figure for total power lissipation are also given in this section. These figures hould be treated with caution since they are quoted for ɔnditions that are rarely attainable in real applications. See limiting values.) For most applications the usable dc ɔurrent will be less than the quoted figure in the quick eference data. Typical power dissipations that can be ɔlerated by the majority of designers are less than 20 W for discrete devices), depending on the heatsinking ırrangement used. The junction temperature (T_J) is usually given as either 150 °C or 175 °C. It is not recommended that the internal device temperature be allowed to exceed this figure.

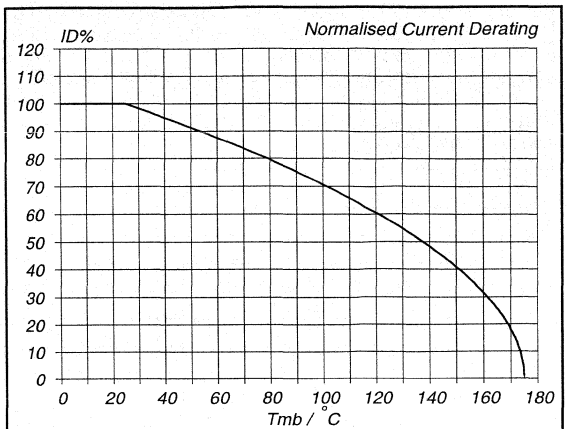


Fig.1 Normalised continuous drain current. ID% = 100 . $I_D/I_{D25\,°C} = f(T_{mb})$; conditions: $V_{GS} \geq 5$ V

Limiting values

This table lists the absolute maximum values of six parameters. The device may be operated right up to these maximum levels however they must not be exceeded, to do so may incur damage to the device.

Drain-source voltage and drain-gate voltage have the same value. The figure given is the maximum voltage that may be applied between the respective terminals. Gate-source voltage, $\pm V_{GS}$, gives the maximum value that may be allowed between the gate and source terminals. To exceed this voltage, even for the shortest period can cause permanent damage to the gate oxide. Two values for the dc drain current, I_D, are quoted, one at a mounting base temperature of 25 °C and one at a mounting base temperature of 100 °C. Again these currents do not represent attainable operating levels. These currents are the values that will cause the junction temperature to reach its maximum value when the mounting base is held at the quoted value. The maximum current rating is therefore a function of the mounting base temperature and the quoted figures are just two points on the derating curve ,see Fig.1.

The third current level quoted is the pulse peak value, I_{DM}. PowerMOS devices generally speaking have a very high peak current handling capability. It is the internal bond wires which connect to the chip that provide the final limitation. The pulse width for which I_{DM} can be applied depends upon the thermal considerations (see section on calculating currents.) The total power dissipation, P_{tot}, and maximum junction temperature are also stated as for the quick reference data. The P_{tot} figure is calculated from the simple quotient given in equation 1 (see section on safe

operating area). It is quoted for the condition where the mounting base temperature is maintained at 25 °C. As an example, for the BUK553-100A the P_{tot} figure is 75 W, dissipating this amount of power while maintaining the mounting base at 25 °C would be a challenge! For higher mounting base temperatures the total power that can be dissipated is less. Obviously if the mounting base temperature was made equal to the max permitted junction temperature, then no power could be dissipated internally. A derating curve is given as part of the graphical data, an example is shown in Fig.2 for a device with a limiting T_j of 175 °C.

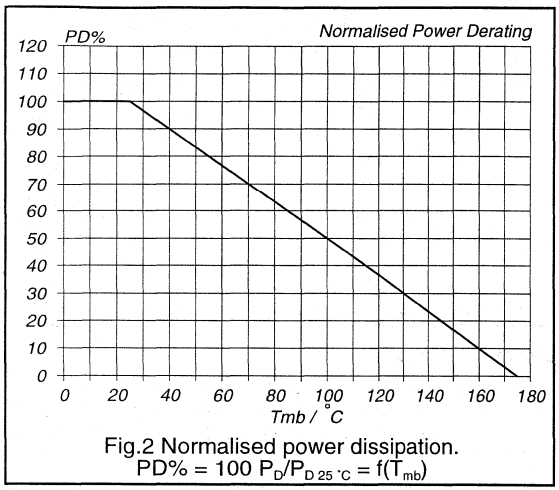


Fig.2 Normalised power dissipation.
PD% = 100 $P_D/P_{D\,25\,°C}$ = f(T_{mb})

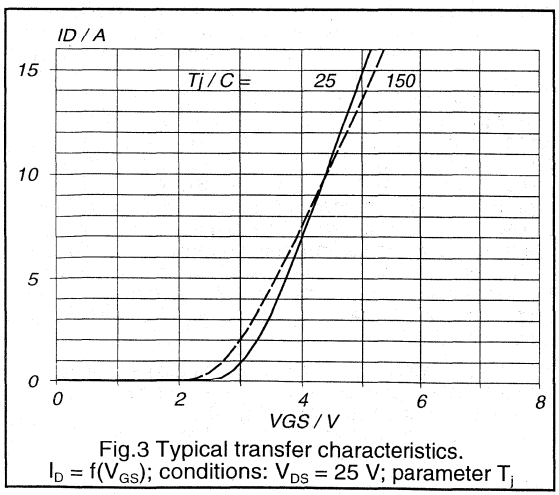


Fig.3 Typical transfer characteristics.
I_D = f(V_{GS}); conditions: V_{DS} = 25 V; parameter T_j

Storage temperature limits are also quoted, usua between -40 /-55 °C and +150 /+175 °C. Both the storag temperature limits and the junction temperature limit a figures at which extensive reliability work is performed l our Quality department. To exceed these figures w cause a reduction in long-term reliability.

Thermal resistance.

For non-isolated packages two thermal resistance valu are given. The value from junction to mounting bas ($R_{thj\text{-}mb}$) indicates how much the junction temperature w be raised above the temperature of the mounting bas when dissipating a given power. Eg a BUK553-100A ha a $R_{thj\text{-}mb}$ of 2 K/W, dissipating 10 W, the junctic temperature will be 20 °C above the temperature of i mounting base. The other figure quoted is from junctic to ambient. This is a much larger figure and indicates ho the junction temperature will rise if the device is NC mounted on a heatsink but operated in free air. Eg for BUK553-100A, $R_{thj\text{-}a}$ = 60 K/W, dissipating 1 W whi mounted in free air will produce a junction temperatu 60 °C above the ambient air temperature.

For isolated packages, (F-packs) the mounting base (th metal plate upon which the silicon chip is mounted) is ful encapsulated in plastic. Therefore it is not possible to giv a thermal resistance figure junction to mounting bas Instead a figure is quoted from junction to heatsink, $R_{thj\text{-}h}$ which assumes the use of heatsink compound. Cai should be taken when comparing thermal resistances isolated and non-isolated types. Consider the followin example:

The non-isolated BUK553-100A has a $R_{thj\text{-}mb}$ of 2 K/W The isolated BUK543-100A has a $R_{thj\text{-}hs}$ of 5 K/W. Thes devices have identical crystals but mounted in differer packages. At first glance the non-isolated type might b expected to offer much higher power (and hence curren handling capability. However for the BUK553-100A th thermal resistance junction to heatsink has to b calculated, this involves adding the extra therm resistance between mounting base and heatsink. Fc most applications some isolation is used, such as a mic washer. The thermal resistance mounting base t heatsink is then of the order 2 K/W. The total therm resistance junction to heatsink is therefore

$R_{thj\text{-}hs}$ (non isolated type) = $R_{thj\text{-}mb}$ + $R_{thmb\text{-}hs}$ = 4 K/W

It can be seen that the real performance differenc between the isolated and non isolated types will not b significant.

Static Characteristics

The parameters in this section characterise breakdow voltage, threshold voltage, leakage currents an on-resistance.

A drain-source breakdown voltage is specified as greate than the limiting value of drain-source voltage. It can b measured on a curve tracer, with gate terminal shorte to the source terminal, it is the voltage at which a drai current of 250 μA is observed. Gate threshold voltage $V_{GS(TO)}$, indicates the voltage required on the gate (wit

espect to the source) to bring the device into its onducting state. For logic level devices this is usually etween 1.0 and 2.0 V and for standard devices between .1 and 4 V.

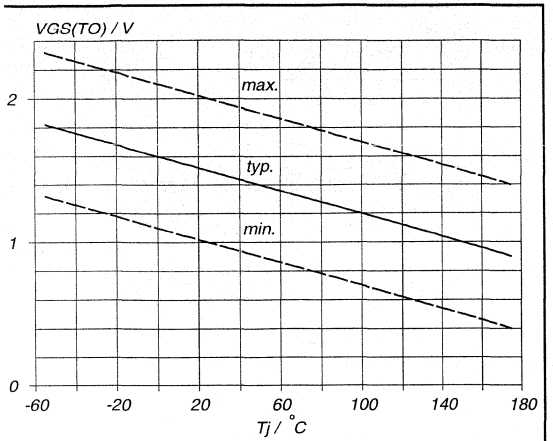


Fig.4 Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

Useful plots in the graphical data are the typical transfer characteristics (Fig.3) showing drain current as a function of V_{GS} and the gate threshold voltage variation with unction temperature (Fig.4). An additional plot also provided is the sub-threshold conduction, showing how he drain current varies with gate-source voltage below he threshold level (Fig.5).

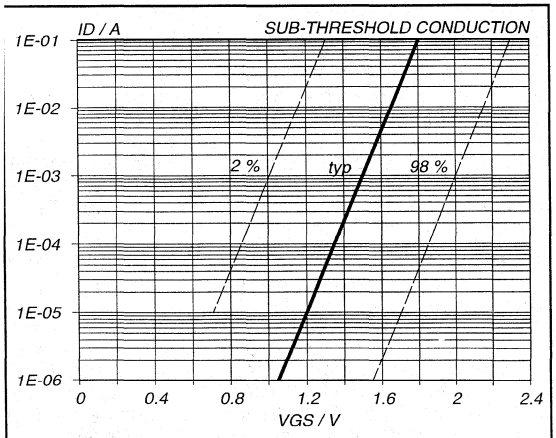


Fig.5 Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

Off-state leakage currents are specified for both the drain-source and gate-source under their respective maximum voltage conditions. Note, although gate-source leakage current is specified in nano-amps, values are typically of the order of a few pico-amps.

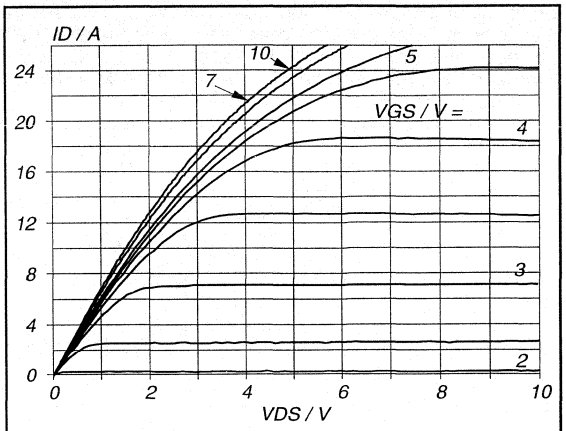


Fig.6 Typical output characteristics, T_j = 25 °C.
$I_D = f(V_{DS})$; parameter V_{GS}

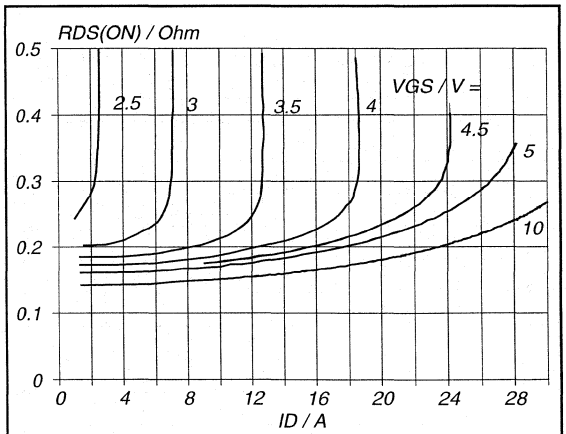


Fig.7 Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

The drain-source on-resistance is very important. It is specified at a gate-source voltage of 5 V for logic level FETs and 10 V for a standard device. The on-resistance for a standard MOSFET cannot be reduced significantly by increasing the gate source voltage above 10 V. Reducing the gate voltage will however increase the on-resistance. For the logic level FET, the on-resistance is given for a gate voltage of 5 V, a further reduction is

possible however at gate voltages up to 10 V, this is demonstrated by the output characteristics, Fig.6 and on-resistance characteristics, Fig.7 for a BUK553-100A.

The on-resistance is a temperature sensitive parameter, between 25 °C and 150 °C it approximately doubles in value. A plot of normalised $R_{DS(ON)}$ versus temperature (Fig.8) is included in each data sheet. Since the MOSFET will normally operate at a T_j higher than 25 °C, when making estimates of power dissipation in the MOSFET, it is important to take into account the higher $R_{DS(ON)}$.

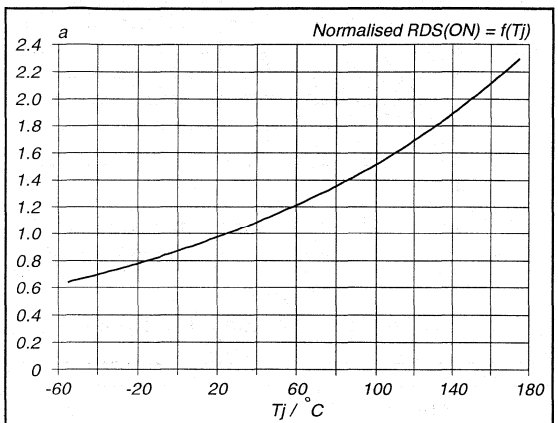


Fig.8 Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 6.5 A; V_{GS} = 5 V

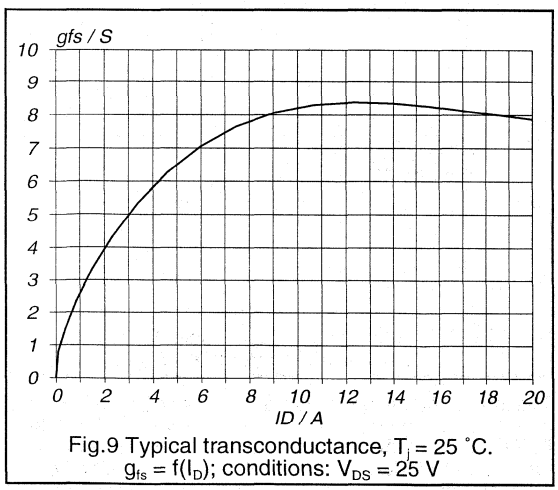


Fig.9 Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

Dynamic Characteristics

These include transconductance, capacitance and switching times. Forward transconductance, g_{fs}, is essentially the gain parameter which indicates the change in drain current that will result from a fluctuation in gate voltage when the device is saturated. (NB saturation of a MOSFET refers to the flat portion of the output characteristics.) Fig.9 shows how g_{fs} varies as a function of the drain current for a BUK553-100A.

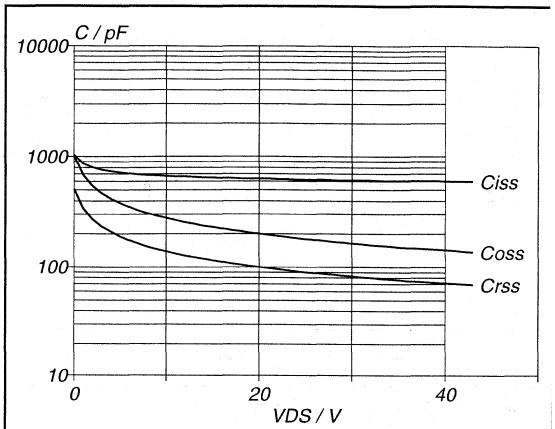


Fig.10 Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

Capacitances are specified by most manufacturers usually in terms of input, output and feedback capacitance. The values quoted are for a drain-source voltage of 25 V. However this is only part of the story as the MOSFET capacitances are strongly voltage dependent, increasing as drain-source voltage is reduced. Fig.10 shows how these capacitances vary with voltage. The usefulness of the capacitance figures is limited. The input capacitance value gives only a rough indication of the charging required by the drive circuit. Perhaps more useful is the gate charge information an example of which is shown in Fig.11. This plot shows how much charge has to be input to the gate to reach a particular gate-source voltage. Eg. to charge a BUK553-100A to V_{GS} = 5 V, starting from a drain-source voltage of 80 V, requires 12.4 nc. The speed at which this charge is to be applied will give the gate circuit current requirements. More information on MOSFET capacitance is given in chapter 1.2.2.

Resistive load switching times are also quoted by most manufacturers, however extreme care should be taken when making comparisons between different manufacturers data. The speed at which a power MOSFET can be switched is essentially limited only by circuit and package inductances. The actual speed in a circuit is determined by how fast the internal capacitances of the MOSFET are charged and discharged by the drive circuit. The switching times are therefore extremely dependent on the circuit conditions employed; a low gate drive resistance will provide for faster switching and vice-versa. The Philips data sheet presents the switching times for all PowerMOS with a resistor between gate and source of 50 Ω. The device is switched from a pulse

enerator with a source impedance also of 50 Ω. The verall impedance of the gate drive circuit is therefore 5 Ω.

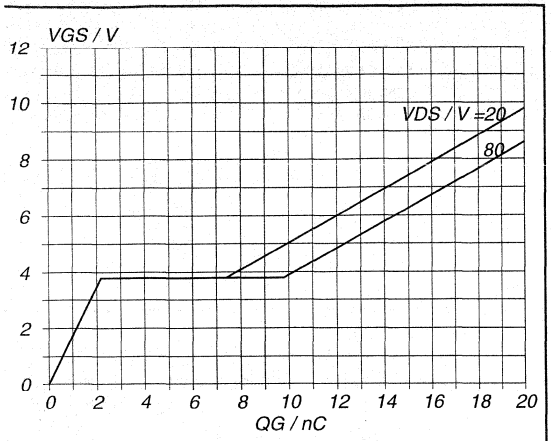


Fig.11 Typical turn-on gate-charge characteristics. V_{GS} = f(Q_G); conditions: I_D = 13 A; parameter V_{DS}

Also presented under dynamic characteristics are the ypical inductances of the package. These inductances ɔecome important when very high switching speeds are ɜmployed such that large dI/dt values exist in the circuit. Ξg. turning-on 30 A within 60 ns gives a dI/dt of 0.5 A/ns. The typical inductance of the source lead is 7.5 nH, from V = -L*dI/dt the potential drop from the source bond pad (point where the source bond wire connects to the chip nternally) to the bottom of the source lead would be 3.75 V. Normally a standard device will be driven with a gate-source voltage of 10 V applied across the gate and source terminals, the actual voltage gate to source on the semiconductor however would only be 6.25 V during the turn-on period! The switching speed is therefore ultimately limited by package inductance.

Reverse diode limiting values and characteristics

The reverse diode is inherent in the vertical structure of the power MOSFET. In some circuits this diode is required to perform a useful function. For this reason the characteristics of the diode are specified. The forward currents permissible in the diode are specified as 'continuous reverse drain current' and 'pulsed reverse drain current'. The forward voltage drop of the diode is also provided together with a plot of the diode characteristic, Fig.12. The switching capability of the diode is given in terms of the reverse recovery parameters, t_{rr} and Q_{rr}.

Because the diode operates as a bipolar device it is subject to charge storage effects. This charge must be removed for the diode to turn-off. The amount of charge stored is given by Q_{rr}, the reverse recovery charge, the

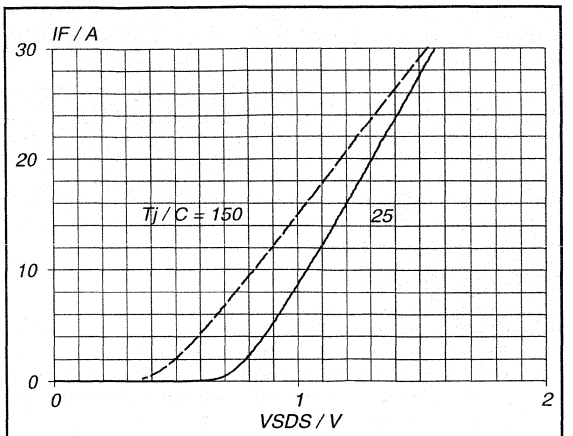


Fig.12 Typical reverse diode current. I_F = f(V_{SDS}); conditions: V_{GS} =) V; parameter T_j

time taken to extract the charge is given by t_{rr}, the reverse recovery time. NB. trr depends very much on the -dI_f/dt in the circuit, t_{rr} is specified in data at 100 A/μs.

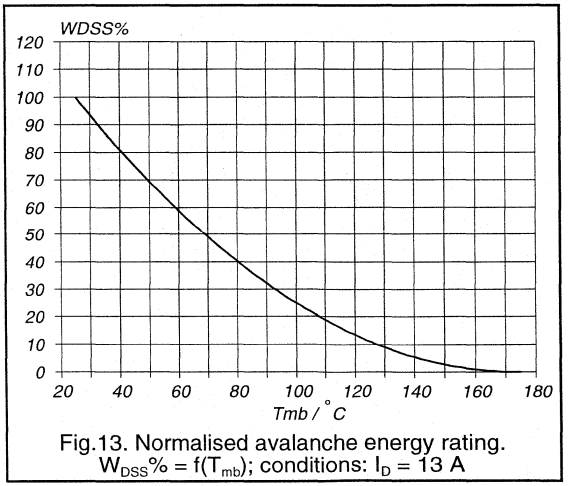


Fig.13. Normalised avalanche energy rating. W_{DSS}% = f(T_{mb}); conditions: I_D = 13 A

Avalanche limiting value

This parameter is an indication as to the ruggedness of the product in terms of its ability to handle a transient overvoltage, ie the voltage exceeds the drain-source voltage limiting value and causes the device to operate in an avalanche condition. The ruggedness is specified in terms of a drain-source non-repetitive unclamped inductive turn-off energy at a mounting base temperature of 25 °C. This energy level must be derated at higher mounting base temperatures as shown in Fig.13. NB. this rating is non-repetitive which means the circuit should not be designed to force the PowerMOS repeatedly into

avalanche. This rating is only to permit the device to survive if exceptional circuit conditions arise such that a transient overvoltage occurs.

The new generation of Philips Medium Voltage MOSFETs also feature a repetitive ruggedness rating. This rating is specified in terms of a drain-source repetitive unclamped inductive turn-off energy at a mounting base temperature of 25 °C, and indicates that the devices are able to withstand repeated momentary excursions into avalanche breakdown provided the maximum junction temperature is not exceeded.

Safe Operating Area

A plot of the safe operating area is presented for every PowerMOS type. Unlike bipolar transistors a PowerMOS exhibits no second breakdown mechanism. The safe operating area is therefore simply defined from the power dissipation that will cause the junction temperature to reach the maximum permitted value.

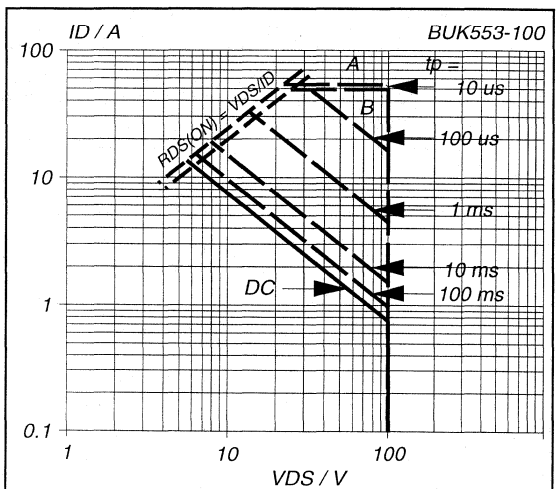


Fig.14 Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

Fig.14 shows the SOA for a BUK553-100. The area is bounded by the limiting drain source voltage, limiting current values and a set of constant power curves for various pulse durations. The plots in data are all for a mounting base temperature of 25 °C. The constant power curves therefore represent the power that raises the junction temperature by an amount T_{jmax} - T_{mb}, ie. 150 °C for a device with a limiting T_j of 175 °C and 125 °C for a device with a limiting T_j of 150 °C. . Clearly in most applications the mounting base temperature will be higher than 25 °C, the SOA would therefore need to be reduced. The maximum power curves are calculated very simply. The dc curve is based upon the thermal resistance junction to mounting base (junction to heatsink in the case of isolated packages), which is substituted into equation 1. The curves for pulsed operation assume a single shot pulse and instead of thermal resistance, a value for transient thermal impedance is used. Transient thermal impedance is supplied as graphical data for each type, an example is shown in Fig.15. For calculation of the single shot power dissipation capability, a value at the required pulse width is read from the D = 0 curve and substituted in to equation 2. (A more detailed explanation of transient thermal impedance and how to use the curves can be found in chapter 7.)

$$P_{tot(dc)} = \frac{T_{jmax} - T_{mb}}{R_{thj-mb}} \quad 1$$

$$P_{tot(pulse)} = \frac{T_{jmax} - T_{mb}}{Z_{thj-mb}} \quad 2$$

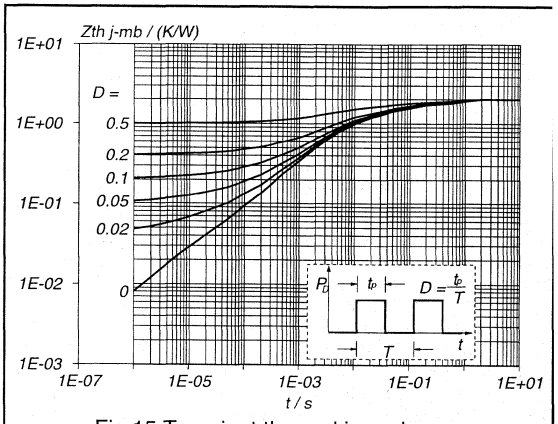


Fig.15 Transient thermal impedance.
Z_{thj-mb} = f(t); parameter D = t_p/T

Examples of how to calculate the maximum power dissipation for a 1 ms pulse are shown below. Example 1 calculates the maximum power assuming a T_j of 175 °C and T_{mb} of 25 °C. This power equates to the 1 ms curve on the SOA plot of Fig.14. Example 2 illustrates how the power capability is reduced if T_{mb} is greater than 25 °C.

Example 1: 1 ms pulse at 25 °C for a BUK553-100A

Z_{th} = 0.32 K/W, T_{jmax} = 175 °C, T_{mb} = 25 °C

$$P_{\max(1\,ms\,pulse)} = \frac{175 - 25}{0.32} = 469\,W$$

The 469 W line is observed on Fig.13, (4.69 A @ 100 V and 15.6 A @ 30 V etc)

Example 2: 1 ms pulse at 75 °C for a BUK553-100A

Z_{th} = 0.32 K/W, T_{jmax} = 175 °C, T_{mb} = 75 °C

$$P_{\max(1\,ms\,pulse)} = \frac{175 - 75}{0.32} = 312\,W$$

herefore with a mounting base temperature of 75 °C the ıaximum permissible power dissipation is reduced by ne third compared with the 25 °C value on the SOA plot.

:alculating Currents

'he current ratings quoted in the data sheet are derived irectly from the maximum power dissipation.

$$I_D(@T_{mb})^2 \cdot R_{DS(ON)}(@T_{jmax}) = P_{tot} \qquad 3$$

ubstituting for P_{tot} from equation 1

$$I_D(@T_{mb}) = \left\{ \frac{T_{jmax} - T_{mb}}{R_{thj-mb} \cdot R_{DS(ON)}(@T_{jmax})} \right\}^{\frac{1}{2}} \qquad 4$$

'o calculate a more realistic current it is necessary to eplace T_{jmax} in equation 4 with the desired operating ınction temperature and T_{mb} with a realistic working 'alue. It is generally recommended that devices are not ıperated continuously at T_{jmax}. For reasons of long term eliability, 125 °C is a more suitable junction operating emperature. A value of T_{mb} between 75 °C and 110 °C is ılso a more typical figure.

As an example a BUK553-100A is quoted as having a dc current rating of 13 A. Assuming a T_{mb} of 100 °C and operating T_j of 125 °C the device current is calculated as follows:

From Fig.8

$$R_{DS(ON)}(@\ 125^oC) = 1.75 \cdot R_{DS(ON)}(@\ 25^oC) = 1.75 \cdot 0.18 = 0.315\,\Omega$$

$R_{thj\text{-}mb}$ = 2 K/W, using equation 4

$$I_D = \left\{ \frac{25}{2 \cdot 0.315} \right\}^{\frac{1}{2}} = 6.3\,A$$

The device could therefore conduct 6.3 A under these conditions which equates to a 12.5 W power dissipation.

Conclusions

The most important information presented in the data sheet is the on-resistance and the maximum voltage drain-source. Current values and maximum power dissipation values should be viewed carefully since they are only achievable if the mounting base temperature is held to 25 °C. Switching times are applicable only for the specific conditions described in the data sheet, when making comparisons between devices from different manufacturers, particular attention should be paid to these conditions.

DEVICE DATA

in alphanumeric sequence

N-channel enhancement mode vertical D-MOS transistor

2N7000

FEATURES

- Low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope, intended for use in relay, high-speed and line transformer drivers.

PINNING - TO-92 VARIANT

PIN	DESCRIPTION
1	drain
2	gate
3	source

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		60	V
I_D	drain current	DC value	280	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 500 mA V_{GS} = 10 V	5	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	3	V

PIN CONFIGURATION

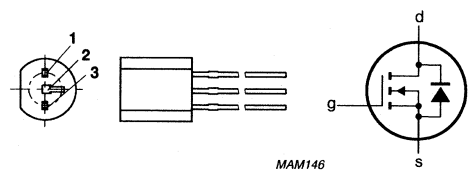


Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

2N7000

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	60	V
V_{DG}	drain-gate voltage		–	60	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	40	V
I_D	drain current	DC value	–	280	mA
I_{DM}	drain current	peak value	–	1.3	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	–	830	mW
T_{stg}	storage temperature range		–55	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	150	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA V_{GS} = 0	60	90	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 48 V V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 15 V V_{DS} = 0	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	0.8	–	3	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 500 mA V_{GS} = 10 V	–	3.5	5	Ω
		I_D = 75 mA V_{GS} = 4.5 V	–	–	5.3	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 200 mA V_{DS} = 10 V	100	200	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	25	40	pF
C_{oss}	output capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	22	30	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	6	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	4	10	ns
t_{off}	turn-off time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	4	10	ns

N-channel enhancement mode vertical D-MOS transistor

2N7000

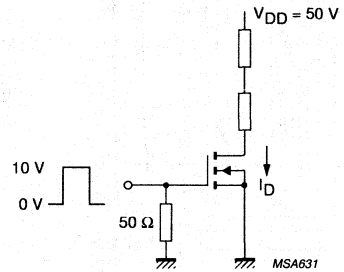


Fig.2 Switching time test circuit.

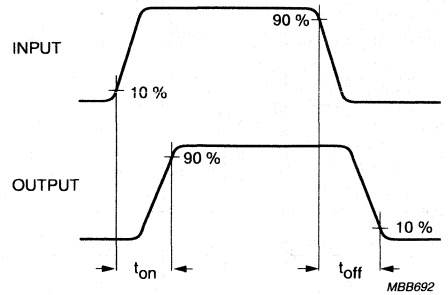


Fig.3 Input and output waveforms.

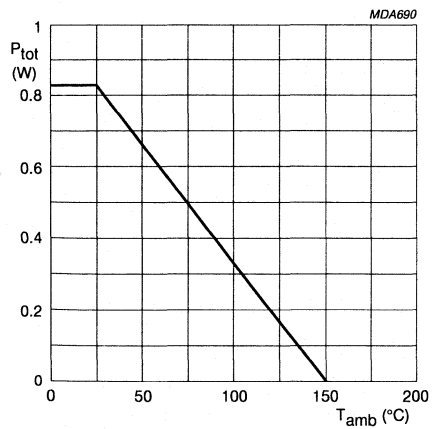


Fig.4 Power derating curve.

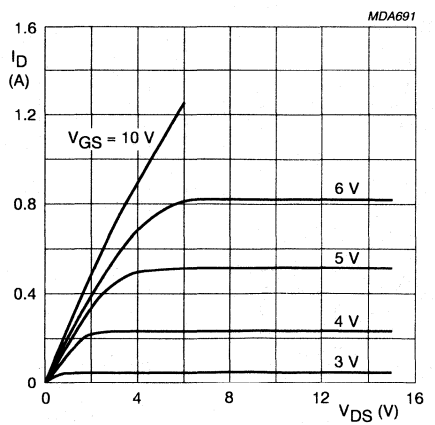


Fig.5 Typical output characteristics; T_j = 25 °C.

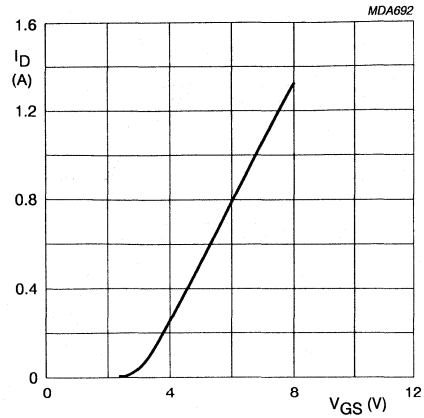


Fig.6 Typical transfer characteristic; V_{DS} = 10 V; T_j = 25 °C.

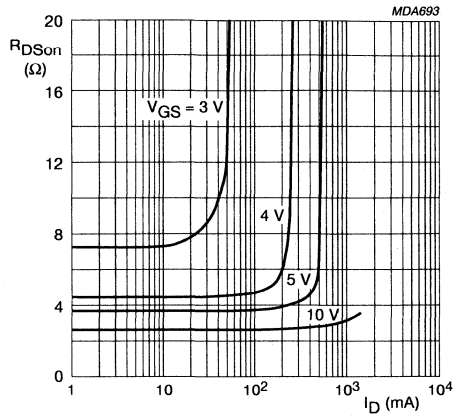


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

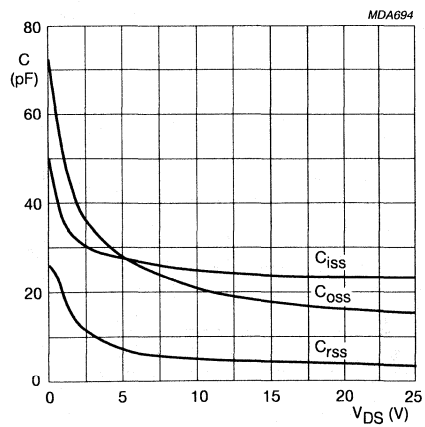
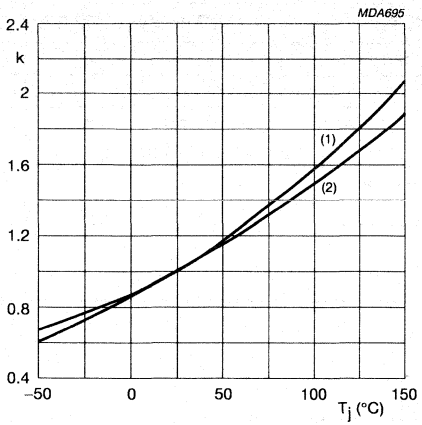


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

N-channel enhancement mode vertical D-MOS transistor

2N7000



(1) I_D = 500 mA; V_{GS} = 10 V.
(2) I_D = 75 mA; V_{GS} = 4.5 V.

Fig.9 Temperature coefficient of drain-source on resistance;

$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$$; typical $R_{DS(on)}$.

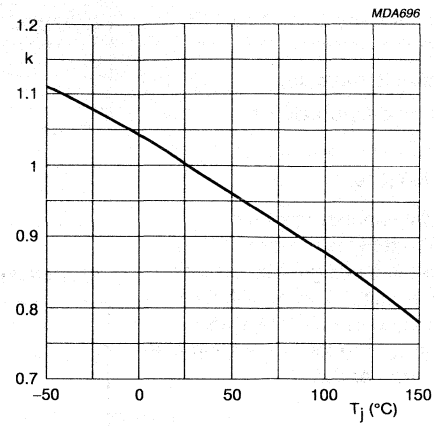


Fig.10 Temperature coefficient of gate-source threshold voltage;

$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}$$; typical $V_{GS(th)}$ at 1 mA.

N-channel vertical D-MOS transistor | 2N7002

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope. It is designed for use as a Surface Mounted Device (SMD) in thin and thick-film circuits, with applications in relay, high-speed and line transformer drivers.

PINNING - SOT23

PIN	DESCRIPTION
1	gate
2	source
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		60	V
I_D	drain current	DC value	180	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 500 mA V_{GS} = 10 V	5	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	3	V

PIN CONFIGURATION

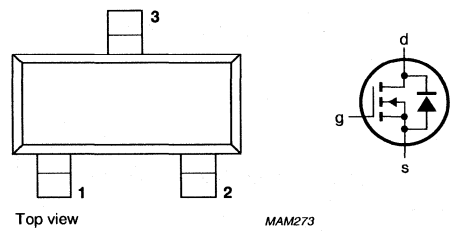


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Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	60	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	40	V
I_D	drain current	DC value	–	180	mA
I_{DM}	drain current	peak value	–	800	mA
P_{tot}	total power dissipation	T_{amb} = 25 °C (note 1) (note 2)	 – –	 300 250	 mW mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

Notes

1. Mounted on a ceramic substrate measuring 10 × 8 × 0.7 mm.
2. Mounted on a printed circuit board.

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	note 1 note 2	430 500	K/W K/W

Notes

1. Mounted on a ceramic substrate measuring 10 × 8 × 0.7 mm.
2. Mounted on a printed circuit board.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA V_{GS} = 0	60	90	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 48 V V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	V_{DS} = 0 $\pm V_{GS}$ = 15 V	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	0.8	–	3	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 500 mA V_{GS} = 10 V	–	3.5	5	Ω
		I_D = 75 mA V_{GS} = 4.5 V	–	–	5.3	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 200 mA V_{DS} = 10 V	100	200	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	25	40	pF
C_{oss}	output capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	22	30	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	6	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	–	10	ns
t_{off}	turn-off time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	–	15	ns

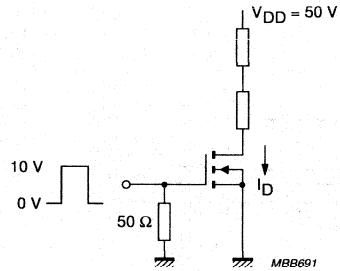


Fig.2 Switching time test circuit.

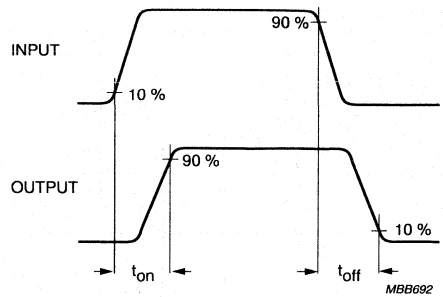
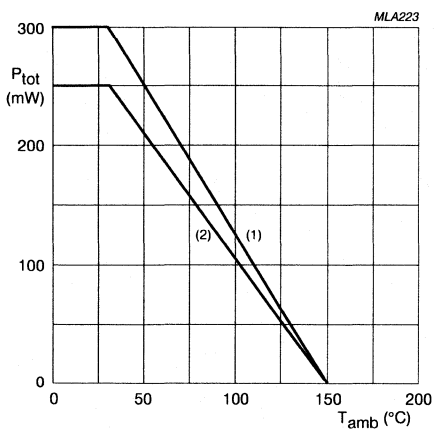


Fig.3 Input and output waveforms.



(1) On ceramic substrate.
(2) On printed circuit board.

Fig.4 Power derating curve.

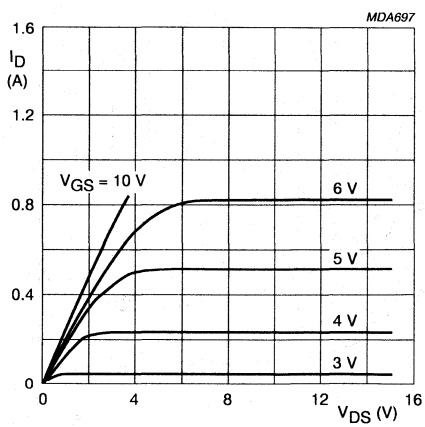


Fig.5 Typical output characteristics; T_j = 25 °C.

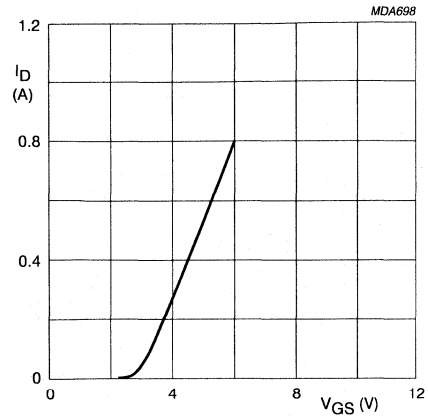


Fig.6 Typical transfer characteristic; V_{DS} = 10 V; T_j = 25 °C.

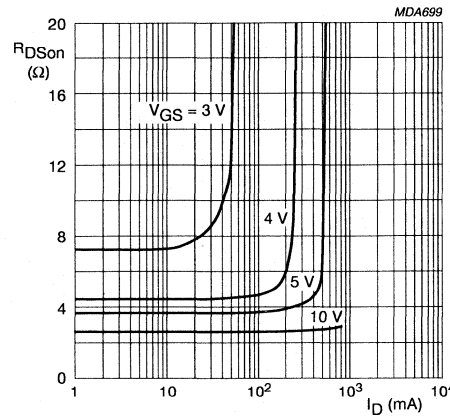


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

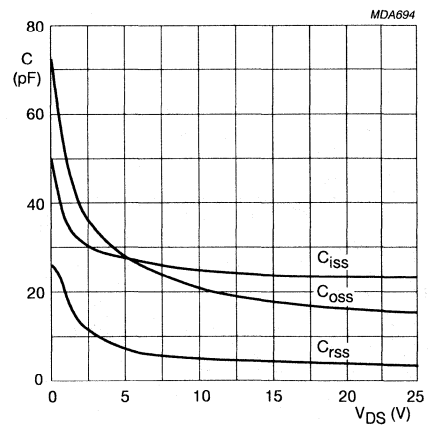
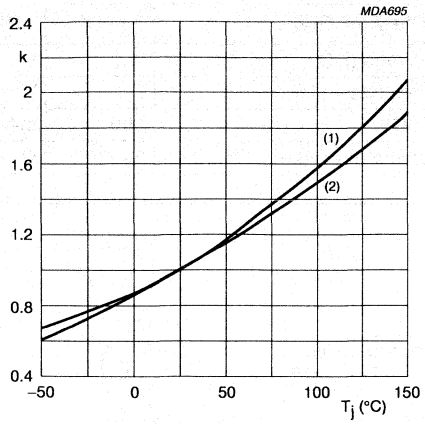


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.



(1) I_D = 500 mA; V_{GS} = 10 V.
(2) I_D = 75 mA; V_{GS} = 4.5 V.

Fig.9 Temperature coefficient of drain-source on-resistance;

$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$$

typical $R_{DS(on)}$.

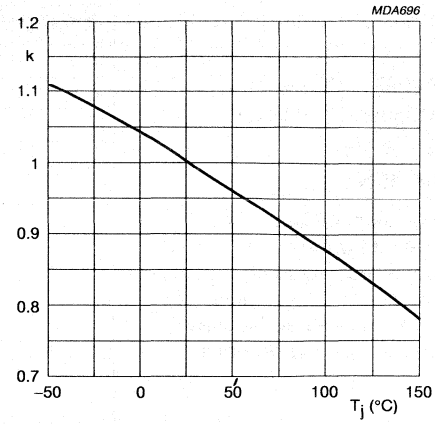


Fig.10 Temperature coefficient of gate-source threshold voltage;

$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}$$

typical $V_{GS(th)}$ at 1 mA.

N-channel enhancement mode vertical D-MOS transistor

BS107

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope. Intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - TO-92 variant

PIN	DESCRIPTION
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage (DC)	200	V
V_{GSth}	gate-source threshold voltage	2.4	V
I_D	drain current (DC)	150	mA
R_{DSon}	drain-source on-state resistance	28	Ω

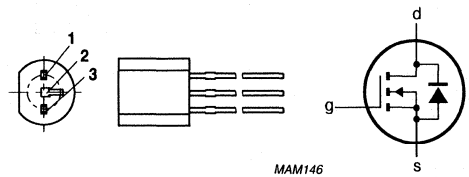


Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BS107

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	drain current	DC	–	150	mA
I_{DM}	drain current	peak	–	300	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	830	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	operating junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	150	K/W

N-channel enhancement mode vertical D-MOS transistor

BS107

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 I_D = 10 μA	200	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 130 V V_{GS} = 0	–	–	30	nA
I_{DSX}	drain-source leakage current	V_{DS} = 70 V V_{GS} = 0.2 V	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 15 V V_{DS} = 0	–	–	10	nA
$V_{GS(th)}$	gate threshold voltage	I_D = 1 mA V_{DS} = V_{GS}	0.8	–	2.4	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA V_{GS} = 2.6 V	–	20	28	Ω
$R_{DS(on)}$	drain-source on-resistance	I_D = 150 mA V_{GS} = 10 V	–	14	–	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 250 mA V_{DS} = 15 V	90	180	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	50	65	pF
C_{oss}	output capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	16	25	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	4	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	switching-on time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	2	10	ns
t_{off}	switching-off time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	4	20	ns

N-channel enhancement mode vertical D-MOS transistor

BS107

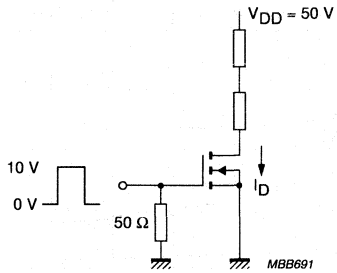


Fig.2 Switching time test circuit.

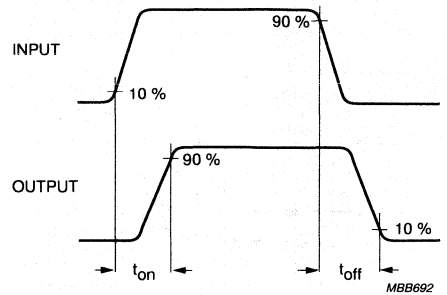


Fig.3 Input and output waveforms.

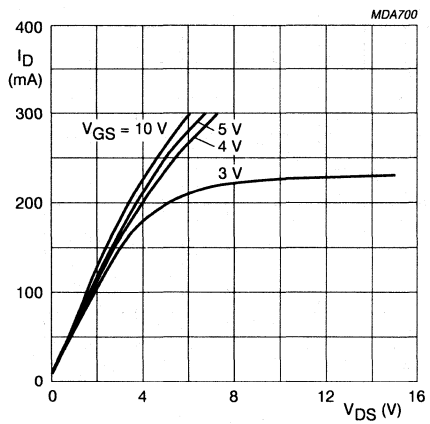


Fig.4 Typical output characteristics; T_j = 25 °C.

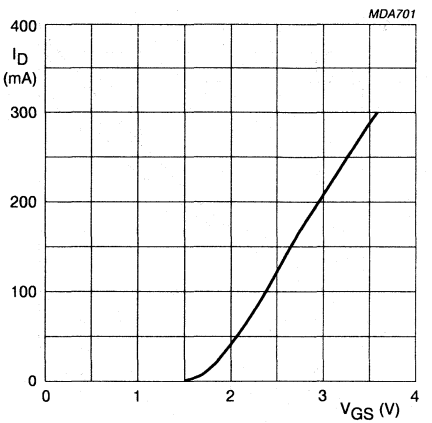


Fig.5 Typical transfer characteristic; V_{DS} = 10 V; T_j = 25 °C.

N-channel enhancement mode vertical D-MOS transistor

BS107

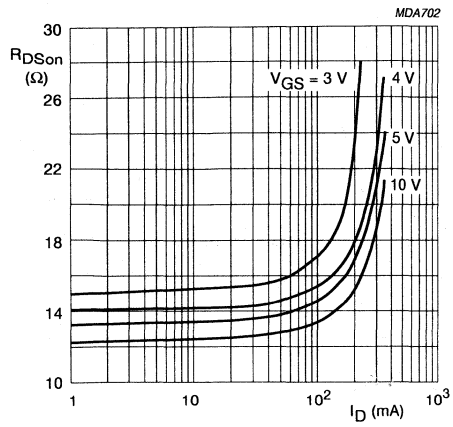


Fig.6 Typical on-resistance as a function of drain current; T_j = 25 °C.

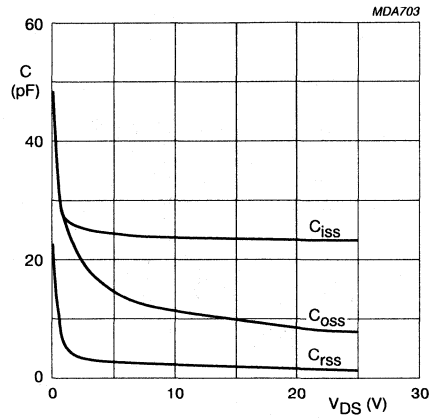
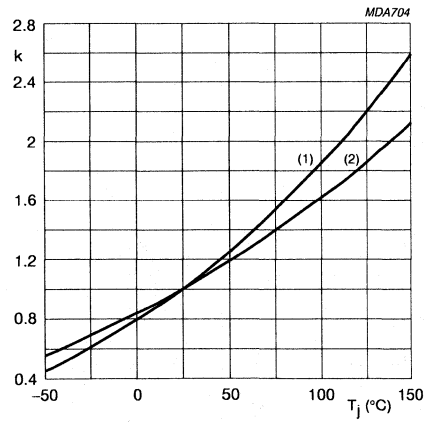


Fig.7 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.



(1) I_D = 150 mA; V_{GS} = 10 V
(2) I_D = 20 mA; V_{GS} = 2.6 V

Fig.8 Temperature coefficient of drain-source on-resistance; $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$; typical $R_{DS(on)}$ at 150 mA/10 V

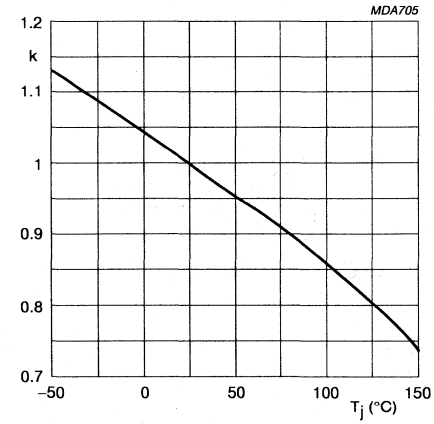


Fig.9 Temperature coefficient of gate-source threshold voltage; $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}$; typical $V_{GS(th)}$ at 1 mA.

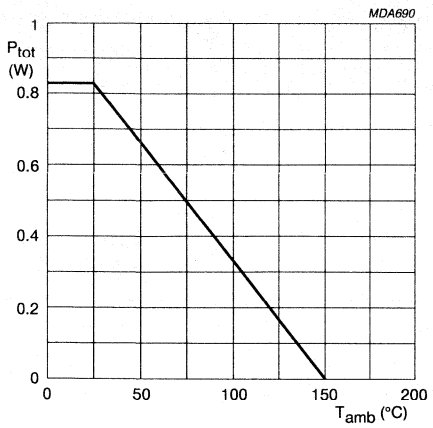


Fig.10 Power derating curve.

N-channel enhancement mode vertical D-MOS transistor

BS107A

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in TO-92 envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

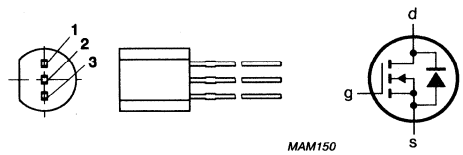
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	250	mA
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.	0.6	W
Drain-source ON-resistance				
I_D = 250 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	4.5	Ω
		max.	6.4	Ω
Transfer admittance				
I_D = 250 mA; V_{GS} = 25 V	$\lvert Y_{fs} \rvert$	min.	200	mS
		typ.	350	mS

PINNING - TO-92

1 = source
2 = gate
3 = drain

PIN CONFIGURATION



Note: Various pinnings are available.

Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BS107A

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	250	mA
Drain current (peak)	I_{DM}	max.	500	mA
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.	0.6	W
Storage temperature	T_{stg}		−55 to +150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for collector lead min. 10 mm × 10 mm.

N-channel enhancement mode vertical D-MOS transistor

BS107A

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage				
I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200	V
Drain-source leakage current				
V_{DS} = 130 V; V_{GS} = 0	I_{DSS}	max.	30	nA
Gate-source leakage current				
V_{GS} = 15 V; V_{DS} = 0	I_{GSS}	max.	10	nA
Gate threshold voltage				
I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min.	1.0	V
		max.	3.0	V
Drain-source ON-resistance				
I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ.	4.5	Ω
		max.	6.4	Ω
I_D = 100 mA; V_{GS} = 10 V	R_{DSon}	typ.	4.2	Ω
		max.	6.0	Ω
Transfer admittance				
I_D = 250 mA; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	min.	200	mS
		typ.	350	mS
Input capacitance at f = 1 MHz				
V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ.	45	pF
Output capacitance at f = 1 MHz				
V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ.	15	pF
Feedback capacitance at f = 1 MHz				
V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ.	3.5	pF
Switching times (see Figs 2 and 3)				
I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ.	5	ns
	t_{off}	typ.	15	ns

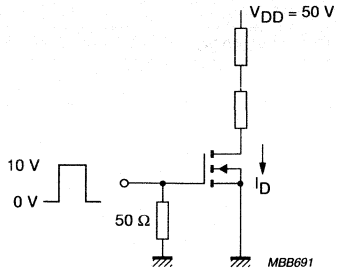


Fig.2 Switching times test circuit.

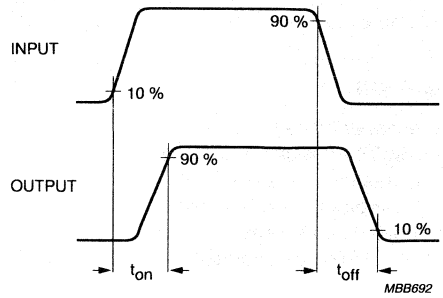


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistor

BS108

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	200	V
I_D	DC drain current	250	mA
$R_{DS(on)}$	drain-source on-resistance	8	Ω
$V_{GS(th)}$	gate-source threshold voltage	1.8	V

PINNING

PIN	DESCRIPTION
1	source
2	gate
3	drain

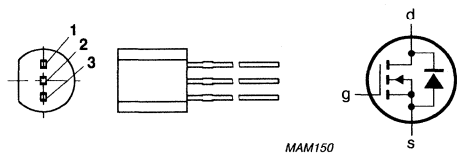


Fig.1 Simplified outline (TO-92) and symbol.

N-channel enhancement mode vertical D-MOS transistor

BS108

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	250	mA
I_{DM}	peak drain current		–	1	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	125 K/W

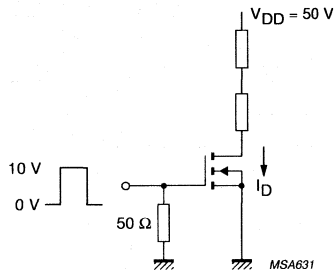
Note

1. Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 × 10 mm

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	200	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 160 V; V_{GS} = 0	–	–	1	μA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	0.4	–	1.8	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 100 mA; V_{GS} = 2.8 V	–	5	8	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 300 mA; V_{DS} = 25 V	200	400	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	50	80	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	5	10	pF
Switching times (see Figs 2 and 2)						
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	20	30	ns



V_{DD} = 50 V

Fig.2 Switching times test circuit.

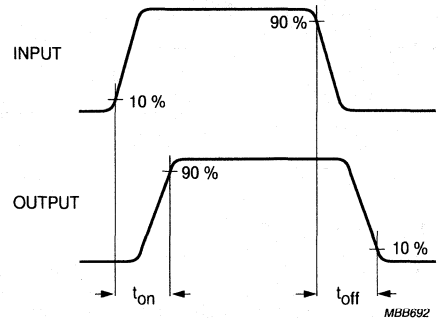


Fig.3 Input and output waveforms.

N-channel vertical D-MOS transistor BS170

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

FEATURES

- Very low $R_{DS(on)}$.
- Direct interface to C-MOS, TTL, etc.
- High-speed switching.
- No secondary breakdown.

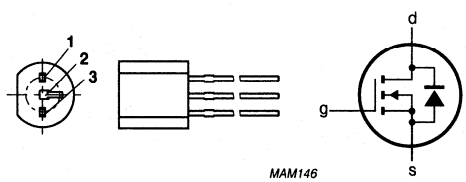
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	60	V
Gate-source voltage	V_{GS}	max.	15	V
Drain current (DC)	I_D	max.	500	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	830	mW
Junction temperature	T_j	max.	150	°C
Drain-source ON-resistance				
V_{GS} = 10 V; I_D = 200 mA	$R_{DS(on)}$	max.	5	Ω

PINNING - TO-92 VARIANT

1 = source
2 = gate
3 = drain

PIN CONFIGURATION



Note: Various pin configurations available.

Fig.1 Simplified outline and symbol.

N-channel vertical D-MOS transistor | BS170

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	60 V
Drain-gate voltage	V_{DG}	max.	60 V
Gate-source voltage	V_{GS}	max.	15 V
Drain current (DC) at T_c = 25 °C	I_D	max.	500 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	830 mW
Storage temperature range	T_{stg}		−55 to +150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	150 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage			
V_{GS} = 0; I_D = 100 µA	$V_{(BR)DS}$	min.	60 V
		typ.	90 V
Gate threshold voltage			
V_{GS} = V_{DS}; I_D = 1 mA	$V_{GS(th)}$	min.	0.8 V
		max.	3.0 V
Gate-source leakage current			
V_{GS} = 15 V; V_{DS} = 0	I_{GSoff}	max.	10 nA
Drain cut-off current			
V_{DS} = 25 V; V_{GS} = 0	I_{DSS}	max.	0.5 µA
Drain-source ON-resistance (note 1)			
V_{GS} = 10 V; I_D = 200 mA	$R_{DS(on)}$	typ.	2.5 Ω
		max.	5.0 Ω
Forward transconductance (note 1)			
V_{DS} = 10 V; I_D = 200 mA; f = 1 kHz	g_{fs}	typ.	200 mS
Capacitances at f = 1 MHz			
V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ.	25 pF
		max.	40 pF
	C_{os}	typ.	22 pF
		max.	30 pF
	C_{rs}	typ.	6 pF
		max.	10 pF
Switching times at I_D = 200 mA			
I_D = 200 mA; V_{DS} = 50 V;	t_{on}	typ.	4 ns
		max.	10 ns
V_{GS} = 0 to 10 V	t_{off}	typ.	4 ns
		max.	10 ns

Note

1. t_p = 80 μs; δ = 0,01.

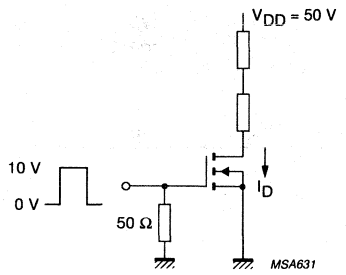


Fig.2 Switching times test circuit.

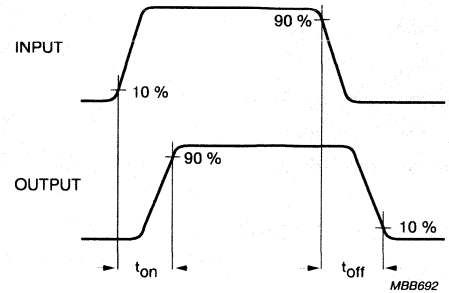


Fig.3 Input and output waveforms.

P-channel enhancement mode vertical D-MOS transistor

BS250

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

FEATURES

- Low $R_{DS(on)}$
- Direct interface to C-MOS
- High-speed switching
- No second breakdown

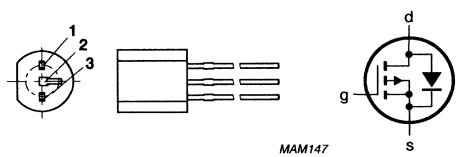
QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	45	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	0.25	A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	0.83	W
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$R_{DS(on)}$	typ.	9	Ω
		max.	14	Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert Y_{fs} \rvert$	typ.	125	mS

PINNING - TO-92 VARIANT

1 = source
2 = gate
3 = drain

PIN CONFIGURATION



Note: Various pinout configurations available.

Fig.1 Simplified outline and symbol.

P-channel enhancement mode vertical D-MOS transistor

BS250

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	45	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	0.25	A
Drain current (peak value)	$-I_{DM}$	max.	0.5	A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	0.83	W
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	150	K/W

Note

1. Transistor mounted on printed-circuit board, max. lead length 4 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage				
$-I_D$ = 100 μA; V_{GS} = 0	$-V_{(BR)DSS}$	min.	45	V
Drain-source leakage current				
$-V_{DS}$ = 25 V; V_{GS} = 0	$-I_{DSS}$	max.	0.5	μA
Gate-source leakage current				
$-V_{GS}$ = 15 V; V_{DS} = 0	$-I_{GSS}$	max.	20	nA
Gate threshold voltage				
$-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min.	1.0	V
		max.	3.5	V
Drain-source ON-resistance				
$-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$R_{DS(on)}$	typ.	9	Ω
		max.	14	Ω
Transfer admittance				
$-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert Y_{fs} \rvert$	typ.	125	mS
Input capacitance at f = 1 MHz				
$-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ.	30	pF
		max.	45	pF
Output capacitance at f = 1 MHz				
$-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ.	20	pF
		max.	30	pF
Feedback capacitance at f = 1 MHz				
$-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ.	5	pF
		max.	10	pF

Switching times (see Figs 2 and 3)

$-I_D = 200$ mA; $-V_{DD} = 40$ V; $-V_{GS} = 0$ to 10 V	t_{on}	typ.	4 ns
	t_{off}	typ.	10 ns

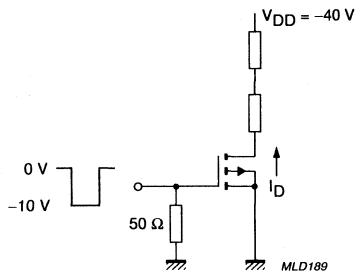


Fig.2 Switching times test circuit.

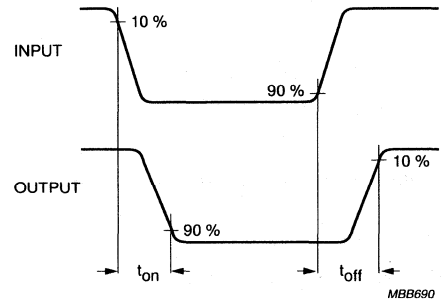


Fig.3 Input and output waveforms.

N-channel enhancement mode MOS transistor

BSH101

FEATURES

- Very low threshold
- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL etc.

APPLICATIONS

- Power management
- DC to DC converters
- Battery powered applications
- 'Glue-logic'; interface between logic blocks and/or periphery
- General purpose switch.

DESCRIPTION

N-channel enhancement mode MOS transistor in a SOT23 SMD package.

PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain

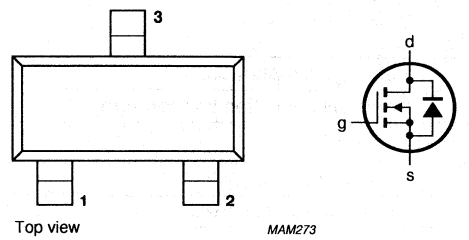


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETERS	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	60	V
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 0.5 A	–	1	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	–	V
I_D	drain current (DC)	T_s = 80 °C	–	0.7	A
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 0.35 A	–	0.6	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

N-channel enhancement mode MOS transistor

BSH101

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	60	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	0.7	A
I_{DM}	peak drain current	note 2	–	2.8	A
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W
		T_{amb} = 25 °C; note 3	–	0.75	W
		T_{amb} = 25 °C; note 4	–	0.54	W
T_{stg}	storage temperature		−55	+150	°C
T_j	operating junction temperature		−55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	0.5	A
I_{SM}	peak pulsed source current	note 2	–	2	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

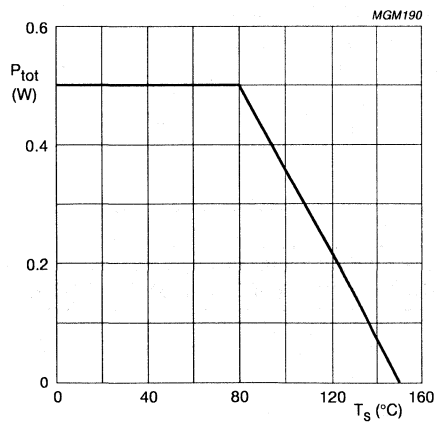
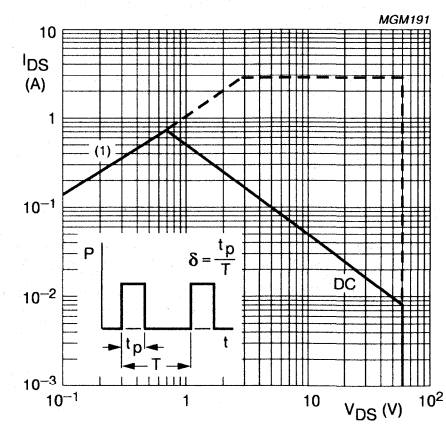


Fig.2 Power derating curve.

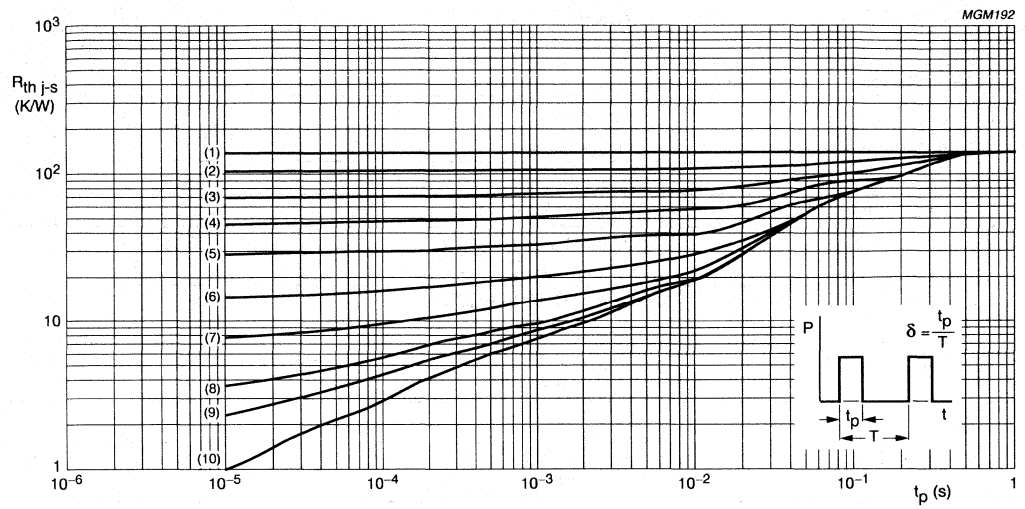


δ = 0.01; T_s = 80 °C.
(1) R_{DSon} limitation.

Fig.3 SOAR.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	140	K/W



(1) $\delta = 1$. (2) $\delta = 0.75$. (3) $\delta = 0.5$. (4) $\delta = 0.33$. (5) $\delta = 0.2$.

(6) $\delta = 0.1$. (7) $\delta = 0.05$. (8) $\delta = 0.02$. (9) $\delta = 0.01$. (10) $\delta = 0$.

Fig.4 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	60	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	1	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 48 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 0.35 A	–	–	0.6	Ω
		V_{GS} = 4.5 V; I_D = 0.175 A	–	–	0.9	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 48 V; f = 1 MHz	–	72.2	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 48 V; f = 1 MHz	–	11.3	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 48 V; f = 1 MHz	–	3.6	–	pF
Q_G	total gate charge	V_{GS} = 10 V; V_{DD} = 30 V; I_D = 0.35 A; T_{amb} = 25 °C	–	2130	–	pC
Q_{GS}	gate-source charge	V_{DD} = 30 V; I_D = 0.35 A; T_{amb} = 25 °C	–	150	–	pC
Q_{GD}	gate-drain charge	V_{DD} = 30 V; I_D = 0.35 A; T_{amb} = 25 °C	–	695	–	pC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to 10 V; V_{DD} = 30 V; I_D = 0.35 A; R_{gen} = 6 Ω	–	3.5	–	ns
t_f	fall time	V_{GS} = 0 to 10 V; V_{DD} = 30 V; I_D = 0.35 A; R_{gen} = 6 Ω	–	3.5	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to 10 V; V_{DD} = 30 V; I_D = 0.35 A; R_{gen} = 6 Ω	–	7	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = 10 to 0 V; V_{DD} = 30 V; I_D = 0.35 A; R_{gen} = 6 Ω	–	9	–	ns
t_r	rise time	V_{GS} = 10 to 0 V; V_{DD} = 30 V; I_D = 0.35 A; R_{gen} = 6 Ω	–	4.5	–	ns
t_{off}	turn-off switching time	V_{GS} = 10 to 0 V; V_{DD} = 30 V; I_D = 0.35 A; R_{gen} = 6 Ω	–	13.5	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 0.5 A	–	–	1	V
t_{rr}	reverse recovery time	I_S = 0.5 A; di/dt = −10 A/μs	–	35	–	ns

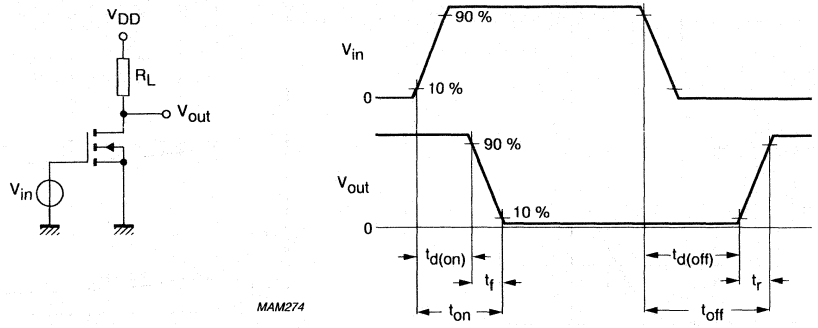
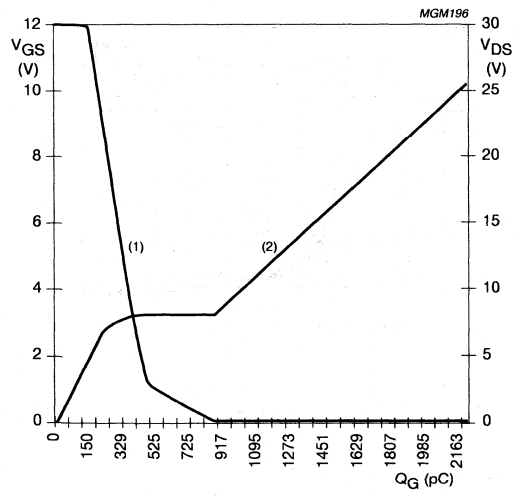
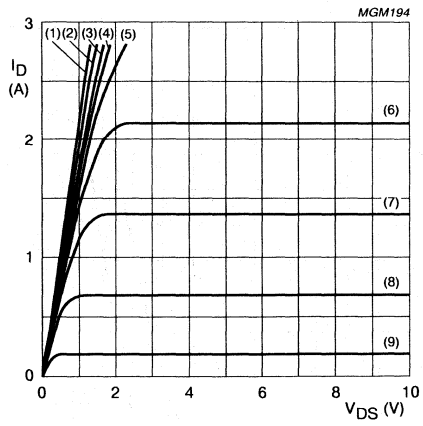


Fig.5 Switching times test circuit with input and output waveforms.



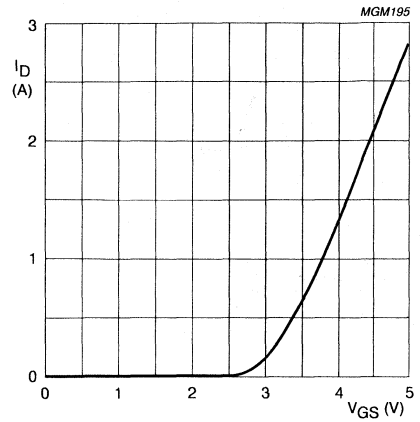
V_{DD} = 30 V; I_D = 0.35 A; T_{amb} = 25 °C.
(1) V_{DS}.
(2) V_{GS}.

Fig.6 Gate-source and drain-source voltages as functions of total gate charge; typical values.



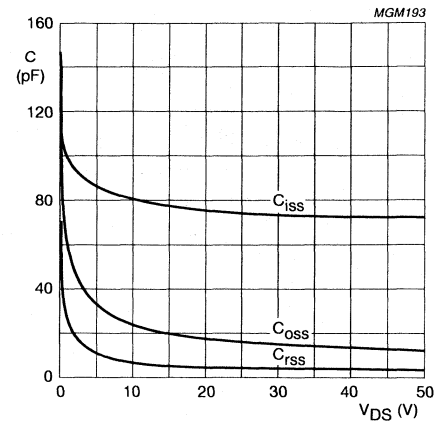
T_{amb} = 25 °C; t_p = 300 μs; δ = 0.
(1) V_{GS} = 10 V.
(2) V_{GS} = 8 V.
(3) V_{GS} = 6 V.
(4) V_{GS} = 5.5 V.
(5) V_{GS} = 5 V.
(6) V_{GS} = 4.5 V.
(7) V_{GS} = 4 V.
(8) V_{GS} = 3.5 V.
(9) V_{GS} = 3 V.

Fig.7 Output characteristics; typical values.



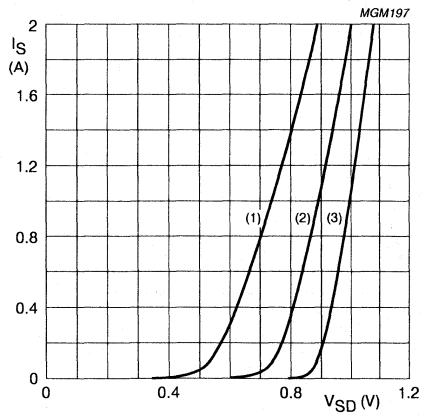
V_{DS} = 10 V; T_{amb} = 25 °C; t_p = 300 μs; δ = 0.

Fig.8 Transfer characteristic; typical values.



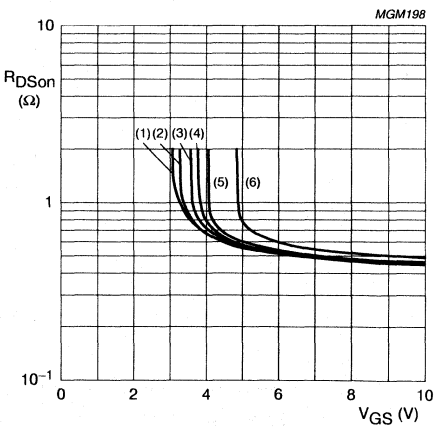
V_{GS} = 0; f = 1 MHz; T_{amb} = 25 °C.

Fig.9 Capacitance as a function of drain-source voltage; typical values.



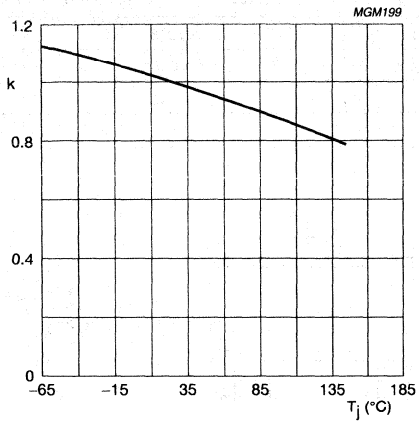
V_{GD} = 0.
(1) T_{amb} = 150 °C.
(2) T_{amb} = 25 °C.
(3) T_{amb} = −65 °C.

Fig.10 Source current as a function of source-drain diode forward voltage; typical values.



T_{amb} = 25 °C; t_p = 300 μs; δ = 0.
(1) I_D = 175 mA.
(2) I_D = 350 mA.
(3) I_D = 700 mA.
(4) I_D = 1 A.
(5) I_D = 1.4 A.
(6) I_D = 2.8 A.

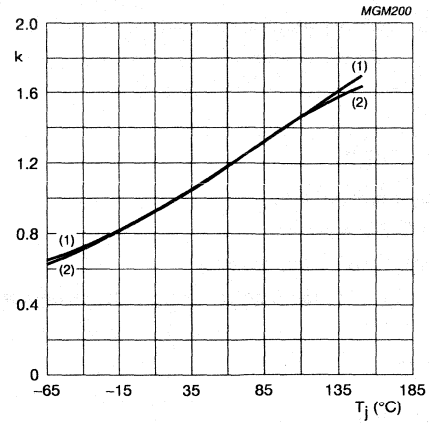
Fig.11 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

V_{GSth} at $V_{DS} = V_{GS}$; I_D = 1 mA.

Fig.12 Temperature coefficient of gate-source threshold voltage as a function of junction temperature; typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

(1) R_{DSon} at V_{GS} = 10 V; I_D = 350 mA.

(2) R_{DSon} at V_{GS} = 4.5 V; I_D = 170 mA.

Fig.13 Temperature coefficient of drain-source on-resistance as a function of junction temperature; typical values.

N-channel enhancement mode MOS transistor

BSH102

FEATURES

- Very low threshold
- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL etc.

APPLICATIONS

- Power management
- DC to DC converters
- Battery powered applications
- 'Glue-logic'; interface between logic blocks and/or periphery
- General purpose switch.

DESCRIPTION

N-channel enhancement mode MOS transistor in a SOT23 SMD package.

PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain

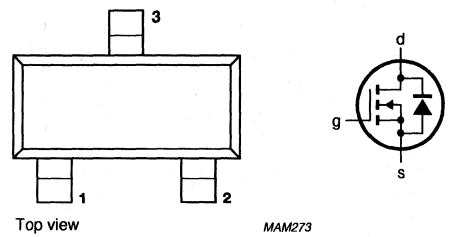


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 0.5 A	–	1	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	–	V
I_D	drain current (DC)	T_s = 80 °C	–	0.85	A
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 0.5 A	–	0.4	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	0.85	A
I_{DM}	peak drain current	note 2	–	3.4	A
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W
		T_{amb} = 25 °C; note 3	–	0.75	W
		T_{amb} = 25 °C; note 4	–	0.54	W
T_{stg}	storage temperature		−55	+150	°C
T_j	operating junction temperature		−55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	0.5	A
I_{SM}	peak pulsed source current	note 2	–	2	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

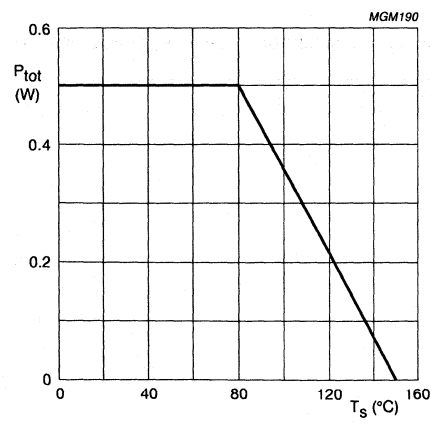
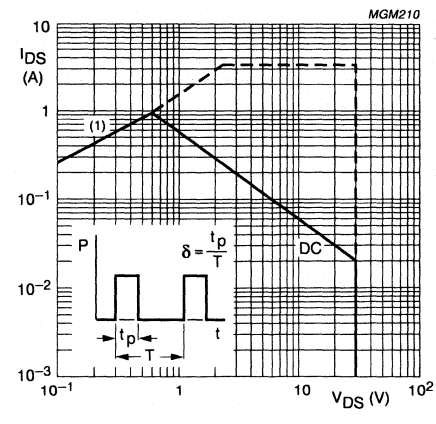


Fig.2 Power derating curve.

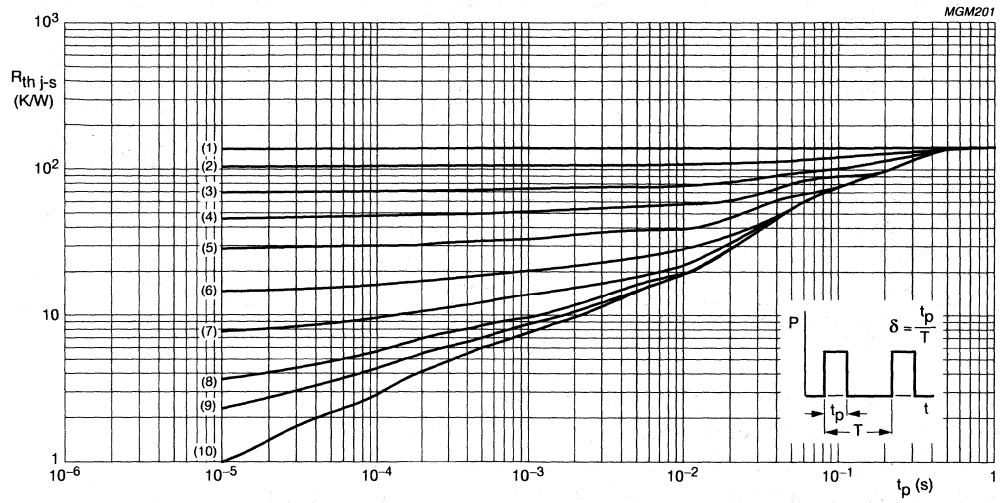


δ = 0.01; T_s = 80 °C.
(1) R_{DSon} limitation.

Fig.3 SOAR.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	140	K/W



(1) $\delta = 1$. (2) $\delta = 0.75$. (3) $\delta = 0.5$. (4) $\delta = 0.33$. (5) $\delta = 0.2$.
(6) $\delta = 0.1$. (7) $\delta = 0.05$. (8) $\delta = 0.02$. (9) $\delta = 0.01$. (10) $\delta = 0$.

Fig.4 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	1	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 24 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 0.5 A	–	–	0.4	Ω
		V_{GS} = 4.5 V; I_D = 0.25 A	–	–	0.6	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	67	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	27	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	13	–	pF
Q_G	total gate charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 0.5 A; T_{amb} = 25 °C	–	2290	–	pC
Q_{GS}	gate-source charge	V_{DD} = 15 V; I_D = 0.5 A; T_{amb} = 25 °C	–	150	–	pC
Q_{GD}	gate-drain charge	V_{DD} = 15 V; I_D = 0.5 A; T_{amb} = 25 °C	–	780	–	pC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 0.5 A; R_{gen} = 6 Ω	–	3.5	–	ns
t_f	fall time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 0.5 A; R_{gen} = 6 Ω	–	4	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 0.5 A; R_{gen} = 6 Ω	–	7.5	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 0.5 A; R_{gen} = 6 Ω	–	8	–	ns
t_r	rise time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 0.5 A; R_{gen} = 6 Ω	–	3	–	ns
t_{off}	turn-off switching time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 0.5 A; R_{gen} = 6 Ω	–	11	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 0.5 A	–	–	1	V
t_{rr}	reverse recovery time	I_S = 0.5 A; di/dt = −100 A/μs	–	25	–	ns

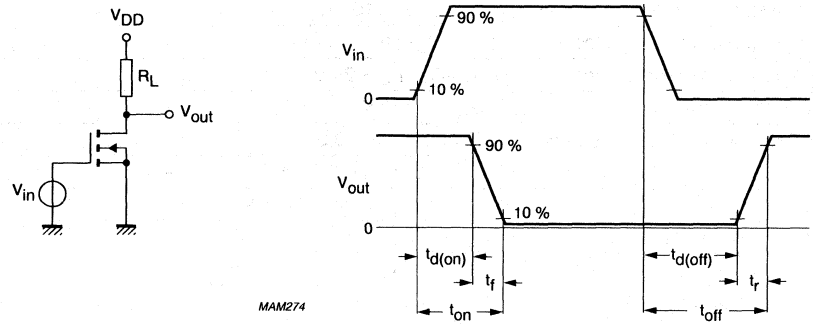
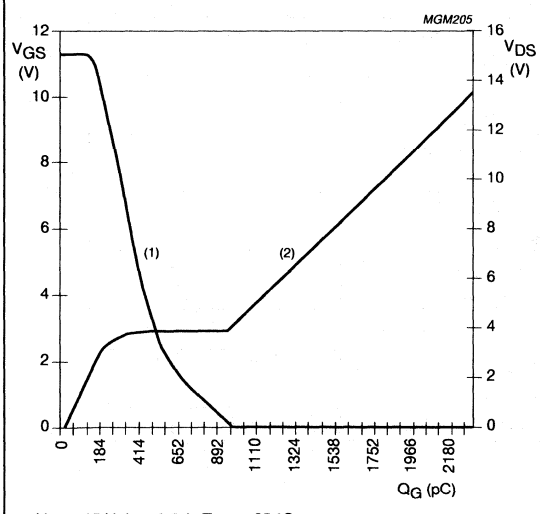
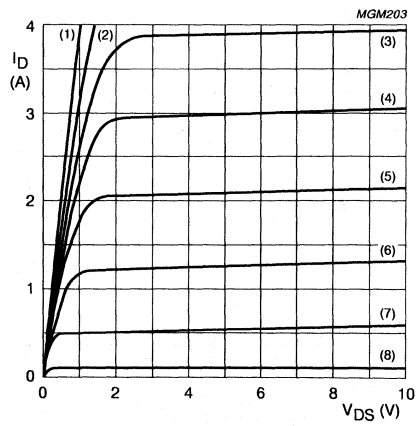


Fig.5 Switching times test circuit with input and output waveforms.



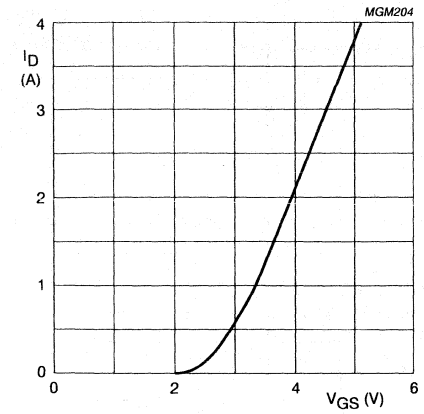
V_{DD} = 15 V; I_D = 0.5 A; T_{amb} = 25 °C.
(1) V_{DS}.
(2) V_{GS}.

Fig.6 Gate-source and drain-source voltages as functions of total gate charge; typical values.



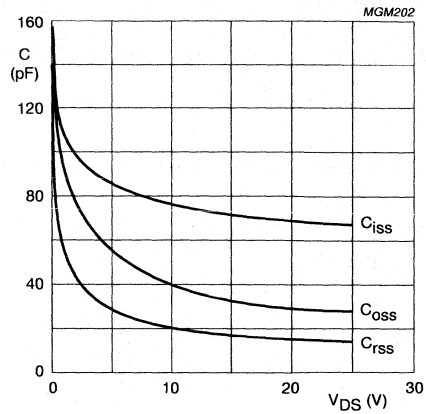
T_{amb} = 25 °C; t_p = 300 µs; δ = 0.
(1) V_{GS} = 10 V.
(2) V_{GS} = 6 V.
(3) V_{GS} = 5 V.
(4) V_{GS} = 4.5 V.
(5) V_{GS} = 4 V.
(6) V_{GS} = 3.5 V.
(7) V_{GS} = 3 V.
(8) V_{GS} = 2.5 V.

Fig.7 Output characteristics; typical values.



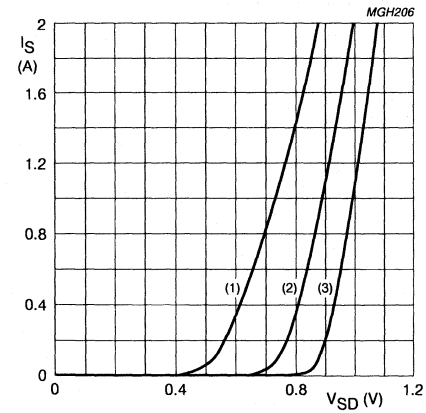
V_{DS} = 10 V; T_{amb} = 25 °C; t_p = 300 µs; δ = 0.

Fig.8 Transfer characteristic; typical values.



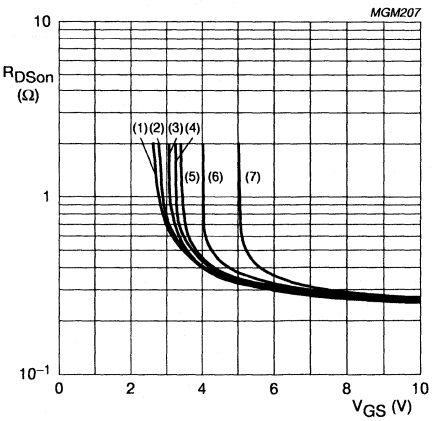
V_{GS} = 0 ; f = 1 MHz; T_{amb} = 25 °C.

Fig.9 Capacitance as a function of drain-source voltage; typical values.



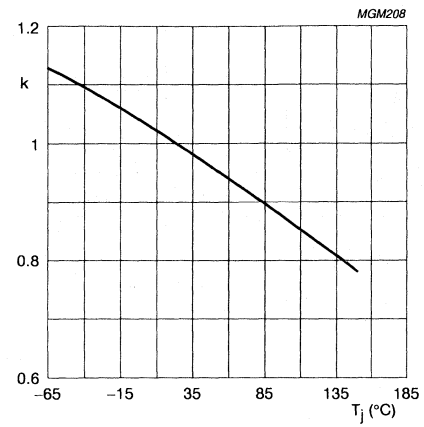
V_{GD} = 0.
(1) T_{amb} = 150 °C.
(2) T_{amb} = 25 °C.
(3) T_{amb} = −65 °C.

Fig.10 Source current as a function of source-drain diode forward voltage; typical values.



T_{amb} = 25 °C; t_p = 300 µs; δ = 0.
(1) I_D = 0.1 A.
(2) I_D = 0.25 A.
(3) I_D = 0.5 A.
(4) I_D = 0.75 A.
(5) I_D = 1 A.
(6) I_D = 2 A.
(7) I_D = 4 A.

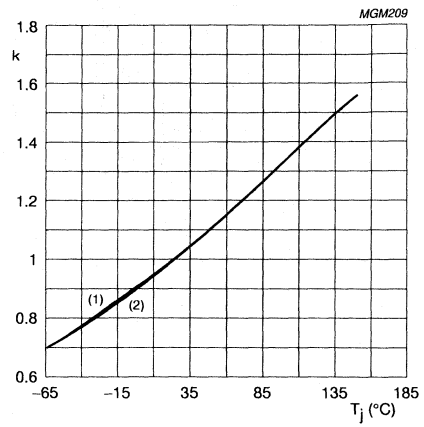
Fig.11 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

V_{GSth} at $V_{DS} = V_{GS}$; I_D = 1 mA.

Fig.12 Temperature coefficient of gate-source threshold voltage as a function of junction temperature; typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

(1) R_{DSon} at V_{GS} = 10 V; I_D = 0.5 mA.

(2) R_{DSon} at V_{GS} = 4.5 V; I_D = 0.25 mA.

Fig.13 Temperature coefficient of drain-source on-resistance as a function of junction temperature; typical values.

N-channel enhancement mode MOS transistor

BSH103

FEATURES

- Very low threshold
- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL etc.

APPLICATIONS

- Power management
- DC to DC converters
- Battery powered applications
- 'Glue-logic'; interface between logic blocks and/or periphery
- General purpose switch.

DESCRIPTION

N-channel enhancement mode MOS transistor in a SOT23 SMD package.

PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain

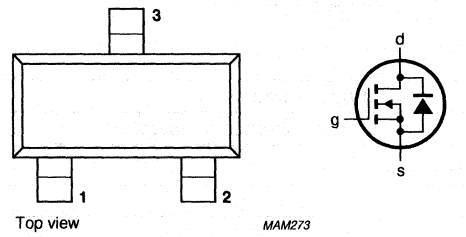


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETERS	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 0.5 A	–	1	V
V_{GS}	gate-source voltage (DC)		–	±8	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	0.4	–	V
I_D	drain current (DC)	T_s = 80 °C	–	0.85	A
R_{DSon}	drain-source on-state resistance	V_{GS} = 2.5 V; I_D = 0.5 A	–	0.5	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GS}	gate-source voltage (DC)		–	±8	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	0.85	A
I_{DM}	peak drain current	note 2	–	3.4	A
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W
		T_{amb} = 25 °C; note 3	–	0.75	W
		T_{amb} = 25 °C; note 4	–	0.54	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	0.5	A
I_{SM}	peak pulsed source current	note 2	–	2	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

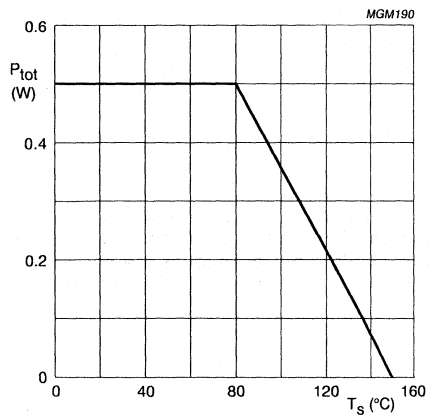
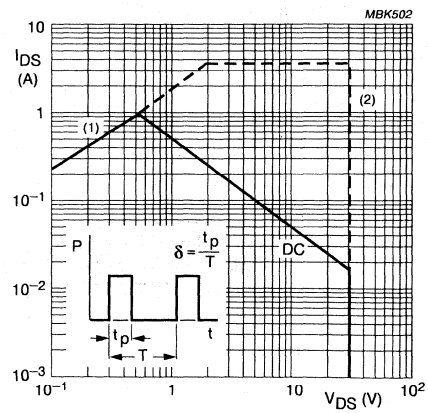


Fig.2 Power derating curve.



δ = 0.01; T_s = 80 °C.
(1) R_{DSon} limitation.
(2) Pulsed.

Fig.3 SOAR.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	140	K/W

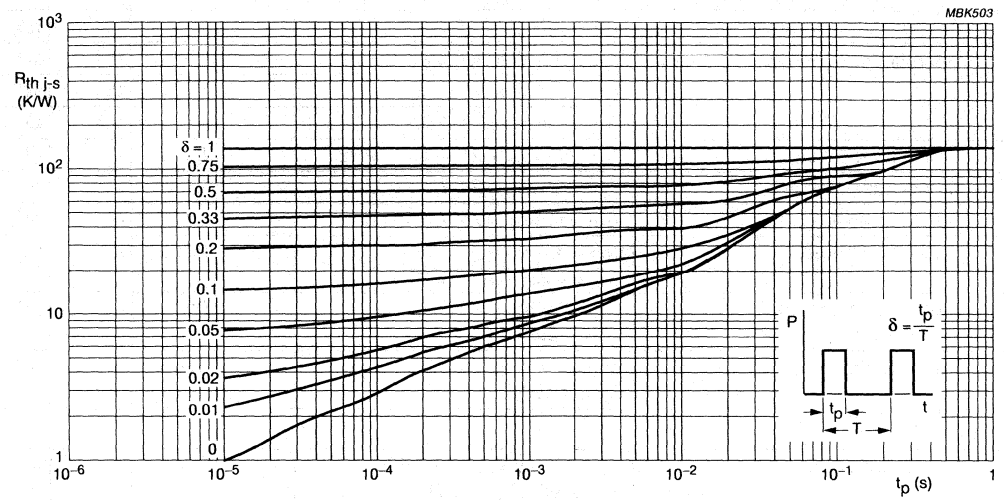


Fig.4 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	0.4	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 24 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±8 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 0.5 A	–	–	0.4	Ω
		V_{GS} = 2.5 V; I_D = 0.5 A	–	–	0.5	Ω
		V_{GS} = 1.8 V; I_D = 0.25 A	–	–	0.6	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	83	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	27	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	14	–	pF
Q_G	total gate charge	V_{GS} = 4.5 V; V_{DD} = 15 V; I_D = 0.5 A; T_{amb} = 25 °C	–	2100	–	pC
Q_{GS}	gate-source charge	V_{DD} = 15 V; I_D = 0.5 A; T_{amb} = 25 °C	–	95	–	pC
Q_{GD}	gate-drain charge	V_{DD} = 15 V; I_D = 0.5 A; T_{amb} = 25 °C	–	670	–	pC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to 8 V; V_{DD} = 15 V; I_D = 0.5 A; R_{gen} = 6 Ω	–	2.5	–	ns
t_f	fall time	V_{GS} = 0 to 8 V; V_{DD} = 15 V; I_D = 0.5 A; R_{gen} = 6 Ω	–	3.5	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to 8 V; V_{DD} = 15 V; I_D = 0.5 A; R_{gen} = 6 Ω	–	6	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = 8 to 0 V; V_{DD} = 15 V; I_D = 0.5 A; R_{gen} = 6 Ω	–	20	–	ns
t_r	rise time	V_{GS} = 8 to 0 V; V_{DD} = 15 V; I_D = 0.5 A; R_{gen} = 6 Ω	–	7	–	ns
t_{off}	turn-off switching time	V_{GS} = 8 to 0 V; V_{DD} = 15 V; I_D = 0.5 A; R_{gen} = 6 Ω	–	27	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 0.5 A	–	–	1	V
t_{rr}	reverse recovery time	I_S = 0.5 A; di/dt = −100 A/μs	–	25	–	ns

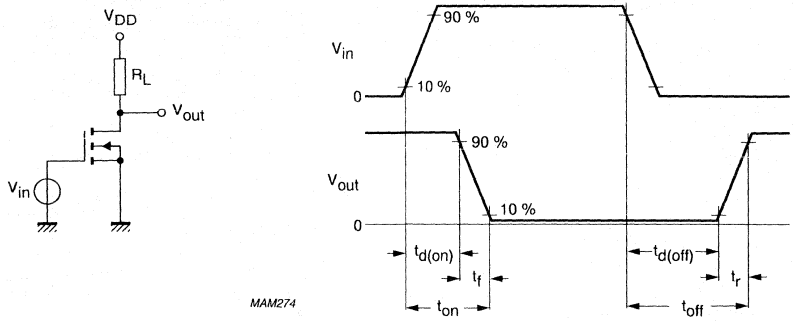
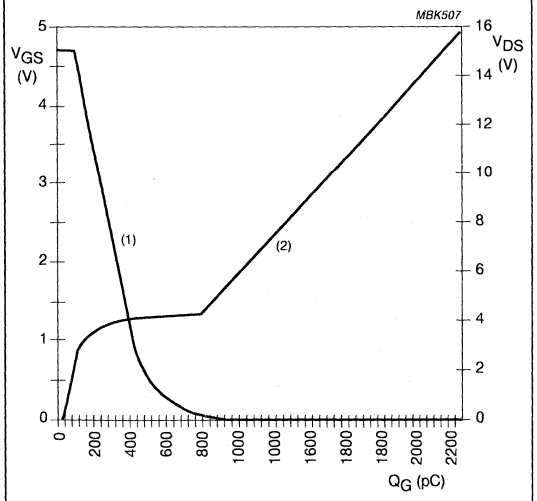
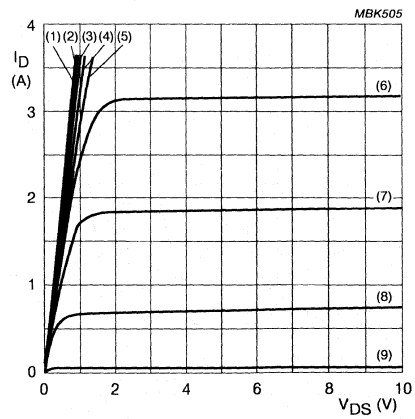


Fig.5 Switching times test circuit with input and output waveforms.



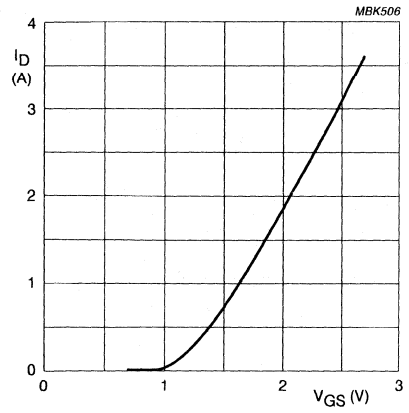
V_{DD} = 15 V; I_D = 0.5 A; T_{amb} = 25 °C.
(1) V_{DS}.
(2) V_{GS}.

Fig.6 Gate-source and drain-source voltages as functions of total gate charge; typical values.



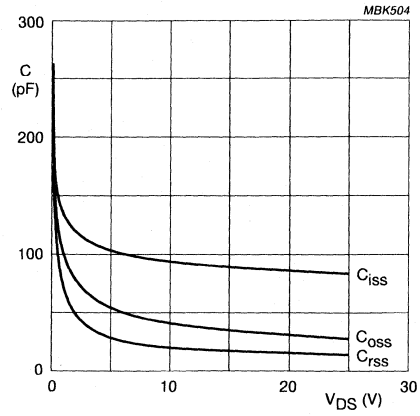
T_{amb} = 25 °C; t_p = 300 μs; δ = 0.
(1) V_{GS} = 7.5 V.
(2) V_{GS} = 5.5 V.
(3) V_{GS} = 4.5 V.
(4) V_{GS} = 3.5 V.
(5) V_{GS} = 3 V.
(6) V_{GS} = 2.5 V.
(7) V_{GS} = 2 V.
(8) V_{GS} = 1.5 V.
(9) V_{GS} = 1 V.

Fig.7 Output characteristics; typical values.



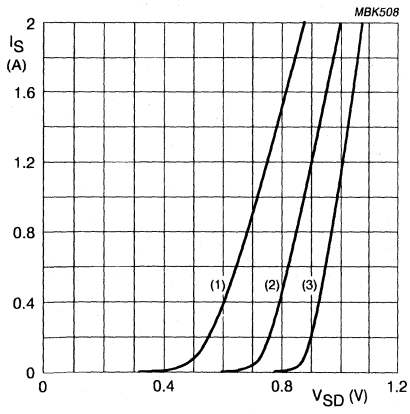
V_{DS} = 10 V; T_{amb} = 25 °C; t_p = 300 µs; δ = 0.

Fig.8 Transfer characteristic; typical values.



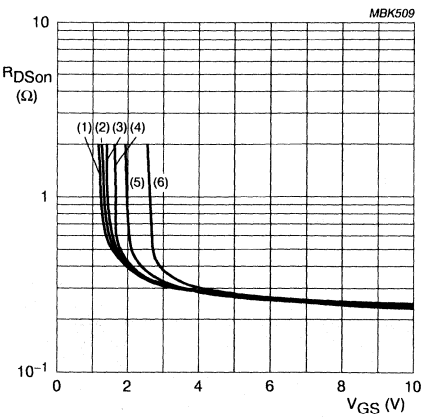
V_{GS} = 0 ; f = 1 MHz; T_{amb} = 25 °C.

Fig.9 Capacitance as a function of drain-source voltage; typical values.



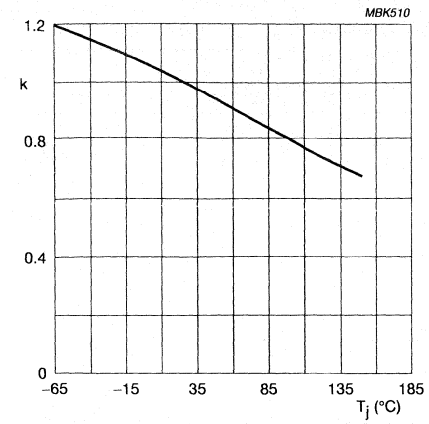
V_{GD} = 0.
(1) T_{amb} = 150 °C.
(2) T_{amb} = 25 °C.
(3) T_{amb} = −65 °C.

Fig.10 Source current as a function of source-drain diode forward voltage; typical values.



T_{amb} = 25 °C; t_p = 300 µs; δ = 0.
(1) I_D = 0.1 A.
(2) I_D = 0.22 A.
(3) I_D = 0.45 A.
(4) I_D = 0.9 A.
(5) I_D = 1.8 A.
(6) I_D = 3.6 A.

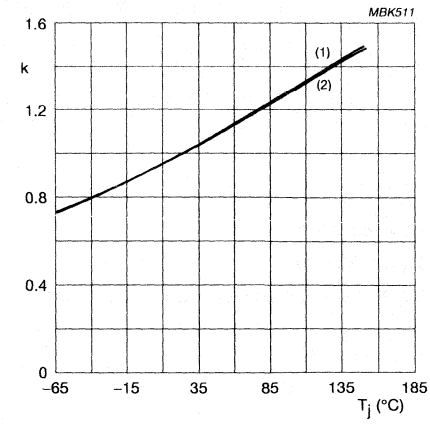
Fig.11 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}.$$

V_{GSth} at $V_{DS} = V_{GS}$; I_D = 1 mA.

Fig.12 Temperature coefficient of gate-source threshold voltage as a function of junction temperature; typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}.$$

(1) R_{DSon} at V_{GS} = 4.5 V; I_D = 0.5 mA.
(2) R_{DSon} at V_{GS} = 2.5 V; I_D = 0.5 mA.

Fig.13 Temperature coefficient of drain-source on-resistance as a function of junction temperature; typical values.

N-channel enhancement mode MOS transistor

BSH105

FEATURES

- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL, etc.
- Very low threshold.

APPLICATIONS

- Power management
- DC - DC converters
- 'Glue-logic': interface between logic blocks and/or periphery
- General purpose switch
- Battery powered applications.

DESCRIPTION

N-channel enhancement mode MOS transistor in a SOT23 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain

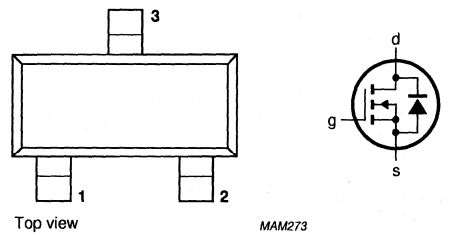


Fig.1 Simplified outline SOT23 and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	20	V
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 0.5 A	–	1	V
V_{GS}	gate-source voltage (DC)		–	±8	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	0.4	–	V
I_D	drain current (DC)	T_s = 80 °C	–	1.21	A
R_{DSon}	drain-source on-state resistance	V_{GS} = 2.5 V; I_D = 0.6 A	–	0.25	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W

PRELIMINARY
See Philips Semiconductors for Design-in information

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	20	V
V_{GS}	gate-source voltage (DC)		–	±8	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	1.21	A
I_{DM}	peak drain current	note 2	–	4.85	A
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W
		T_{amb} = 25 °C; note 3	–	0.75	W
		T_{amb} = 25 °C; note 4	–	0.54	W
T_{stg}	storage temperature		−55	+150	°C
T_j	operating junction temperature		−55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	0.5	A
I_{SM}	peak pulsed source current	note 2	–	2	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	140	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	20	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	0.4	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 16 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±8 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 0.6 A	–	–	200	mΩ
		V_{GS} = 2.5 V; I_D = 0.6 A	–	–	250	mΩ
		V_{GS} = 1.8 V; I_D = 0.3 A	–	–	300	mΩ
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 16 V; f = 1 MHz	–	145	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 16 V; f = 1 MHz	–	63.5	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 16 V; f = 1 MHz	–	27.5	–	pF
Q_G	total gate charge	V_{GS} = 4.5 V; V_{DD} = 20 V; I_D = 1 A; T_{amb} = 25 °C	–	3530	–	pC
Q_{GS}	gate-source charge	V_{DD} = 20 V; I_D = 1 A; T_{amb} = 25 °C	–	233	–	pC
Q_{GD}	gate-drain charge	V_{DD} = 20 V; I_D = 1 A; T_{amb} = 25 °C	–	1500	–	pC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to 8 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	2	–	ns
t_f	fall time	V_{GS} = 0 to 8 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	4.5	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to 8 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	6.5	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = 8 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	45	–	ns
t_r	rise time	V_{GS} = 8 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	20	–	ns
t_{off}	turn-off switching time	V_{GS} = 8 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	65	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 0.5 A	–	–	1	V
t_{rr}	reverse recovery time	I_S = 0.5 A; di/dt = −100 A/μs	–	170	–	ns

N-channel enhancement mode MOS transistor

BSH106

FEATURES

- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL, etc.
- Very low threshold.

APPLICATIONS

- Power management
- DC - DC converters
- 'Glue-logic': interface between logic blocks and/or periphery
- General purpose switch
- Battery powered applications.

DESCRIPTION

N-channel enhancement mode MOS transistor in a SOT363 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT363

PIN	SYMBOL	DESCRIPTION
1	d	drain
2	d	drain
3	g	gate
4	s	source
5	d	drain
6	d	drain

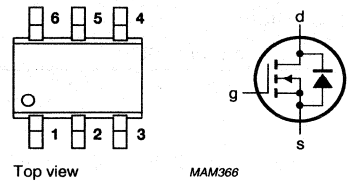


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	20	V
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 0.7 A	–	1	V
V_{GS}	gate-source voltage (DC)		–	±8	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	0.4	–	V
I_D	drain current (DC)	T_s = 80 °C	–	1.43	A
R_{DSon}	drain-source on-state resistance	V_{GS} = 2.5 V; I_D = 0.7 A	–	0.25	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	0.7	W

PRELIMINARY
Philips Semiconductors for Design-in information
See Philips Semiconductors

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	20	V
V_{GS}	gate-source voltage (DC)		–	±8	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	1.43	A
I_{DM}	peak drain current	note 2	–	5.74	A
P_{tot}	total power dissipation	T_s = 80 °C	–	0.7	W
		T_{amb} = 25 °C; note 3	–	0.98	W
		T_{amb} = 25 °C; note 4	–	0.66	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	0.7	A
I_{SM}	peak pulsed source current	note 2	–	2.8	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	100	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	20	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	0.4	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 16 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±8 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 0.7 A	–	–	200	mΩ
		V_{GS} = 2.5 V; I_D = 0.7 A	–	–	250	mΩ
		V_{GS} = 1.8 V; I_D = 3.5 A	–	–	300	mΩ
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 16 V; f = 1 MHz	–	145	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 16 V; f = 1 MHz	–	63.5	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 16 V; f = 1 MHz	–	27.5	–	pF
Q_G	total gate charge	V_{GS} = 4.5 V; V_{DD} = 20 V; I_D = 1 A; T_{amb} = 25 °C	–	3530	–	pC
Q_{GS}	gate-source charge	V_{DD} = 20 V; I_D = 1 A; T_{amb} = 25 °C	–	233	–	pC
Q_{GD}	gate-drain charge	V_{DD} = 20 V; I_D = 1 A; T_{amb} = 25 °C	–	1500	–	pC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to 8 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	2	–	ns
t_f	fall time	V_{GS} = 0 to 8 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	4.5	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to 8 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	6.5	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = 8 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	45	–	ns
t_r	rise time	V_{GS} = 8 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	20	–	ns
t_{off}	turn-off switching time	V_{GS} = 8 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	65	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 0.7 A	–	–	1	V
t_{rr}	reverse recovery time	I_S = 0.5 A; di/dt = –100 A/μs	–	170	–	ns

N-channel enhancement mode MOS transistor

BSH107

FEATURES

- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL, etc.
- Very low threshold.

APPLICATIONS

- 'Glue-logic': interface between logic blocks and/or periphery
- Power management
- DC to DC converters
- General purpose switch
- Battery powered applications.

DESCRIPTION

N-channel enhancement mode MOS transistor in a SOT457 (TSOP6) SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	d	drain
2	d	drain
3	g	gate
4	s	source
5	d	drain
6	d	drain

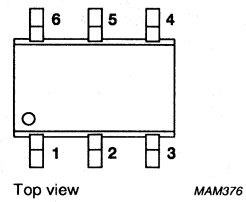


Fig.1 Simplified outline (SOT457) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	20	V
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 0.8 A	–	1	V
V_{GS}	gate-source voltage (DC)		–	±8	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	0.4	–	V
I_D	drain current (DC)	T_s = 80 °C	–	2.5	A
R_{DSon}	drain-source on-state resistance	V_{GS} = 2.5 V; I_D = 1.2 A	–	0.09	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	0.8	W

OBJECTIVE
See Philips Semiconductors for Design-in information

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	20	V
V_{GS}	gate-source voltage (DC)		–	±8	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	2.5	A
I_{DM}	peak drain current	note 2	–	10	A
P_{tot}	total power dissipation	T_s = 80 °C; note 1	–	0.8	W
		T_{amb} = 25 °C; note 3	–	1.09	W
		T_{amb} = 25 °C; note 4	–	0.7	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C; note 1	–	0.8	A
I_{SM}	peak pulsed source current	note 2	–	3.2	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	87.5	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	20	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	0.4	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 16 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{DS} = 0; V_{GS} = ±8 V	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 1.2 A	–	–	0.075	Ω
		V_{GS} = 2.5 V; I_D = 1.2 A	–	–	0.09	Ω
		V_{GS} = 1.8 V; I_D = 0.6 A	–	–	0.11	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 16 V; f = 1 MHz	–	t.b.f.	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 16 V; f = 1 MHz	–	t.b.f.	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 16 V; f = 1 MHz	–	t.b.f.	–	pF
Q_G	total gate charge	V_{GS} = 4.5 V; V_{DD} = 20 V; I_D = 1 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Q_{GS}	gate-source charge	V_{DD} = 20 V; I_D = 1 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Q_{GD}	gate-drain charge	V_{DD} = 20 V; I_D = 1 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to 8 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_f	fall time	V_{GS} = 0 to 8 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to 8 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = 8 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_r	rise time	V_{GS} = 8 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_{off}	turn-off switching time	V_{GS} = 8 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 0.8 A	–	–	1	V
t_{rr}	reverse recovery time	I_S = 0.5 A; di/dt = –100 A/μs	–	t.b.f.	–	ns

P-channel enhancement mode MOS transistor

BSH201

FEATURES

- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL etc.

APPLICATIONS

- Power management
- DC to DC converters
- Battery powered applications
- 'Glue-logic'; interface between logic blocks and/or periphery
- General purpose switch.

DESCRIPTION

P-channel enhancement mode MOS transistor in a SOT23 SMD package.

PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain

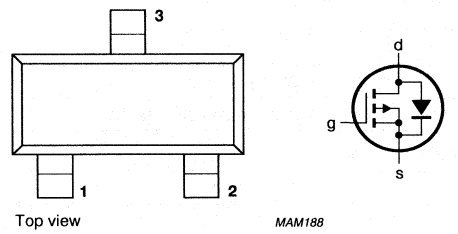


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–60	V
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = –0.38 A	–	–1.3	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = –1 mA	–1	–	V
I_D	drain current (DC)	T_s = 80 °C	–	–0.44	A
R_{DSon}	drain-source on-state resistance	V_{GS} = –10 V; I_D = –0.16 A	–	2.5	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

OBJECTIVE
See Philips Semiconductors for Design-in information

P-channel enhancement mode MOS transistor

BSH201

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	−60	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	−0.34	A
I_{DM}	peak drain current	note 2	–	−1.37	A
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W
		T_{amb} = 25 °C; note 3	–	0.75	W
		T_{amb} = 25 °C; note 4	–	0.54	W
T_{stg}	storage temperature		−55	+150	°C
T_j	operating junction temperature		−55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	−0.38	A
I_{SM}	peak pulsed source current	note 2	–	−1.52	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	140	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−60	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−1	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −48 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = −10 V; I_D = −0.16 A	–	–	2.5	Ω
		V_{GS} = −4.5 V; I_D = −0.08 A	–	–	3.75	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −48 V; f = 1 MHz	–	tbf	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −48 V; f = 1 MHz	–	tbf	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −48 V; f = 1 MHz	–	tbf	–	pF
Q_G	total gate charge	V_{GS} = −10 V; V_{DD} = −10 V; I_D = −0.5 A; T_{amb} = 25 °C	–	tbf	–	pC
Q_{GS}	gate-source charge	V_{DD} = −10 V; I_D = −0.5 A; T_{amb} = 25 °C	–	tbf	–	pC
Q_{GD}	gate-drain charge	V_{DD} = −10 V; I_D = −0.5 A; T_{amb} = 25 °C	–	tbf	–	pC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to −10 V; V_{DD} = −10 V; I_D = −0.5 A; R_{gen} = 6 Ω	–	tbf	–	ns
t_r	rise time	V_{GS} = 0 to −10 V; V_{DD} = −10 V; I_D = −0.5 A; R_{gen} = 6 Ω	–	tbf	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to −10 V; V_{DD} = −10 V; I_D = −0.5 A; R_{gen} = 6 Ω	–	tbf	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = −10 to 0 V; V_{DD} = −10 V; I_D = −0.5 A; R_{gen} = 6 Ω	–	tbf	–	ns
t_f	fall time	V_{GS} = −10 to 0 V; V_{DD} = −10 V; I_D = −0.5 A; R_{gen} = 6 Ω	–	tbf	–	ns
t_{off}	turn-off switching time	V_{GS} = −10 to 0 V; V_{DD} = −10 V; I_D = −0.5 A; R_{gen} = 6 Ω	–	tbf	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = −0.38 A	–	–	−1.3	V
t_{rr}	reverse recovery time	I_S = −0.25 A; di/dt = 100 A/μs	–	tbf	–	ns

P-channel enhancement mode MOS transistor

BSH202

FEATURES

- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL etc.

APPLICATIONS

- Power management
- DC to DC converters
- Battery powered applications
- 'Glue-logic'; interface between logic blocks and/or periphery
- General purpose switch.

DESCRIPTION

P-channel enhancement mode MOS transistor in a SOT23 SMD package.

PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain

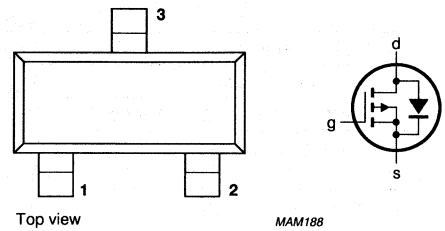


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = –0.38 A	–	–1.3	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = –1 mA	–1	–	V
I_D	drain current (DC)	T_s = 80 °C	–	–0.57	A
R_{DSon}	drain-source on-state resistance	V_{GS} = –10 V; I_D = –0.28 A	–	0.9	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

PRELIMINARY
See Philips Semiconductors for Design-in information

P-channel enhancement mode MOS transistor

BSH202

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	–0.57	A
I_{DM}	peak drain current	note 2	–	–2.29	A
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W
		T_{amb} = 25 °C; note 3	–	0.75	W
		T_{amb} = 25 °C; note 4	–	0.54	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	–0.38	A
I_{SM}	peak pulsed source current	note 2	–	–1.52	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

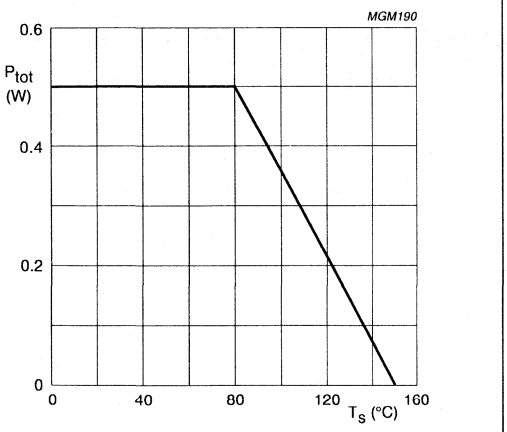
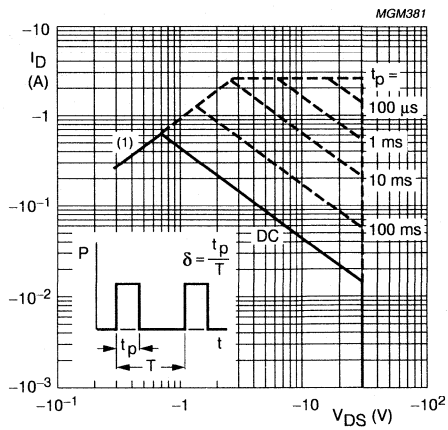


Fig.2 Power derating curve.

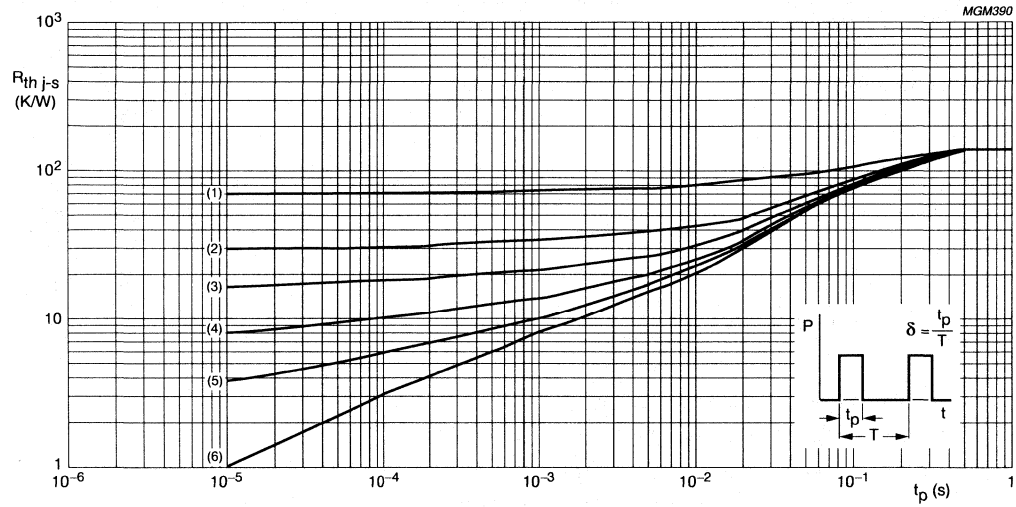


T_{amb} = 25 °C.
(1) R_{DSon} limitation.

Fig.3 SOAR.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	140	K/W



(1) $\delta = 0.5$. (2) $\delta = 0.2$. (3) $\delta = 0.1$.
(4) $\delta = 0.05$. (5) $\delta = 0.02$. (6) $\delta = 0$.

Fig.4 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−1	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −24 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = −10 V; I_D = −0.28 A	–	–	0.9	Ω
		V_{GS} = −4.5 V; I_D = −0.14 A	–	–	1.35	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	75	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	28	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	7.3	–	pF
Q_G	total gate charge	V_{GS} = −10 V; V_{DD} = −15 V; I_D = −0.3 A; T_{amb} = 25 °C	–	2200	–	pC
Q_{GS}	gate-source charge	V_{DD} = −15 V; I_D = −0.3 A; T_{amb} = 25 °C	–	200	–	pC
Q_{GD}	gate-drain charge	V_{DD} = −15 V; I_D = −0.3 A; T_{amb} = 25 °C	–	400	–	pC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to −10 V; V_{DD} = −15 V; I_D = −0.5 A; R_{gen} = 6 Ω	–	1.8	–	ns
t_r	rise time	V_{GS} = 0 to −10 V; V_{DD} = −15 V; I_D = −0.5 A; R_{gen} = 6 Ω	–	3.2	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to −10 V; V_{DD} = −15 V; I_D = −0.5 A; R_{gen} = 6 Ω	–	5	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = −10 to 0 V; V_{DD} = −15 V; I_D = −0.5 A; R_{gen} = 6 Ω	–	20	–	ns
t_f	fall time	V_{GS} = −10 to 0 V; V_{DD} = −15 V; I_D = −0.5 A; R_{gen} = 6 Ω	–	9	–	ns
t_{off}	turn-off switching time	V_{GS} = −10 to 0 V; V_{DD} = −15 V; I_D = −0.5 A; R_{gen} = 6 Ω	–	29	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = −0.5 A	–	–	−1.3	V
t_{rr}	reverse recovery time	I_S = −0.5 A; di/dt = 100 A/μs	–	71	–	ns

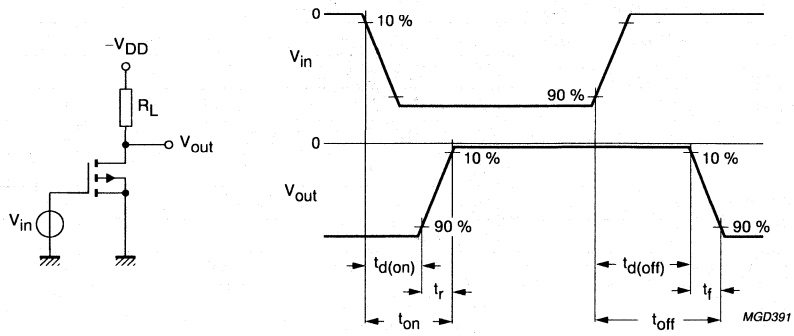
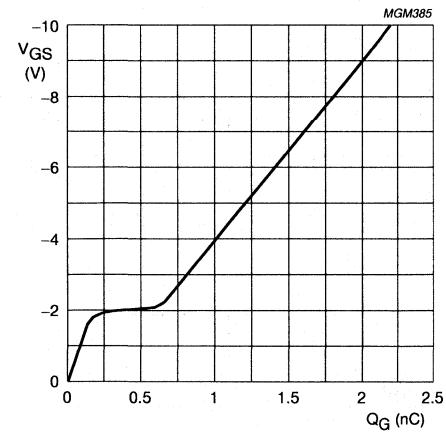
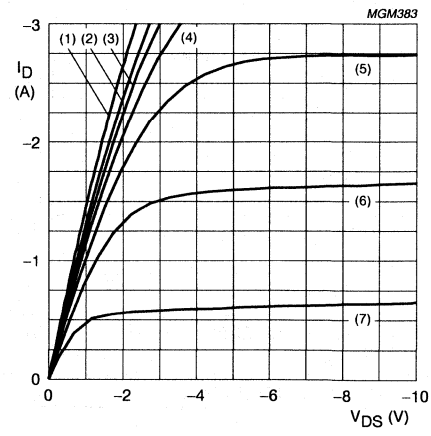


Fig.5 Switching times test circuit with input and output waveforms.



V_{DD} = −15 V; I_D = −0.3 A; T_{amb} = 25 °C.

Fig.6 Gate-source voltage as a function of gate charge; typical values.



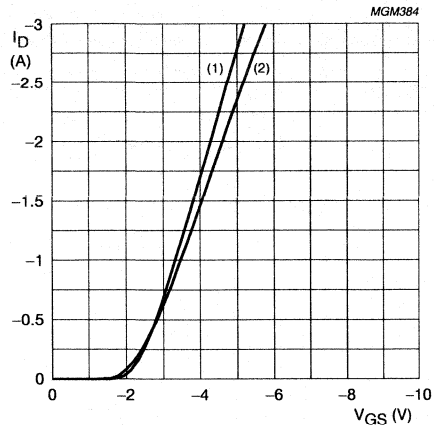
T_{amb} = 25 °C; t_p = 300 µs; δ = 0.

(1) V_{GS} = −10 V.
(2) V_{GS} = −8 V.
(3) V_{GS} = −7 V.
(4) V_{GS} = −6 V.
(5) V_{GS} = −5 V.
(6) V_{GS} = −4 V.
(7) V_{GS} = −3 V.

Fig.7 Output characteristics; typical values.

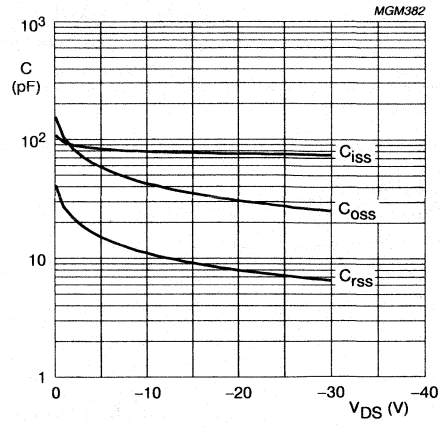
P-channel enhancement mode MOS transistor

BSH202



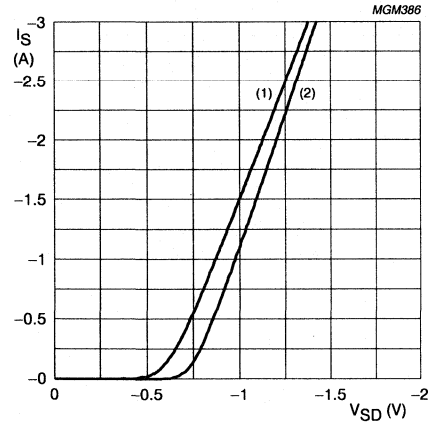
V_{DS} = −10 V; t_p = 300 µs; δ = 0.
(1) T_{amb} = 25 °C.
(2) T_{amb} = 150 °C.

Fig.8 Transfer characteristic; typical values.



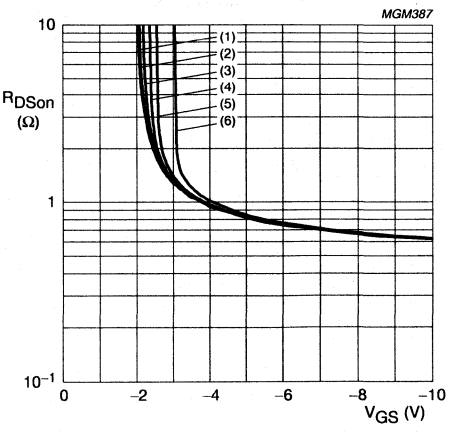
V_{GS} = 0 ; f = 1 MHz; T_j = 25 °C.

Fig.9 Capacitance as a function of drain-source voltage; typical values.



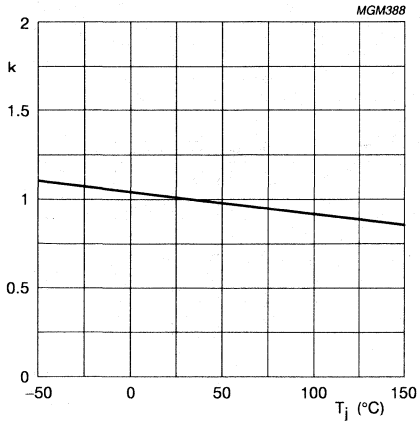
V_{GD} = 0.
(1) T_{amb} = 150 °C.
(2) T_{amb} = 25 °C.

Fig.10 Source current as a function of source-drain diode forward voltage; typical values.



T_{amb} = 25 °C; t_p = 300 µs; δ = 0.
(1) I_D = −10 mA.
(2) I_D = −20 mA.
(3) I_D = −50 mA.
(4) I_D = −100 mA.
(5) I_D = −200 mA.
(6) I_D = −500 mA.

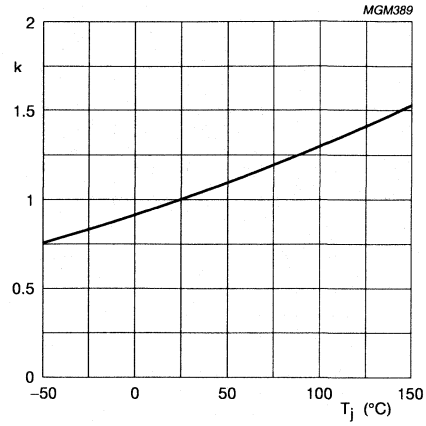
Fig.11 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

V_{GSth} at $V_{DS} = V_{GS}$; $I_D = -1$ mA.

Fig.12 Temperature coefficient of gate-source threshold voltage as a function of junction temperature; typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

R_{DSon} at $V_{GS} = -10$ V; $I_D = -0.3$ A.

Fig.13 Temperature coefficient of drain-source on-resistance as a function of junction temperature; typical values.

P-channel enhancement mode MOS transistor

BSH203

FEATURES

- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL, etc.

APPLICATIONS

- 'Glue-logic': interface between logic blocks and/or periphery
- Power management
- DC to DC converters
- General purpose switch
- Battery powered applications.

DESCRIPTION

P-channel enhancement mode MOS transistor in a SOT23 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain

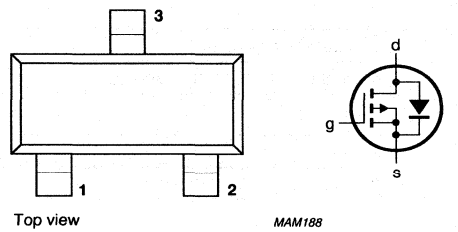


Fig.1 Simplified outline (SOT23) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = –0.38 A	–	–1.3	V
V_{GS}	gate-source voltage (DC)		–	±8	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = –1 mA	–0.4	–	V
I_D	drain current (DC)	T_s = 80 °C	–	–0.57	A
R_{DSon}	drain-source on-state resistance	V_{GS} = –2.5 V; I_D = –0.28 A	–	1.1	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W

PRELIMINARY
See Philips Semiconductors for Design-in information

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{GS}	gate-source voltage (DC)		–	±8	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	–0.57	A
I_{DM}	peak drain current	note 2	–	–2.29	A
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W
		T_{amb} = 25 °C; note 3	–	0.75	W
		T_{amb} = 25 °C; note 4	–	0.54	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	–0.38	A
I_{SM}	peak pulsed source current	note 2	–	–1.52	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	140	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−0.4	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −24 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{DS} = 0; V_{GS} = ±8 V	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = −4.5 V; I_D = −0.28 A	–	–	0.9	Ω
		V_{GS} = −2.5 V; I_D = −0.28 A	–	–	1.1	Ω
		V_{GS} = −1.8 V; I_D = −0.14 A	–	–	1.2	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	125	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	25.6	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	6.55	–	pF
Q_G	total gate charge	V_{GS} = −4.5 V; V_{DD} = −10 V; I_D = −0.5 A; T_{amb} = 25 °C	–	1970	–	pC
Q_{GS}	gate-source charge	V_{DD} = −10 V; I_D = −0.5 A; T_{amb} = 25 °C	–	173	–	pC
Q_{GD}	gate-drain charge	V_{DD} = −10 V; I_D = −0.5 A; T_{amb} = 25 °C	–	400	–	pC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to −8 V; V_{DD} = −10 V; I_D = −0.5 A; R_{gen} = 6 Ω	–	1.5	–	ns
t_r	rise time	V_{GS} = 0 to −8 V; V_{DD} = −10 V; I_D = −0.5 A; R_{gen} = 6 Ω	–	3	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to −8 V; V_{DD} = −10 V; I_D = −0.5 A; R_{gen} = 6 Ω	–	4.5	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = −8 to 0 V; V_{DD} = −10 V; I_D = −0.5 A; R_{gen} = 6 Ω	–	30	–	ns
t_f	fall time	V_{GS} = −8 to 0 V; V_{DD} = −10 V; I_D = −0.5 A; R_{gen} = 6 Ω	–	15	–	ns
t_{off}	turn-off switching time	V_{GS} = −8 to 0 V; V_{DD} = −10 V; I_D = −0.5 A; R_{gen} = 6 Ω	–	45	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = −0.38 A	–	–	−1.3	V
t_{rr}	reverse recovery time	I_S = −0.5 A; di/dt = 100 A/μs	–	40	–	ns

P-channel enhancement mode MOS transistor

BSH205

FEATURES

- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL, etc.
- Very low threshold.

APPLICATIONS

- Power management
- DC - DC converters
- General purpose switch
- 'Glue-logic': interface between logic blocks and/or periphery
- Battery powered applications.

DESCRIPTION

P-channel enhancement mode MOS transistor in a SOT23 plastic SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain

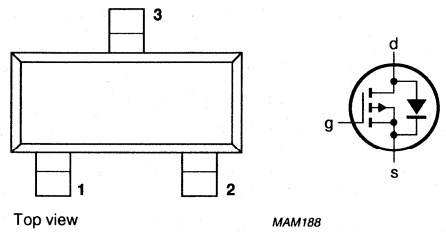


Fig.1 Simplified outline SOT23 and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–12	V
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = –0.38 A	–	–1.3	V
V_{GS}	gate-source voltage (DC)		–	±8	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = –1 mA	–0.4	–	V
I_D	drain current (DC)	T_s = 80 °C	–	–0.86	A
R_{DSon}	drain-source on-state resistance	V_{GS} = –2.5 V; I_D = –0.43 A	–	0.5	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W

PRELIMINARY
See Philips Semiconductors for Design-in information

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–12	V
V_{GS}	gate-source voltage (DC)		–	±8	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	–0.86	A
I_{DM}	peak drain current	note 2	–	–3.43	A
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W
		T_{amb} = 25 °C; note 3	–	0.75	W
		T_{amb} = 25 °C; note 4	–	0.54	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	–0.38	A
I_{SM}	peak pulsed source current	note 2	–	–1.52	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	140	K/W

P-channel enhancement mode MOS transistor

BSH205

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−12	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−0.4	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −9.6 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±8 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = −4.5 V; I_D = −0.43 A	–	–	0.4	Ω
		V_{GS} = −2.5 V; I_D = −0.43 A	–	–	0.5	Ω
		V_{GS} = −1.8 V; I_D = −0.21 A	–	–	0.6	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −9.6 V; f = 1 MHz	–	195	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −9.6 V; f = 1 MHz	–	90.3	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −9.6 V; f = 1 MHz	–	38.3	–	pF
Q_G	total gate charge	V_{GS} = −4.5 V; V_{DD} = −10 V; I_D = −0.5 A; T_{amb} = 25 °C	–	3500	–	pC
Q_{GS}	gate-source charge	V_{DD} = −10 V; I_D = −0.5 A; T_{amb} = 25 °C	–	233	–	pC
Q_{GD}	gate-drain charge	V_{DD} = −10 V; I_D = −0.5 A; T_{amb} = 25 °C	–	1100	–	pC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to −8 V; V_{DD} = −10 V; I_D = −0.5 A; R_{gen} = 6 Ω	–	1.5	–	ns
t_r	rise time	V_{GS} = 0 to −8 V; V_{DD} = −10 V; I_D = −0.5 A; R_{gen} = 6 Ω	–	3.5	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to −8 V; V_{DD} = −10 V; I_D = −0.5 A; R_{gen} = 6 Ω	–	6	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = −8 to 0 V; V_{DD} = −10 V; I_D = −0.5 A; R_{gen} = 6 Ω	–	120	–	ns
t_f	fall time	V_{GS} = −8 to 0 V; V_{DD} = −10 V; I_D = −0.5 A; R_{gen} = 6 Ω	–	50	–	ns
t_{off}	turn-off switching time	V_{GS} = −8 to 0 V; V_{DD} = −10 V; I_D = −0.5 A; R_{gen} = 6 Ω	–	170	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = −0.38 A	–	–	−1.3	V

P-channel enhancement mode MOS transistor

BSH206

FEATURES

- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL, etc.
- Very low threshold.

APPLICATIONS

- Power management
- DC - DC converters
- General purpose switch
- 'Glue-logic': interface between logic blocks and/or periphery
- Battery powered applications.

DESCRIPTION

P-channel enhancement mode MOS transistor in a SOT363 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT363

PIN	SYMBOL	DESCRIPTION
1	d	drain
2	d	drain
3	g	gate
4	s	source
5	d	drain
6	d	drain

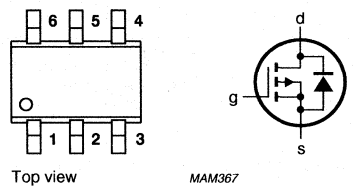


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–12	V
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = –0.54 A	–	–1.3	V
V_{GS}	gate-source voltage (DC)		–	±8	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = –1 mA	–0.4	–	V
I_D	drain current (DC)	T_s = 80 °C	–	–1	A
R_{DSon}	drain-source on-state resistance	V_{GS} = –2.5 V; I_D = –0.5 A	–	0.5	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	0.7	W

PRELIMINARY
See Philips Semiconductors for Design-in information

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–12	V
V_{GS}	gate-source voltage (DC)		–	±8	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	–1	A
I_{DM}	peak drain current	note 2	–	–4	A
P_{tot}	total power dissipation	T_s = 80 °C	–	0.7	W
		T_{amb} = 25 °C; note 3	–	0.98	W
		T_{amb} = 25 °C; note 4	–	0.66	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	–0.54	A
I_{SM}	peak pulsed source current	note 2	–	–2.16	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	100	K/W

P-channel enhancement mode MOS transistor

BSH206

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−12	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−0.4	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −9.6 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±8 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = −4.5 V; I_D = −0.5 A	–	–	0.4	Ω
		V_{GS} = −2.5 V; I_D = −0.5 A	–	–	0.5	Ω
		V_{GS} = −1.8 V; I_D = −0.25 A	–	–	0.6	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −9.6 V; f = 1 MHz	–	195	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −9.6 V; f = 1 MHz	–	90.3	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −9.6 V; f = 1 MHz	–	38.3	–	pF
Q_G	total gate charge	V_{GS} = −4.5 V; V_{DD} = −10 V; I_D = −0.5 A; T_{amb} = 25 °C	–	3500	–	pC
Q_{GS}	gate-source charge	V_{DD} = −10 V; I_D = −0.5 A; T_{amb} = 25 °C	–	233	–	pC
Q_{GD}	gate-drain charge	V_{DD} = −10 V; I_D = −0.5 A; T_{amb} = 25 °C	–	1100	–	pC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to −8 V; V_{DD} = −10 V; I_D = −0.5 A; R_{gen} = 6 Ω	–	1.5	–	ns
t_r	rise time	V_{GS} = 0 to −8 V; V_{DD} = −10 V; I_D = −0.5 A; R_{gen} = 6 Ω	–	3.5	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to −8 V; V_{DD} = −10 V; I_D = −0.5 A; R_{gen} = 6 Ω	–	5	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = −8 to 0 V; V_{DD} = −10 V; I_D = −0.5 A; R_{gen} = 6 Ω	–	120	–	ns
t_f	fall time	V_{GS} = −8 to 0 V; V_{DD} = −10 V; I_D = −0.5 A; R_{gen} = 6 Ω	–	50	–	ns
t_{off}	turn-off switching time	V_{GS} = −8 to 0 V; V_{DD} = −10 V; I_D = −0.5 A; R_{gen} = 6 Ω	–	170	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = −0.54 A	–	–	−1.3	V

P-channel enhancement mode MOS transistor

BSH207

FEATURES

- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL, etc.
- Very low threshold.

APPLICATIONS

- 'Glue-logic': interface between logic blocks and/or periphery
- Power management
- DC to DC converters
- General purpose switch
- Battery powered applications.

DESCRIPTION

P-channel enhancement mode MOS transistor in a SOT457 (TSOP6) SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	d	drain
2	d	drain
3	g	gate
4	s	source
5	d	drain
6	d	drain

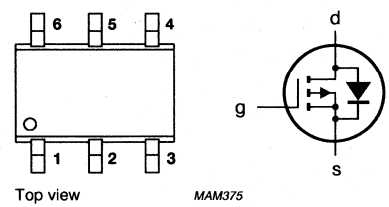


Fig.1 Simplified outline (SOT457) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–12	V
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = –0.62 A	–	–1.3	V
V_{GS}	gate-source voltage (DC)		–	±8	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = –1 mA	–0.4	–	V
I_D	drain current (DC)	T_s = 80 °C	–	–2	A
R_{DSon}	drain-source on-state resistance	V_{GS} = –2.5 V; I_D = –1 A	–	0.15	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	0.8	W

OBJECTIVE
See Philips Semiconductors for Design-in information

P-channel enhancement mode MOS transistor

BSH207

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	−12	V
V_{GS}	gate-source voltage (DC)		–	±8	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	−2	A
I_{DM}	peak drain current	note 2	–	−7.9	A
P_{tot}	total power dissipation	T_s = 80 °C; note 1	–	0.8	W
		T_{amb} = 25 °C; note 3	–	1.09	W
		T_{amb} = 25 °C; note 4	–	0.7	W
T_{stg}	storage temperature		−55	+150	°C
T_j	operating junction temperature		−55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C; note 1	–	−0.62	A
I_{SM}	peak pulsed source current	note 2	–	−2.48	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	87.5	K/W

P-channel enhancement mode MOS transistor

BSH207

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−12	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−0.4	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −9.6 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{DS} = 0; V_{GS} = ±8 V	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = −4.5 V; I_D = −1 A	–	–	0.12	Ω
		V_{GS} = −2.5 V; I_D = −1 A	–	–	0.15	Ω
		V_{GS} = −1.8 V; I_D = −0.5 A	–	–	0.18	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −9.6 V; f = 1 MHz	–	t.b.f.	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −9.6 V; f = 1 MHz	–	t.b.f.	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −9.6 V; f = 1 MHz	–	t.b.f.	–	pF
Q_G	total gate charge	V_{GS} = −4.5 V; V_{DD} = −10 V; I_D = −1 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Q_{GS}	gate-source charge	V_{DD} = −10 V; I_D = −1 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Q_{GD}	gate-drain charge	V_{DD} = −10 V; I_D = −1 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to −8 V; V_{DD} = −10 V; I_D = −1 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_r	rise time	V_{GS} = 0 to −8 V; V_{DD} = −10 V; I_D = −1 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to −8 V; V_{DD} = −10 V; I_D = −1 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = −8 to 0 V; V_{DD} = −10 V; I_D = −1 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_f	fall time	V_{GS} = −8 to 0 V; V_{DD} = −10 V; I_D = −1 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_{off}	turn-off switching time	V_{GS} = −8 to 0 V; V_{DD} = −10 V; I_D = −1 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = −0.62 A	–	–	−1.3	V
t_{rr}	reverse recovery time	I_S = −0.5 A; di/dt = 100 A/μs	–	t.b.f.	–	ns

P-channel enhancement mode MOS transistor BSH299

FEATURES

- Low threshold voltage
- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL, etc.

APPLICATIONS

- Power management
- Battery powered applications e.g. cellular phones
- General purpose switch.

DESCRIPTION

P-channel enhancement mode MOS transistor in a SOT363 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT363

PIN	SYMBOL	DESCRIPTION
1	d	drain
2	d	drain
3	g	gate
4	s	source
5	d	drain
6	d	drain

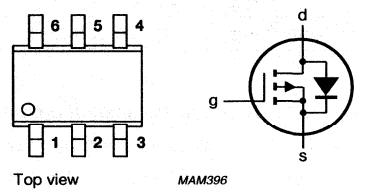


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–50	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = –1 mA; V_{DS} = V_{GS}	–0.8	–2	V
I_D	drain current (DC)	T_s = 80 °C	–	–0.2	A
R_{DSon}	drain-source on-state resistance	I_D = –0.13 A; V_{GS} = –10 V	–	10	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	0.7	W

OBJECTIVE
See Philips Semiconductors for Design-in information

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–50	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	–0.2	A
I_{DM}	peak drain current	note 2	–	–0.8	A
P_{tot}	total power dissipation	T_s = 80 °C; see Fig.2	–	0.7	W
		T_{amb} = 25 °C; note 3; see Fig.2	–	0.98	W
		T_{amb} = 25 °C; note 4; see Fig.2	–	0.66	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	150	°C

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on a printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on a printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point; see Fig.4	100	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−50	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−0.8	–	−2	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −40 V	–	–	−100	nA
		V_{GS} = 0; V_{DS} = −50 V	–	–	−10	μA
		V_{GS} = 0; V_{DS} = −50 V; T_j = 125 °C	–	–	−60	μA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±10	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = −10 V; I_D = −0.13 A; see Fig.10	–	–	10	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = −25 V; I_D = −0.13 A	50	–	–	mS
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −25 V; f = 1 MHz; see Fig.7	–	25	45	pF
C_{oss}	output capacitance		–	15	25	pF
C_{rss}	reverse transfer capacitance		–	3.5	12	pF
Switching times (see Figs 5 and 6)						
t_{on}	turn-on switching time	V_{GS} = 0 to −10 V; V_{DD} = −40 V; I_D = −0.2 A	–	3	–	ns
t_{off}	turn-off switching time	V_{GS} = −10 to 0 V; V_{DD} = −40 V; I_D = −0.2 A	–	7	–	ns

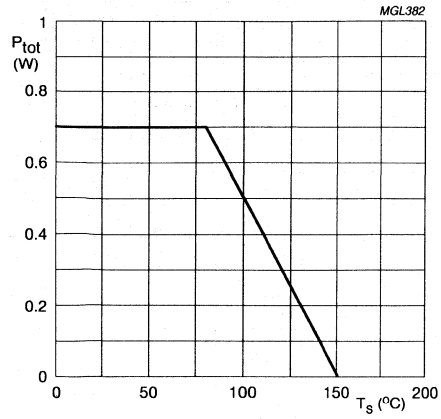


Fig.2 Power derating curve.

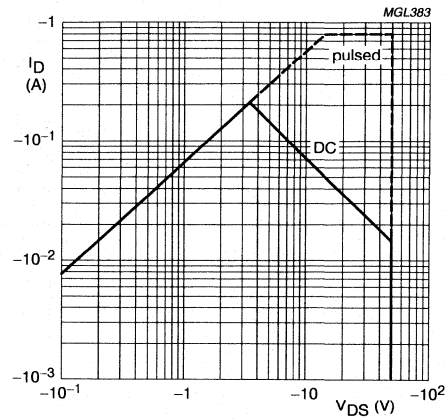


Fig.3 SOAR.

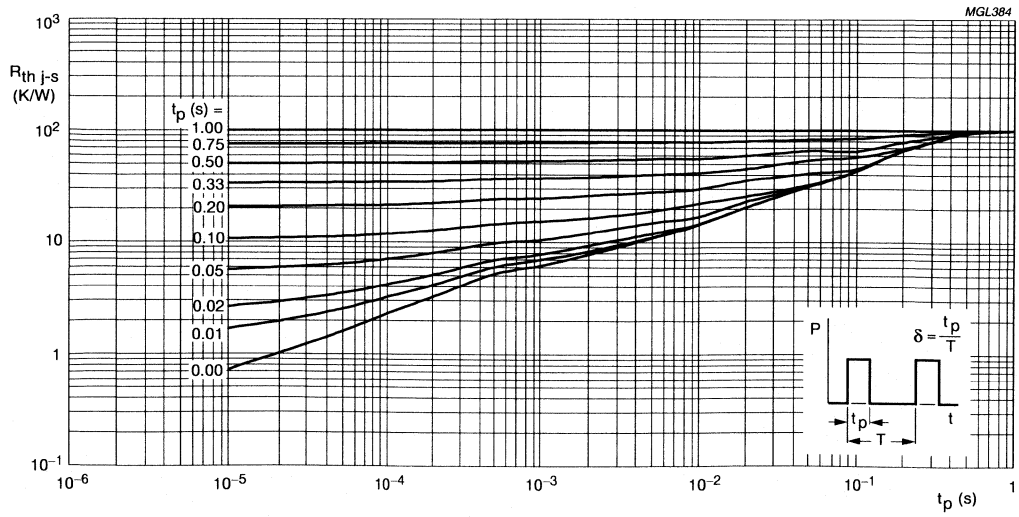


Fig.4 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

P-channel enhancement mode MOS transistor BSH299

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−50	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−0.8	–	−2	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −40 V	–	–	−100	nA
		V_{GS} = 0; V_{DS} = −50 V	–	–	−10	μA
		V_{GS} = 0; V_{DS} = −50 V; T_j = 125 °C	–	–	−60	μA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±10	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = −10 V; I_D = −0.13 A; see Fig.10	–	–	10	Ω
$\|y_{fs}\|$	forward transfer admittance	V_{DS} = −25 V; I_D = −0.13 A	50	–	–	mS
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −25 V; f = 1 MHz; see Fig.7	–	25	45	pF
C_{oss}	output capacitance		–	15	25	pF
C_{rss}	reverse transfer capacitance		–	3.5	12	pF
Switching times (see Figs 5 and 6)						
t_{on}	turn-on switching time	V_{GS} = 0 to −10 V; V_{DD} = −40 V; I_D = −0.2 A	–	3	–	ns
t_{off}	turn-off switching time	V_{GS} = −10 to 0 V; V_{DD} = −40 V; I_D = −0.2 A	–	7	–	ns

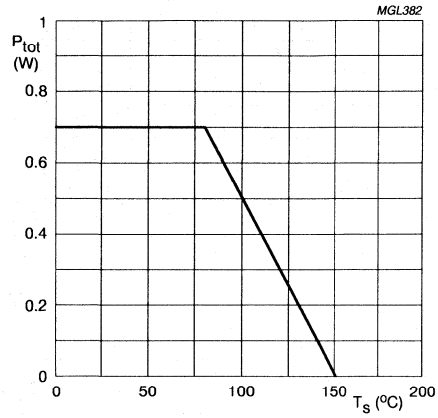


Fig.2 Power derating curve.

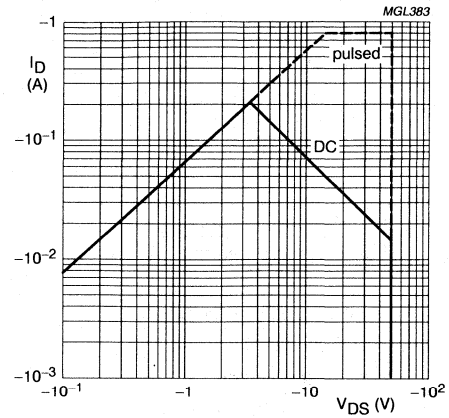


Fig.3 SOAR.

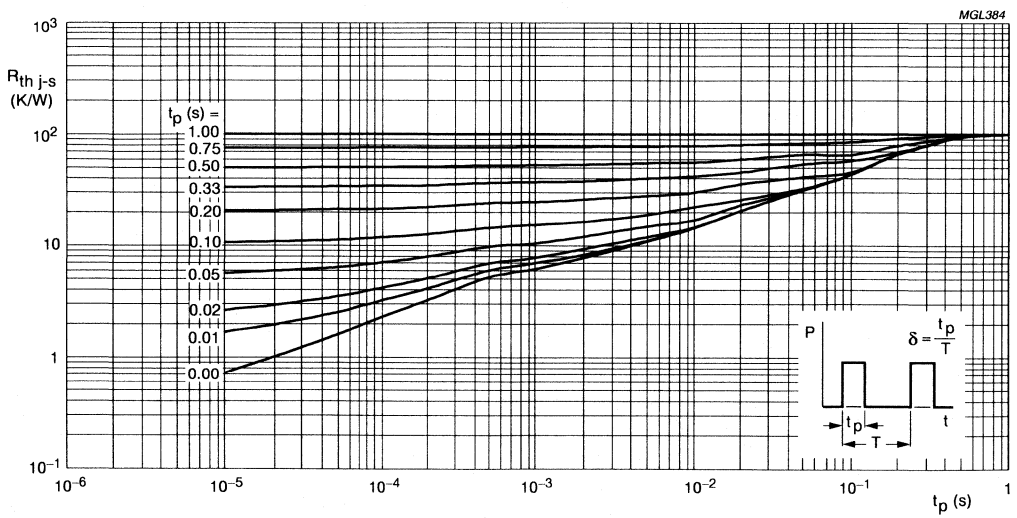


Fig.4 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

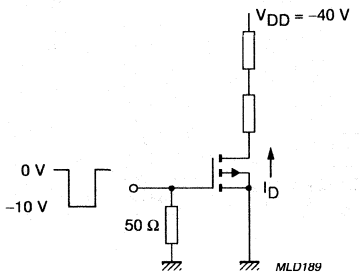


Fig.5 Switching time test circuit.

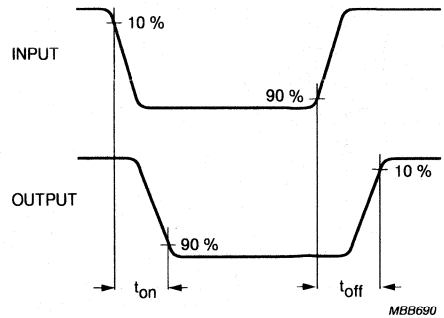
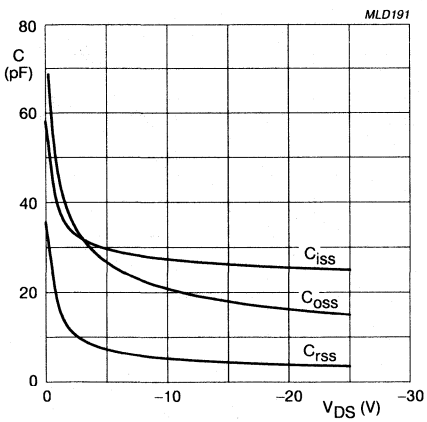
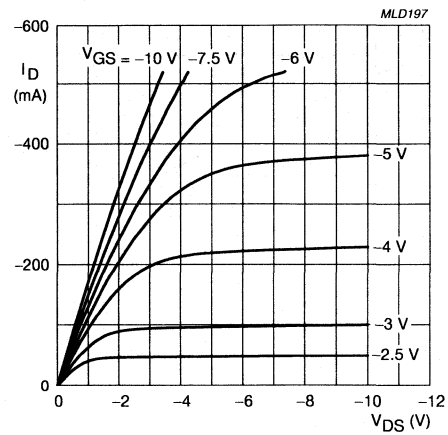


Fig.6 Input and output waveforms.



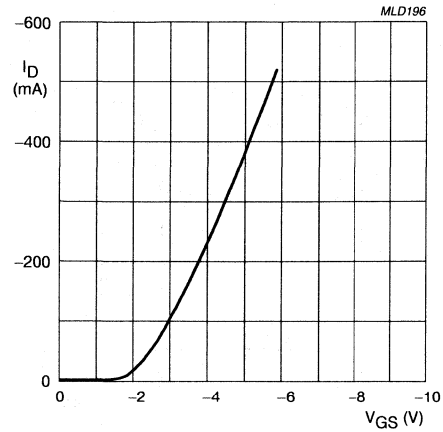
V_{GS} = 0; T_j = 25 °C; f = 1 MHz.

Fig.7 Capacitance as a function of drain-source voltage; typical values.



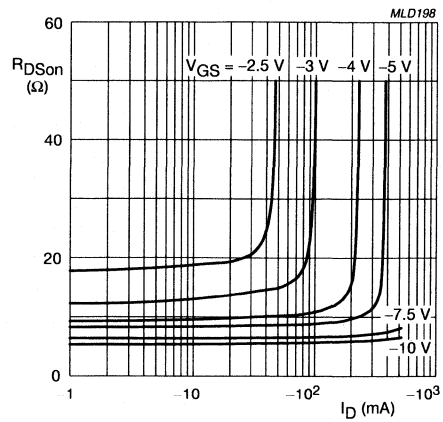
T_j = 25 °C.

Fig.8 Output characteristics; typical values.



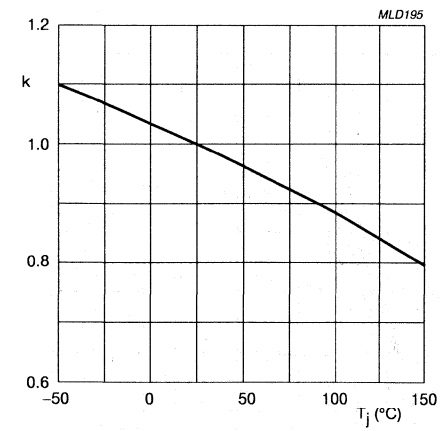
V_{DS} = −10 V; T_j = 25 °C.

Fig.9 Transfer characteristics; typical values.



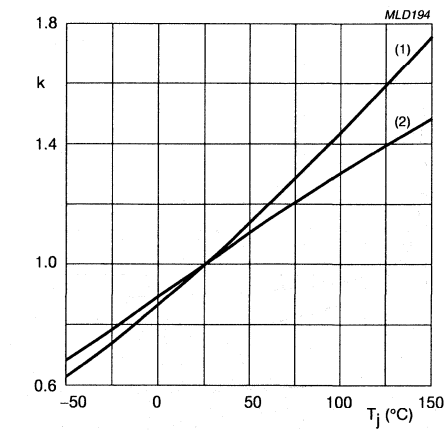
T_j = 25 °C; t_p = 300 μs; δ = 0.

Fig.10 Drain-source on-state resistance as a function of drain current; typical values.



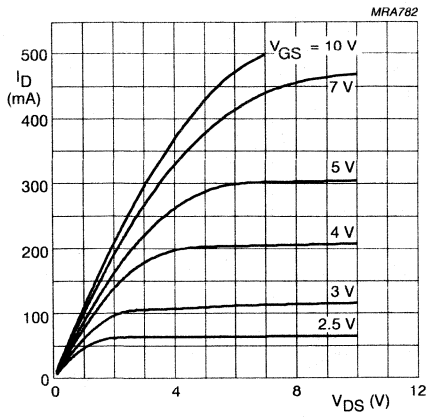
k = (V_{GSth} at T_j)/(V_{GSth} at 25 °C).
I_D = −1 mA; V_{DS} = V_{GS}.

Fig.11 Temperature coefficient of gate-source threshold voltage as a function of junction temperature; typical values.



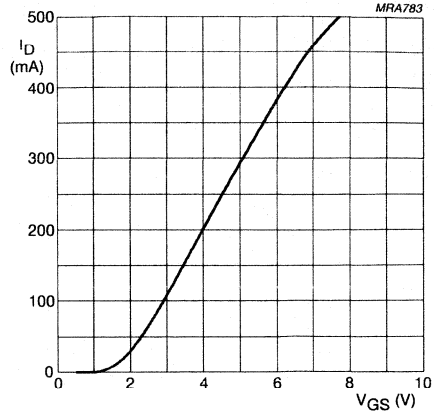
k = (R_{DSon} at T_j)/(R_{DSon} at 25 °C).
(1) I_D = −130 mA; V_{GS} = −10 V.
(2) I_D = −20 mA; V_{GS} = −2.4 V.

Fig.12 Temperature coefficient of drain-source on-resistance as a function of junction temperature; typical values.



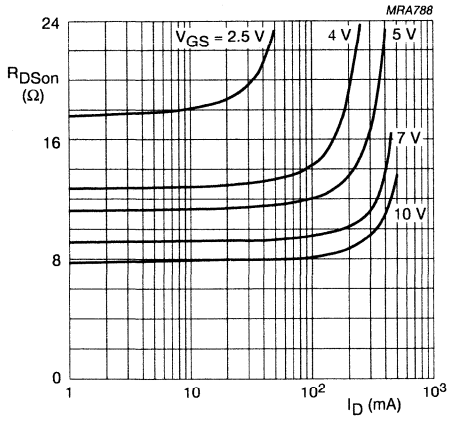
T_j = 25 °C.

Fig.4 Typical output characteristics.



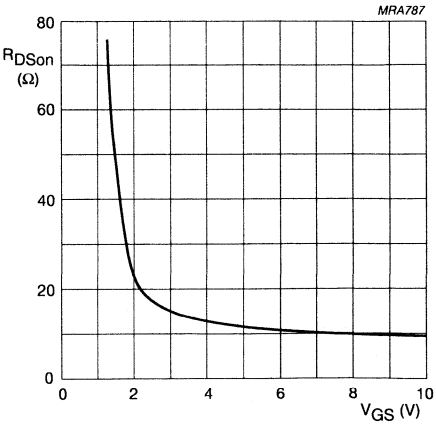
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Typical transfer characteristics.



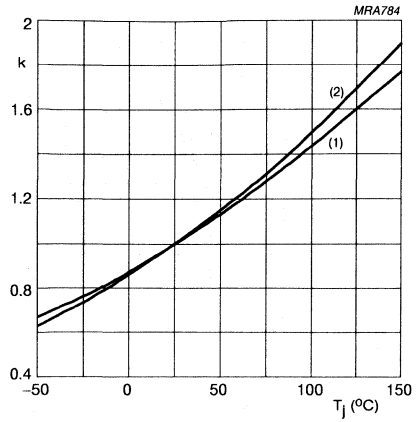
T_j = 25 °C.

Fig.6 Drain-source on-resistance as a function of drain current, typical values.



V_{DS} = 0.1 V; T_j = 25 °C.

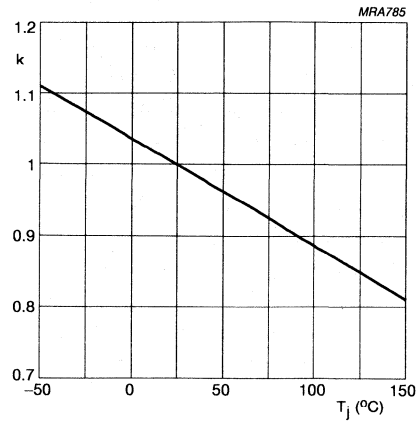
Fig.7 Drain-source on-resistance as a function of gate-source voltage, typical values.



$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}.$$

Typical $R_{DS(on)}$ at 100 mA/10 V.
(1) I_D = 10 mA; V_{GS} = 2.5 V.
(2) I_D = 100 mA; V_{GS} = 10 V.

Fig.8 Temperature coefficient of drain-source on-resistance.



$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ 25 °C}}.$$

Typical $V_{GS(th)}$ at 1 mA.

Fig.9 Temperature coefficient gate-source threshold voltage.

N-channel enhancement mode vertical D-MOS transistor

BSN20

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

APPLICATIONS

- Thin and thick film circuits
- General purpose fast switching applications.

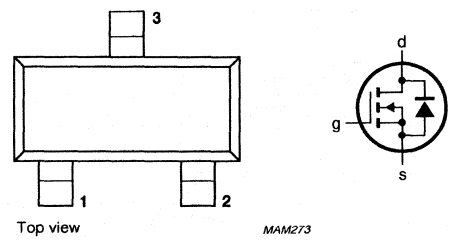
DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT23 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain



Marking code: M8p.

Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		50	V
I_D	drain current (DC)		100	mA
R_{DSon}	drain-source on-state resistance	I_D = 100 mA; V_{GS} = 10 V	15	Ω
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	1.8	V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	50	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	100	mA
I_{DM}	peak drain current		–	300	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C; note 1	–	300	mW
		up to T_{amb} = 25 °C; note 2	–	250	mW
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	430	K/W
		note 2	500	K/W

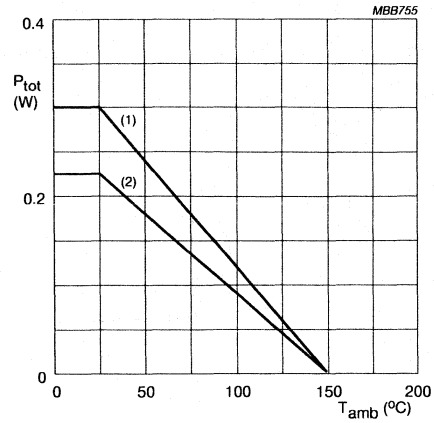
Notes to the Limiting values and Thermal characteristics

1. Device mounted on a ceramic substrate, 10 × 8 × 0.7 mm.
2. Device mounted on a printed-circuit board.

CHARACTERISTICS

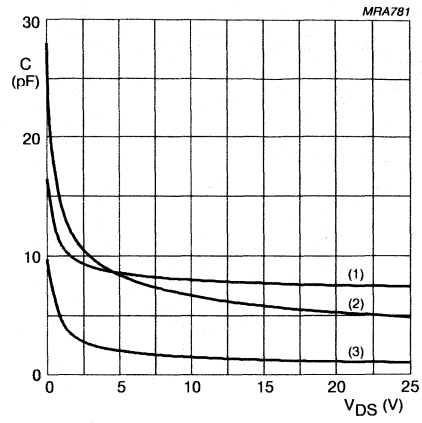
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	50	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	0.4	–	1.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 40 V	–	–	1	μA
I_{GSS}	gate-source leakage current	V_{DS} = 0; V_{GS} = ±20 V	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 100 mA	–	8	15	Ω
		V_{GS} = 5 V; I_D = 100 mA	–	14	20	Ω
		V_{GS} = 2.5 V; I_D = 10 mA	–	18	30	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = 10 V; I_D = 100 mA	40	80	–	mS
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 10 V; f = 1 MHz	–	8	15	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 10 V; f = 1 MHz	–	7	15	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 10 V; f = 1 MHz	–	2	5	pF
Switching times						
t_{on}	turn-on time	V_{GS} = 0 to 10 V; V_{DD} = 20 V; I_D = 100 mA	–	2	5	ns
t_{off}	turn-off time	V_{GS} = 10 to 0 V; V_{DD} = 20 V; I_D = 100 mA	–	5	10	ns



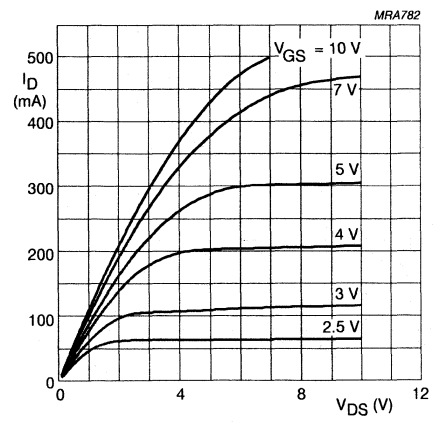
(1) Mounted on a ceramic substrate.
(2) Mounted on a printed-circuit board.

Fig.2 Power derating curves.



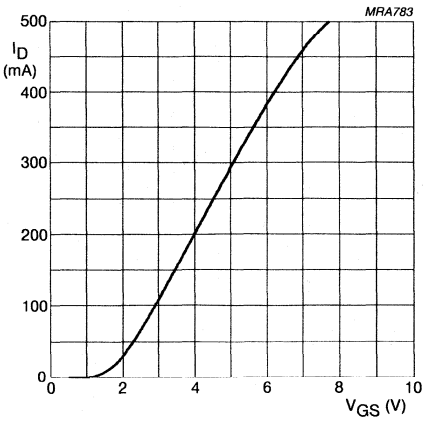
V_{GS} = 0; T_j = 25 °C; f = 1 MHz.
(1) C_{is}.
(2) C_{os}.
(3) C_{rs}.

Fig.3 Capacitance as a function of drain source voltage; typical values.



T_j = 25 °C.

Fig.4 Typical output characteristics.

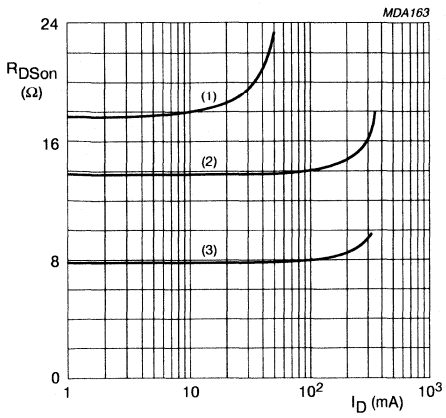


V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Typical transfer characteristics.

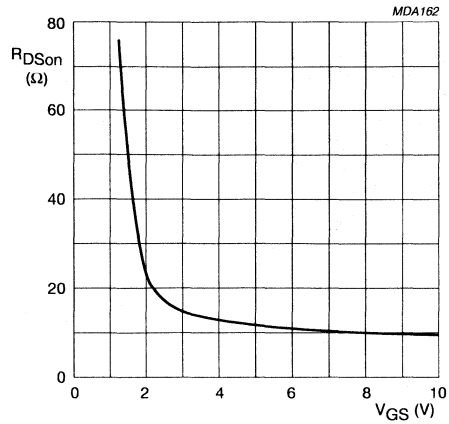
N-channel enhancement mode vertical D-MOS transistor

BSN20



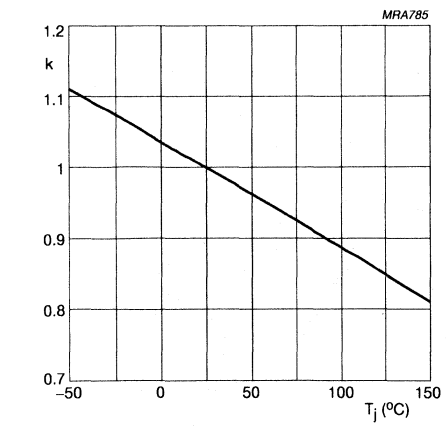
T_j = 25 °C.
(1) V_{GS} = 2.5 V.
(2) V_{GS} = 5 V.
(3) V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of drain current; typical values.



V_{DS} = 0.1 V; T_j = 25 °C.

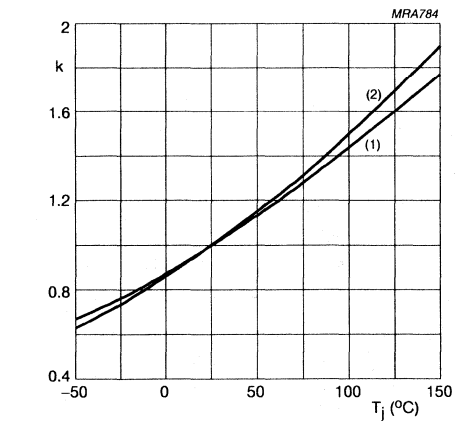
Fig.7 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

Typical V_{GSth} at 1 mA.

Fig.8 Temperature coefficient of gate-source threshold voltage.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

(1) I_D = 10 mA; V_{GS} = 2.5 V.
(2) I_D = 100 mA; V_{GS} = 10 V.

Fig.9 Temperature coefficient of drain-source on-state resistance.

N-channel enhancement mode vertical D-MOS transistor

BSN20W

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

APPLICATIONS

- Thin and thick film circuits
- General purpose fast switching applications.

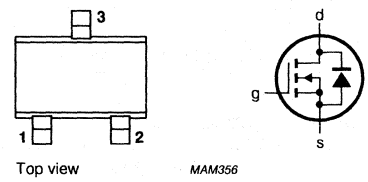
DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a 3 pin plastic SOT323 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT323

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain



Marking code: M8t.

Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		50	V
V_{GSth}	gate-source threshold voltage		1.8	V
I_D	drain current (DC)		80	mA
R_{DSon}	drain-source on-state resistance		15	Ω
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	200	mW

Note

1. Device mounted on a printed-circuit board.

N-channel enhancement mode vertical D-MOS transistor

BSN20W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	50	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	80	mA
I_{DM}	peak drain current		–	300	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	200	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	625	K/W

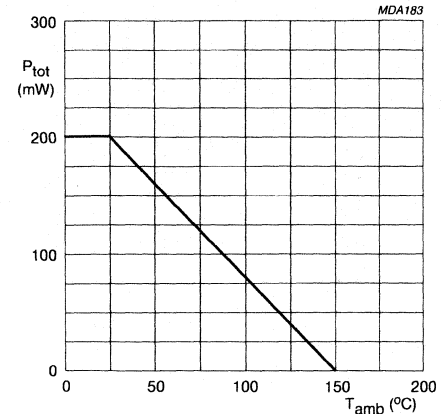
Note to the Limiting values and Thermal characteristics

1. Device mounted on a printed-circuit board.

CHARACTERISTICS

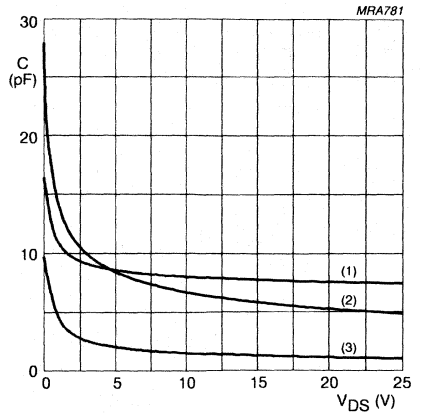
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 µA	50	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{GS} = V_{DS}$; I_D = 1 mA	0.4	–	1.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 40 V	–	–	1	µA
I_{GSS}	gate-source leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 80 mA	–	8	15	Ω
		V_{GS} = 5 V; I_D = 80 mA	–	14	20	Ω
		V_{GS} = 2.5 V; I_D = 10 mA	–	18	30	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 10 V; f = 1 MHz	–	8	15	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 10 V; f = 1 MHz	–	7	15	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 10 V; f = 1 MHz	–	2	5	pF
Switching times						
t_{on}	turn-on time	V_{GS} = 0 to 10 V; V_{DD} = 20 V; I_D = 80 mA	–	2	5	ns
t_{off}	turn-off time	V_{GS} = 10 to 0 V; V_{DD} = 20 V; I_D = 80 mA	–	5	10	ns



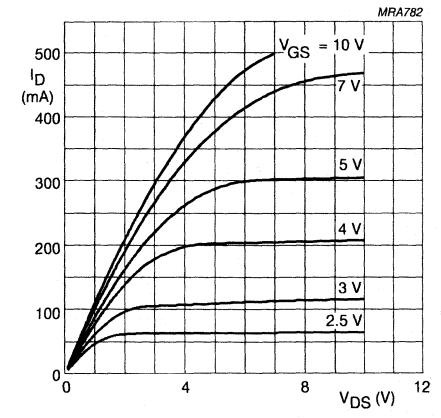
Device mounted on a printed-circuit board.

Fig.2 Power derating curve.



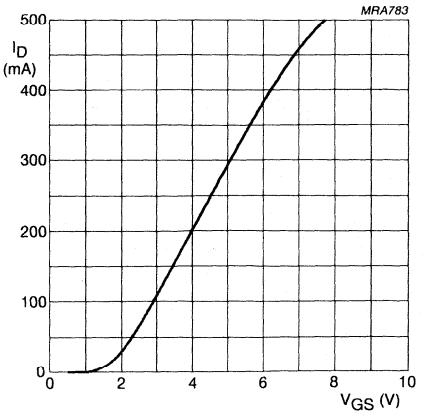
V_{GS} = 0; T_j = 25 °C; f = 1 MHz.
(1) C_{iss}.
(2) C_{oss}.
(3) C_{rss}.

Fig.3 Capacitance as a function of drain-source voltage; typical values.



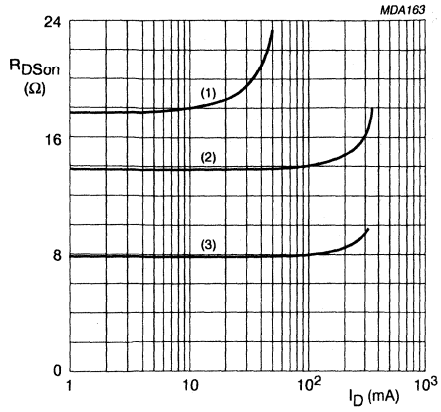
T_j = 25 °C.

Fig.4 Output characteristics; typical values.



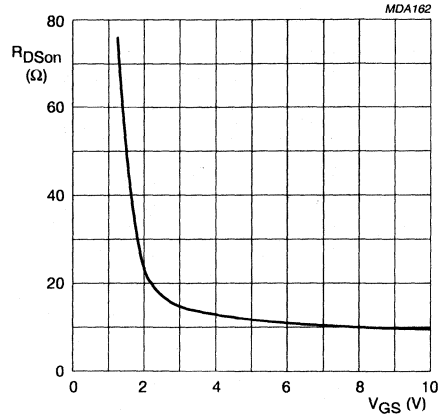
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Transfer characteristics; typical values.



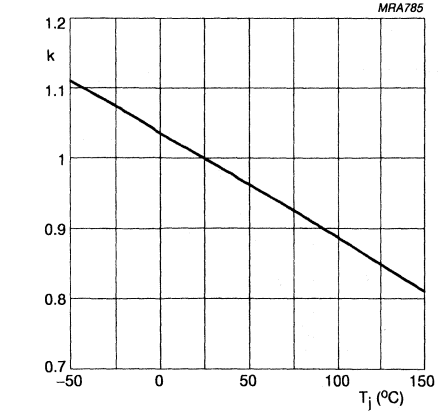
T_j = 25 °C.
(1) V_{GS} = 2.5 V.
(2) V_{GS} = 5 V.
(3) V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of drain current; typical values.



V_{DS} = 0.1 V; T_j = 25 °C.

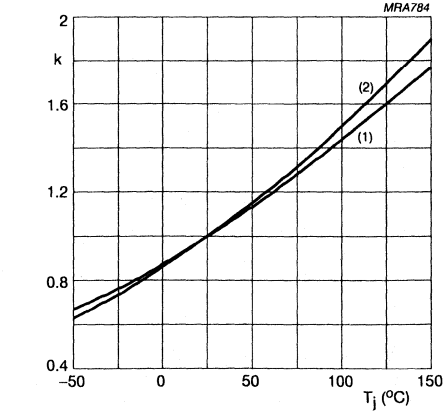
Fig.7 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

Typical V_{GSth} at 1 mA.

Fig.8 Temperature coefficient of gate-source threshold voltage.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

Typical R_{DSon} at 100 mA / 10 V.
(1) I_D = 10 mA; V_{GS} = 2.5 V.
(2) I_D = 100 mA; V_{GS} = 10 V.

Fig.9 Temperature coefficient of drain-source on-state resistance.

N-channel enhancement mode vertical D-MOS transistor

BSN205; BSN205A

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope. Designed primarily as a line current interrupter in telephone sets, it can also be applied in other applications such as in relays, line and high speed transformer drivers etc.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown
- Low $R_{DS(on)}$

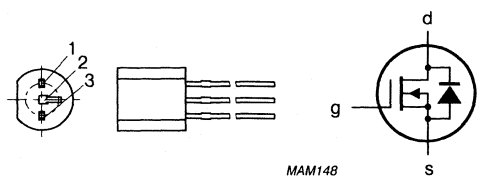
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance I_D = 400 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	4.5 Ω 6 Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\lvert Y_{fs} \rvert$	min. typ.	200 mS 350 mS

PINNING - TO-92 VARIANT

BSN205	BSN205A
1 = gate	1 = source
2 = drain	2 = gate
3 = source	3 = drain

PIN CONFIGURATION



Note: various pinout configurations available.

Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BSN205; BSN205A

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Drain current (peak)	I_{DM}	max.	1.2	A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1	W
Storage temperature range	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

Note

1. Transistor mounted on printed-circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm × 10 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)\ DSS}$	min.	200	V
Drain-source leakage current V_{DS} = 160 V; V_{GS} = 0	I_{DSS}	max.	1	μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.8 2.8	V V
Drain-source ON-resistance I_D = 400 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	4 6	Ω Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\lvert Y_{fs} \rvert$	min. typ.	200 350	mS mS
Input capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ. max.	45 60	pF pF

Output capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ. max.	15 pF 25 pF
Feedback capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ. max.	3.5 pF 10 pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DD} = 50 V V_{GS} = 0 to 10 V	t_{on}	typ. max.	5 ns 10 ns
	t_{off}	typ. max.	15 ns 20 ns

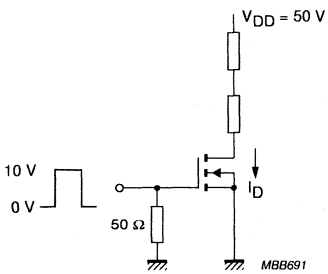


Fig.2 Switching time test circuit.

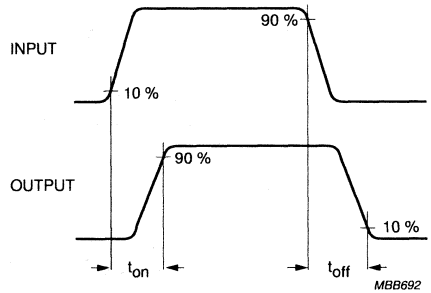


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistors

BSN254 BSN254A

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistors in TO-92 variant envelope and designed for use as line current interrupters in telephone sets and for application in relay, high-speed and line-transformer drivers.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown
- Low $R_{DS\ (on)}$

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	250	V
Drain current (DC)	I_D	max.	300	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source on-resistance				
I_D = 300 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	5.0	Ω
		max.	7.0	Ω
Gate-source threshold voltage	$V_{GS(th)}$	max.	2	V

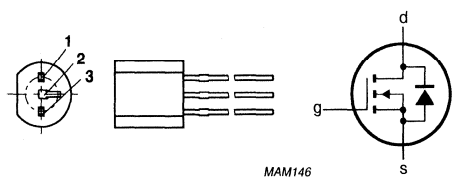
PINNING (BSN254)

1 = gate
2 = drain
3 = source

PINNING (BSN254A)

1 = source
2 = gate
3 = drain

PIN CONFIGURATION - TO-92 VARIANT



Note: Various pinnings are available on request.

Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistors

BSN254 BSN254A

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	250	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Drain current (peak)	I_{DM}	max.	1.2	A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1	W
Storage temperature range	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

Note

1. Device mounted on printed-circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm × 10 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage				
I_D = 10 μA; V_{GS} = 0	$V_{(BR)\ DSS}$	min.	250	V
Drain-source leakage current				
V_{DS} = 200 V; V_{GS} = 0	I_{DSS}	max.	1	μA
Gate-source leakage current				
$\pm V_{GS}$ = 20 V; V_{DS} = 0	$\pm I_{GSS}$	max.	100	nA
Gate threshold voltage				
I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min.	0.8	V
		max.	2.0	V
Drain-source on-resistance				
I_D = 300 mA; V_{GS} = 10 V	$R_{DS\ (on)}$	typ.	5.0	Ω
		max.	7.0	Ω
I_D = 20 mA; V_{GS} = 2.4 V	$R_{DS(on)}$	max.	10	Ω
Transfer admittance				
I_D = 300 mA; V_{DS} = 25 V	$\lvert Y_{fs} \rvert$	min.	200	mS
		typ.	400	mS
Input capacitance at f = 1 MHz				
V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ.	65	pF
		max.	90	pF

Output capacitance at f = 1 MHz			
V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ.	20 pF
		max.	30 pF
Feedback capacitance at f = 1 MHz			
V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ.	5 pF
		max.	15 pF
Switching times (see Figs 2 and 3)			
I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ.	5 ns
		max.	10 ns
	t_{off}	typ.	20 ns
		max.	30 ns

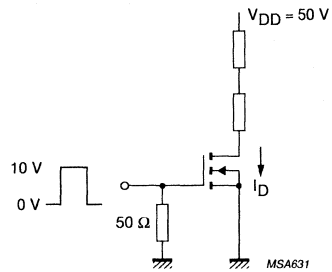


Fig.2 Switching times test circuit.

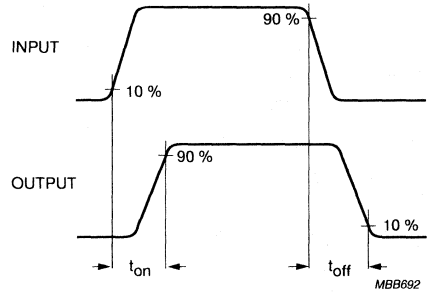


Fig.3 Input and output waveforms.

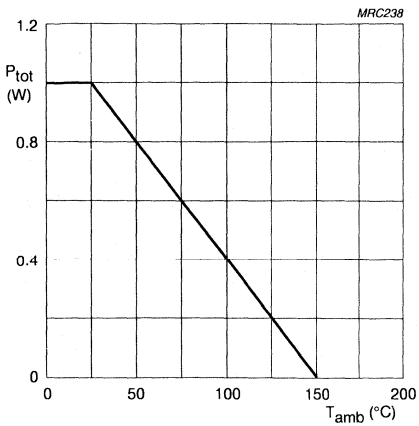


Fig.4 Power derating curve.

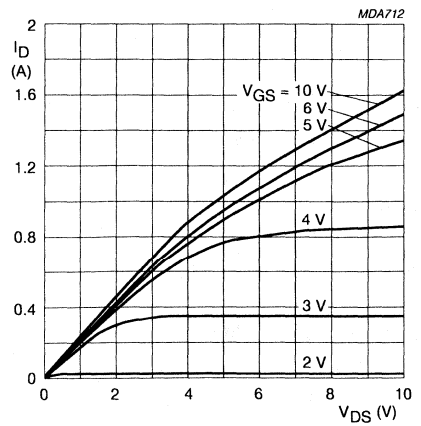


Fig.5 Output characteristics; T_j = 25 °C; typical values.

N-channel enhancement mode vertical D-MOS transistors

BSN254
BSN254A

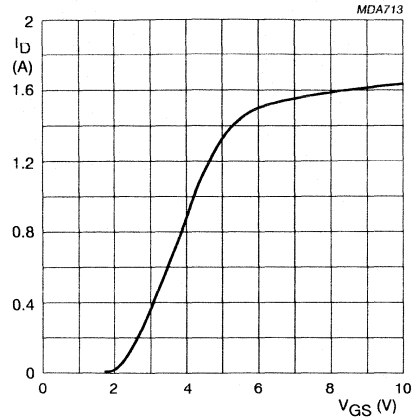


Fig.6 Transfer characteristic; V_{DS} = 10 V; T_j = 25 °C; typical value.

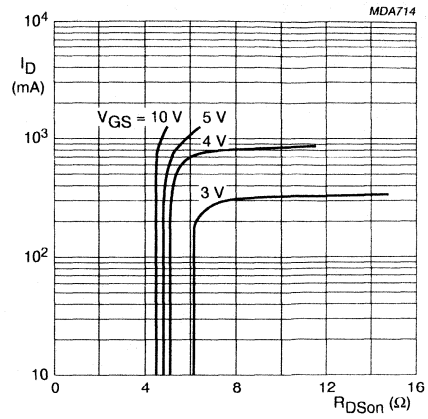


Fig.7 On-resistance as a function of drain current; T_j = 25 °C; typical values.

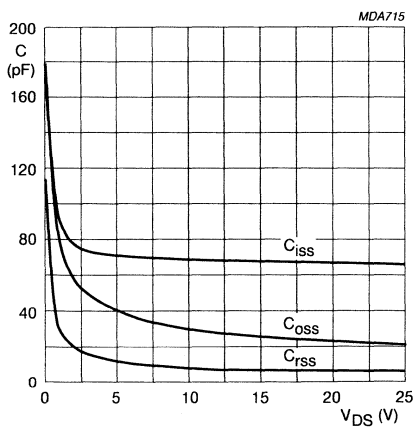


Fig.8 Capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C; typical values.

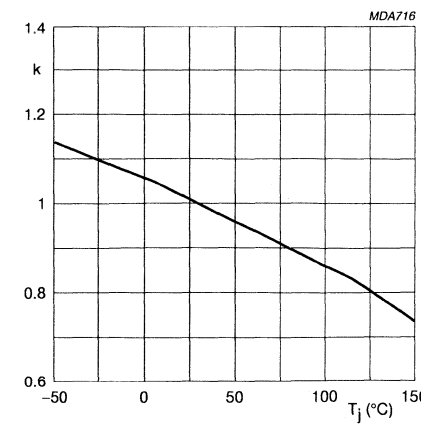


Fig.9

$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C};$$

$V_{GS(th)}$ at 1 mA; typical values

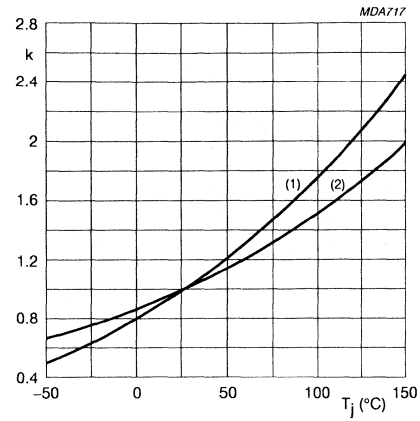


Fig.10

$$k = \frac{R_{DS\,(on)} \text{ at } T_j}{R_{DS\,(on)} \text{ at } 25\ °C};$$

typical values.

N-channel enhancement mode vertical D-MOS transistor

BSN274; BSN274A

FEATURES

- Direct interface to C-MOS, TTL, etc., due to low threshold voltage
- High speed switching
- No secondary breakdown

DESCRIPTION

Silicon n-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high speed and line transformer drivers.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	270	V
I_D	drain current (DC)	250	mA
$R_{DS(on)}$	drain-source on-resistance	8	Ω
$V_{GS(th)}$	threshold voltage	2	V

PINNING (BSN274)

PIN	DESCRIPTION
1	gate
2	drain
3	source

PINNING (BSN274A)

PIN	DESCRIPTION
1	source
2	gate
3	drain

Note: Other pinnings are available on request.

PIN CONFIGURATION - TO-92 VARIANT

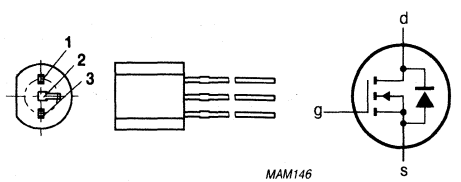


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	270	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	drain current	DC	–	250	mA
I_{DM}	drain current	peak	–	1	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1	W
T_{stg}	storage temperature range		–65	150	°C
T_j	operating junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	125	K/W

Notes

1. Transistor mounted on printed circuit board, maximum lead length 4 mm, mounting pad for drain leads minimum 10 mm × 10 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 I_D = 10 μA	270	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 220 V V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate threshold voltage	I_D = 1 mA V_{DS} = V_{GS}	0.8	–	2	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 250 mA V_{GS} = 10 V	–	6.5	8	Ω
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA V_{GS} = 2.4 V	–	9	14	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 250 mA V_{DS} = 25 V	200	400	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	65	90	pF
C_{oss}	output capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	20	30	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{rss}	feedback capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	5	15	pF
Switching times (see Figs 2 and 2)						
t_{on}	switching-on time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	5	10	ns
t_{off}	switching-off time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	20	30	ns

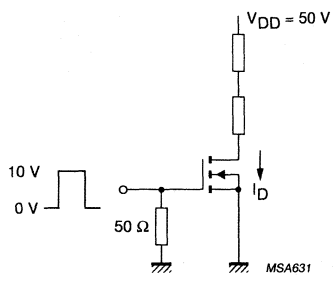


Fig.2 Switching time test circuit.

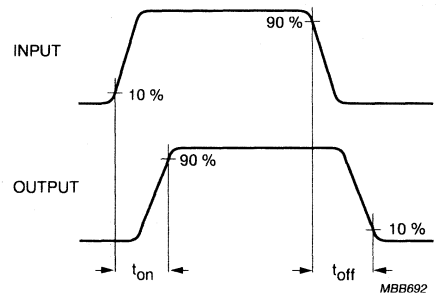


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistors

BSN304; BSN304A

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - TO-92 variant

PIN	DESCRIPTION
BSN304	
1	gate
2	drain
3	source
BSN304A	
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	
V_{DS}	drain-source voltage		–	300	V
I_D	DC drain current		–	250	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	1	W
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 250 mA; V_{GS} = 10 V	–	8	Ω
$V_{GS(off)}$	gate-source cut-off voltage	I_D = 1 mA; V_{GS} = V_{DS}	0.8	2	V

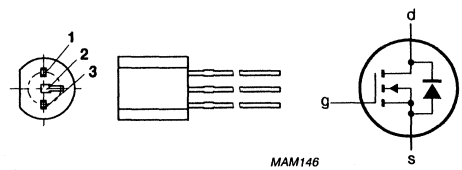


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	300	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	250	mA
I_{DM}	peak drain current		–	1	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C; note 1	–	1	W
T_{stg}	storage temperature		−65	+150	°C
T_j	operating junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient; note 1	125 K/W

Note

1. Device mounted on an epoxy printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm x 10 mm.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	300	–	–	V
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}	0.8	–	2	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 250 mA; V_{GS} = 10 V	–	6.7	8	Ω
		I_D = 20 mA; V_{GS} = 2.4 V	–	7.9	14	Ω
I_{DSS}	drain-source leakage current	V_{DS} = 240 V; V_{GS} = 0	–	–	100	nA
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 250 mA; V_{DS} = 25 V	200	380	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	57	90	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	15	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	2.6	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	2.5	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 10 to 0 V	–	17	30	ns

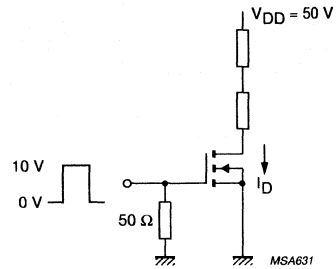


Fig.2 Switching times test circuit.

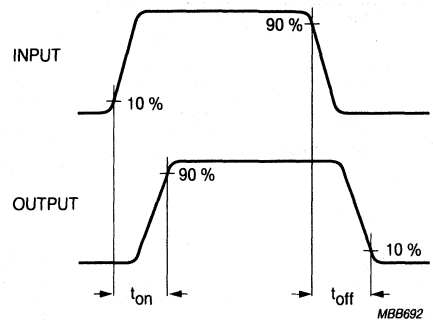


Fig.3 Input and output waveforms.

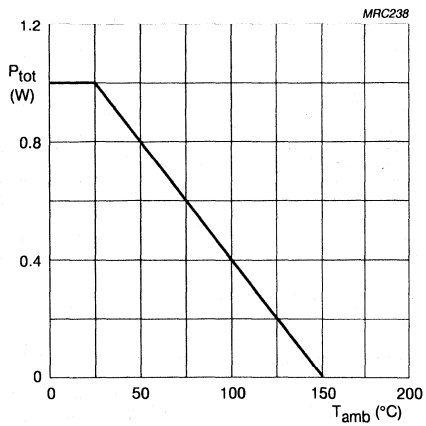
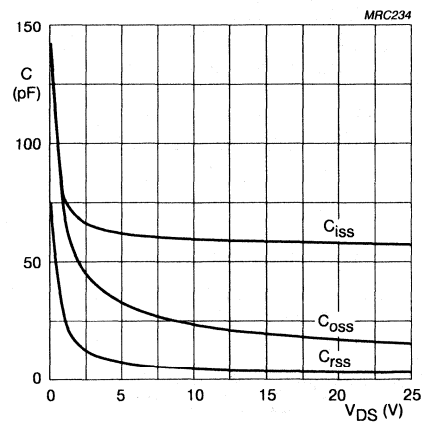
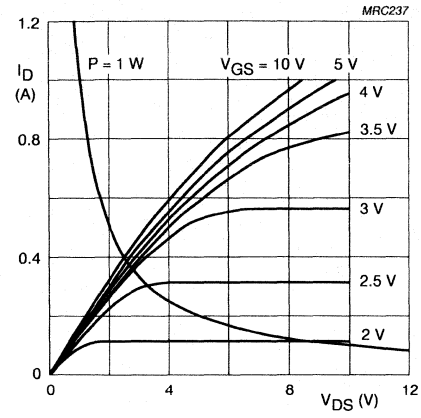


Fig.4 Power derating curve.



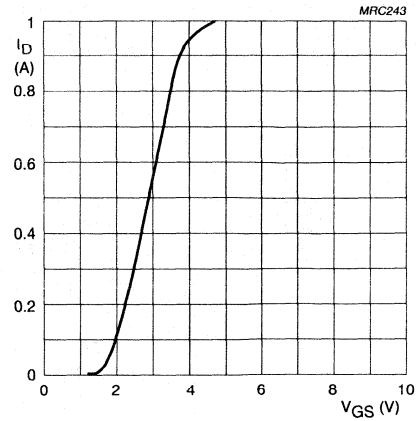
V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

Fig.5 Capacitance as a function of drain-source voltage, typical values.



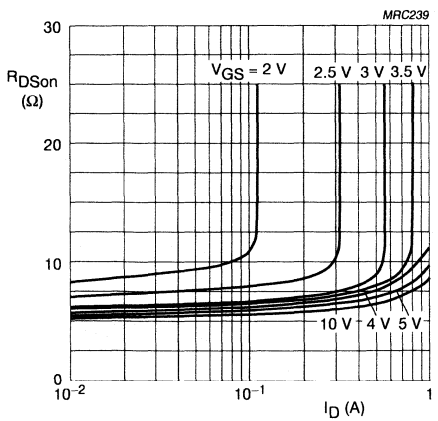
T_j = 25 °C.

Fig.6 Typical output characteristics.



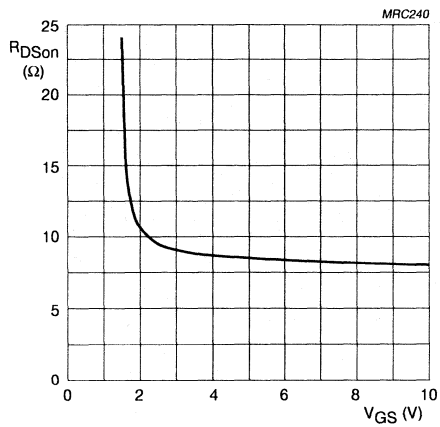
V_{DS} = 10 V; T_j = 25 °C.

Fig.7 Typical transfer characteristics.



T_j = 25 °C.

Fig.8 Drain-source on-resistance as a function of drain current, typical values.



V_{DS} = 100 mV; T_j = 25 °C.

Fig.9 Drain-source on-resistance as a function of gate-source voltage, typical values.

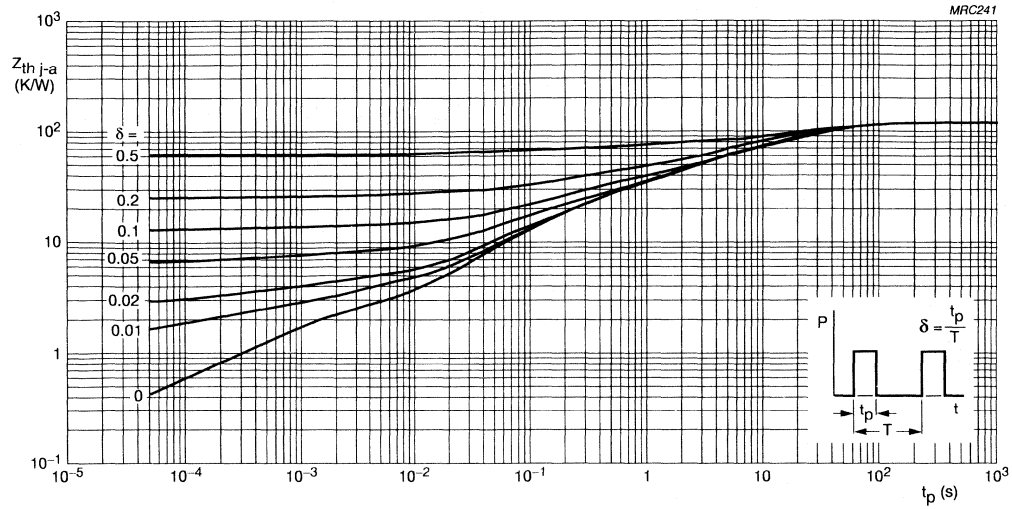
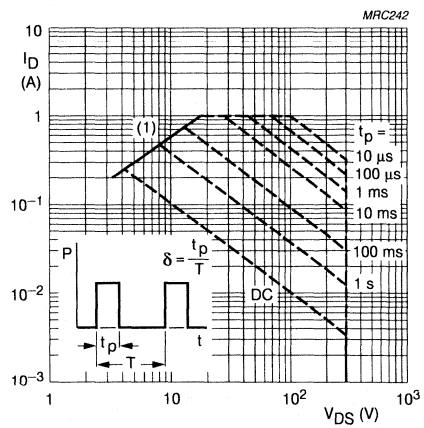


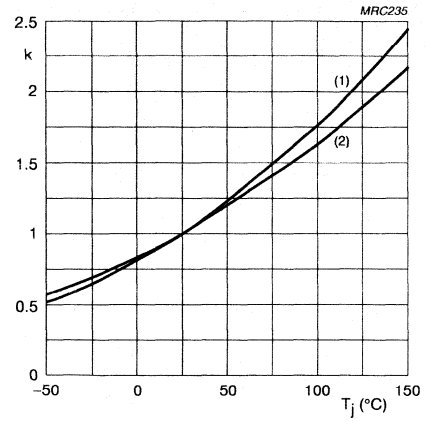
Fig.10 Transient thermal resistance from junction to ambient as a function of pulse time.



δ = 0.01; T_{amb} = 25 °C.

(1) $R_{DS(on)}$ limitation.

Fig.11 SOAR curve.

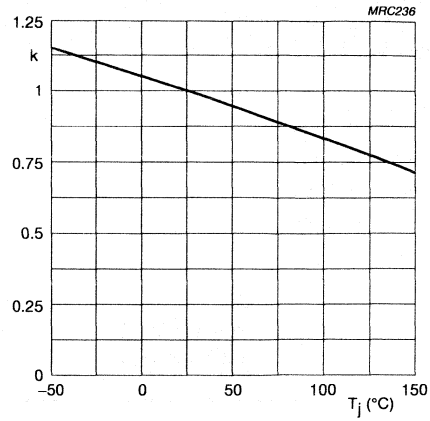


$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}.$$

Typical $R_{DS(on)}$;

(1) I_D = 250 mA; V_{GS} = 10 V.
(2) I_D = 20 mA; V_{GS} = 2.4 V.

Fig.12 Temperature coefficient of drain-source on-resistance.



$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}.$$

Fig.13 Temperature coefficient of gate-source threshold voltage.

N-channel enhancement mode vertical D-MOS transistor

BSP030

FEATURES

- High speed switching
- No secondary breakdown
- Very low on-state resistance.

APPLICATIONS

- Motor and actuator drivers
- Power management
- Synchronized rectification.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a 4-pin plastic SOT223 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT223

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	d	drain
3	s	source
4	d	drain

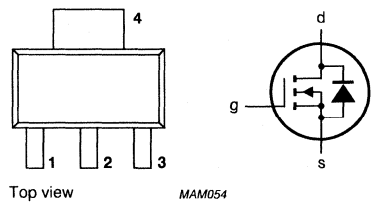


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{SD}	source-drain diode forward voltage	I_S = 1.25 A	–	1	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}	1	2.8	V
I_D	drain current (DC)	T_s = 100 °C	–	10	A
R_{DSon}	drain-source on-state resistance	I_D = 5 A; V_{GS} = 10 V	–	0.03	Ω
P_{tot}	total power dissipation	T_s = 100 °C	–	5	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 100 °C; note 1	–	10	A
I_{DM}	peak drain current	note 2	–	40	A
P_{tot}	total power dissipation	T_s = 100 °C	–	5	W
		T_{amb} = 25 °C; note 3	–	3.3	W
		T_{amb} = 25 °C; note 4	–	1.25	W
T_{stg}	storage temperature		−65	+150	°C
T_j	operating junction temperature		−65	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 100 °C	–	5	A
I_{SM}	peak pulsed source current	note 2	–	20	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Value based on printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Value based on printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	10	K/W

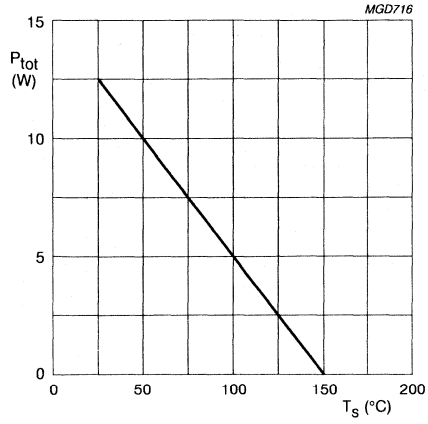
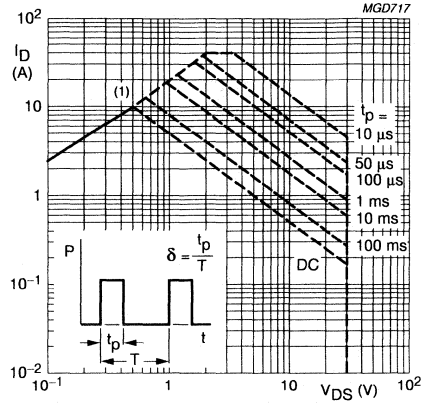


Fig.2 Power derating curve.



$\delta = 0.01$; $T_s = 100$ °C.
(1) R_{DSon} limitation.

Fig.3 SOAR.

CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	1	–	2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 24 V	–	–	500	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 2.5 A	–	–	0.05	Ω
		V_{GS} = 10 V; I_D = 5 A	–	–	0.03	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	750	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	450	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	200	–	pF
Q_g	total gate charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 5 A; T_{amb} = 25 °C	–	28	–	nC
Q_{gs}	gate-source charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 5 A; T_{amb} = 25 °C	–	2.5	–	nC
Q_{gd}	gate-drain charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 5 A; T_{amb} = 25 °C	–	10.5	–	nC
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	14	–	ns
t_f	fall time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	18	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	32	60	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	29	–	ns
t_r	rise time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	33	–	ns
t_{off}	turn-off switching time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	62	150	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 1.25 A	–	–	1	V
t_{rr}	reverse recovery time	I_S = 1.25 A; di/dt = −100 A/μs	–	70	–	ns

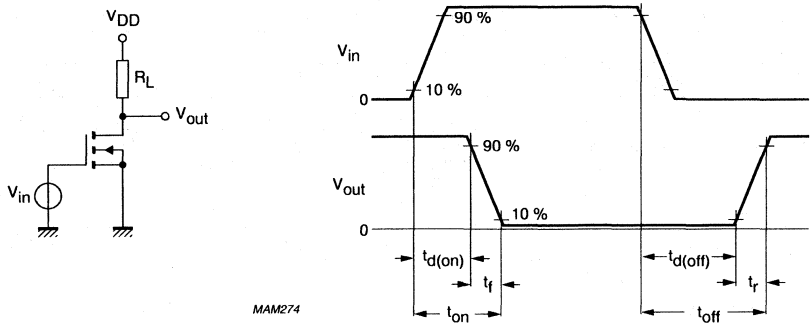


Fig.4 Switching time test circuit; input and output waveforms.

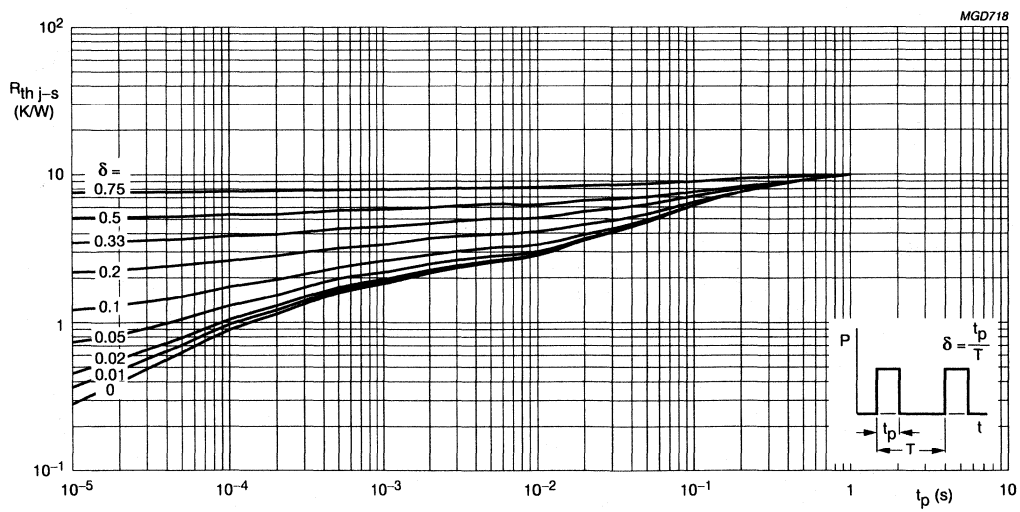
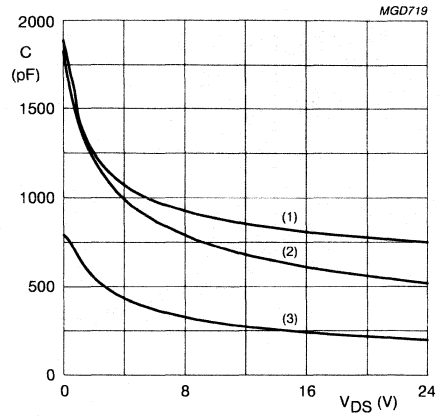
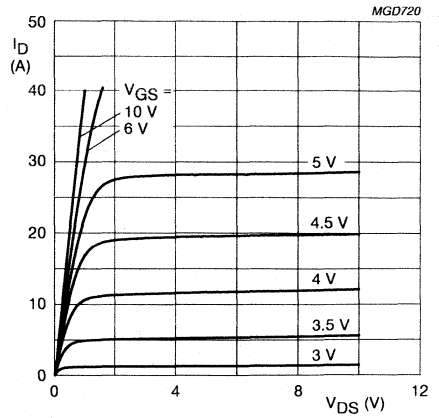


Fig.5 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.



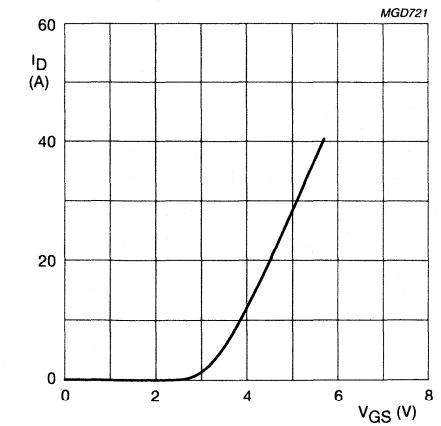
V_{GS} = 0; f = 1 MHz; T_j = 25 °C.
(1) C_{iss}.
(2) C_{oss}.
(3) C_{rss}.

Fig.6 Capacitance as a function of drain-source voltage; typical values.



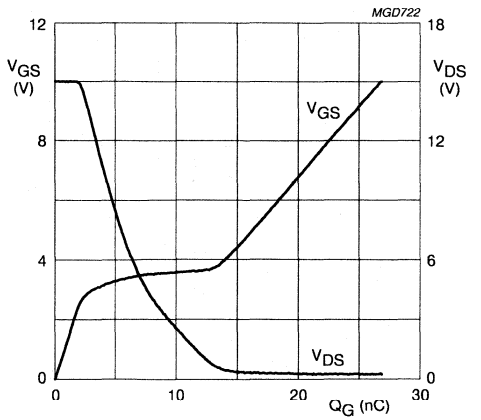
T_{amb} = 25 °C; t_p = 80 µs; δ = 0.

Fig.7 Output characteristics; typical values.



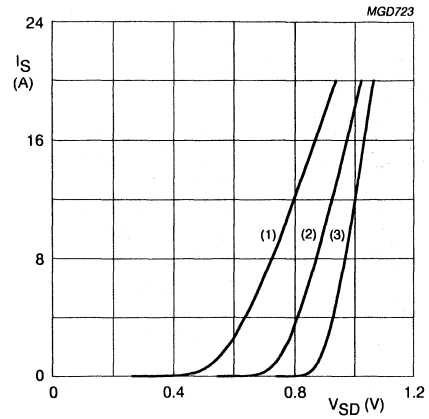
V_{DS} = 10 V; T_{amb} = 25 °C; t_p = 80 µs; δ = 0.

Fig.8 Transfer characteristics; typical values.



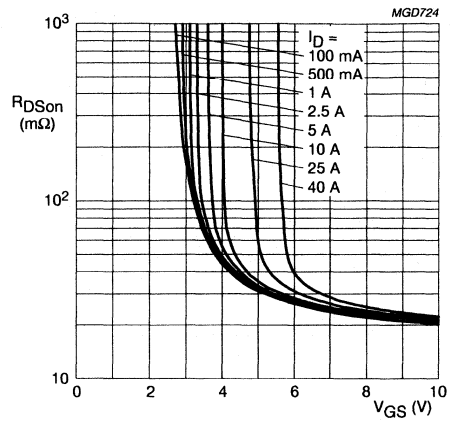
V_{DD} = 12.5 V; I_D = 5 A; T_{amb} = 25 °C.

Fig.9 Gate-source voltage and drain-source voltage as a function of total gate charge; typical values.



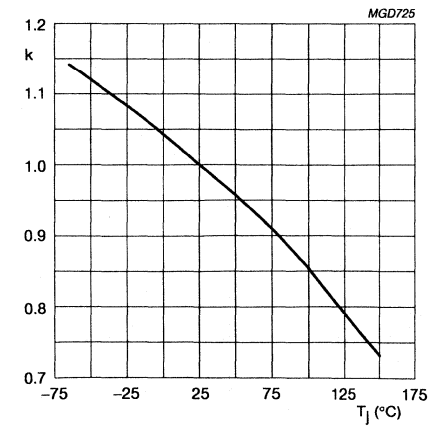
V_{GD} = 0.
(1) T_{amb} = 150 °C; t_p = 80 µs; δ = 0.
(2) T_{amb}= 25 °C; t_p = 80 µs; δ = 0.
(3) T_{amb}= −65 °C; t_p = 80 µs; δ = 0.

Fig.10 Source current as a function of source-drain diode forward voltage; typical values.



T_{amb} = 25 °C; t_p = 80 µs; δ = 0.
$V_{DS} \geq I_D \times R_{DSon}$.

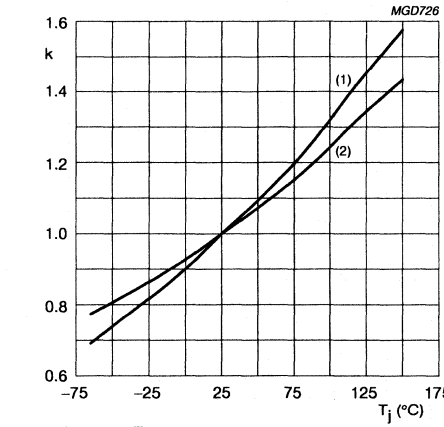
Fig.11 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

V_{GSth} at $V_{DS} = V_{GS}$; I_D = 1 mA.

Fig.12 Temperature coefficient of gate-source threshold voltage as a function of junction temperature; typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

(1) R_{DSon} at V_{GS} = 10 V; I_D = 5 A.
(2) R_{DSon} at V_{GS} = 4.5 V; I_D = 2.5 A.

Fig.13 Temperature coefficient of drain-source on-state resistance as a function of junction temperature; typical values.

P-channel enhancement mode vertical D-MOS transistor

BSP090

FEATURES

- High speed switching
- No secondary breakdown
- Very low on-state resistance.

APPLICATIONS

- Motor and actuator drivers
- Power management
- Synchronized rectification.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a 4-pin plastic SOT223 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT223

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	d	drain
3	s	source
4	d	drain

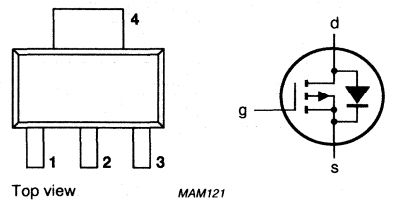


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	−30	V
V_{SD}	source-drain diode forward voltage	I_S = −1.25 A	–	−1.3	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = −1 mA; V_{DS} = V_{GS}	−1	−2.8	V
I_D	drain current (DC)	T_s = 100 °C	–	−5.7	A
R_{DSon}	drain-source on-state resistance	I_D = −2.8 A; V_{GS} = −10 V	–	0.09	Ω
P_{tot}	total power dissipation	T_s = 100 °C	–	5	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 100 °C; note 1	–	–5.7	A
I_{DM}	peak drain current	note 2	–	–22	A
P_{tot}	total power dissipation	T_s = 100 °C	–	5	W
		T_{amb} = 25 °C; note 3	–	3.3	W
		T_{amb} = 25 °C; note 4	–	1.25	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–65	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 100 °C	–	–3.8	A
I_{SM}	peak pulsed source current	note 2	–	–15	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	10	K/W

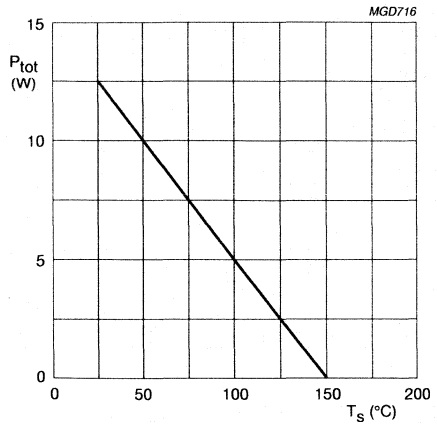
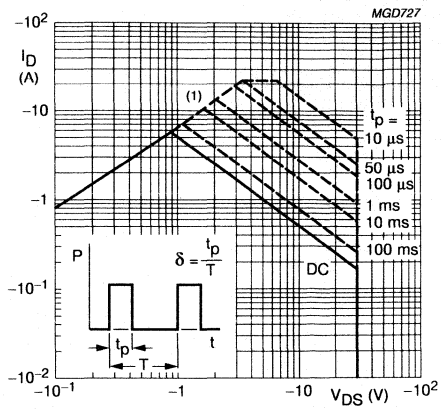


Fig.2 Power derating curve.



δ = 0.01; T_s = 100 °C.
(1) R_{DSon} limitation.

Fig.3 SOAR.

P-channel enhancement mode vertical D-MOS transistor

BSP090

CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−1	–	−2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −24 V	–	–	−500	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = −4.5 V; I_D = −1.4 A	–	–	0.15	Ω
		V_{GS} = −10 V; I_D = −2.8 A	–	–	0.09	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	800	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	400	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	100	–	pF
Q_g	total gate charge	V_{GS} = −10 V; V_{DD} = −15 V; I_D = −2.8 A; T_{amb} = 25 °C	–	21	–	nC
Q_{gs}	gate-source charge	V_{GS} = −10 V; V_{DD} = −15 V; I_D = −2.8 A; T_{amb} = 25 °C	–	2.5	–	nC
Q_{gd}	gate-drain charge	V_{GS} = −10 V; V_{DD} = −15 V; I_D = −2.8 A; T_{amb} = 25 °C	–	6	–	nC
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to −10 V; V_{DD} = −15 V; I_D = −1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	6	–	ns
t_r	rise time	V_{GS} = 0 to −10 V; V_{DD} = −15 V; I_D = −1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	6	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to −10 V; V_{DD} = −15 V; I_D = −1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	12	25	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = −10 to 0 V; V_{DD} = −15 V; I_D = −1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	55	–	ns
t_f	fall time	V_{GS} = −10 to 0 V; V_{DD} = −15 V; I_D = −1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	40	–	ns
t_{off}	turn-off switching time	V_{GS} = −10 to 0 V; V_{DD} = −15 V; I_D = −1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	95	190	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = −1.25 A	–	–	−1.3	V
t_{rr}	reverse recovery time	I_S = −1.25 A; di/dt = 100 A/μs	–	70	–	ns

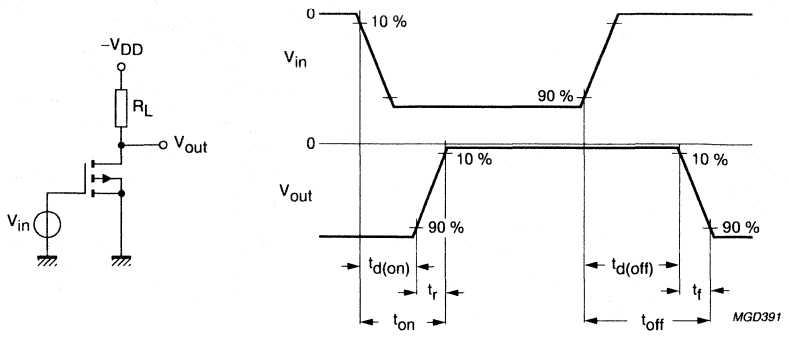


Fig.4 Switching time test circuit; input and output waveforms.

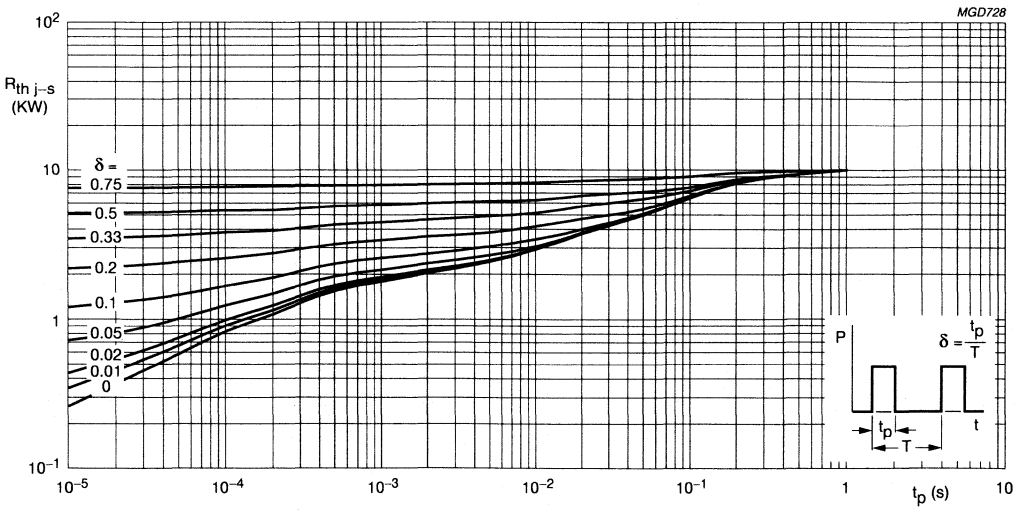
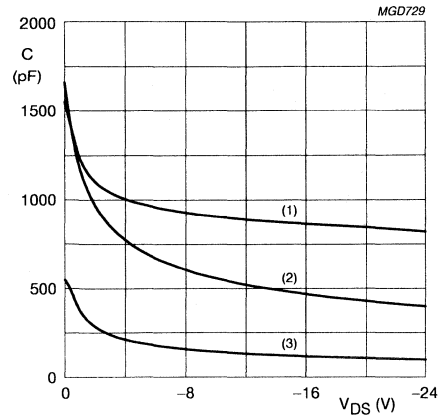
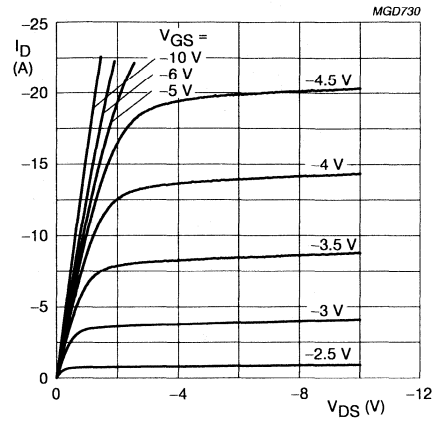


Fig.5 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.



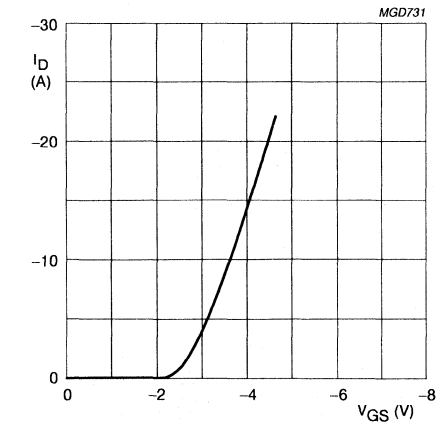
V_{GS} = 0; f = 1 MHz; T_j = 25 °C.
(1) C_{iss}.
(2) C_{oss}.
(3) C_{rss}.

Fig.6 Capacitance as a function of drain-source voltage; typical values.



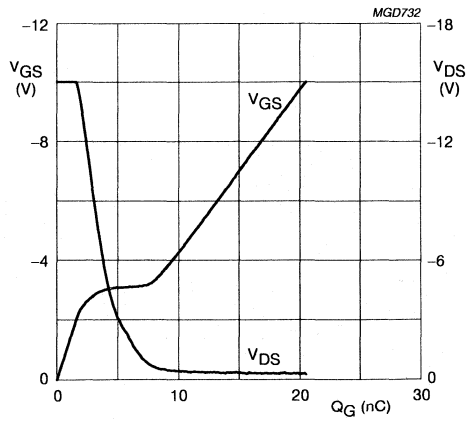
T_{amb} = 25 °C; t_p = 80 µs; δ = 0.

Fig.7 Output characteristics; typical values.



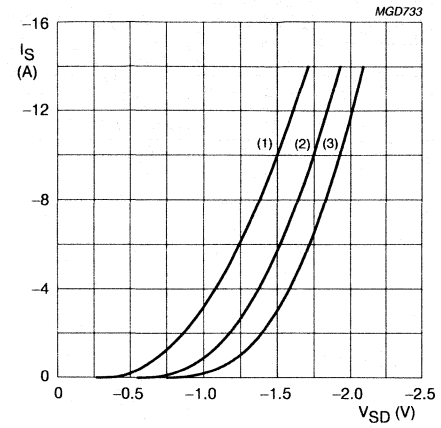
V_{DS} = −10 V; T_{amb} = 25 °C; t_p = 80 µs; δ = 0.

Fig.8 Transfer characteristics; typical values.



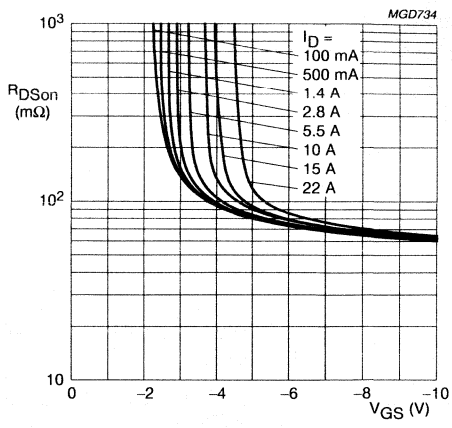
V_{DD} = −15 V; I_D = −2.8 A; T_{amb} = 25 °C.

Fig.9 Gate-source voltage and drain-source voltage as a function of total gate charge; typical values.



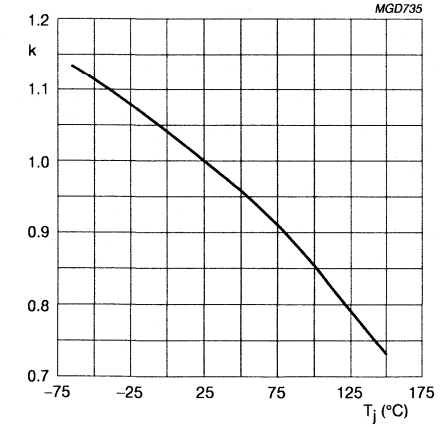
V_{GD} = 0.
(1) T_{amb} = 150 °C; t_p = 80 µs; δ = 0.
(2) T_{amb} = 25 °C; t_p = 80 µs; δ = 0.
(3) T_{amb} = −65 °C; t_p = 80 µs; δ = 0.

Fig.10 Source current as a function of source-drain diode forward voltage; typical values.



T_{amb} = 25 °C; t_p = 80 µs; δ = 0.
$V_{DS} \geq I_D \times R_{DSon}$.

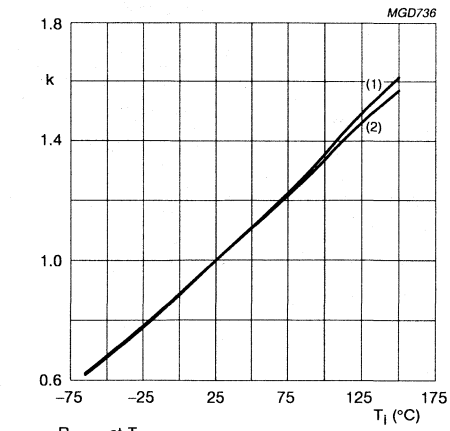
Fig.11 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

V_{GSth} at V_{DS} = V_{GS}; I_D = −1 mA.

Fig.12 Temperature coefficient of gate-source threshold voltage as a function of junction temperature; typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

(1) R_{DSon} at V_{GS} = −10 V; I_D = −2.8 A.
(2) R_{DSon} at V_{GS} = −4.5 V; I_D = −1.4 A.

Fig.13 Temperature coefficient of drain-source on-resistance as a function of junction temperature; typical values.

N-channel enhancement mode vertical D-MOS transistor

BSP100

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Low-loss motor and actuator drivers
- Power switching.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a plastic SOT223 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT223

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	d	drain
3	s	source
4	d	drain

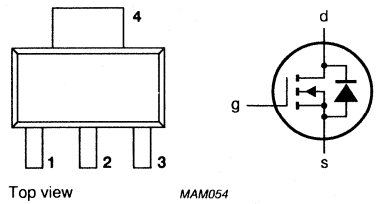


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{SD}	source-drain diode forward voltage	I_S = 1.25 A	–	1.2	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}	1	2.8	V
I_D	drain current (DC)		–	3.5	A
R_{DSon}	drain-source on-state resistance	I_D = 2.2 A; V_{GS} = 10 V	–	0.1	Ω
P_{tot}	total power dissipation	T_s = 100 °C	–	5	W

N-channel enhancement mode vertical D-MOS transistor

BSP100

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)	$T_s \leq 100°C$	–	3.5	A
I_{DM}	peak drain current	note 1	–	14	A
P_{tot}	total power dissipation	$T_s = 100$ °C	–	5	W
		$T_{amb} = 25$ °C; note 2	–	1.65	W
T_{stg}	storage temperature		−65	+150	°C
T_j	operating junction temperature		–	150	°C
Source-drain diode					
I_S	source current (DC)	$T_s \leq 100°C$	–	2	A
I_{SM}	peak pulsed source current	note 1	–	7	A

Notes

1. Pulse width and duty cycle limited by maximum junction temperature.
2. Device mounted on an epoxy printed-circuit board, 40 × 40 × 1.5 mm; mounting pad for drain lead minimum 6 cm^2.

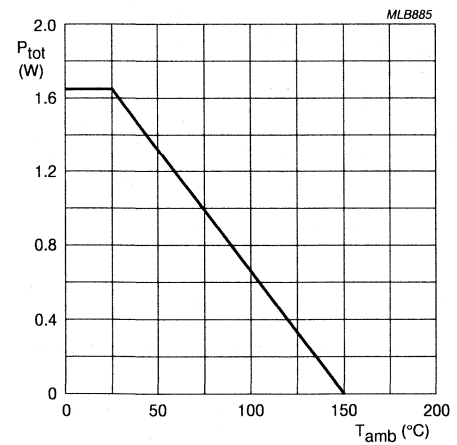
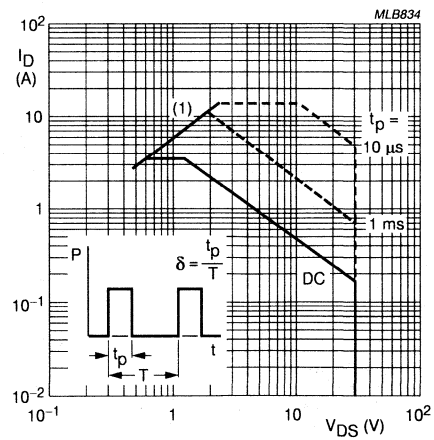


Fig.2 Power derating curve.



δ = 0.01.
Solder point temperature $T_s = 100$ °C.
(1) R_{DSon} limitation.

Fig.3 SOAR.

N-channel enhancement mode vertical D-MOS transistor

BSP100

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	75	K/W
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point		10	K/W

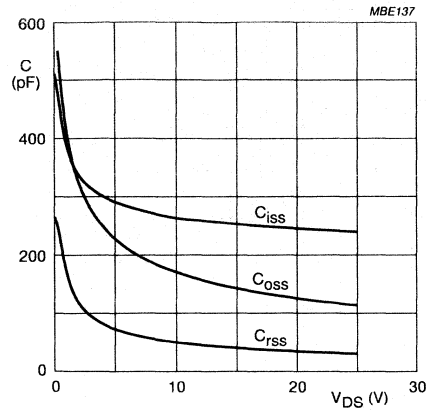
Note

1. Device mounted on an epoxy printed-circuit board, 40 × 40 × 1.5 mm; mounting pad for drain lead minimum 6 cm^2.

CHARACTERISTICS

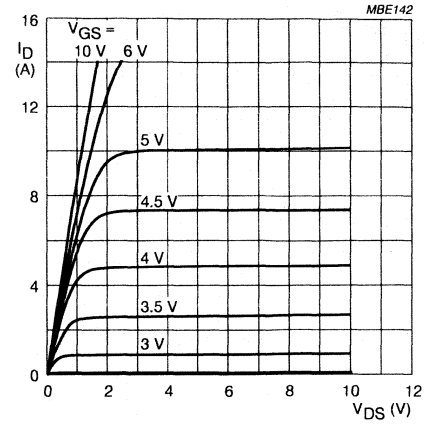
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	1	–	2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 24 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
I_{Don}	on-state drain current	V_{GS} = 10 V; V_{DS} = 1 V	3.5	–	–	A
		V_{GS} = 4.5 V; V_{DS} = 5 V	2	–	–	A
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 1 A	–	0.11	0.2	Ω
		V_{GS} = 10 V; I_D = 2.2 A	–	0.08	0.1	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = 20 V; I_D = 2.2 A	2	4.5	–	S
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	–	250	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	–	140	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	–	50	–	pF
Q_G	total gate charge	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	–	10	30	nC
Q_{GS}	gate-source charge	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	–	1	–	nC
Q_{GD}	gate-drain charge	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	–	2.5	–	nC
Switching times						
t_{on}	turn-on time	V_{GS} = 0 to 10 V; V_{DD} = 20 V; I_D = 1 A; R_L = 20 Ω	–	15	40	ns
t_{off}	turn-off time	V_{GS} = 10 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_L = 20 Ω	–	25	75	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 1.25 A	–	–	1.2	V
t_{rr}	reverse recovery time	I_S = 1.25 A; di/dt = 100 A/μs	–	35	100	ns



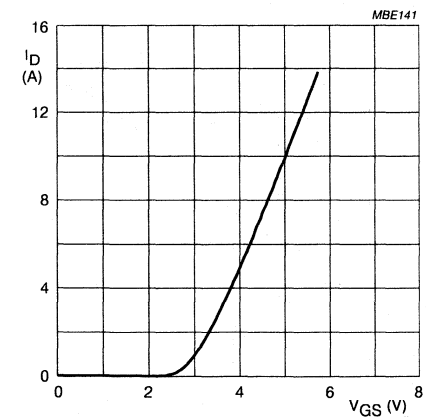
V_{GS} = 0.
T_j = 25 °C.

Fig.4 Capacitance as a function of drain-source voltage; typical values.



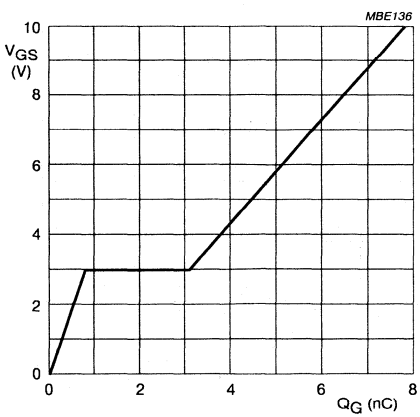
T_j = 25 °C.

Fig.5 Output characteristics; typical values.



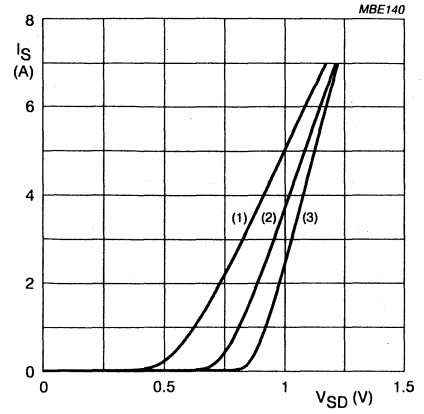
V_{DS} = 10 V.
T_j = 25 °C.

Fig.6 Transfer characteristic; typical values.



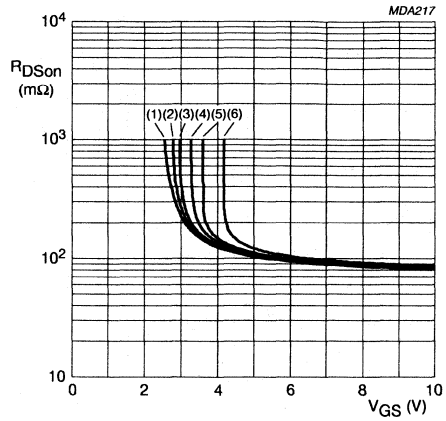
V_{DD} = 15 V.
I_D = 3.5 A.

Fig.7 Gate-source voltage as a function of total gate charge.



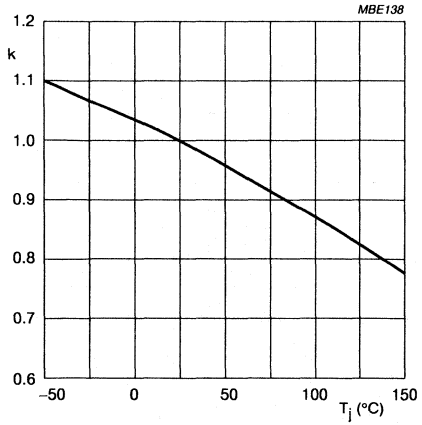
V_{GD} = 0.
(1) T_j = 150 °C.
(2) T_j = 25 °C.
(3) T_j = −55 °C.

Fig.8 Source current as a function of source-drain diode forward voltage.



$V_{DS} \geq I_D \times R_{DSon}$; T_j = 25 °C.
(1) I_D = 0.1 A.
(2) I_D = 0.5 A.
(3) I_D = 1 A.
(4) I_D = 2.2 A.
(5) I_D = 3.5 A.
(6) I_D = 7 A.

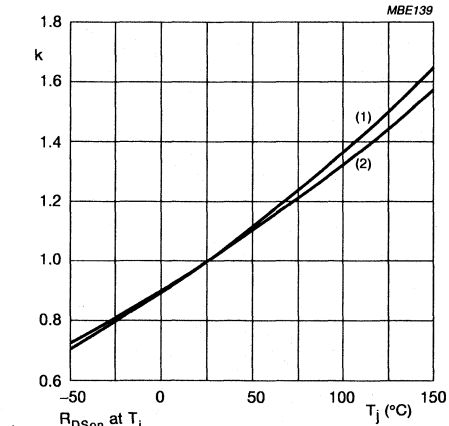
Fig.9 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

Typical V_{GSth} at I_D = 1 mA; V_{DS} = V_{GS} = V_{GSth}.

Fig.10 Temperature coefficient of gate-source threshold voltage.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

Typical R_{DSon} at:
(1) I_D = 2.2 A; V_{GS} = 10 V.
(2) I_D = 1 A; V_{GS} = 4.5 V.

Fig.11 Temperature coefficient of drain-source on-resistance.

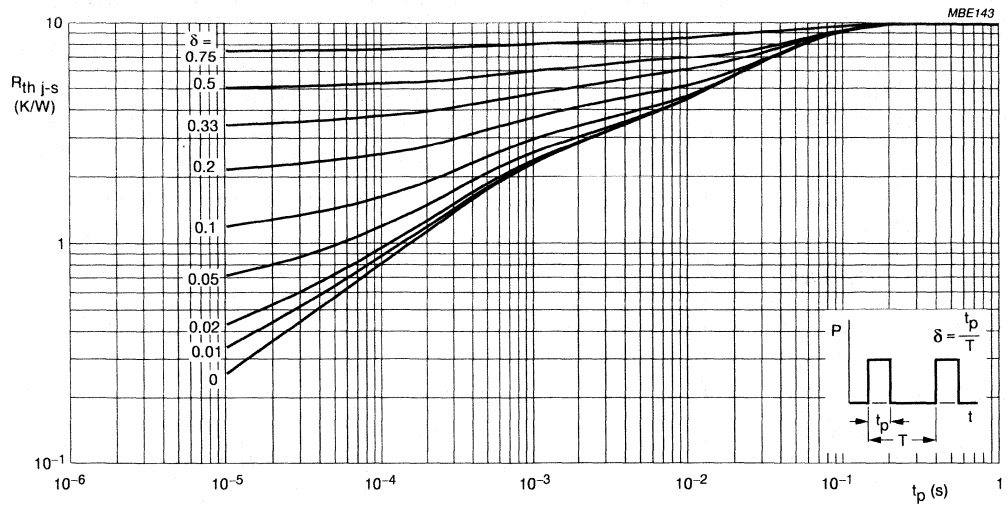


Fig.12 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

N-channel enhancement mode vertical D-MOS transistor

BSP106

FEATURES

- Very low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use in relay, high-speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage	–	60	V
I_D	drain current	DC value	425	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 200 mA V_{GS} = 10 V	4	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	3	V

PIN CONFIGURATION

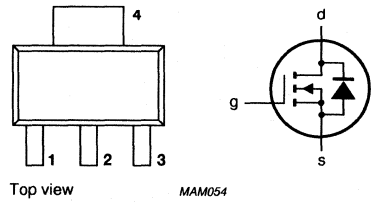


Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BSP106

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	60	V
V_{DG}	drain-gate voltage		–	60	V
$\pm V_{GSO}$	gate-source voltage		–	20	V
I_D	drain current	DC value	–	425	mA
I_{DM}	drain current	peak value	–	850	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–55	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3	K/W

Note

1. Device mounted on an epoxy printed-circuit board 40 x 40 x 1.5 mm; mounting pad for the drain lead minimum 6 cm^2.

N-channel enhancement mode vertical D-MOS transistor

BSP106

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA V_{GS} = 0	60	90	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 48 V V_{GS} = 0	–	–	1	μA
		V_{DS} = 25 V V_{GS} = 0	–	–	0.5	μA
$\pm I_{GSS}$	gate-source leakage current	V_{DS} = 0 $\pm V_{GS}$ = 15 V	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	0.8	–	3	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 200 mA V_{GS} = 10 V	–	2.5	4	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 200 mA V_{DS} = 10 V	100	200	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	25	40	pF
C_{oss}	output capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	22	30	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	6	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	2	5	ns
t_{off}	turn-off time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10	–	10	15	ns

N-channel enhancement mode vertical D-MOS transistor

BSP106

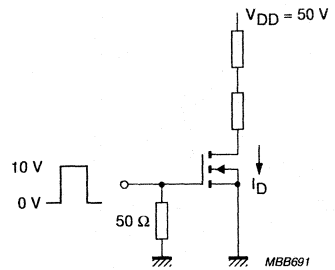


Fig.2 Switching time test circuit.

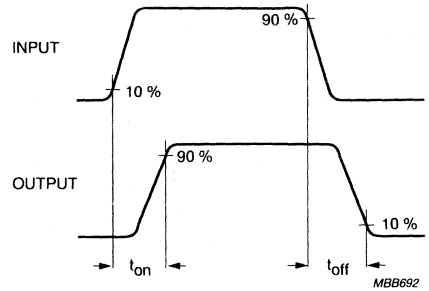


Fig.3 Input and output waveforms.

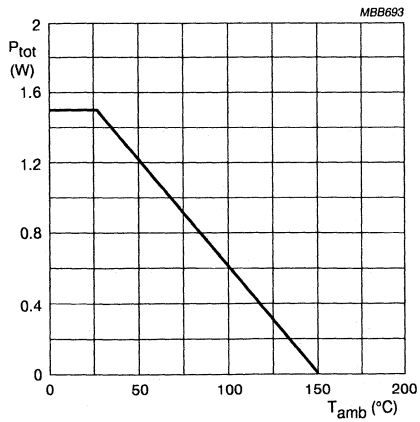


Fig.4 Power derating curve.

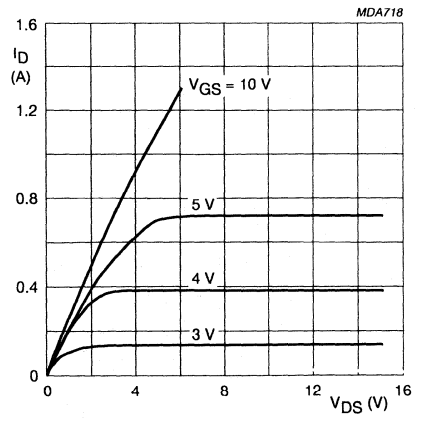


Fig.5 Typical output characteristics; T_j = 25 °C.

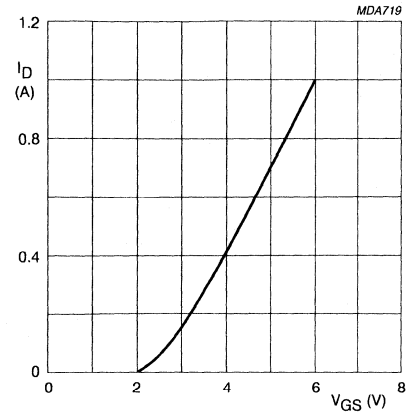


Fig.6 Typical transfer characteristic; V_{DS} = 10 V; T_j = 25 °C.

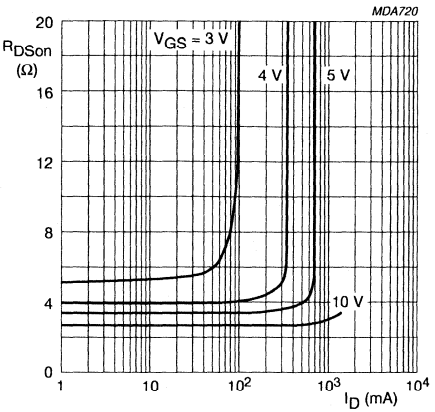


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

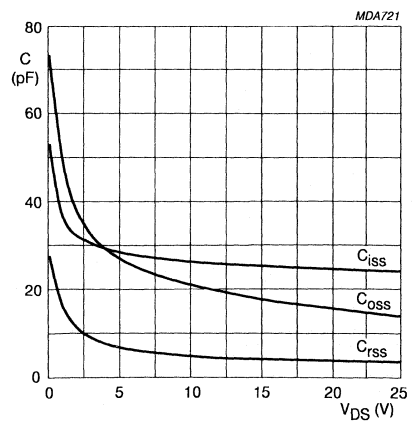


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

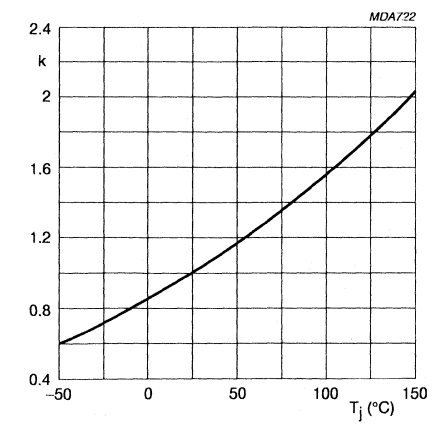


Fig.9 Temperature coefficient of drain-source on-resistance;

$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C};$$

typical $R_{DS(on)}$ at 200 mA/10 V.

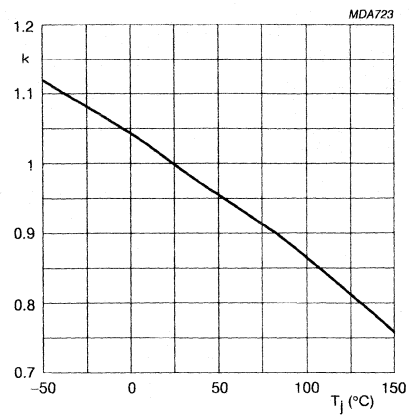


Fig.10 Temperature coefficient of gate-source threshold voltage;

$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C};$$

$V_{GS(th)}$ at 1 mA.

N-channel enhancement mode vertical D-MOS transistor

BSP107

FEATURES

- Direct interface to C-MOS, TTL, etc. due to low threshold voltage
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope. Intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer driver switching.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage (DC)	200	V
$V_{GS(th)}$	gate-source threshold voltage	2.4	V
I_D	drain current (DC)	200	mA
$R_{DS(on)}$	drain-source on-state resistance	28	Ω

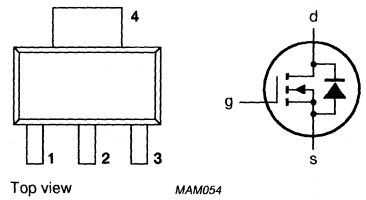


Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BSP107

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	drain current	DC	–	200	mA
I_{DM}	drain current	peak	–	350	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	1.5	W
T_{stg}	storage temperature range		−65	150	°C
T_j	operating junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3	K/W

Note

1. Device mounted on an epoxy printed circuit board, 40 mm × 40 mm × 1.5 mm. Mounting pad for the drain lead minimum 6 cm^2.

N-channel enhancement mode vertical D-MOS transistor

BSP107

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 I_D = 10 μA	200	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 130 V V_{GS} = 0	–	–	30	nA
I_{DSX}	drain-source leakage current	V_{DS} = 70 V V_{GS} = 0.2 V	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	± V_{GS} = 15 V V_{DS} = 0	–	–	10	nA
$V_{GS(th)}$	gate threshold voltage	I_D =1 mA V_{DS} = V_{GS}	0.8	–	2.4	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA V_{GS} = 2.6 V	–	20	28	Ω
$R_{DS(on)}$	drain-source on-resistance	I_D = 150 mA V_{GS} = 10 V	–	14	–	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 250 mA V_{DS} = 15 V	90	180	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	50	65	pF
C_{oss}	output capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	16	25	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	4	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	switching-on time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 – 10 V	–	2	10	ns
t_{off}	switching-off time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 – 10 V	–	5	20	ns

N-channel enhancement mode vertical D-MOS transistor

BSP107

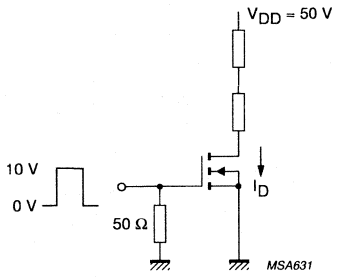


Fig.2 Switching time test circuit.

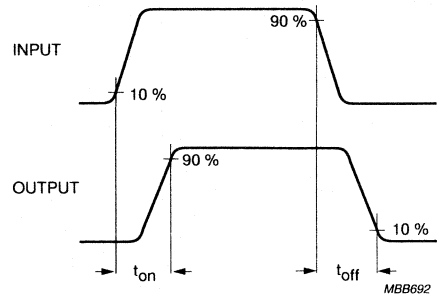


Fig.3 Input and output waveforms.

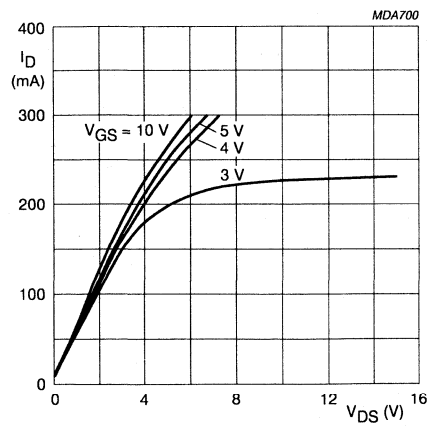


Fig.4 Typical output characteristics; T_j = 25° C.

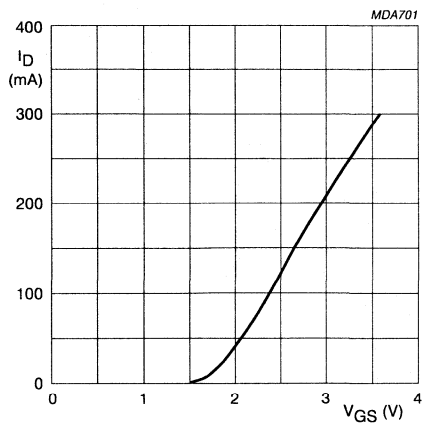


Fig.5 Typical transfer characteristics; V_{DS} = 10 V; T_j = 25° C.

N-channel enhancement mode vertical D-MOS transistor

BSP107

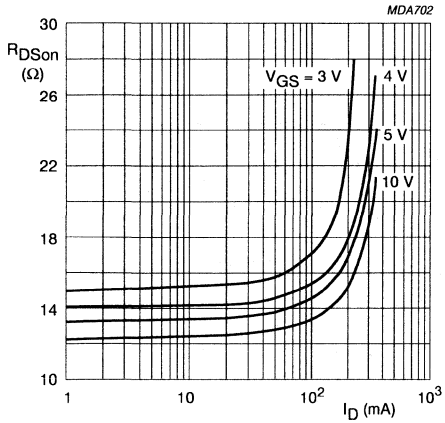


Fig.6 Typical on-resistance as a function of drain current; T_j = 25° C.

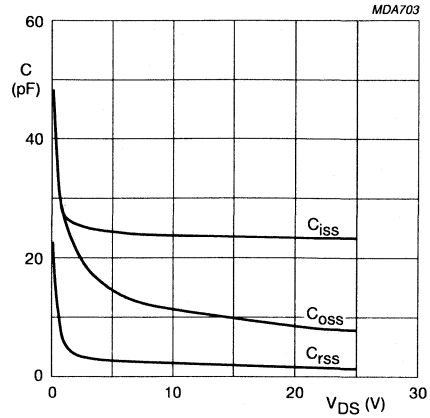
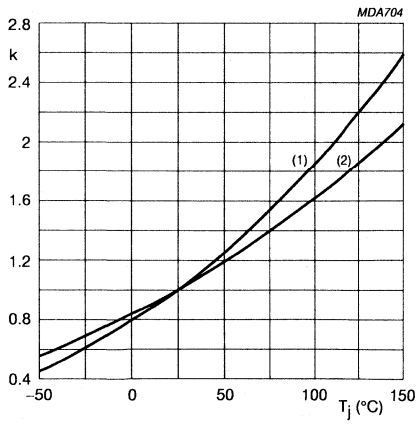


Fig.7 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25° C



(1) I_D = 150 mA; V_{GS} = 10 V;
(2) I_D = 20 mA; V_{GS} = 2.6 V

Fig.8 Temperature coefficient of drain-source on resistance;

$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C};$$

typical $R_{DS(on)}$ at 150 mA/10 V;

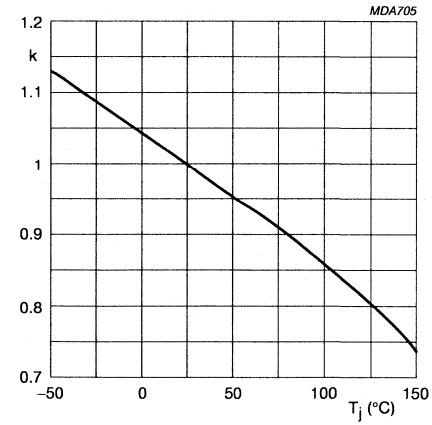


Fig.9 Temperature coefficient of gate-source threshold voltage;

$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C};$$

typical $V_{GS(th)}$ at 1 mA.

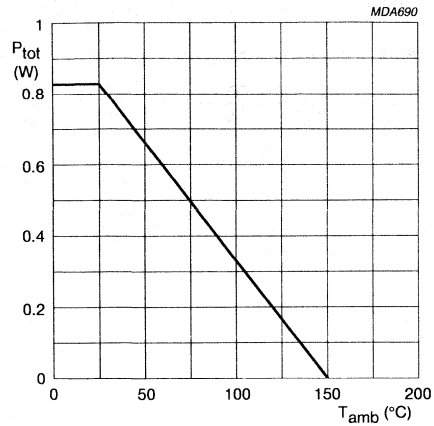


Fig.10 Power derating curve.

N-channel enhancement mode vertical D-MOS transistor

BSP108

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use in relay, high-speed and line-transformer drivers.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

PINNING - SOT223

1 = gate
2 = drain
3 = source
4 = drain

Marking code

BSP108

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	500	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1.5	W
Drain-source ON-resistance				
		typ.	2.0	Ω
I_D = 500 mA; V_{GS} = 10 V	$R_{DS(on)}$	max.	3.0	Ω
Transfer admittance				
I_D = 500 mA; V_{DS} = 15 V	$\|Y_{fs}\|$	min.	150	mS
		typ.	300	mS

PIN CONFIGURATION

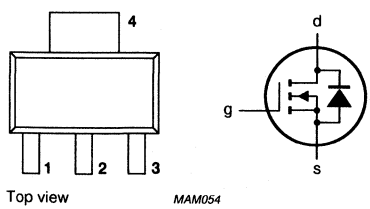


Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BSP108

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	500 mA
Drain current (peak)	I_{DM}	max.	1.0 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5 W
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	83.3 K/W

Note

1. Device mounted on an epoxy printed-circuit board 40 mm × 40 mm × 1.5 mm; mounting pad for the collector lead min. 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage			
I_D = 10 μA; V_{GS} = 0	$V_{(BR)\ DSS}$	min.	80 V
Gate threshold voltage			
I_D = 1 mA; V_{GS} = V_{DS}	$V_{GS\ (th)}$	min. max.	1.5 V 3.5 V
Gate-source leakage current			
$\pm V_{GS}$ = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Drain-source leakage current			
V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	1.0 μA
Drain-source ON-resistance			
I_D = 500 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	2.0 Ω 3.0 Ω
Transfer admittance			
I_D = 500 mA; V_{DS} = 15 V	$\lvert Y_{fs} \rvert$	min. typ.	150 mS 300 mS
Input capacitance at f = 1 MHz;			
V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	45 pF 60 pF
Output capacitance at f = 1 MHz;			
V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	30 pF 45 pF

Feedback capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ.	8 pF
		max.	12 pF
Switching times (see Figs 2 and 3)			
I_D = 500 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ.	4 ns
		max.	8 ns
	t_{off}	typ.	10 ns
		max.	15 ns

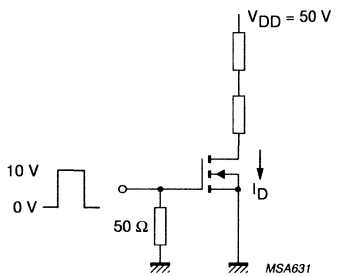


Fig.2 Switching times test circuit.

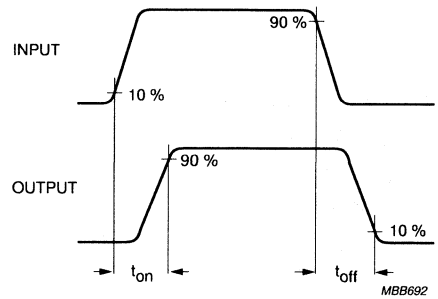


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistor

BSP108

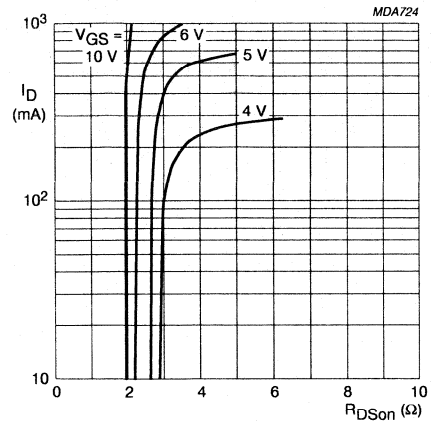


Fig.4 T_j = 25 °C; typical values.

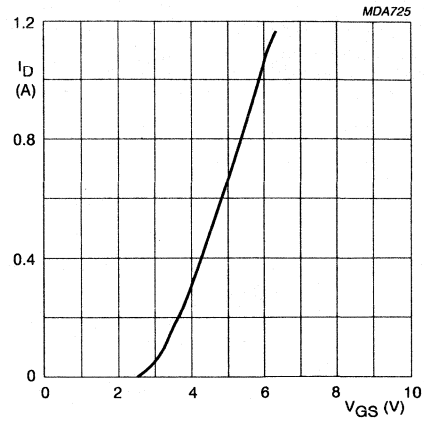


Fig.5 T_j = 25 °C; typical values at V_{DS} = 10 V.

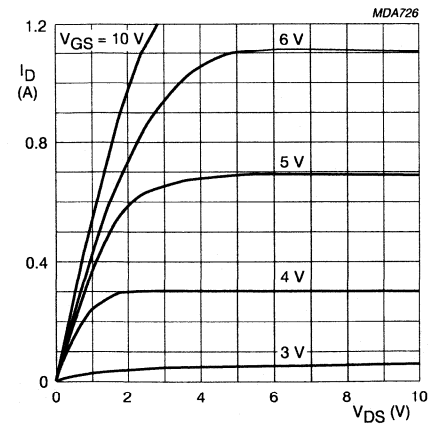


Fig.6 T_j = 25 °C; typical values.

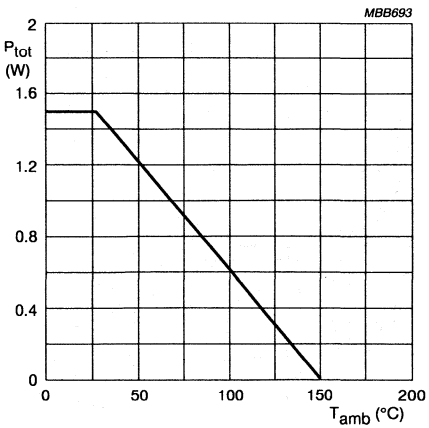


Fig.7 Power derating curve.

N-channel enhancement mode vertical D-MOS transistor

BSP108

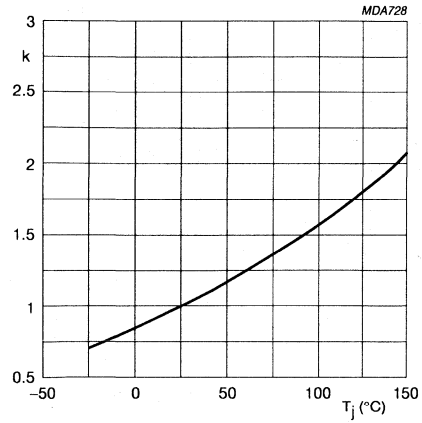


Fig.8

$$k = \frac{R_{DS\,on} \text{ at } T_j}{R_{DS\,on} \text{ at } 25\ °C};$$

typical values at 500 mA/10 V.

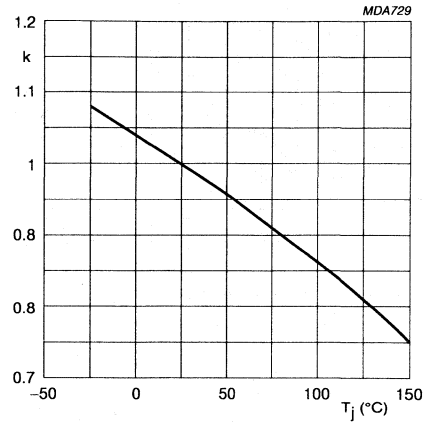


Fig.9

$$k = \frac{V_{GS\,(th)} \text{ at } T_j}{V_{GS\,(th)} \text{ at } 25\ °C};$$

$V_{GS(th)}$ at 1 mA; typical values.

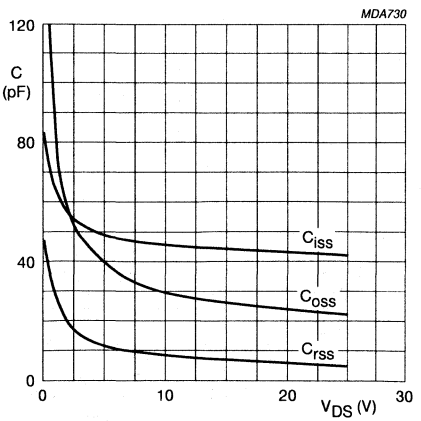


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-channel enhancement mode vertical D-MOS transistor

BSP110

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and designed for use in telephone ringer circuits and for application in relay, high-speed and line transformer drivers.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80	V
Drain source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	100	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	325	mA
Total power dissipation up to $T_{amb} = 25$ °C	P_{tot}	max.	1.5	W
Drain-source ON-resistance $I_D = 200$ mA; $V_{GS} = 10$ V	$R_{DS(on)}$	typ.	4.5	Ω
		max.	7	Ω
Transfer admittance $I_D = 200$ mA; $V_{DS} = 15$ V	$\lvert Y_{fs} \rvert$	min.	75	mS
		typ.	150	mS

PINNING - SOT223

1 = gate
2 = drain
3 = source
4 = drain

MARKING CODE

BSP110

PIN CONFIGURATION

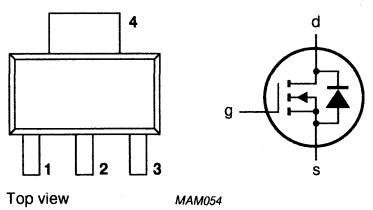


Fig.1 Simplfied outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BSP110

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80	V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	100	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	325	mA
Drain current (peak)	I_{DM}	max.	650	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5	W
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	83.3	K/W

Note

1. Device mounted on an epoxy printed-circuit board 40 mm × 40 mm × 1.5 mm; mounting pad for the drain lead min. 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)\ DSS}$	min.	80	V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	1.0	μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$I_{GS(th)}$	min. max.	0.8 2.8	V V
Drain-source ON-resistance (see Fig.4) I_D = 150 mA; V_{GS} = 5 V	$R_{DS(on)}$	typ. max.	7 10	Ω Ω
I_D = 200 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	4.5 7	Ω Ω
Transfer admittance I_D = 200 mA; V_{DS} = 5 V	$\lvert Y_{fs} \rvert$	min. typ.	75 150	mS mS
Input capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	15 30	pF pF

N-channel enhancement mode vertical D-MOS transistor

BSP110

Output capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ.	13 pF
		max.	20 pF
Feedback capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ.	3 pF
		max.	6 pF
Switching times (see Figs 2 and 3)			
I_D = 200 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ.	2 ns
		max.	5 ns
	t_{off}	typ.	5 ns
		max.	10 ns

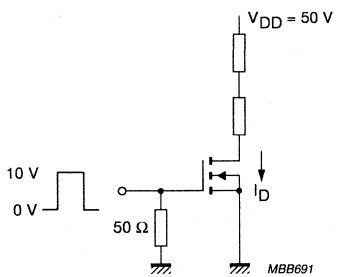


Fig.2 Switching time test circuit.

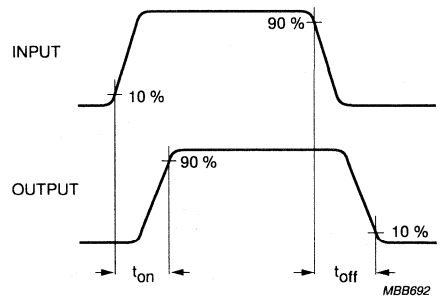


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistor

BSP110

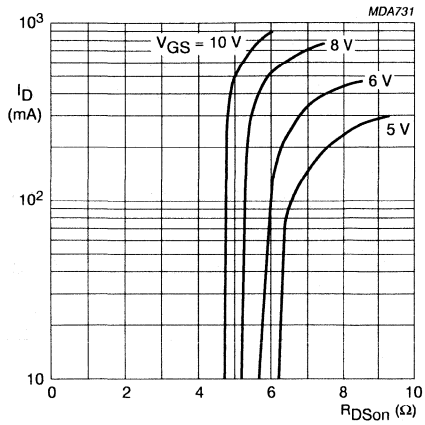


Fig.4 T_j = 25 °C; typical values.

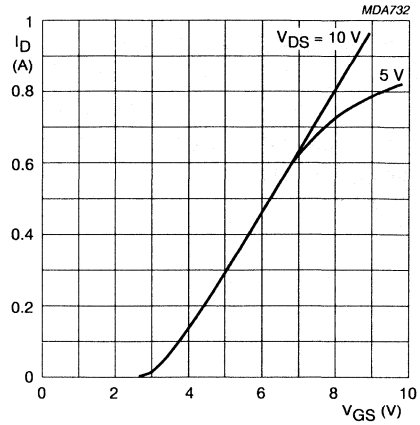


Fig.5 T_j = 25 °C; typical values.

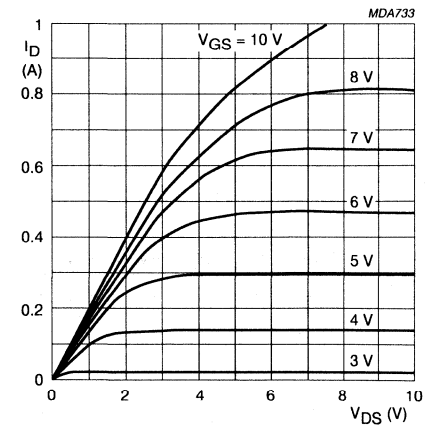


Fig.6 T_j = 25 °C; typical values.

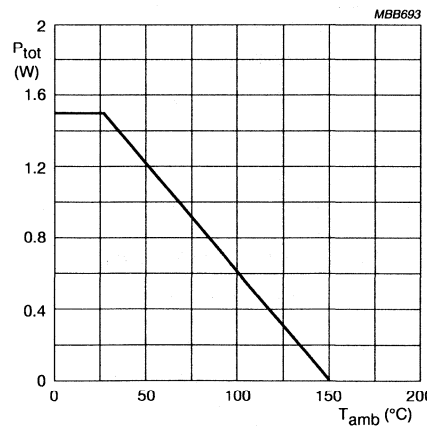


Fig.7 Power derating curve.

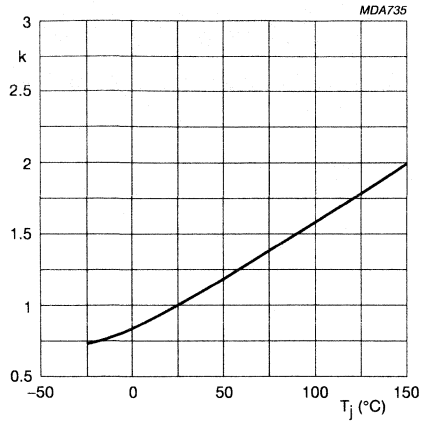


Fig.8

$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C};$$

typical values at 150 mA/5 V.

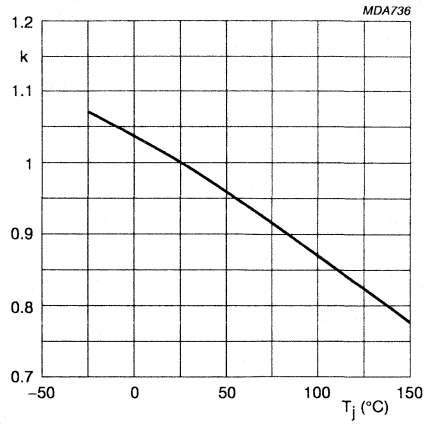


Fig.9

$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C};$$

$V_{GS(th)}$ at 1 mA; typical values.

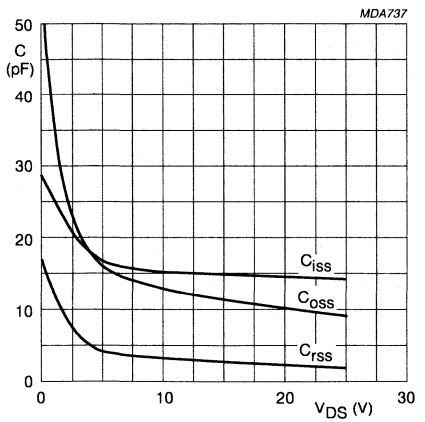


Fig.10 $T_j = 25$ °C; $V_{GS} = 0$; f = 1 MHz; typical values.

N-channel enhancement mode vertical D-MOS transistor

BSP120

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and designed for use as a line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200	V
Drain-current (DC)	I_D	max.	250	mA
Drain-source ON-resistance I_D = 250 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	7	Ω
		max.	12	Ω
Gate threshold voltage	$V_{GS(th)}$	max.	2.8	V

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

PINNING - SOT223

1 = gate
2 = drain
3 = source
4 = drain

Marking code

BSP120

PIN CONFIGURATION

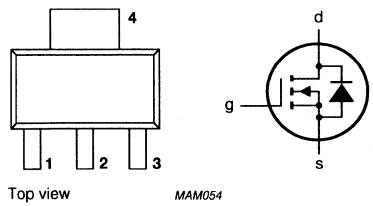


Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BSP120

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Drain current (peak)	I_{DM}	max.	800 mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5 W
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	83.3 K/W

Note

1. Device mounted on an epoxy printed-circuit board 40 mm × 40 mm × 1.5 mm; mounting pad for the drain lead min. 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage			
I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200 V
Drain-source leakage current			
V_{DS} =160 V; V_{GS} = 0	I_{DSS}	max.	1.0 μA
Gate-source leakage current			
V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Drain-source ON-resistance (see Fig.4)			
I_D = 250 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	7 Ω 12 Ω
Gate threshold voltage			
I_D = 1 mA; V_{GS} = V_{DS}	$V_{GS(th)}$	min. max.	0.8 V 2.8 V
Transfer admittance			
I_D = 250 mA; V_{DS} = 15 V	$\lvert Y_{fs} \rvert$	min. typ.	125 mS 250 mS
Input capacitance at f = 1 MHz;			
V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	45 pF 65 pF
Output capacitance at f = 1 MHz;			
V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	20 pF 30 pF

N-channel enhancement mode vertical D-MOS transistor

BSP120

Feedback capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ.	5 pF
		max.	10 pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ.	3 ns
		max.	6 ns
	t_{off}	typ.	15 ns
		max.	20 ns

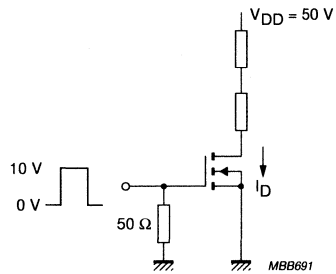


Fig.2 Switching time test circuit.

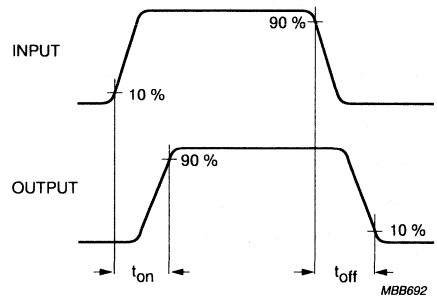


Fig.3 Input and output waveforms.

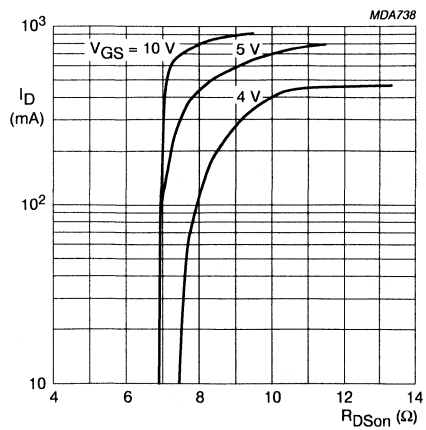


Fig.4 T_j = 25 °C; typical values.

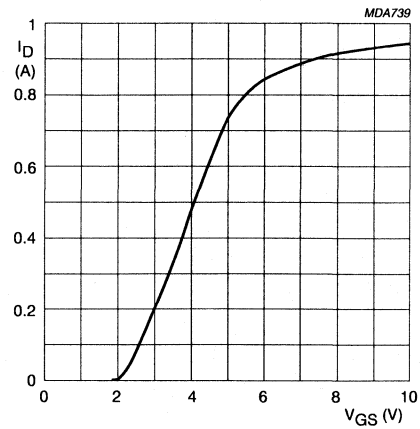


Fig.5 T_j = 25 °C; V_{DS} = 10 V; typical values.

N-channel enhancement mode vertical D-MOS transistor

BSP120

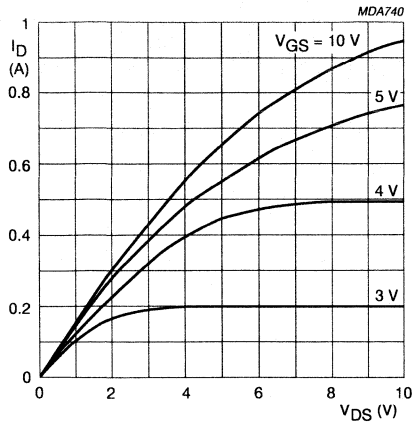


Fig.6 T_j = 25 °C; typical values.

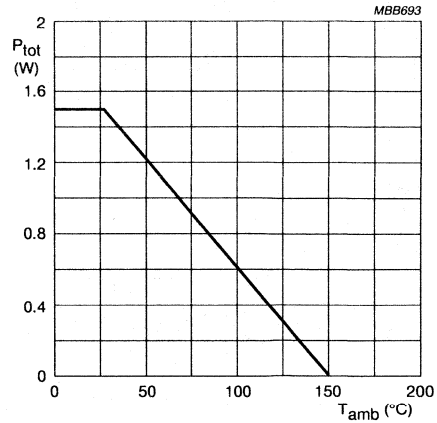


Fig.7 Power derating curve.

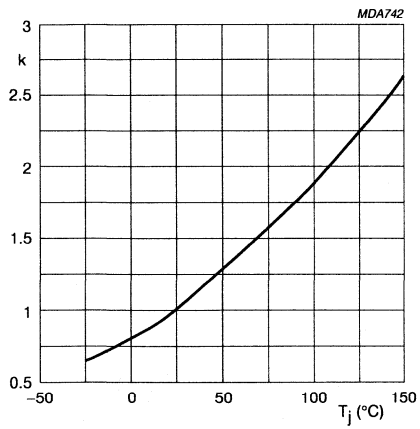


Fig.8

$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C};$$

at 250 mA/10 V; typical values.

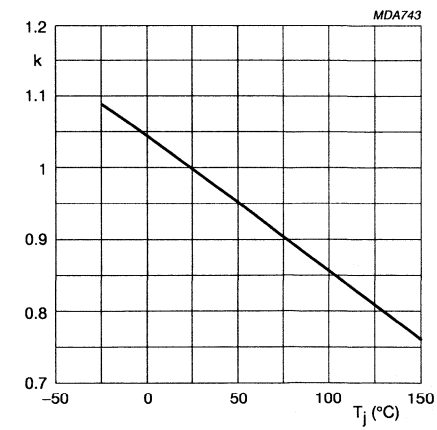


Fig.9

$$k = \frac{V_{GS\,(th)} \text{ at } T_j}{V_{GS\,(th)} \text{ at } 25\ °C};$$

$V_{GS(th)}$ at 1 mA; typical values.

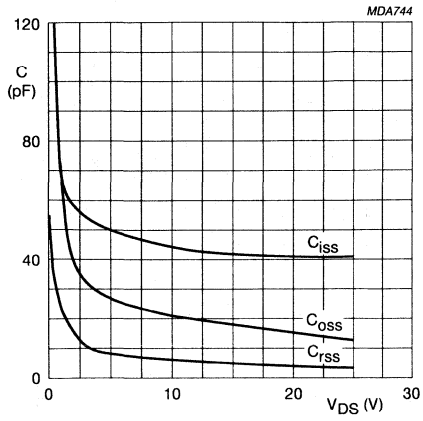


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-channel enhancement mode vertical D-MOS transistor

BSP121

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and designed for use as a line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	350	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1.5	W
Drain-source on-resistance I_D = 400 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	4.5 6.0	Ω Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\lvert Y_{fs} \rvert$	min. typ.	200 350	mS mS

PINNING - SOT223

1 = gate
2 = drain
3 = source
4 = drain

Marking code

BSP121

PIN CONFIGURATION

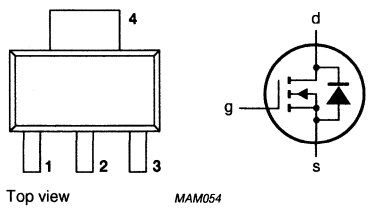


Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BSP121

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	350	mA
Drain current (peak)	I_{DM}	max.	1.2	A
Total power dissipation up to				
T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5	W
Storage temperature range	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{thj\text{-}a}$	=	83.3	K/W

Note

1. Device mounted on an epoxy printed-circuit board 40 mm × 40 mm × 1.5 mm; mounting pad for the drain lead min. 6 cm^2.

N-channel enhancement mode vertical D-MOS transistor

BSP121

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage			
I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200 V
Drain-source leakage current			
V_{DS} = 160 V; V_{GS} = 0	I_{DSS}	max.	1.0 μA
V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	200 nA
Gate-source leakage current			
± V_{GS} = 20 V; V_{DS} = 0	$\pm I_{GSS}$	max.	100 nA
Gate threshold voltage			
I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min.	0.8 V
		max.	2.8 V
Drain-source on-resistance			
I_D = 400 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	4.5 Ω
		max.	6.0 Ω
Transfer admittance			
I_D = 400 mA; V_{DS} = 25 V	$\lvert Y_{fs} \rvert$	min.	200 mS
		typ.	350 mS
Input capacitance at f = 1 MHz			
V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ.	45 pF
		max.	60 pF
Output capacitance at f = 1 MHz			
V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ.	15 pF
		max.	25 pF
Feedback capacitance at f = 1 MHz			
V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ.	3.5 pF
		max.	10 pF
Switching times (see Figs 2 and 3)			
I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ.	5 pF
		max.	10 pF
	t_{off}	typ.	15 ns
		max.	20 ns

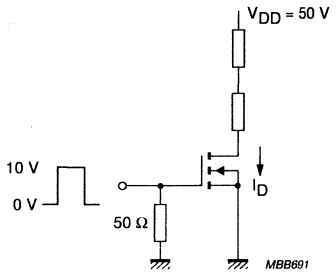


Fig.2 Switching time test circuit

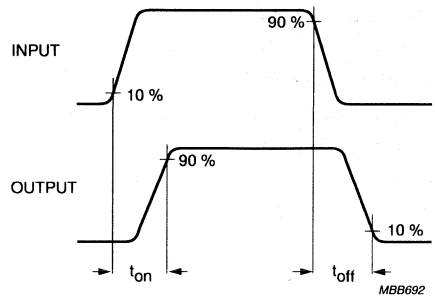


Fig.3 Input and output waveforms.

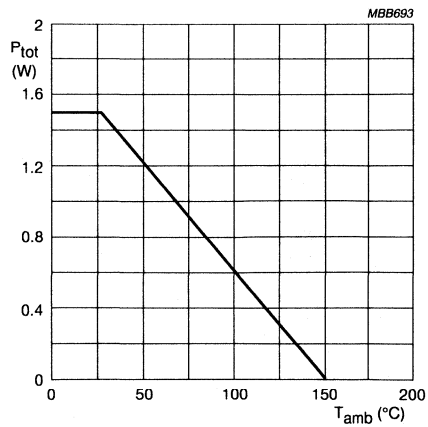


Fig.4 Power derating curve.

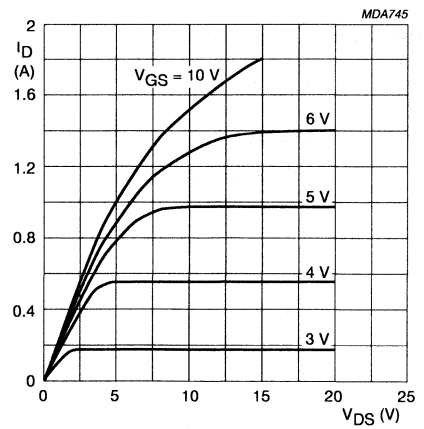


Fig.5 Output characteristic; T_j = 25 °C; typical value.

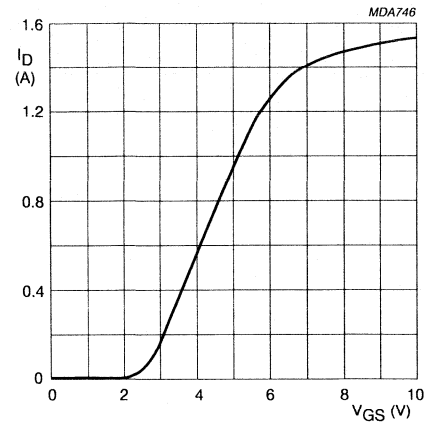


Fig.6 Transfer characteristic; V_{DS} = 10 V; T_j = 25 °C; typical values.

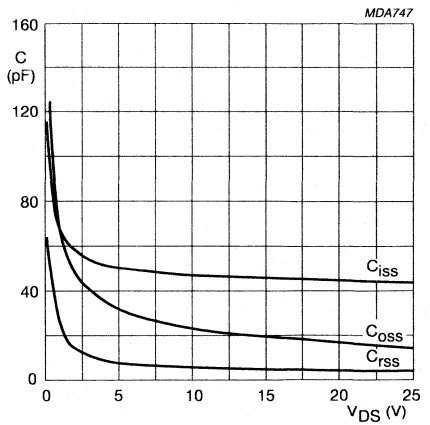


Fig.7 Capacitance as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C; typical values.

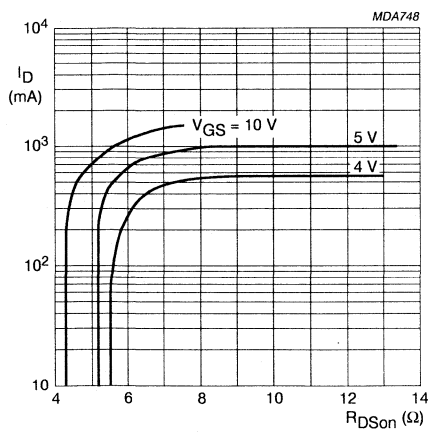


Fig.8 T_j = 25 °C; typical values.

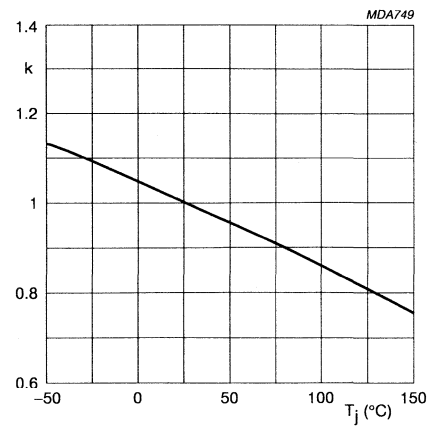


Fig.9

$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C};$$

$V_{GS(th)}$ at 1 mA; typical values.

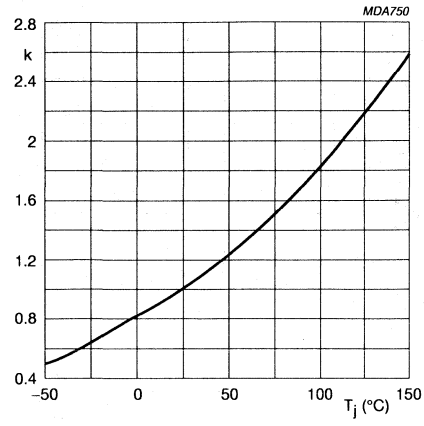


Fig.10

$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C};$$

at 400 mA/10 V; typical values.

N-channel enhancement mode vertical D-MOS transistor

BSP122

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	200	V
I_D	DC drain current	550	mA
$R_{DS(on)}$	drain-source on-resistance	2.5	Ω
$V_{GS(th)}$	gate-source threshold voltage	2	V

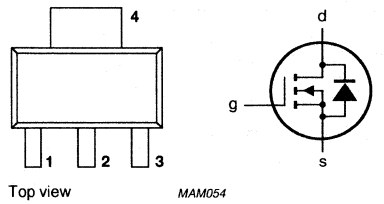


Fig.1 Simplified outline (SOT223) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	550	mA
I_{DM}	peak drain current		–	3	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3 K/W

Note

1. Device mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm^2.

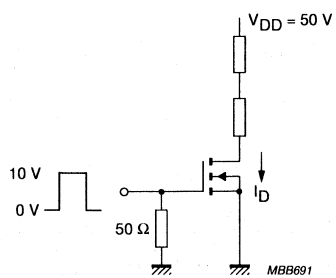
N-channel enhancement mode vertical D-MOS transistor

BSP122

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	200	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 160 V; V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	0.4	–	2	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 750 mA; V_{GS} = 10 V	–	1.6	2.5	Ω
		I_D = 20 mA; V_{GS} = 2.4 V	–	2.5	–	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 750 mA; V_{DS} = 25 V	400	800	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	165	–	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	40	–	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	9	–	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 750 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	–	35	ns
t_{off}	turn-off time	I_D = 750 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	–	50	ns



V_{DD} = 50 V.

Fig.2 Switching times test circuit.

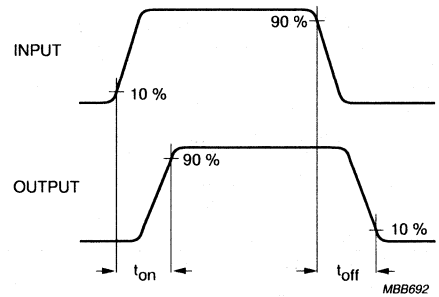


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistor

BSP126

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and designed for use as a line interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching.
- No secondary breakdown.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	250	V
Drain current (DC)	I_D	max.	350	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1.5	W
Drain-source on-resistance				
I_D = 300 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	5.0	Ω
		max.	7.0	Ω
Gate-source threshold voltage	$V_{GS(th)}$	max.	2	V

PINNING - SOT223

1 = gate
2 = drain
3 = source
4 = drain

Marking code

BSP126

PIN CONFIGURATION

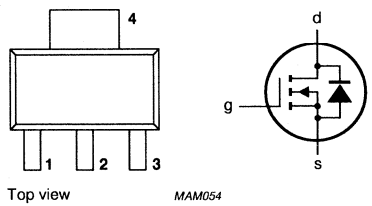


Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BSP126

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	250	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	350	mA
Drain current (peak)	I_{DM}	max.	1.2	A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5	W
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	83.3	K/W

Note

1. Device mounted on an epoxy printed-circuit board 40 mm × 40 mm × 1.5 mm; mounting pad for the drain lead min. 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage				
I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	250	V
Drain-source leakage current				
V_{DS} = 200 V; V_{GS} = 0	I_{DSS}	max.	1.0	μA
Gate-source leakage current				
± V_{GS} = 20 V; V_{DS} = 0	$\pm I_{GSS}$	max.	100	nA
Gate threshold voltage				
I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min.	0.8	V
		max.	2.0	V
Drain-source on-resistance				
I_D = 300 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	5.0	Ω
		max.	7.0	Ω
I_D = 20 mA; V_{GS} = 2.4 V	$R_{DS(on)}$	max.	10	Ω
Transfer admittance				
I_D = 300 mA; V_{DS} = 25 V	$\lvert Y_{fs} \rvert$	min.	200	mS
		typ.	400	mS
Input capacitance at f = 1 MHz;				
V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ.	65	pF
		max.	90	pF
Output capacitance at f = 1 MHz;				
V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ.	20	pF
		max.	30	pF

N-channel enhancement mode vertical D-MOS transistor

BSP126

Feedback capacitance at f = 1 MHz; V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ.	5 pF
		max.	15 pF
Switching times (see Figs 2 and 3)			
I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ.	5 ns
		max.	10 ns
	t_{off}	typ.	20 ns
		max.	30 ns

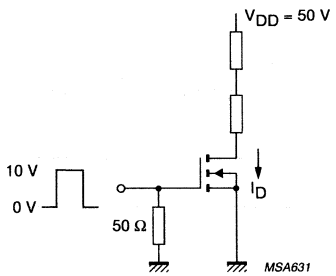


Fig.2 Switching time test circuit.

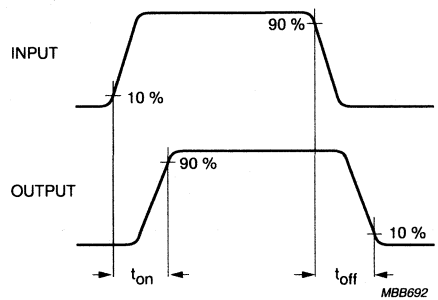


Fig.3 Input and output waveforms.

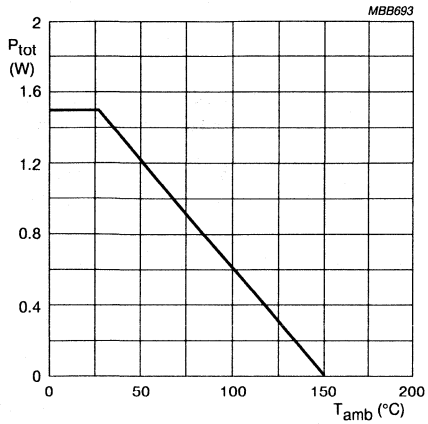


Fig.4 Power derating curve.

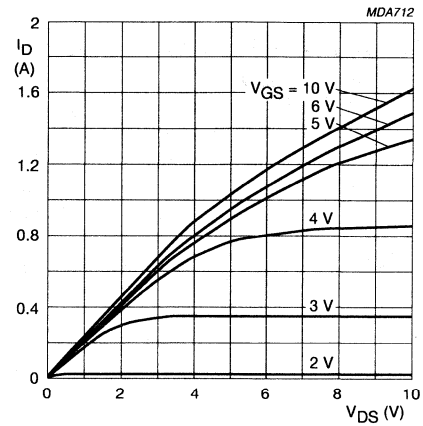


Fig.5 Output characteristics; T_j = 25 °C; typical values.

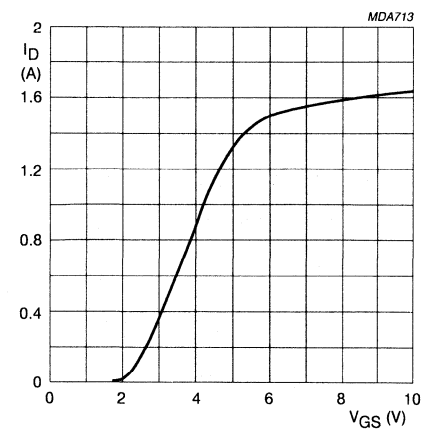


Fig.6 Transfer characteristic; V_{DS} = 10 V; T_j = 25 °C; typical value.

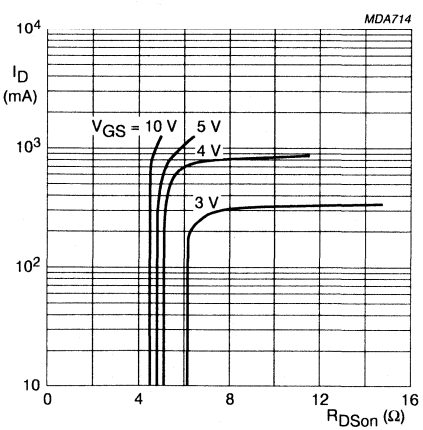


Fig.7 On-resistance as a function of drain current; T_j = 25 °C; typical values.

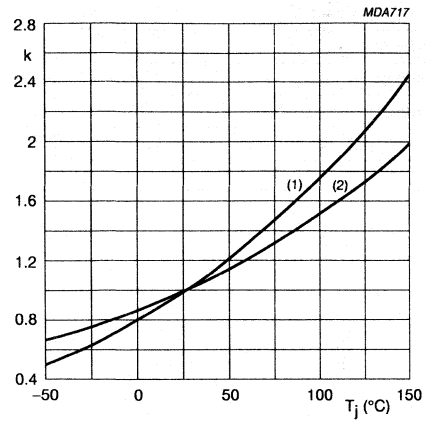


Fig.8 $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$; typical values.

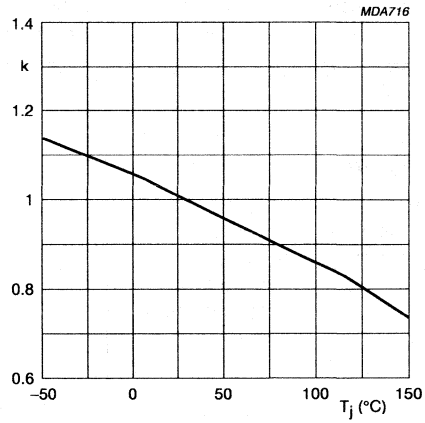


Fig.9 $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}$; $V_{GS(th)}$ at 1 mA; typical values.

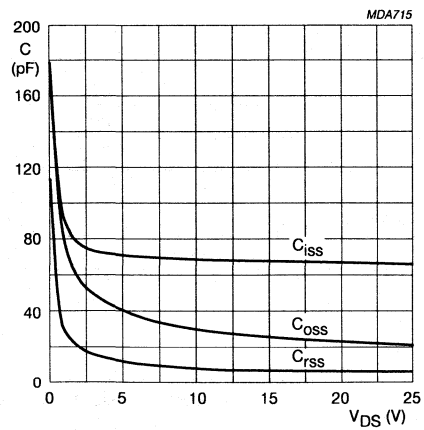


Fig.10 Capacitances as a function of drain-source voltage; $V_{GS} = 0$; f = 1 MHz; $T_j = 25$ °C; typical values.

N-channel enhancement mode vertical D-MOS transistor

BSP127

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	270	V
I_D	DC drain current	350	mA
$R_{DS(on)}$	drain-source on-resistance	8	Ω
$V_{GS(th)}$	gate-source threshold voltage	2	V

PINNING - SOT223

PIN	DESCRIPTION
Code: BSP127	
1	gate
2	drain
3	source
4	drain

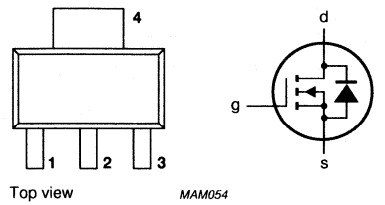


Fig.1 Simplified outline (SOT223) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	270	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	350	mA
I_{DM}	peak drain current		–	1.4	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3 K/W

Note

1. Device mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm^2.

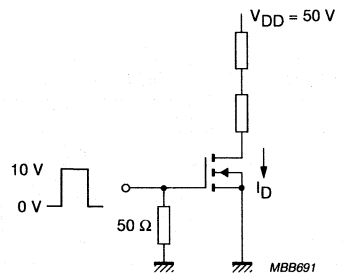
N-channel enhancement mode vertical D-MOS transistor

BSP127

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	270	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 220 V; V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	0.8	–	2	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 250 mA; V_{GS} = 10 V	–	6.5	8	Ω
		I_D = 20 mA; V_{GS} = 2.4 V	–	9	14	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 250 mA; V_{DS} = 25 V	200	400	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	55	80	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	5	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	20	30	ns



V_{DD} = 50 V.

Fig.2 Switching times test circuit.

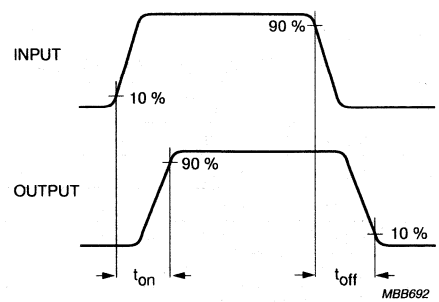


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistor

BSP128

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
Code: BSP128	
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	200	V
I_D	DC drain current	350	mA
$R_{DS(on)}$	drain-source on-resistance	8	Ω
$V_{GS(th)}$	gate-source threshold voltage	1.8	V

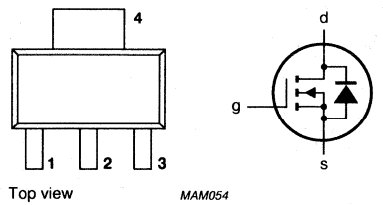


Fig.1 Simplified outline (SOT223) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	350	mA
I_{DM}	peak drain current		–	1.4	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		−65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3 K/W

Note

1. Device mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm^2.

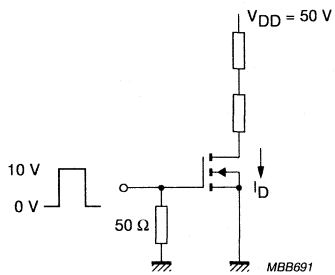
N-channel enhancement mode vertical D-MOS transistor

BSP128

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	200	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 160 V; V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	0.4	–	1.8	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 100 mA; V_{GS} = 2.8 V	–	5	8	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 300 mA; V_{DS} = 25 V	200	400	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	50	80	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	5	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	20	30	ns



V_{DD} = 50 V.

Fig.2 Switching times test circuit.

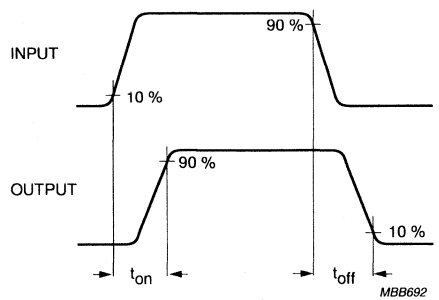


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistor

BSP130

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

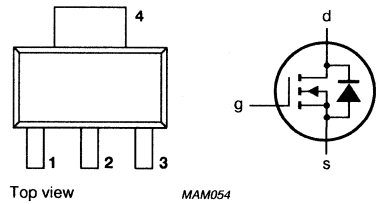
N-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	300	V
I_D	DC drain current		–	300	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	1.5	W
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 250 mA; V_{GS} = 10 V	–	8	Ω
$V_{GS(off)}$	gate-source cut-off voltage	I_D = 1 mA; $V_{DS} = V_{GS}$	0.8	2	V



Top view MAM054

Marking code
BSP130.

Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BSP130

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	300	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	300	mA
I_{DM}	peak drain current		–	1.4	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C; note 1	–	1.5	W
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient; note 1	83.3 K/W

Note

1. Device mounted on an epoxy printed-circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm^2.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	300	–	–	V
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}	0.8	–	2	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA; V_{GS} = 2.4 V	–	7.9	14	Ω
		I_D = 250 mA; V_{GS} = 10 V	–	6.7	8	Ω
I_{DSS}	drain-source leakage current	V_{DS} = 240 V; V_{GS} = 0	–	–	100	nA
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 250 mA; V_{DS} = 25 V	200	380	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	57	90	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	15	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	2.6	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	2.5	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 10 to 0 V	–	17	30	ns

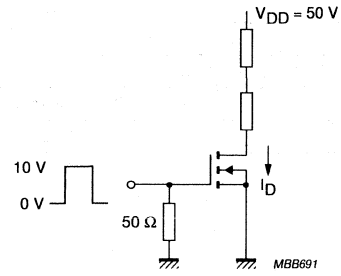


Fig.2 Switching times test circuit.

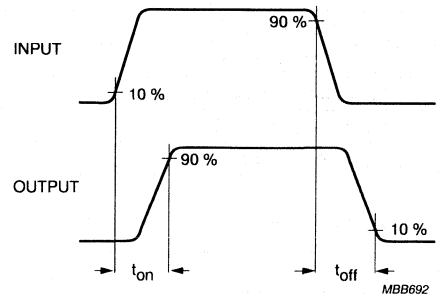


Fig.3 Input and output waveforms.

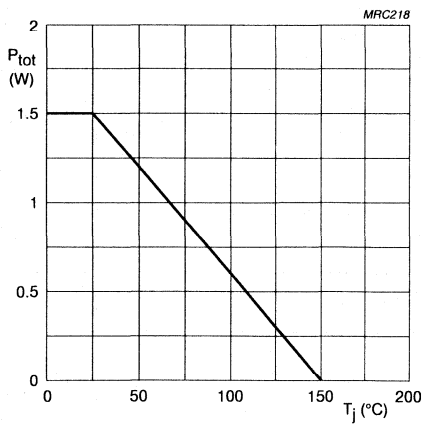
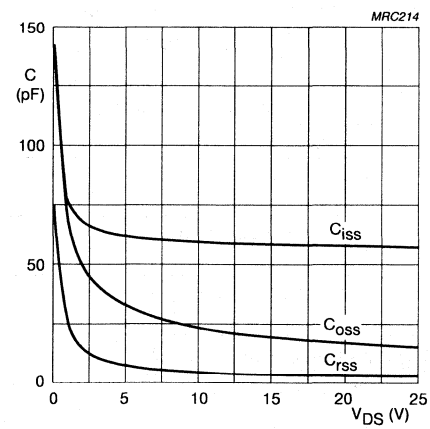


Fig.4 Power derating curve.

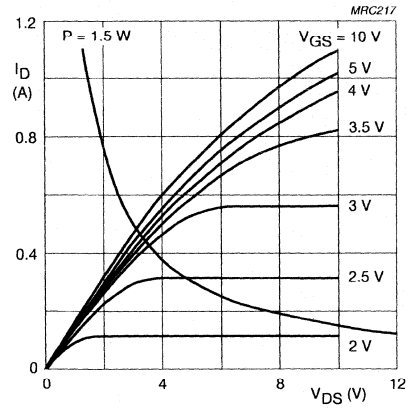


V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

Fig.5 Capacitance as a function of drain-source voltage, typical values.

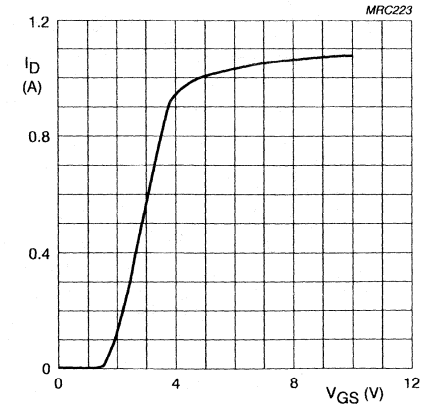
N-channel enhancement mode vertical D-MOS transistor

BSP130



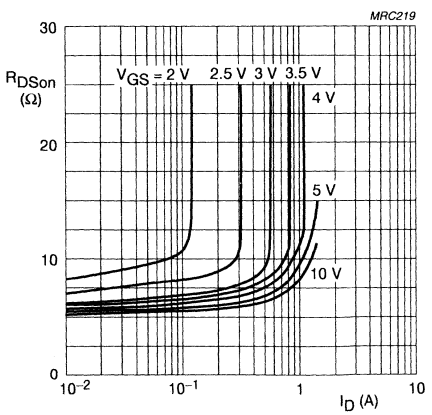
T_j = 25 °C.

Fig.6 Typical output characteristics.



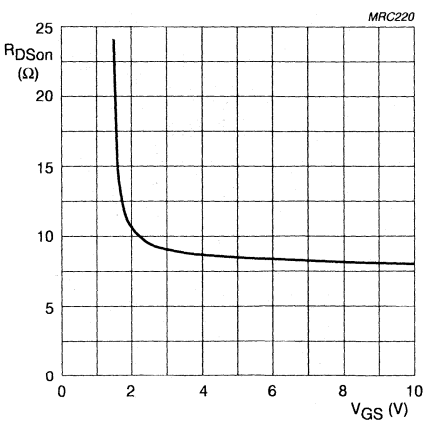
V_{DS} = 10 V; T_j = 25 °C.

Fig.7 Typical transfer characteristics.



T_j = 25 °C.

Fig.8 Drain-source on-resistance as a function of drain current, typical values.



V_{DS} = 100 mV; T_j = 25 °C.

Fig.9 Drain-source on-resistance as a function of gate-source voltage, typical values.

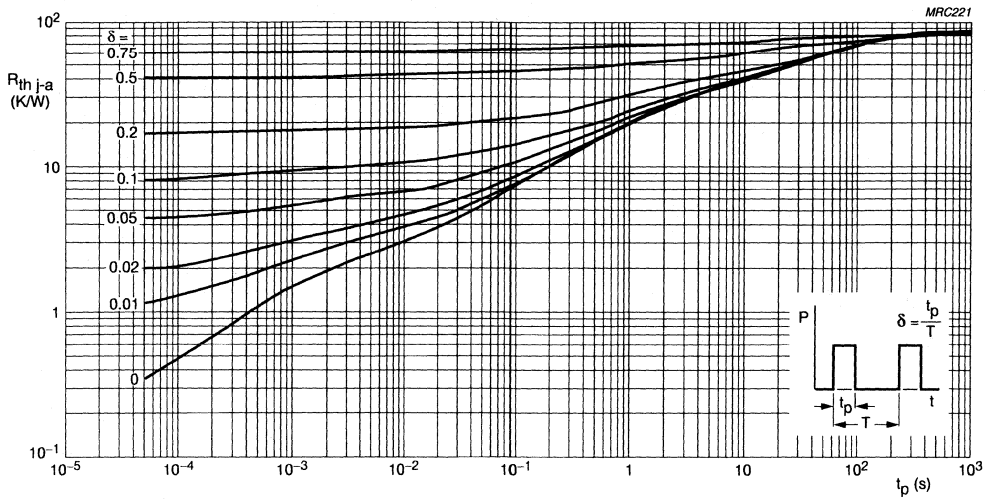
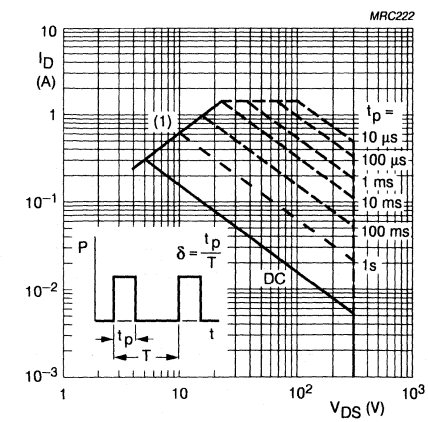
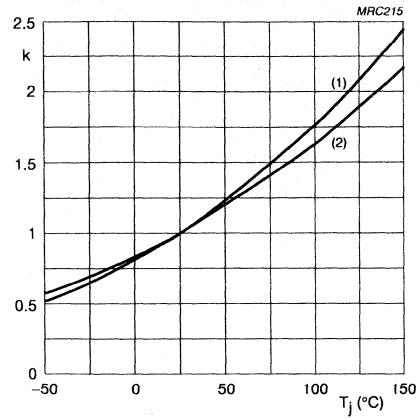


Fig.10 Transient thermal resistance from junction to ambient as a function of pulse time.



δ = 0.01; T_{amb} = 25 °C.
(1) $R_{DS(on)}$ limitation.

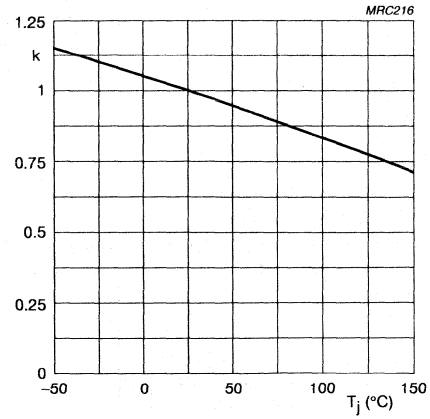
Fig.11 SOAR curve.



$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$$

Typical $R_{DS(on)}$;
(1) I_D = 250 mA; V_{GS} = 10 V.
(2) I_D = 20 mA; V_{GS} = 2.4 V.

Fig.12 Temperature coefficient of drain-source on-resistance.



$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}.$$

Typical $V_{GS(th)}$ at 1 mA.

Fig.13 Temperature coefficient of gate-source threshold voltage.

P-channel enhancement mode vertical D-MOS transistor

BSP204; BSP204A

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope, intended for use in relay, high-speed and line transformer drivers.

PINNING - TO-92 variant (BSP204)

PIN	DESCRIPTION
1	gate
2	drain
3	source

PINNING - TO-92 variant (BSP204A)

PIN	DESCRIPTION
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$-V_{DS}$	drain-source voltage		200	V
$-I_D$	drain current	DC value	250	mA
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 200 mA $-V_{GS}$ = 10 V	15	Ω
$V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA $V_{GS} = V_{DS}$	2.8	V

PIN CONFIGURATION

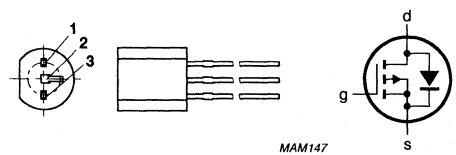


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage		–	20	V
$-I_D$	drain current	DC value	–	250	mA
$-I_{DM}$	drain current	peak value	–	600	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1	W
T_{stg}	storage temperature range		−65	150	°C
T_j	junction temperature		–	150	°C

Note

1. Device mounted on an epoxy printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm x 10 mm.

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	125	K/W

Note

1. Device mounted on an epoxy printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm x 10 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-I_D$ = 10 μA V_{GS} = 0	200	–	–	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 160 V V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	–	–	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA $V_{GS} = V_{DS}$	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 200 mA $-V_{GS}$ = 10 V	–	10	15	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	$-I_D$ = 200 mA $-V_{DS}$ = 25 V	100	200	–	mS
C_{iss}	input capacitance	$-V_{DS}$ = 25 V $-V_{GS}$ = 0 f = 1 MHz	–	65	90	pF
C_{oss}	output capacitance	$-V_{DS}$ = 25 V $-V_{GS}$ = 0 f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	$-V_{DS}$ = 25 V $-V_{GS}$ = 0 f = 1 MHz	–	6	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	20	30	ns

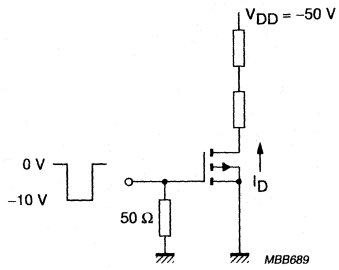


Fig.2 Switching time test circuit.

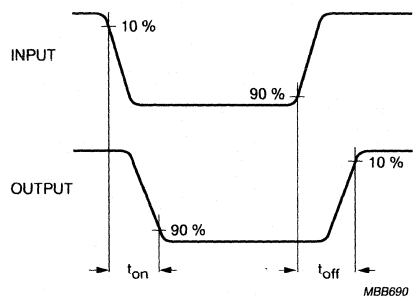


Fig.3 Input and output waveforms.

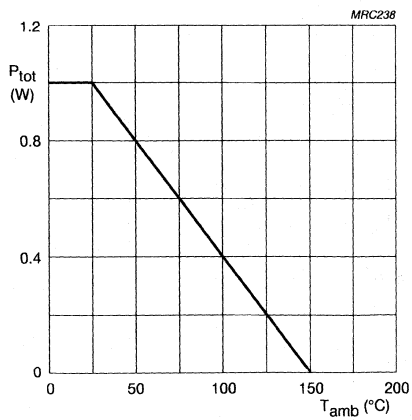


Fig.4 Power derating curve.

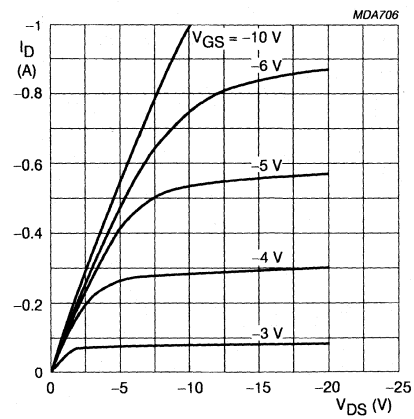


Fig.5 Typical output characteristics; T_j = 25 °C.

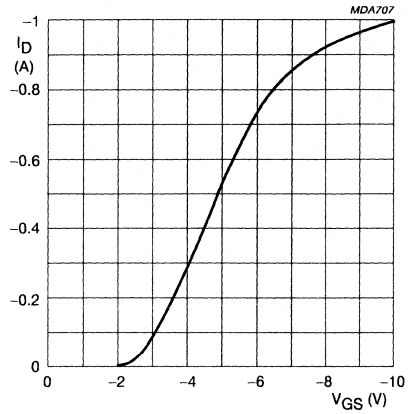


Fig.6 Typical transfer characteristic; $-V_{DS} = 10$ V; $T_j = 25$ °C.

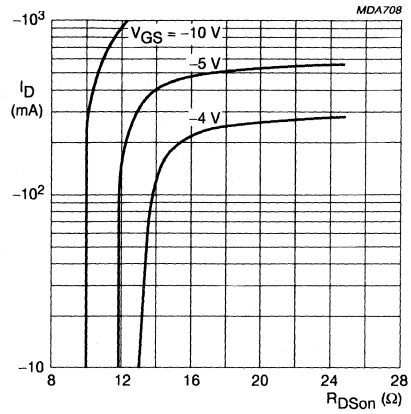


Fig.7 Typical on-resistance as a function of drain current; $T_j = 25$ °C.

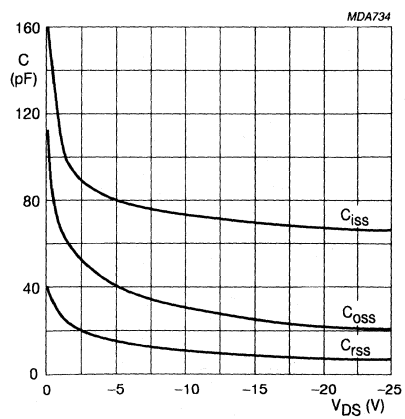


Fig.8 Typical capacitances as a function of drain-source voltage; $V_{GS} = 0$; $f = 1$ MHz; $T_j = 25$ °C.

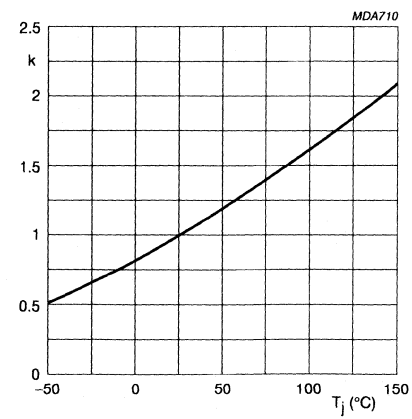


Fig.9 Temperature coefficient of drain-source on-resistance;

$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C};$$

typical $R_{DS(on)}$ at −200 mA/−10 V.

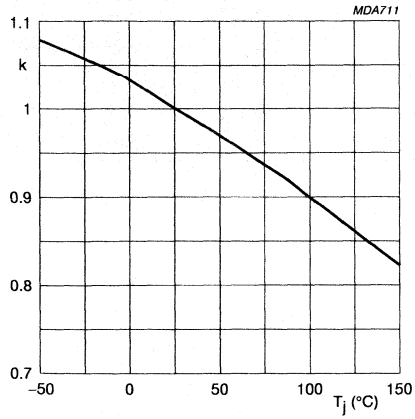


Fig.10 Temperature coefficient of gate-source threshold voltage;

$$k = \frac{-V_{GS(th)} \text{ at } T_j}{-V_{GS(th)} \text{ at } 25\ °C};$$

typical $-V_{GS(th)}$ at −1 mA.

P-channel enhancement mode vertical D-MOS transistor

BSP205

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use in relay, high-speed and line-transformer drivers.

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60	V
Drain current (DC)	$-I_D$	max.	275	mA
Drain-source ON-resistance				
$-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$R_{DS(on)}$	max.	10	Ω
Gate threshold voltage	$-V_{GS(th)}$	max.	3.5	V

FEATURES

- Very low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

PINNING - SOT223

1 = gate
2 = drain
3 = source
4 = drain

PIN CONFIGURATION

Marking code

BSP205

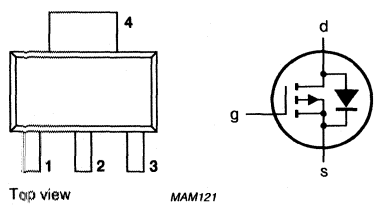


Fig.1 Simplified outline and symbol.

P-channel enhancement mode vertical D-MOS transistor

BSP205

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	275	mA
Drain current (peak)	$-I_{DM}$	max.	550	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5	W
Storage temperature range	T_{stg}		−65 to 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	83.3	K/W

Note

1. Device mounted on an epoxy printed-circuit board 40 mm × 40 mm × 1.5 mm; mounting pad for the drain lead min. 6 cm^2.

P-channel enhancement mode vertical D-MOS transistor

BSP205

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage			
$-I_D$ = 10 μA; V_{GS} = 0	$-V_{(BR)DSS}$	min.	60 V
Drain-source leakage current			
$-V_{DS}$ = 48 V; V_{GS} = 0	$-I_{DSS}$	max.	1.0 μA
Gate-source leakage current			
± V_{GS} = 20 V; V_{DS} = 0	$\pm I_{GSS}$	max.	100 nA
Gate threshold voltage			
$-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min.	1.5 V
		max.	3.5 V
Drain-source ON-resistance			
$-I_D$ = 200 mA ; $-V_{GS}$ = 10 V	$R_{DS(on)}$	typ.	7.5 Ω
		max.	10 Ω
Transfer admittance			
$-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert Y_{fs} \rvert$	min.	60 mS
		typ.	125 mS
Input capacitance at f = 1 MHz;			
$-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ.	30 pF
		max.	45 pF
Output capacitance at f = 1 MHz;			
$-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ.	20 pF
		max.	30 pF
Feedback capacitance at f = 1 MHz;			
$-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ.	5 pF
		max.	10 pF
Switching times (see Figs 2 and 3)			
$-I_D$ = 200 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on}	typ.	3 ns
		max.	6 ns
	t_{off}	typ.	10 ns
		max.	15 ns

P-channel enhancement mode vertical D-MOS transistor

BSP205

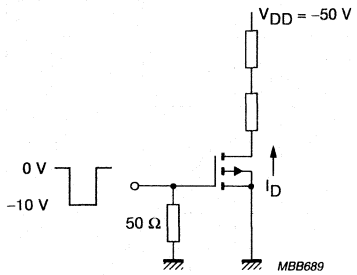


Fig.2 Switching time test circuit.

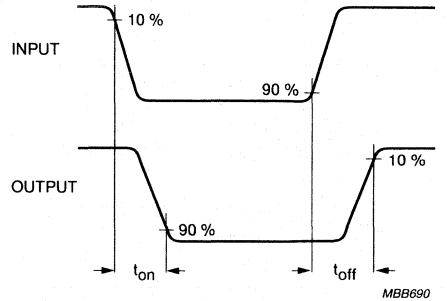


Fig.3 Input and output waveforms.

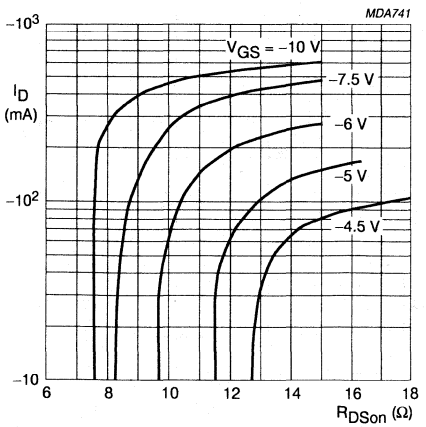


Fig.4 ON-resistance as a function of drain current; T_j = 25 °C; typical values.

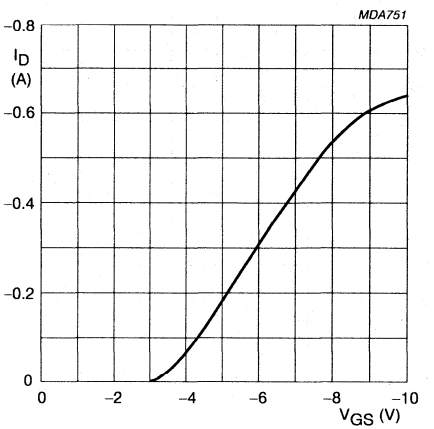


Fig.5 Transfer characteristics; $-V_{DS}$ = 10 V; T_j = 25 °C; typical values.

P-channel enhancement mode vertical D-MOS transistor

BSP205

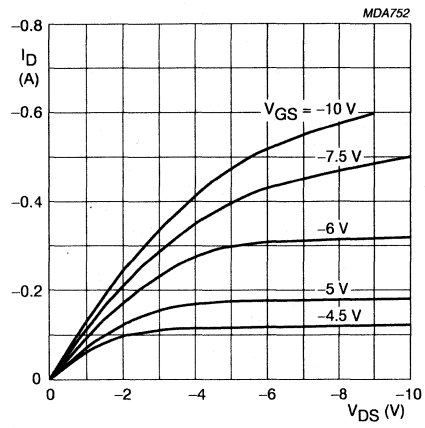


Fig.6 Output characteristics; T_j = 25 °C; typical values.

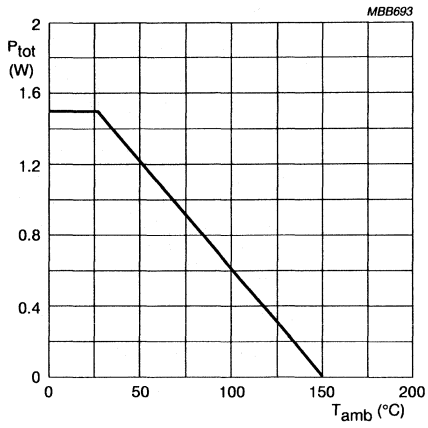


Fig.7 Power derating curve.

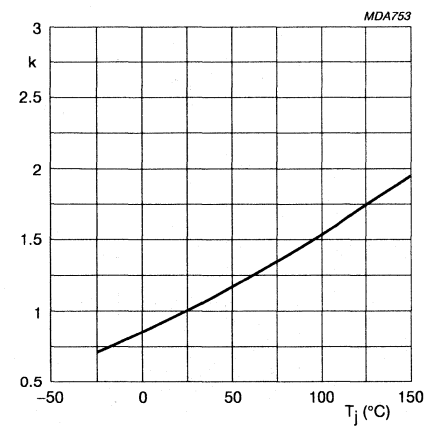


Fig.8

$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C};$$

at −200 mA/−10 V; typical values.

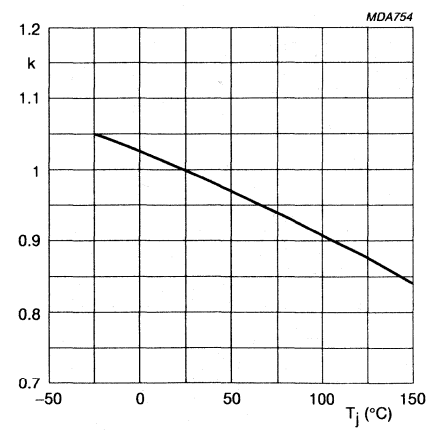


Fig.9

$$k = \frac{-V_{GS(th)} \text{ at } T_j}{-V_{GS(th)} \text{ at } 25\ °C};$$

$-V_{GS(th)}$ at −1 mA; typical values.

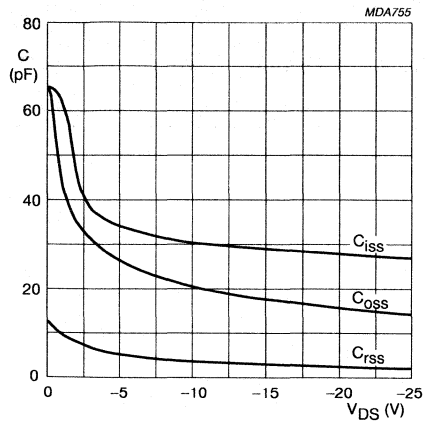


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

P-channel enhancement mode vertical D-MOS transistor

BSP206

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use in relay, high-speed and line-transformer drivers.

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60 V
Drain current (DC)	$-I_D$	max.	350 mA
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$R_{DS(on)}$	max.	6 Ω
Gate threshold voltage	$-V_{GS(th)}$	max.	3.5 V

FEATURES

- Very low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

PINNING - SOT223

1 = gate
2 = drain
3 = source
4 = drain

Marking code

BSP206

PIN CONFIGURATION

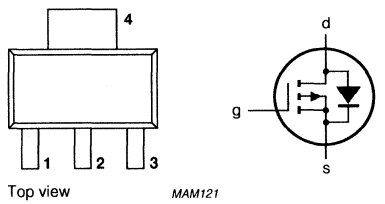


Fig.1 Simplfied outline and symbol.

P-channel enhancement mode vertical D-MOS transistor

BSP206

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	350 mA
Drain current (peak)	$-I_{DM}$	max.	700 mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5 W
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	83.3 K/W

Note

1. Device mounted on an epoxy printed-circuit board 40 mm × 40 mm × 1.5 mm; mounting pad for the drain lead min. 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage $-I_D$ = 10 μA; V_{GS} = 0	$-V_{(BR)DSS}$	min.	60 V
Drain-source leakage current $-V_{DS}$ = 48 V; V_{GS} = 0	$-I_{DSS}$	max.	1.0 μA
Gate-source leakage current $\pm V_{GS}$ = 20 V; V_{DS} = 0	$\pm I_{GSS}$	max.	100 nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$R_{DS(on)}$	typ. max.	4.5 Ω 6 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert Y_{fs} \rvert$	min. typ.	100 mS 200 mS
Input capacitance at f = 1 MHz; $-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ. max.	55 pF 70 pF
Output capacitance at f = 1 MHz; $-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ. max.	30 pF 45 pF
Feedback capacitance at f = 1 MHz; $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ. max.	8 pF 12 pF
Switching times (see Figs 2 and 3) $-I_D$ = 200 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on}	typ. max.	4 ns 8 ns
	t_{off}	typ. max.	15 ns 25 ns

P-channel enhancement mode vertical D-MOS transistor

BSP206

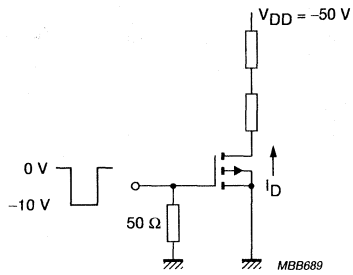


Fig.2 Switching time test circuit.

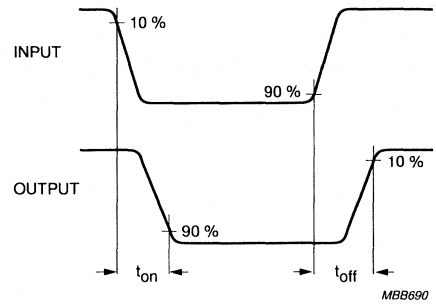


Fig.3 Input and output waveforms.

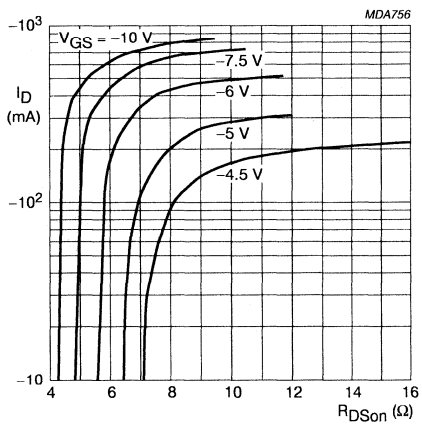


Fig.4 ON-resistance as a function of drain current; T_j = 25 °C; typical values.

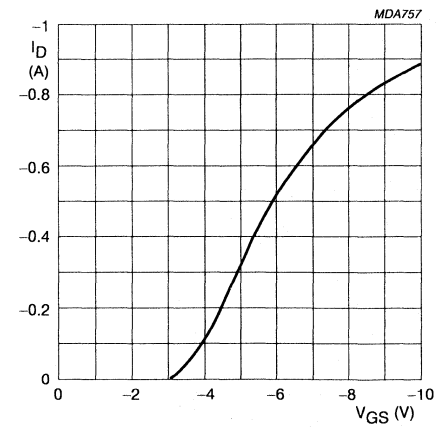


Fig.5 Transfer characteristics; $-V_{DS}$ = 10 V; T_j = 25 °C; typical values.

P-channel enhancement mode vertical D-MOS transistor

BSP206

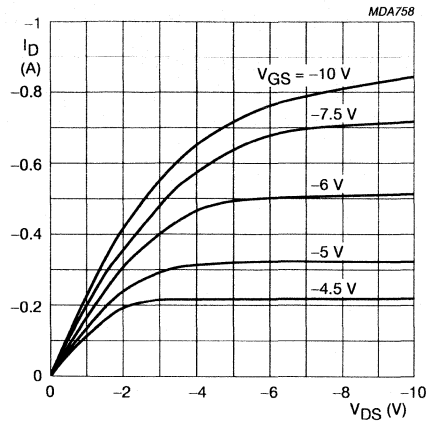


Fig.6 Output characteristics; T_j = 25° C; typical values.

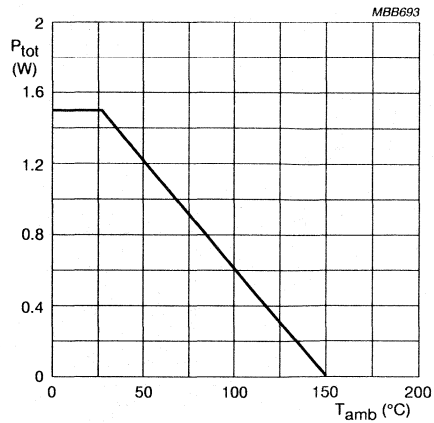


Fig.7 Power derating curve.

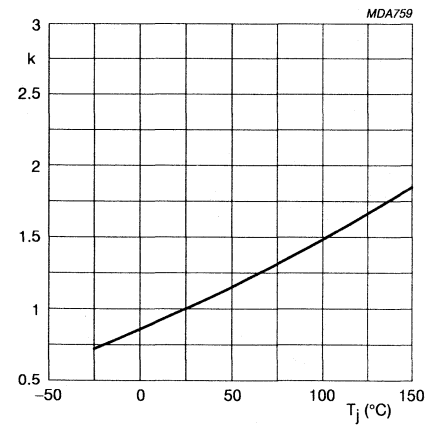


Fig.8

$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C};$$

at −200 mA/−10 V; typical values

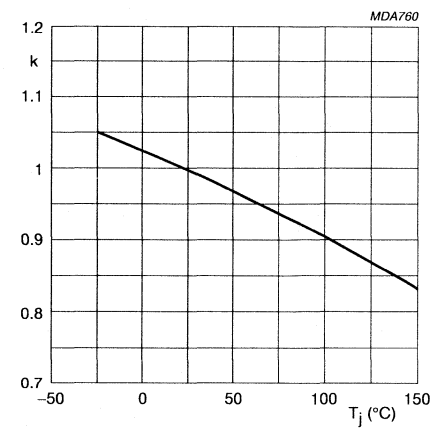


Fig.9

$$k = \frac{-V_{GS\,(th)} \text{ at } T_j}{-V_{GS\,(th)} \text{ at } 25\ °C};$$

$-V_{GS(th)}$ at −1 mA; typical values.

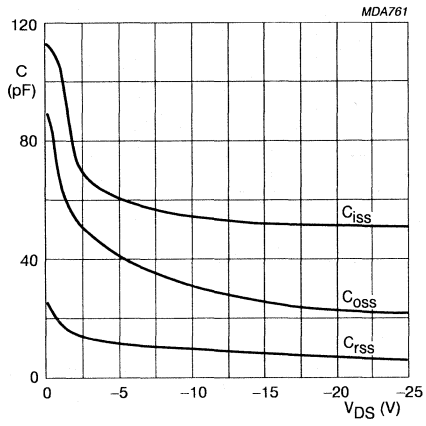


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

P-channel enhancement mode vertical D-MOS transistor

BSP220

FEATURES

- Low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use in relay, high-speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$-V_{DS}$	drain-source voltage		200	V
$-I_D$	drain current	DC value	225	mA
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 200 mA $-V_{GS}$ = 10 V	12	Ω
$-V_{GS(th)}$	gate-source threshold voltage		2.8	V

PIN CONFIGURATION

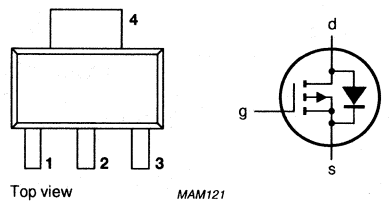


Fig.1 Simplified outline and symbol.

P-channel enhancement mode vertical D-MOS transistor

BSP220

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$-I_D$	drain current	DC value	–	225	mA
$-I_{DM}$	drain current	peak value	–	600	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

Note

1. Device mounted on an epoxy printed-circuit board 40 x 40 x 1.5 mm; mounting pad for the drain lead minimum 6 cm^2.

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3	K/W

Note

1. Device mounted on an epoxy printed-circuit board 40 x 40 x 1.5 mm; mounting pad for the drain lead minimum 6 cm^2.

P-channel enhancement mode vertical D-MOS transistor

BSP220

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-I_D$ = 10 μA V_{GS} = 0	200	–	–	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 160 V V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	–	–	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA V_{GS} = V_{DS}	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 200 mA $-V_{GS}$ = 10 V	–	10	12	Ω
$\|Y_{fs}\|$	transfer admittance	$-I_D$ = 200 mA $-V_{DS}$ = 25 V	100	200	–	mS
C_{iss}	input capacitance	$-V_{DS}$ = 25 V V_{GS} = 0 f = 1 MHz	–	65	90	pF
C_{oss}	output capacitance	$-V_{DS}$ = 25 V V_{GS} = 0 f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	$-V_{DS}$ = 25 V V_{GS} = 0 f = 1 MHz	–	6	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	5	20	ns
t_{off}	turn-off time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	20	30	ns

P-channel enhancement mode vertical D-MOS transistor

BSP220

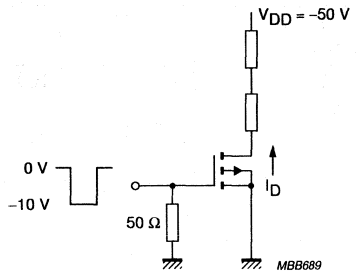


Fig.2 Switching time test circuit.

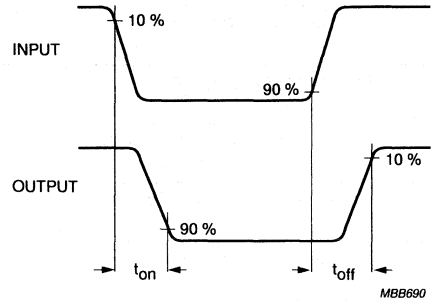


Fig.3 Input and output waveforms.

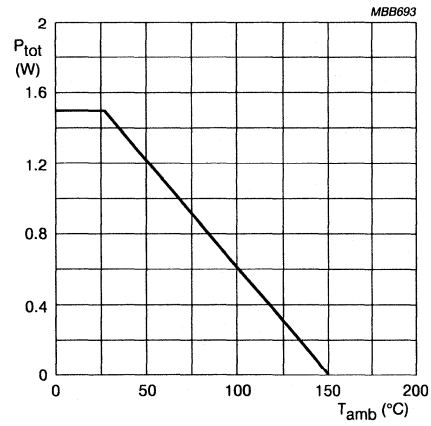


Fig.4 Power derating curve.

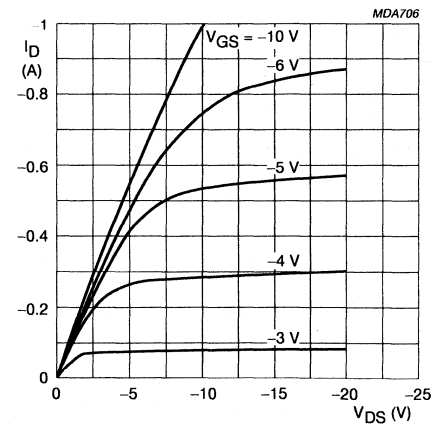


Fig.5 Typical output characteristics; T_j = 25 °C.

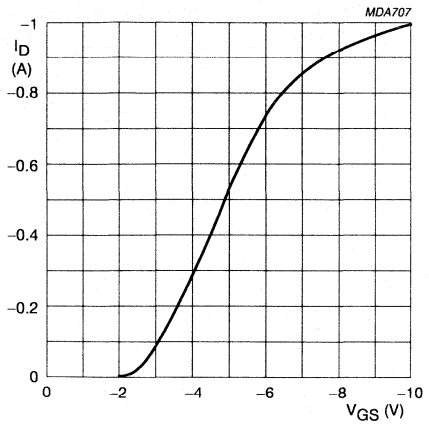


Fig.6 Typical transfer characteristic; $-V_{DS}$ = 10 V; T_j = 25 °C.

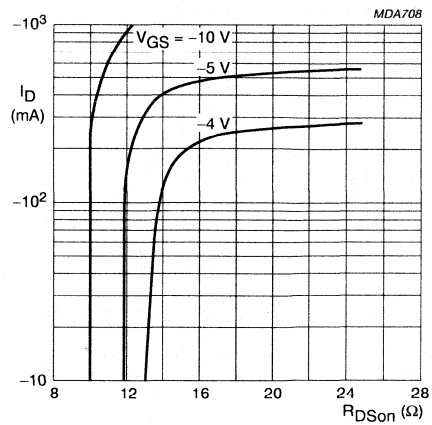


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

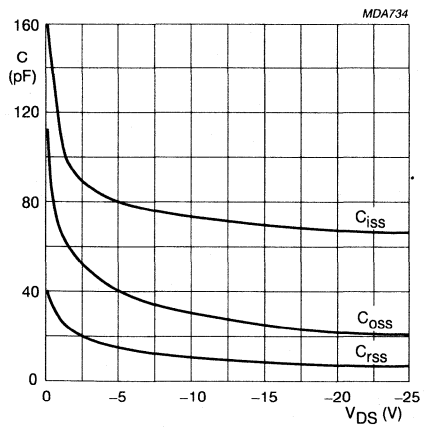


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

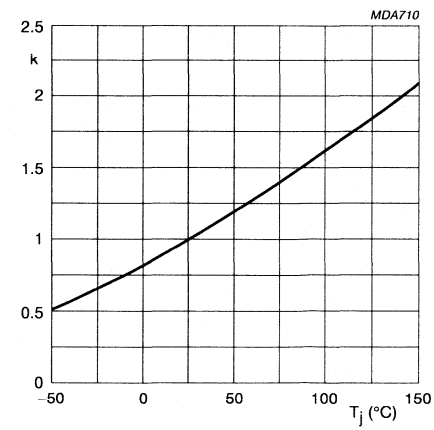


Fig.9 Temperature coefficient of drain-source on-resistance;

$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C};$$

typical $R_{DS(on)}$ at −200 mA/−10 V.

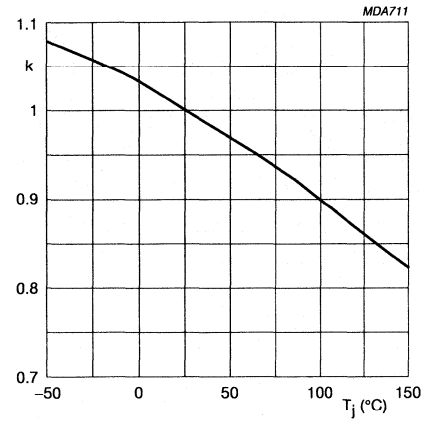


Fig.10 Temperature coefficient of gate-source threshold voltage;

$$k = \frac{V_{GS\,(th)} \text{ at } T_j}{V_{GS\,(th)} \text{ at } 25\ °C};$$

typical $-V_{GS(th)}$ at -1 mA.

P-channel enhancement mode vertical D-MOS transistor

BSP225

FEATURES

- Low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope, intended for use in relay, high-speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$-V_{DS}$	drain-source voltage		250	V
$-I_D$	drain current	DC value	225	mA
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 200 mA $-V_{GS}$ = 10 V	15	Ω
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA $V_{GS} = V_{DS}$	2.8	V

PIN CONFIGURATION

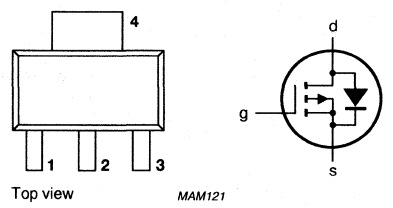


Fig.1 Simplified outline and symbol.

P-channel enhancement mode vertical D-MOS transistor

BSP225

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		–	250	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$-I_D$	drain current	DC value	–	225	mA
$-I_{DM}$	drain current	peak value	–	600	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

Note

1. Device mounted on an epoxy printed-circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain lead minimum 6 cm^2.

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3	K/W

Note

1. Device mounted on an epoxy printed-circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain lead minimum 6 cm^2.

P-channel enhancement mode vertical D-MOS transistor

BSP225

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-I_D$ = 10 μA V_{GS} = 0	250	–	–	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 200 V V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	V_{DS} = 0 $\pm V_{GS}$ = 20 V	–	–	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA $V_{GS} = V_{DS}$	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 200 mA $-V_{GS}$ = 10 V	–	10	15	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	$-I_D$ = 200 mA $-V_{DS}$ = 25 V	100	200	–	mS
C_{iss}	input capacitance	$-V_{DS}$ = 25 V $-V_{GS}$ = 0 f = 1 MHz	–	65	90	pF
C_{oss}	output capacitance	$-V_{DS}$ = 25 V $-V_{GS}$ = 0 f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	$-V_{DS}$ = 25 V $-V_{GS}$ = 0 f = 1 MHz	–	6	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	20	30	ns

P-channel enhancement mode vertical D-MOS transistor

BSP225

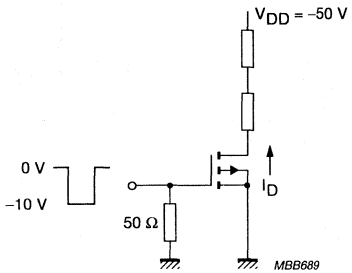


Fig.2 Switching time test circuit.

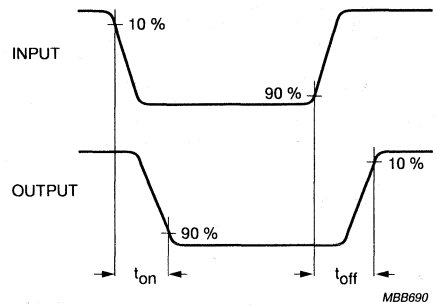


Fig.3 Input and output waveforms.

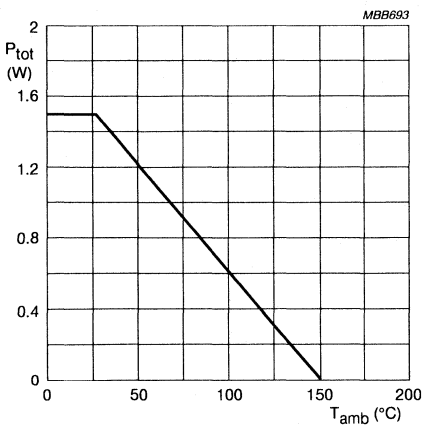


Fig.4 Power derating curve.

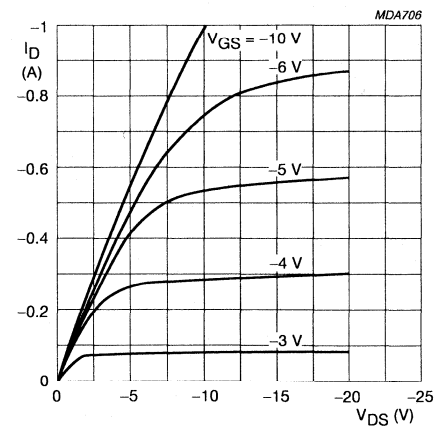


Fig.5 Typical output characteristics; T_j = 25 °C.

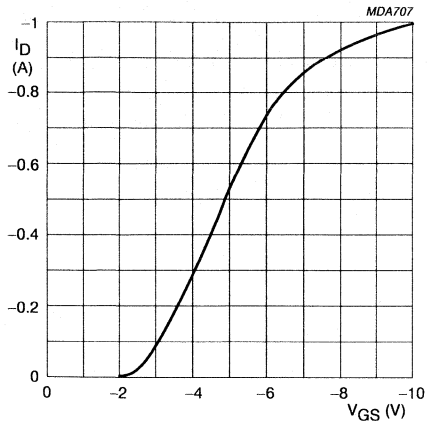


Fig.6 Typical transfer characteristic; $-V_{DS} = 10$ V; $T_j = 25$ °C.

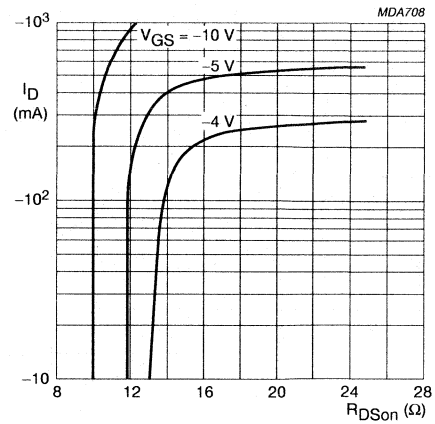


Fig.7 Typical on-resistance as a function of drain current; $T_j = 25$ °C; $R_{DS(on)} = f(I_D)$.

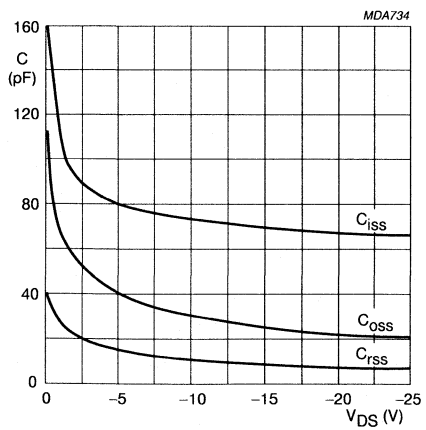


Fig.8 Typical capacitances as a function of drain-source voltage; $V_{GS} = 0$; $f = 1$ MHz; $T_j = 25$ °C.

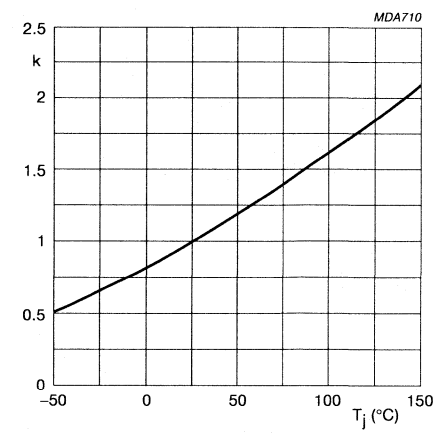


Fig.9 Temperature coefficient of drain-source on-resistance;

$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C};$$

typical $R_{DS(on)}$ at −200 mA/−10 V.

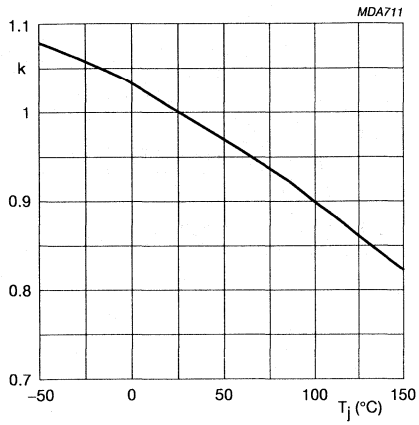


Fig.10 Temperature coefficient of gate-source threshold voltage;

$$k = \frac{-V_{GS(th)} \text{ at } T_j}{-V_{GS(th)} \text{ at } 25\ °C};$$

typical $V_{GS(th)}$ at −1 mA.

P-channel enhancement mode vertical D-MOS transistor

BSP230

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

APPLICATIONS

- Line current interruptor in telephone sets
- Relay, high speed and line transformer drivers.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a SOT223 plastic SMD package.

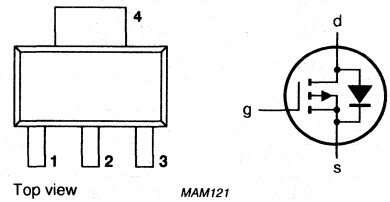


Fig.1 Simplified outline and symbol.

PINNING - SOT223

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	d	drain
3	s	source
4	d	drain

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	−300	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = −1 mA; V_{DS} = V_{GS}	−1.95	−2.8	V
I_D	drain current (DC)		–	−210	mA
R_{DSon}	drain-source on-state resistance	I_D = −170 mA; V_{GS} = −10 V	–	17	Ω
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	1.5	W

P-channel enhancement mode vertical D-MOS transistor

BSP230

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–300	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	–210	mA
I_{DM}	peak drain current		–	–0.75	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	1.5	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	83.3	K/W

Note to the Limiting values and Thermal characteristics

1. Device mounted on an epoxy printed-circuit board, 40 × 40 × 1.5 mm; mounting pad for drain lead minimum 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = –10 μA	–300	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = –1 mA	–1.95	–	–2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = –240 V	–	–	–100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = –10 V; I_D = –170 mA	–	–	17	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = –25 V; I_D = –170 mA	100	–	–	mS
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = –25 V; f = 1 MHz	–	60	90	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = –25 V; f = 1 MHz	–	15	30	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = –25 V; f = 1 MHz	–	5	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	V_{GS} = 0 to –10 V; V_{DD} = –50 V; I_D = –250 mA	–	5	10	ns
t_{off}	turn-off time	V_{GS} = –10 to 0 V; V_{DD} = –50 V; I_D = –250 mA	–	15	30	ns

P-channel enhancement mode vertical D-MOS transistor

BSP230

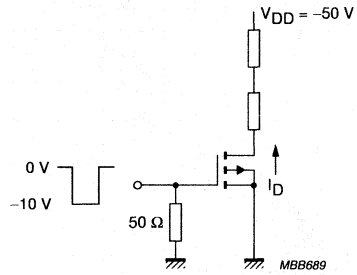


Fig.2 Switching time test circuit.

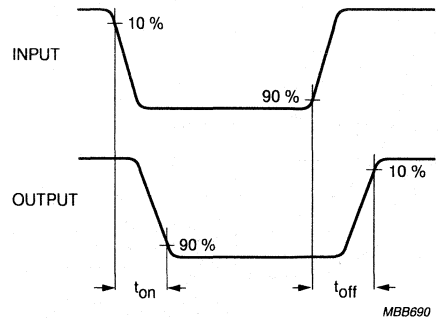


Fig.3 Input and output waveforms.

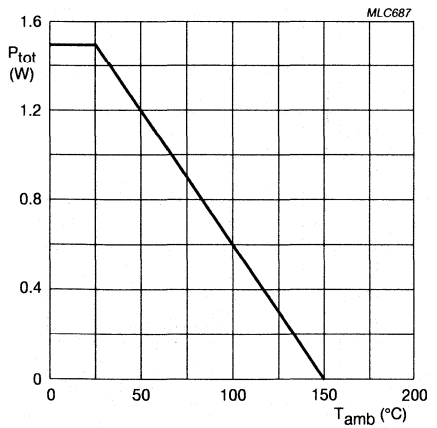
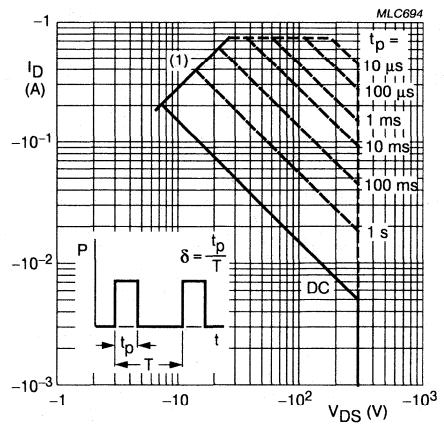


Fig.4 Power derating curve.

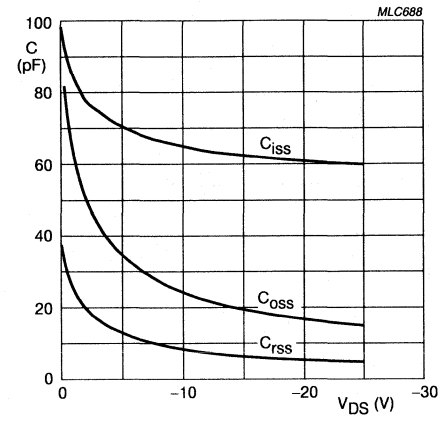


δ = 0.01.
T_{amb} = 25 °C.
(1) R_{DSon} limitation.

Fig.5 DC SOAR.

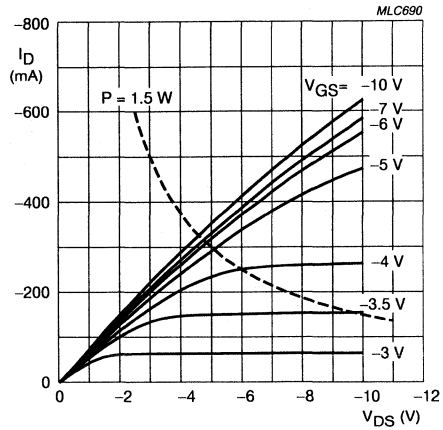
P-channel enhancement mode vertical D-MOS transistor

BSP230



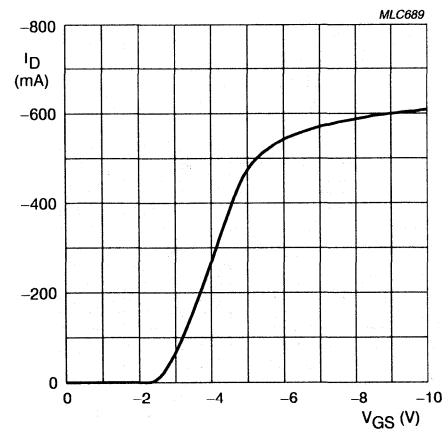
V_{GS} = 0.
T_j = 25 °C.
f = 1 MHz.

Fig.6 Capacitance as a function of drain source voltage; typical values.



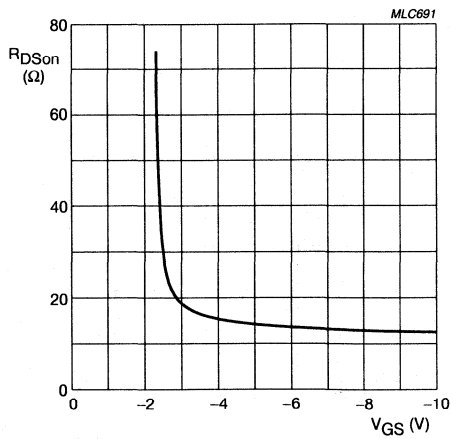
T_j = 25 °C.

Fig.7 Typical output characteristics.



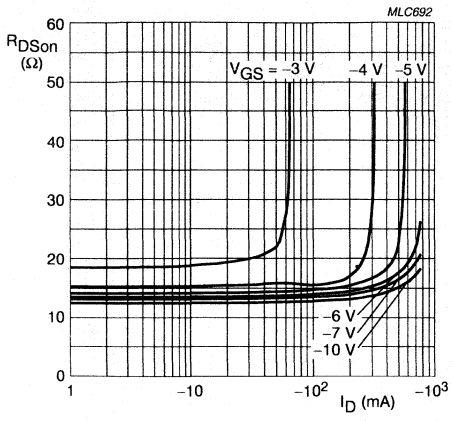
V_{DS} = −25 V.
T_j = 25 °C.

Fig.8 Typical transfer characteristics.



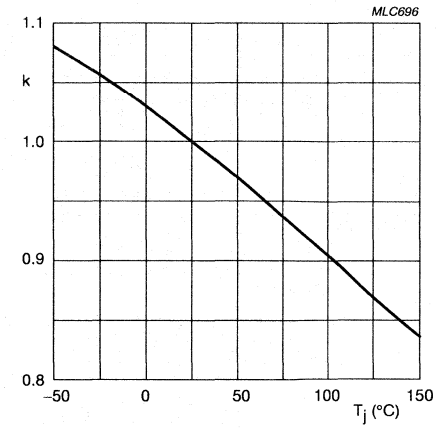
I_D = −170 mA.
T_j = 25 °C.

Fig.9 Drain-source on-state resistance as a function of gate-source voltage; typical values.



T_j = 25 °C.

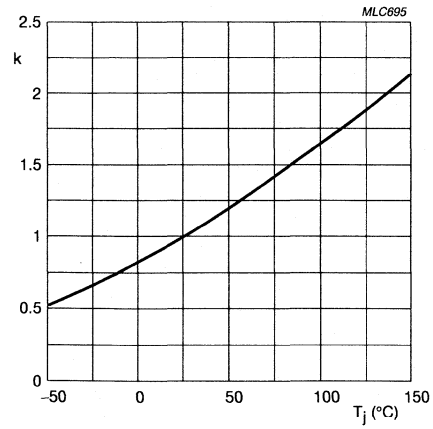
Fig.10 Drain-source on-state resistance as a function of drain current; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

Typical V_{GSth} at I_D = −1 mA; V_{DS} = V_{GS}.

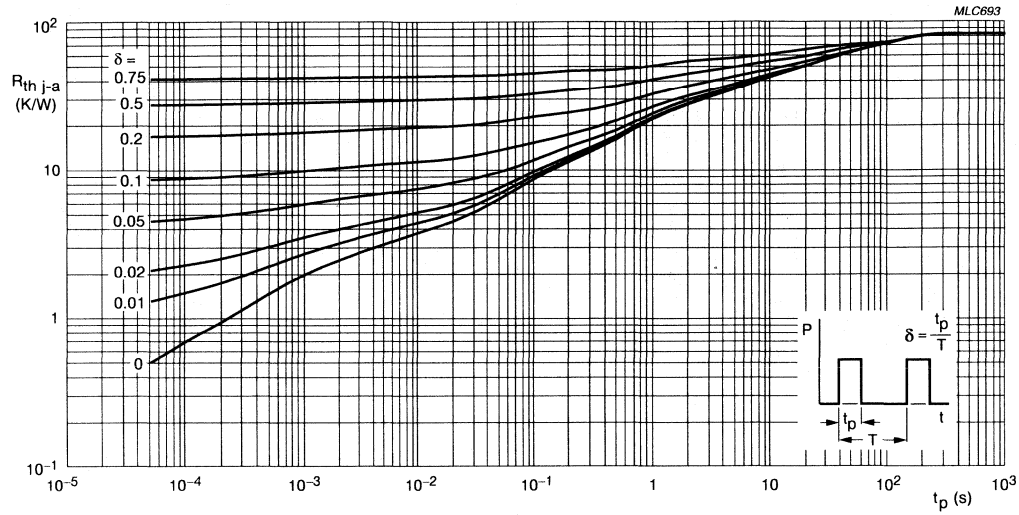
Fig.11 Temperature coefficient of gate-source threshold voltage.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

Typical R_{DSon} at I_D = −170 mA; V_{GS} = −10 V.

Fig.12 Temperature coefficient of drain-source on-state resistance.



T_{amb} = 25 °C.

Fig.13 Transient thermal resistance from junction to ambient as a function of pulse time; typical values.

P-channel enhancement mode vertical D-MOS transistor

BSP250

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Low-loss motor and actuator drivers
- Power switching.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a SOT223 plastic SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT223

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	d	drain
3	s	source
4	d	drain

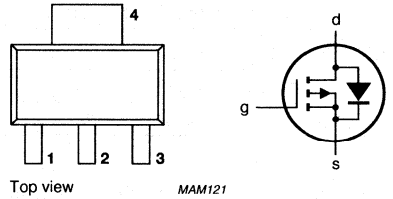


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{SD}	source-drain diode forward voltage	I_S = –1.25 A	–	–1.6	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = –1 mA; V_{DS} = V_{GS}	–1	–2.8	V
I_D	drain current (DC)		–	–3	A
R_{DSon}	drain-source on-state resistance	I_D = –1 A; V_{GS} = –10 V	–	0.25	Ω
P_{tot}	total power dissipation	T_s = 100 °C	–	5	W

P-channel enhancement mode vertical D-MOS transistor

BSP250

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)	$T_s \leq 100$ °C	–	–3	A
I_{DM}	peak drain current	note 1	–	–12	A
P_{tot}	total power dissipation	$T_s = 100$ °C	–	5	W
		$T_{amb} = 25$ °C; note 2	–	1.65	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C
Source-drain diode					
I_S	source current (DC)	$T_s \leq 100$ °C	–	–1.5	A
I_{SM}	peak pulsed source current	note 1	–	–6	A

Notes

1. Pulse width and duty cycle limited by maximum junction temperature.
2. Device mounted on an epoxy printed-circuit board, 40 × 40 × 1.5 mm; mounting pad for drain lead minimum 6 cm^2.

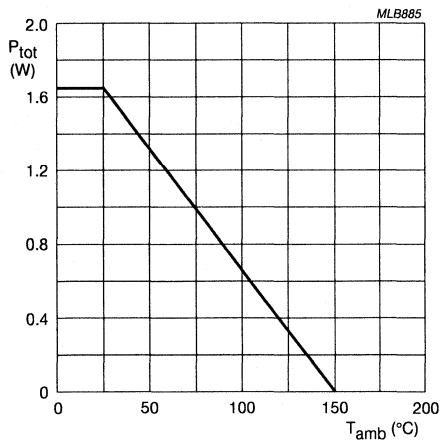
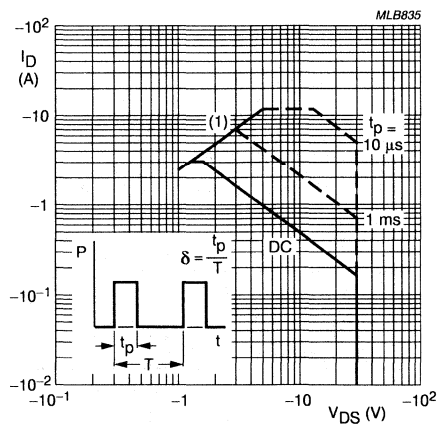


Fig.2 Power derating curve.



δ = 0.01.
Soldering point temperature $T_s = 100$ °C.
(1) R_{DSon} limitation.

Fig.3 SOAR.

P-channel enhancement mode vertical D-MOS transistor

BSP250

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	75	K/W
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point		10	K/W

Note

1. Device mounted on an epoxy printed-circuit board, 40 × 40 × 1.5 mm; mounting pad for drain lead minimum 6 cm^2.

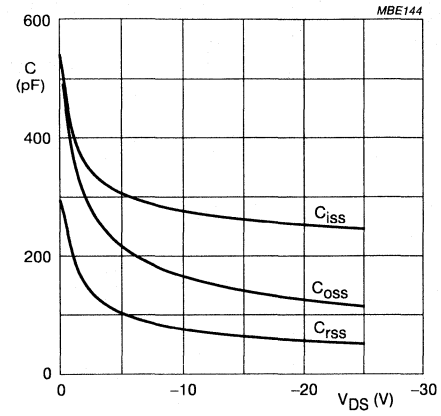
CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−1	–	−2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −24 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
I_{Don}	on-state drain current	V_{GS} = −10 V; V_{DS} = −1 V	−3	–	–	A
		V_{GS} = −4.5 V; V_{DS} = −5 V	−1	–	–	A
R_{DSon}	drain-source on-state resistance	V_{GS} = −4.5 V; I_D = −0.5 A	–	0.33	0.4	Ω
		V_{GS} = −10 V; I_D = −1 A	–	0.22	0.25	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = −20 V; I_D = −1 A	1	2	–	S
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −20 V; f = 1 MHz	–	250	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −20 V; f = 1 MHz	–	140	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −20 V; f = 1 MHz	–	50	–	pF
Q_G	total gate charge	V_{GS} = −10 V; V_{DS} = −15 V; I_D = −2.3 A	–	10	25	nC
Q_{GS}	gate-source charge	V_{GS} = −10 V; V_{DS} = −15 V; I_D = −2.3 A	–	1	–	nC
Q_{GD}	gate-drain charge	V_{GS} = −10 V; V_{DS} = −15 V; I_D = −2.3 A	–	3	–	nC
Switching times						
t_{on}	turn-on time	V_{GS} = 0 to −10 V; V_{DD} = −20 V; I_D = −1 A; R_L = 20 Ω	–	20	80	ns
t_{off}	turn-off time	V_{GS} = −10 to 0 V; V_{DD} = −20 V; I_D = −1 A; R_L = 20 Ω	–	50	140	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = −1.25 A	–	–	−1.6	V
t_{rr}	reverse recovery time	I_S = −1.25 A; di/dt = 100 A/μs	–	150	200	ns

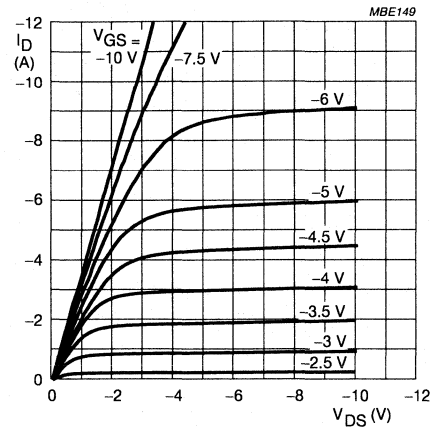
P-channel enhancement mode vertical D-MOS transistor

BSP250



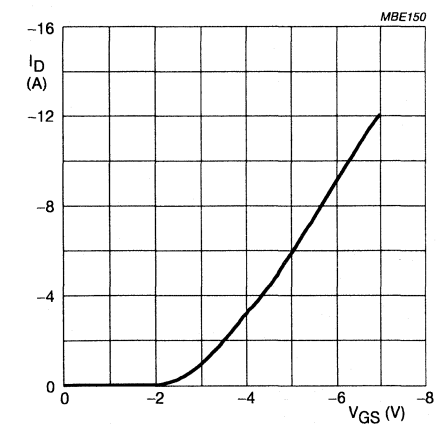
V_{GS} = 0.
T_j = 25 °C.

Fig.4 Capacitance as a function of drain source voltage; typical values.



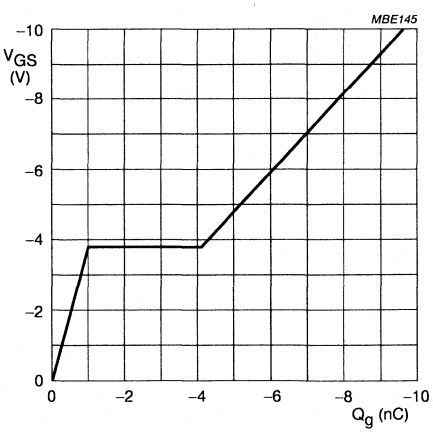
T_j = 25 °C.

Fig.5 Output characteristics; typical values.



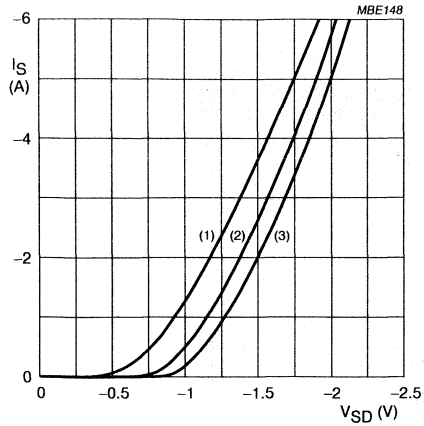
V_{DS} = −10 V.
T_j = 25 °C.

Fig.6 Transfer characteristic, typical values.



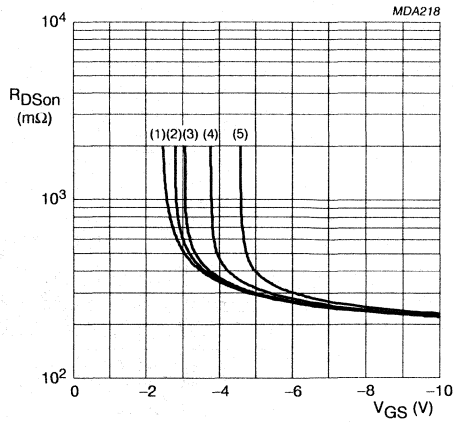
V_{DD} = −15 V.
I_D = −3 A.

Fig.7 Gate-source voltage as a function of total gate charge.



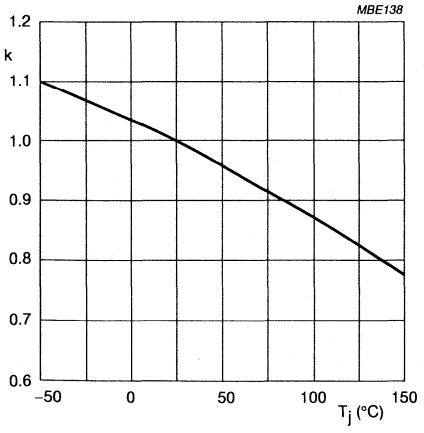
V_{GD} = 0.
(1) T_j = 150 °C.
(2) T_j = 25 °C.
(3) T_j = −55 °C.

Fig.8 Source current as a function of source-drain diode forward voltage.



$-V_{DS} \geq -I_D \times R_{DSon}$; T_j = 25 °C.
(1) I_D = −0.1 A.
(2) I_D = −0.5 A.
(3) I_D = −1 A.
(4) I_D = −3 A.
(5) I_D = −6 A.

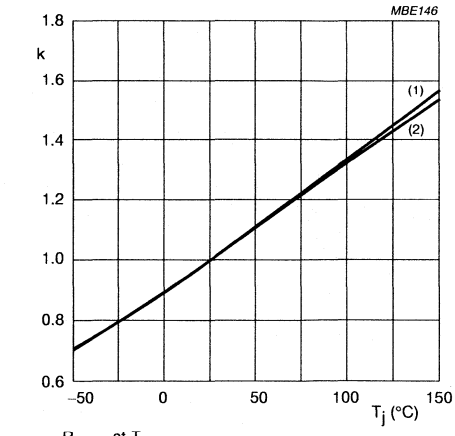
Fig.9 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

Typical V_{GSth} at I_D = −1 mA; V_{DS} = V_{GS} = V_{GSth}.

Fig.10 Temperature coefficient of gate-source threshold voltage.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

Typical R_{DSon} at:
(1) I_D = −1 A; V_{GS} = −10 V.
(2) I_D = −0.5 A; V_{GS} = −4.5 V.

Fig.11 Temperature coefficient of drain-source on-resistance.

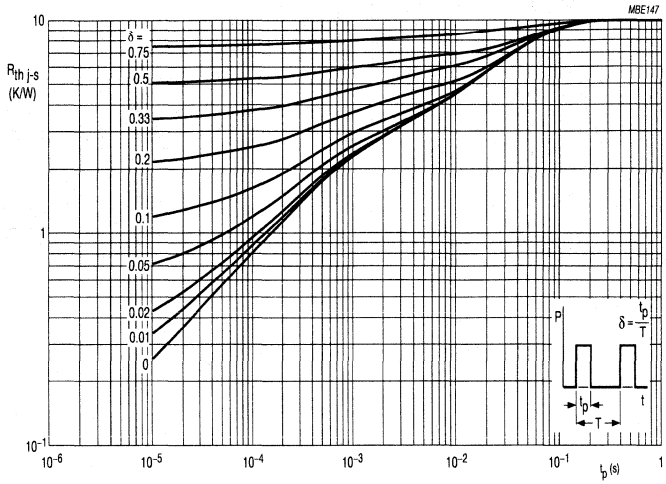


Fig.12 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

P-channel enhancement mode vertical D-MOS transistor

BSP254; BSP254A

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel vertical D-MOS transistor in a TO-92 variant envelope and intended for use as a line current interruptor in relay, high-speed and line transformer drivers.

PINNING - TO-92 variant BSP254

PIN	DESCRIPTION
1	gate
2	drain
3	source

PINNING - TO-92 variant BSP254A

PIN	DESCRIPTION
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	–250	V
V_{GSO}	gate-source voltage	open drain	–	–	±20	V
$\|Y_{fs}\|$	forward transfer admittance	I_D = –200 mA; V_{DS} = –25V	100	200	–	mS
I_D	drain current (DC)		–	–	–0.2	A
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = –10 V; I_D = –200 mA	–	10	15	Ω
P_{tot}	total power dissipation	T_{amb} = 25 °C	–	–	1	W

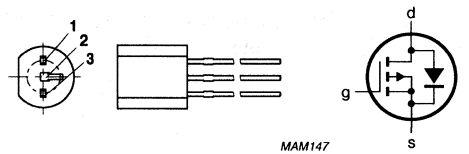


Fig.1 Simplified outline and symbol.

P-channel enhancement mode vertical D-MOS transistor

BSP254; BSP254A

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		–	250	V
V_{GSO}	gate-source voltage	open drain	–	20	V
$-I_D$	drain current	DC	–	0.2	A
$-I_{DM}$	drain current	peak value	–	0.6	A
P_{tot}	total power dissipation	T_{amb} = 25 °C (note 1)	–	1	W
T_{stg}	storage temperature range		–65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	125	K/W

Note

1. Transistor mounted on printed circuit board, maximum lead length 4 mm, mounting pad for drain lead minimum 10 mm x 10 mm.

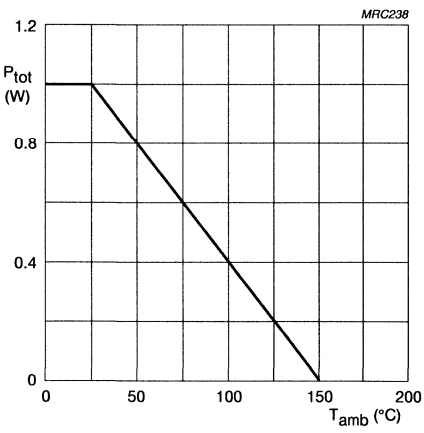


Fig.2 Power derating curve.

P-channel enhancement mode vertical D-MOS transistor

BSP254; BSP254A

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-V_{GS}$ = 0 $-I_D$ = 10 μA	250	–	–	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 200 V V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	–	–	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	V_{GS} = V_{DS} $-I_D$ = 1 mA	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-V_{GS}$ = 10 V $-I_D$ = 200 mA;	–	10	15	Ω
$\|Y_{fs}\|$	transfer admittance	$-V_{DS}$ = 25 V $-I_D$ = 200 mA	100	200	–	mS
C_{iss}	input capacitance	note 1	–	65	90	pF
C_{oss}	output capacitance	note 1	–	20	30	pF
C_{rss}	feedback capacitance	note 1	–	6	15	pF
t_{on}	turn-on time	note 2	–	5	10	ns
t_{off}	turn-off time	note 2	–	20	30	ns

Notes

1. Measured at f = 1 MHz; $-V_{DS}$ = 25 V; V_{GS} = 0.
2. $-V_{GS}$ = 0 to 10 V; $-I_D$ = 250 mA; $-V_{DD}$ = 50 V.

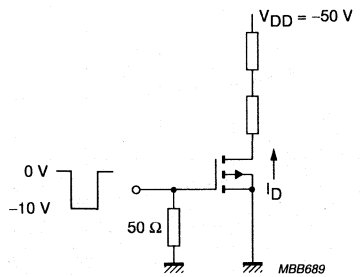


Fig.3 Switching times test circuit.

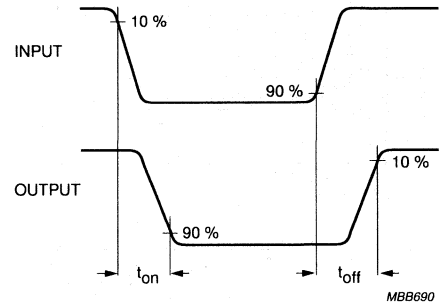


Fig.4 Input and output waveforms.

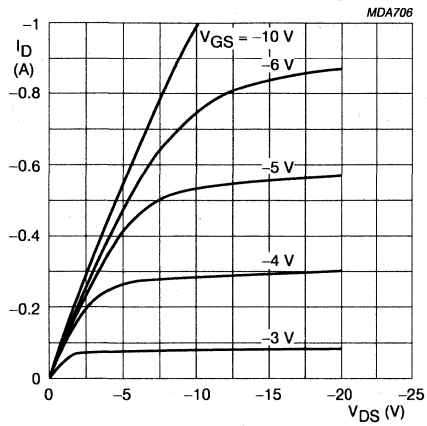


Fig.5 Typical output characteristics; T_j = 25 °C.

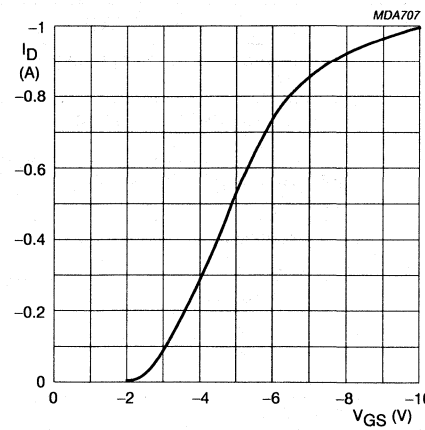


Fig.6 Typical transfer characteristic; V_{DS} = −10 V; T_j = 25 °C.

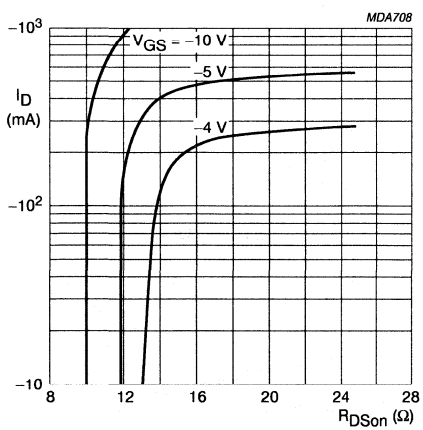


Fig.7 Typical on-resistance as a function of drain current, T_j = 25 °C.

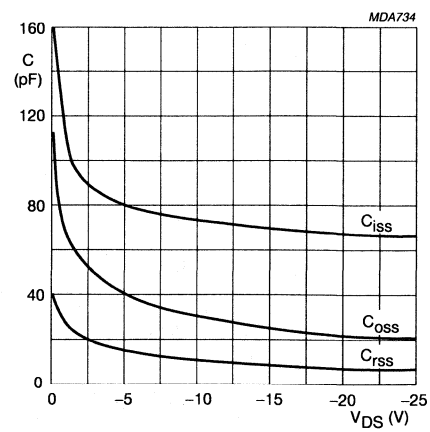


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

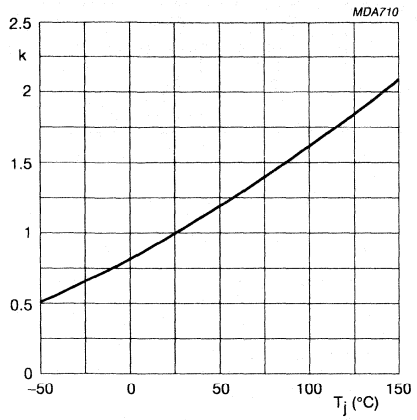


Fig.9

$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$$

typical $R_{DS(on)}$ at −200 mA/−10 V.

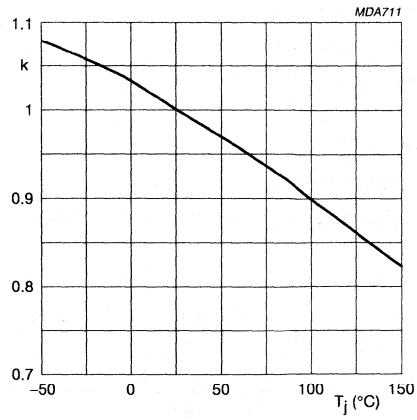


Fig.10

$$k = \frac{-V_{GS(th)} \text{ at } T_j}{-V_{GS(th)} \text{ at } 25\ °C}$$

typical $V_{GS(th)}$ at −1 mA.

P-channel enhancement mode vertical D-MOS transistor

BSP255

FEATURES

- Direct interface to C-MOS, TTL etc
- Low threshold voltage
- High speed switching
- No secondary breakdown.

APPLICATIONS

- Line current interrupter in telephone sets
- Relay, high speed and line transformer drivers.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a 4-pin plastic SOT223 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT223

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	d	drain
3	s	source
4	d	drain

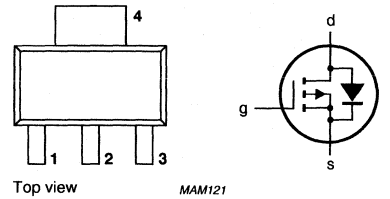


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	−300	V
V_{SD}	source-drain diode forward voltage	I_S = −0.5 A	–	−1.8	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = −1 mA; V_{DS} = V_{GS}	−0.8	−2	V
I_D	drain current (DC)	T_s = 100 °C	–	−325	mA
R_{DSon}	drain-source on-state resistance	I_D = −160 mA; V_{GS} = −10 V	–	17	Ω
P_{tot}	total power dissipation	T_s = 100 °C	–	4	W

P-channel enhancement mode vertical D-MOS transistor

BSP255

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–300	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 100 °C; note 1	–	–325	mA
I_{DM}	peak drain current	note 2	–	–1.3	A
P_{tot}	total power dissipation	T_s = 100 °C	–	4	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–65	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 100 °C	–	–0.5	A
I_{SM}	peak pulsed source current	note 2	–	–2	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.

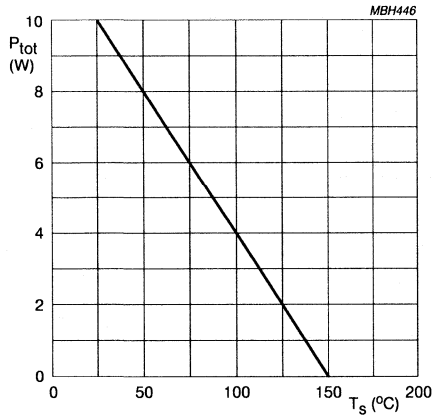
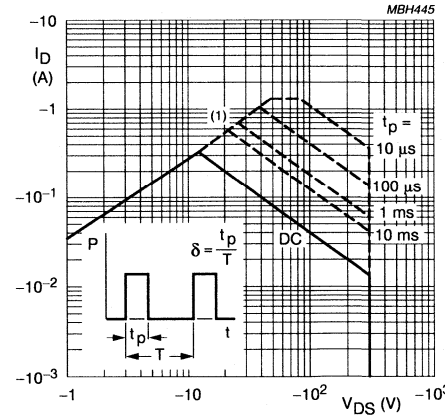


Fig.2 Power derating curve.



δ = 0.01; T_S = 100 °C.
(1) R_{DSon} limitation.

Fig.3 DC SOAR.

P-channel enhancement mode vertical D-MOS transistor

BSP255

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	12	K/W

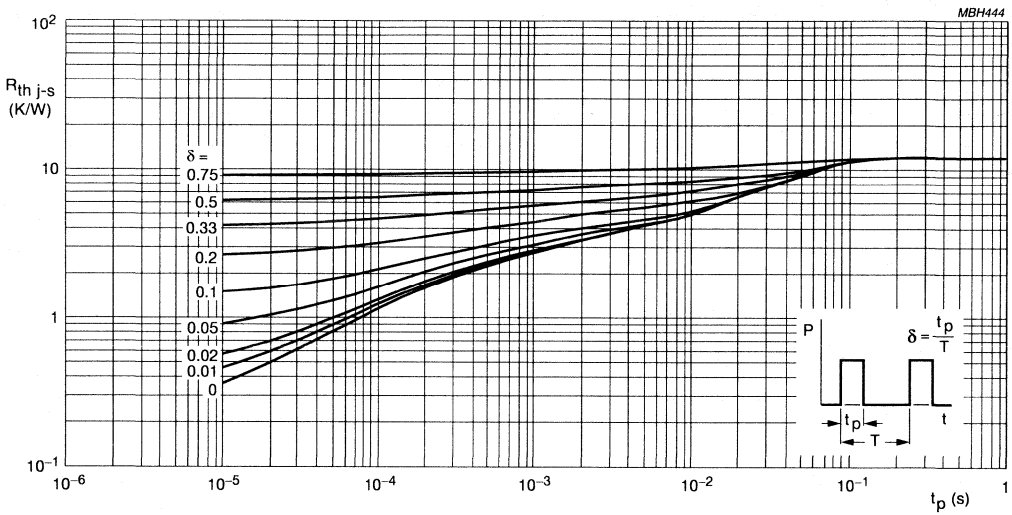


Fig.4 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

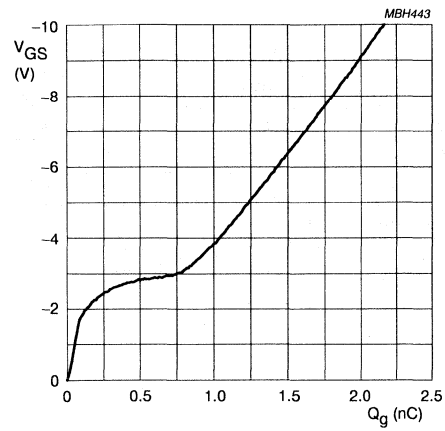
P-channel enhancement mode vertical D-MOS transistor

BSP255

CHARACTERISTICS

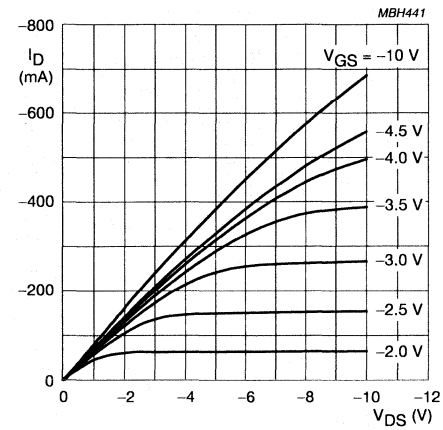
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−300	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−0.8	–	−2	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −240 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = −10 V; I_D = −160 mA	–	–	17	Ω
		V_{GS} = −4.5 V; I_D = −80 mA	–	–	20	Ω
		V_{GS} = −2.8 V; I_D = −50 mA	–	–	25	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −50 V; f = 1 MHz	–	45	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −50 V; f = 1 MHz	–	15	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −50 V; f = 1 MHz	–	3	–	pF
Q_g	total gate charge	V_{GS} = −10 V; V_{DD} = −50 V; I_D = −160 mA; T_{amb} = 25 °C	–	2.3	–	nC
Q_{gs}	gate-source charge	V_{GS} = −10 V; V_{DD} = −50 V; I_D = −160 mA; T_{amb} = 25 °C	–	0.1	–	nC
Q_{gd}	gate-drain charge	V_{GS} = −10 V; V_{DD} = −50 V; I_D = −160 mA; T_{amb} = 25 °C	–	0.7	–	nC
Switching times (see Fig.11)						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to −10 V; V_{DD} = −50 V; I_D = −160 mA; R_{gen} = 50 Ω	–	2.4	–	ns
t_r	rise time		–	1.6	–	ns
t_{on}	turn-on switching time		–	4	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = −10 to 0 V; V_{DD} = −50 V; I_D = −160 mA; R_{gen} = 50 Ω	–	13	–	ns
t_f	fall time		–	12	–	ns
t_{off}	turn-off switching time		–	25	–	ns
Source-drain diode						
V_{SD}	source-drain forward voltage	V_{GD} = 0; I_S = −0.5 A	–	–	−1.8	V



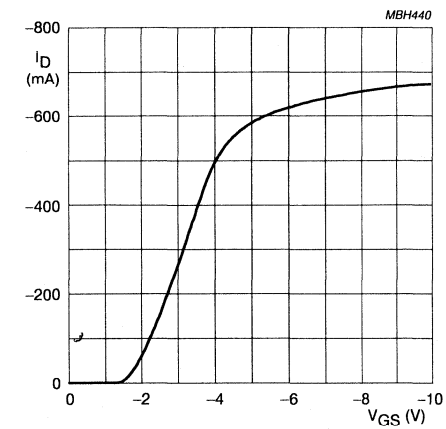
V_{DD} = −50 V; I_D = −180 mA.

Fig.5 Gate-source voltage as a function of total gate charge; typical values.



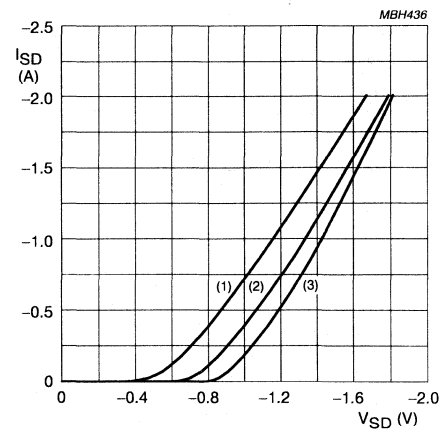
T_j = 25 °C.

Fig.6 Output characteristics; typical values.



V_{DS} = −10 V; T_j = 25 °C.

Fig.7 Transfer characteristics; typical values.

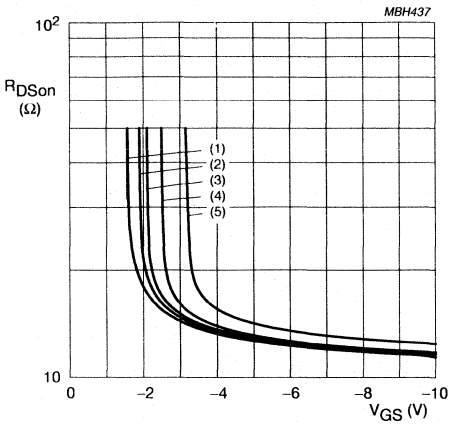


V_{GD} = 0.
(1) T_j = 150 °C.
(2) T_j = 25 °C.
(3) T_j = −65 °C.

Fig.8 Source-drain current as a function of source-drain diode forward voltage; typical values.

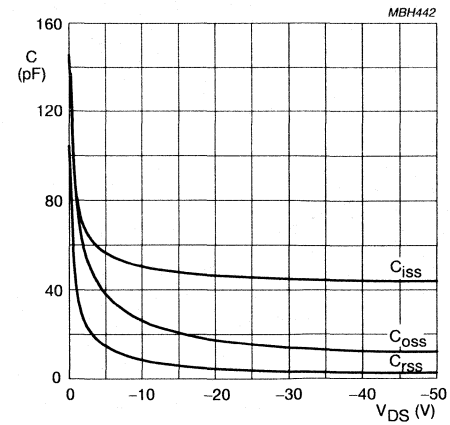
P-channel enhancement mode vertical D-MOS transistor

BSP255



$V_{DS} \geq I_D \times R_{DSon}$; T_j = 25 °C.
(1) I_D = −10 mA.
(2) I_D = −50 mA.
(3) I_D = −80 mA.
(4) I_D = −160 mA.
(5) I_D = −325 mA.

Fig.9 Drain source on-state resistance as a function of gate-source voltage; typical values.



V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

Fig.10 Capacitance as a function of drain-source voltage; typical values.

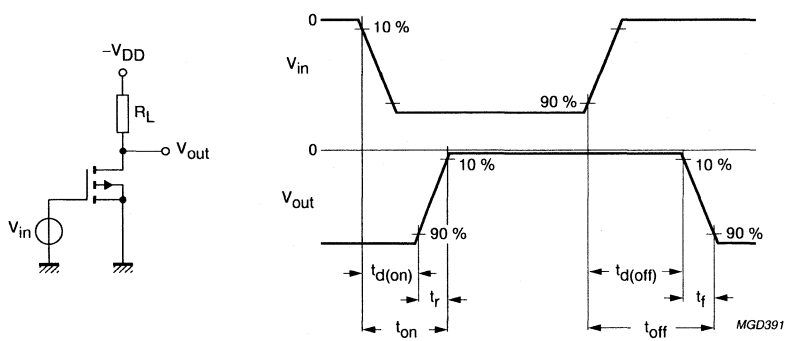
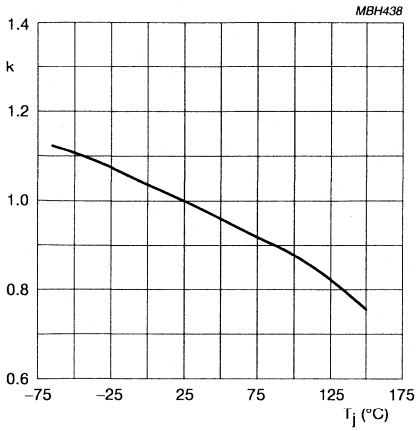


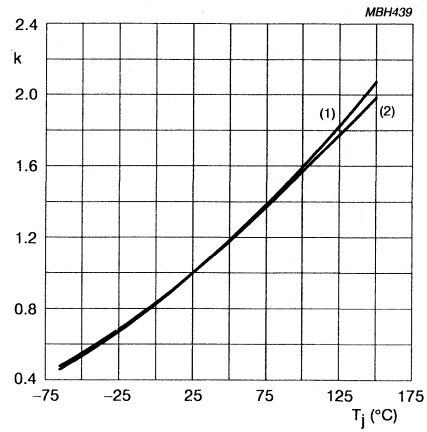
Fig.11 Switching time test circuit and input and output waveforms.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

V_{GSth} at $V_{DS} = V_{GS}$; $I_D = -1$ mA.

Fig.12 Temperature coefficient of gate-source threshold voltage as a function of junction temperature; typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

(1) $V_{GS} = -4.5$ V; $I_D = -80$ mA.
(2) $V_{GS} = -2.8$ V; $I_D = -50$ mA.

Fig.13 Temperature coefficient of drain-source on-state resistance as a function of junction temperature; typical values.

P-channel enhancement mode vertical D-MOS transistor

BSP304; BSP304A

FEATURES

- Direct interface to C-MOS, TTL etc.
- High speed switching
- No secondary breakdown.

APPLICATIONS

- Intended for use as a Line current interruptor in telephone sets and for applications in relay, high speed and line transformer drivers.

PINNING - TO-92 variant

PIN	SYMBOL	DESCRIPTION
BSP304		
1	g	gate
2	d	drain
3	s	source
BSP304A		
1	s	source
2	g	gate
3	d	drain

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a TO-92 variant package.

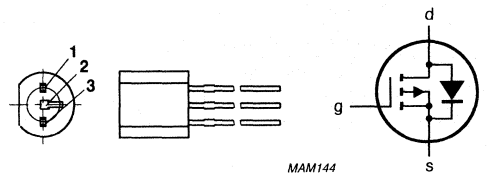


Fig.1 Simplified outline and symbol.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	300	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	$I_D = -1$ mA; $V_{DS} = V_{GS}$	−1.95	−2.8	V
I_D	drain current (DC)		–	−170	mA
R_{DSon}	drain-source on-state resistance	$I_D = -170$ mA; $V_{GS} = -10$ V	–	17	Ω
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	1	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	−300	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	−170	mA
I_{DM}	peak drain current		–	−0.75	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	1	W
T_{stg}	storage temperature		−65	+150	°C
T_j	operating junction temperature		–	150	°C

Note

1. Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for drain lead minimum 1 cm^2.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	125	K/W

Note

1. Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for drain lead minimum 1 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−300	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = −1 mA	−1.95	–	−2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −240 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = −10 V; I_D = −170 mA	–	–	17	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = −25 V; I_D = −170 mA	100	–	–	mS
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −25 V; f = 1 MHz	–	60	90	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −25 V; f = 1 MHz	–	15	30	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −20 V; f = 1 MHz	–	5	15	pF
SWITCHING TIMES (see Figs 2 and 3)						
t_{on}	turn-on time	V_{GS} = 0 to −10 V; V_{DD} = −50 V; I_D = −250 mA	–	5	10	ns
t_{off}	turn-off time	V_{GS} = −10 to 0 V; V_{DD} = −50 V; I_D = −250 mA	–	15	30	ns

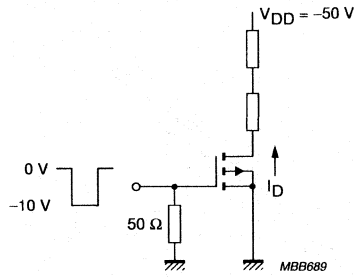


Fig.2 Switching time test circuit.

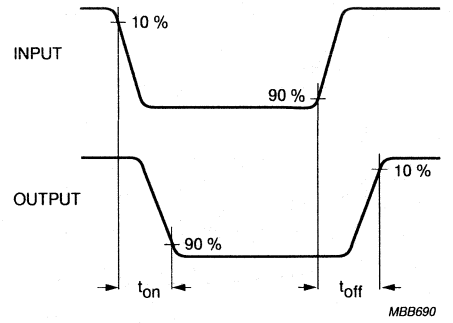


Fig.3 Input and output waveforms.

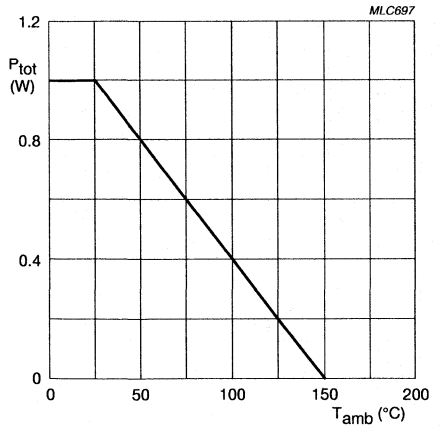
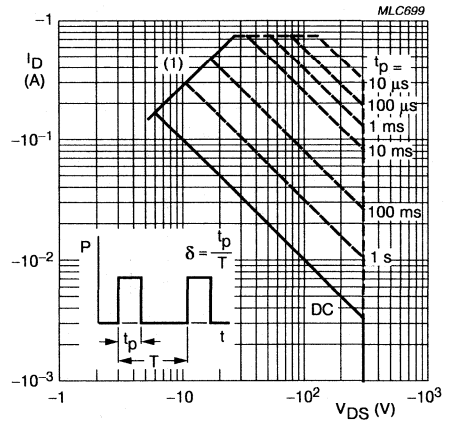
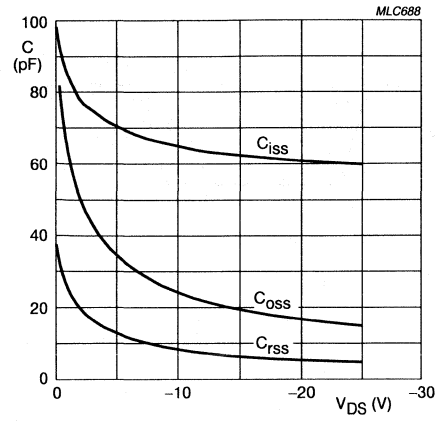


Fig.4 Power derating curve.



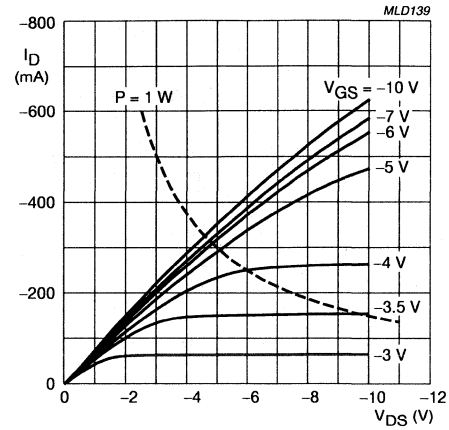
δ = 0.01.
T_{amb} = 25 °C.
(1) R_{DSon} limitation.

Fig.5 DC SOAR.



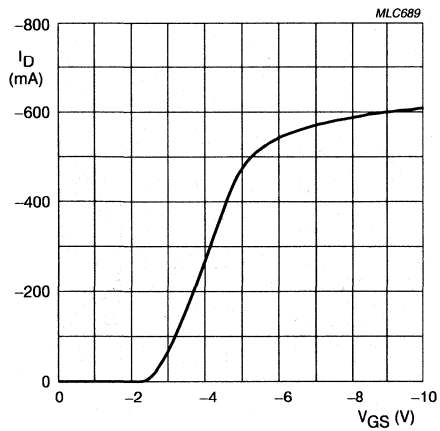
V_{GS} = 0.
T_j = 25 °C.
f = 1 MHz.

Fig.6 Capacitance as a function of drain source voltage; typical values.



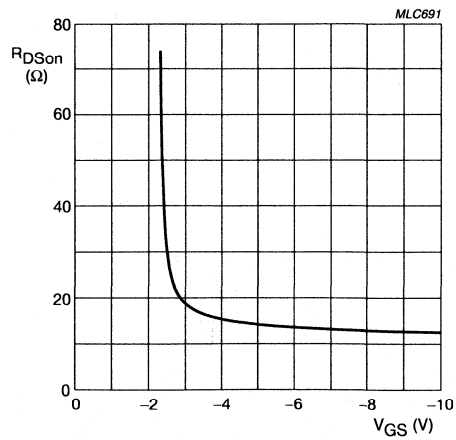
T_j = 25 °C.

Fig.7 Typical output characteristics.



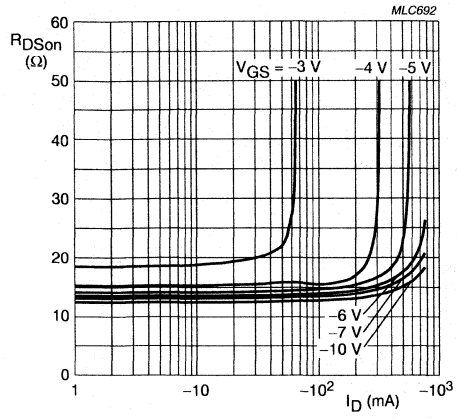
V_{DS} = −25 V.
T_j = 25 °C.

Fig.8 Typical transfer characteristics.



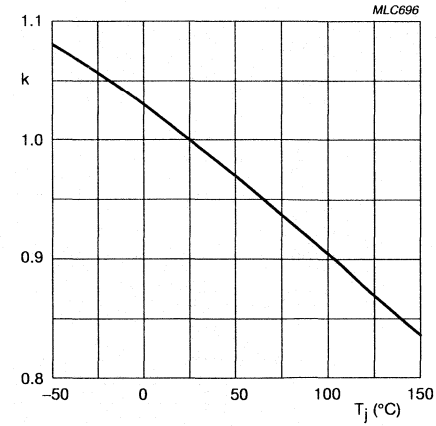
I_D = −170 mA.
T_j = 25 °C.

Fig.9 Drain-source on-state resistance as a function of gate-source voltage; typical values.



T_j = 25 °C.

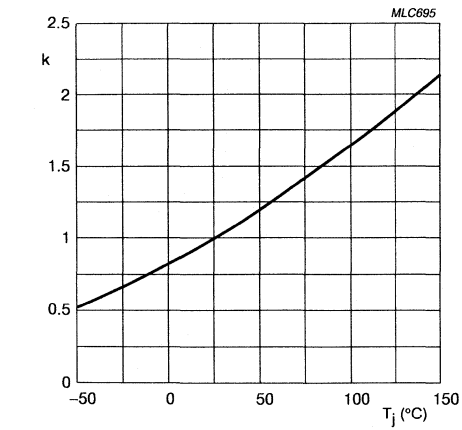
Fig.10 Drain-source on-state resistance as a function of drain current; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

Typical V_{GSth} at I_D = −1 mA; V_{DS} = V_{GS}.

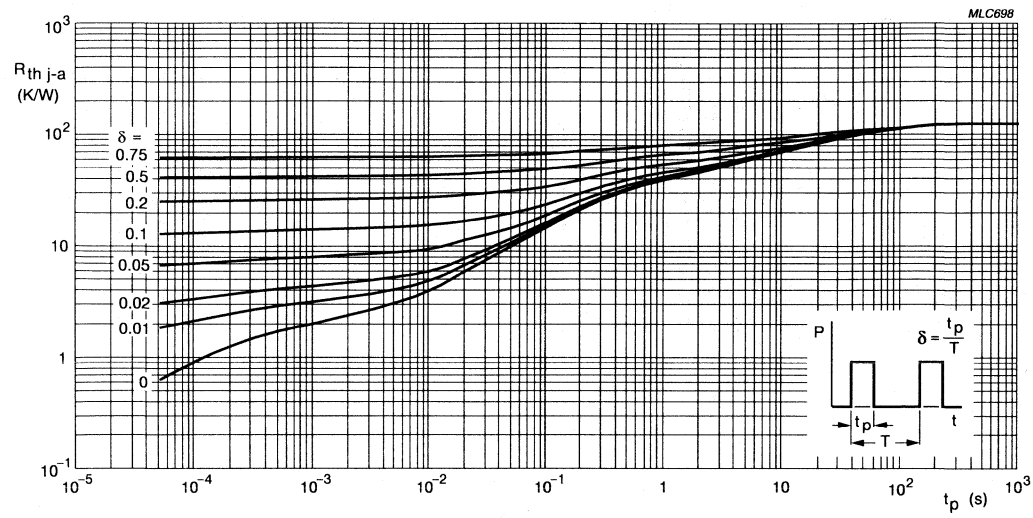
Fig.11 Temperature coefficient of gate-source threshold voltage.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

Typical R_{DSon} at I_D = −170 mA; V_{GS} = −10 V.

Fig.12 Temperature coefficient of drain-source on-state resistance.



T_{amb} = 25 °C.

Fig.13 Transient thermal resistance from junction to ambient as a function of pulse time; typical values.

N-channel enhancement mode vertical D-MOS transistor

BSP89

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope, intended for use as a surface-mounted device in line current interrupters in telephone sets and for application in relay, high speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
Code: BSP89	
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	240	V
I_D	DC drain current	350	mA
$R_{DS(on)}$	drain-source on-resistance	6	Ω
$V_{GS(th)}$	gate-source threshold voltage	2	V

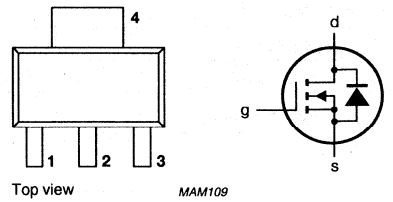


Fig.1 Simplified outline (SOT223) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	240	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	350	mA
I_{DM}	peak drain current		–	1.4	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		−65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3 K/W

Note

1. Transistor mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm^2.

N-channel enhancement mode vertical D-MOS transistor

BSP89

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	240	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 60 V; V_{GS} = 0	–	–	200	nA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	0.8	–	2	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 340 mA; V_{GS} = 10 V	–	4	6	Ω
		I_D = 340 mA; V_{GS} = 4.5 V	–	–	10	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 340 mA; V_{DS} = 25 V	140	350	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	65	140	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	5	9	pF
Switching times (see Figs 3 and 4)						
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	20	30	ns

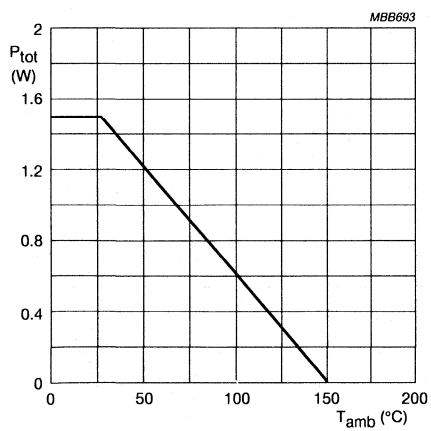


Fig.2 Power derating curve.

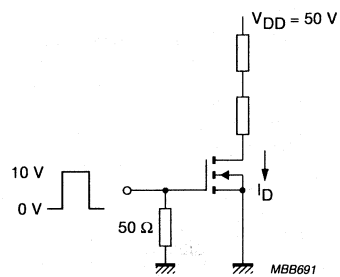


Fig.3 Switching times test circuit.

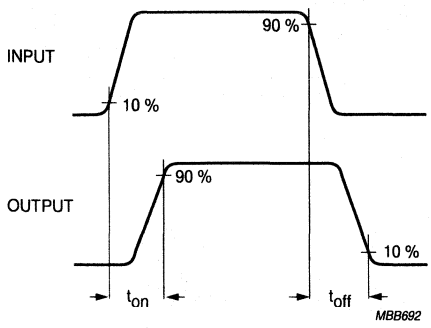


Fig.4 Input and output waveforms.

P-channel enhancement mode vertical D-MOS transistor

BSP92

FEATURES

- Low threshold voltage $V_{GS(th)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
$-V_{DS}$	drain-source voltage	240	V
$-I_D$	DC drain current	180	mA
$R_{DS(on)}$	drain-source on-resistance	20	Ω
$-V_{GS(th)}$	gate-source threshold voltage	1.8	V

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope, intended for use as a surface-mounted device in line current interruptor in telephone sets and for application in relay, high speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

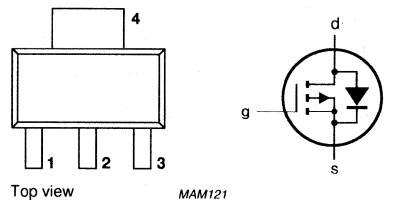


Fig.1 Simplified outline (SOT223) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		–	240	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$-I_D$	DC drain current		–	180	mA
$-I_{DM}$	peak drain current		–	720	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3 K/W

Note

1. Transistor mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm^2.

P-channel enhancement mode vertical D-MOS transistor

BSP92

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-I_D$ = 10 μA; V_{GS} = 0	240	–	–	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 200 V; V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA; V_{GS} = V_{DS}	0.8	–	2	V
$-V_{GS}$	gate-source voltage	$-I_D$ = 50 mA; $-V_{DS}$ = 5 V	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 180 mA; $-V_{GS}$ = 10 V	–	10	20	Ω
		$-I_D$ = 100 mA; $-V_{GS}$ = 5 V	–	–	18	Ω
		$-I_D$ = 25 mA; $-V_{GS}$ = 2.8 V	–	–	20	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	$-I_D$ = 180 mA; $-V_{DS}$ = 25 V	100	200	–	mS
C_{iss}	input capacitance	$-V_{DS}$ = 25 V; V_{GS} = 0; f = 1 MHz	–	65	90	pF
C_{oss}	output capacitance	$-V_{DS}$ = 25 V; V_{GS} = 0; f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	$-V_{DS}$ = 25 V; V_{GS} = 0; f = 1 MHz	–	6	15	pF
Switching times (see Figs 3 and 4)						
t_{on}	turn-on time	$-I_D$ = 250 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	$-I_D$ = 250 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	–	20	30	ns

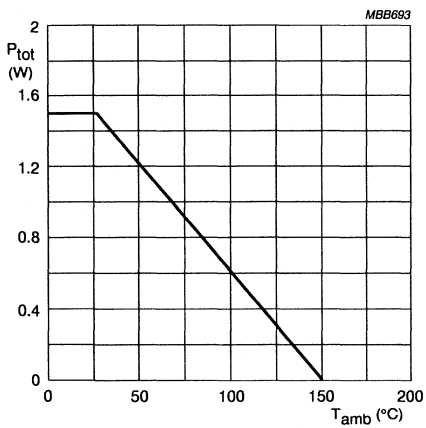


Fig.2 Power derating curve.

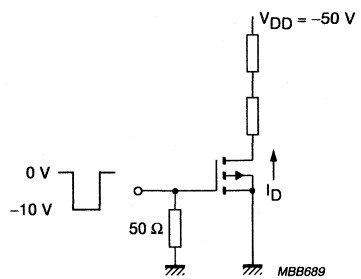


Fig.3 Switching times test circuit.

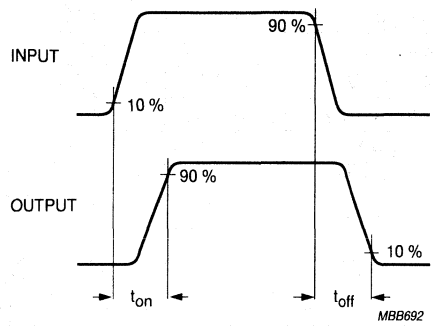


Fig.4 Input and output waveforms.

P-channel enhancement mode vertical D-MOS transistor

BSS84

FEATURES

- Low threshold voltage
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

APPLICATIONS

- Line current interrupter in telephone sets
- Relay, high speed and line transformer drivers.

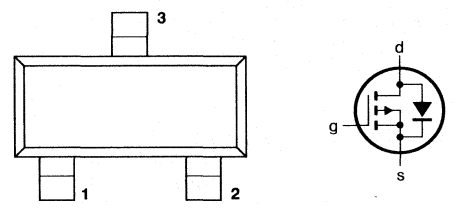
DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a SOT23 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain



Marking code: SP

Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	−50	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	$I_D = -1$ mA; $V_{DS} = V_{GS}$	−0.8	−2	V
I_D	drain current (DC)		–	−130	mA
R_{DSon}	drain-source on-state resistance	$I_D = -130$ mA; $V_{GS} = -10$ V	–	10	Ω
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	250	mW

P-channel enhancement mode vertical D-MOS transistor

BSS84

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–50	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	–130	mA
I_{DM}	peak drain current		–	–520	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	250	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	500	K/W

Note to the Limiting values and Thermal characteristics

1. Device mounted on a printed-circuit board.

CHARACTERISTICS

$T_j = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = -10$ µA	–50	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = V_{GS}$; $I_D = -1$ mA	–0.8	–	–2	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0$; $V_{DS} = -40$ V	–	–	–100	nA
		$V_{GS} = 0$; $V_{DS} = -50$ V	–	–	–10	µA
		$V_{GS} = 0$; $V_{DS} = -50$ V; $T_j = 125$ °C	–	–	–60	µA
I_{GSS}	gate leakage current	$V_{DS} = 0$; $V_{GS} = \pm 20$ V	–	–	±10	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = -10$ V; $I_D = -130$ mA	–	–	10	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	$V_{DS} = -25$ V; $I_D = -130$ mA	50	–	–	mS
C_{iss}	input capacitance	$V_{GS} = 0$; $V_{DS} = -25$ V; f = 1 MHz	–	25	45	pF
C_{oss}	output capacitance	$V_{GS} = 0$; $V_{DS} = -25$ V; f = 1 MHz	–	15	25	pF
C_{rss}	reverse transfer capacitance	$V_{GS} = 0$; $V_{DS} = -25$ V; f = 1 MHz	–	3.5	12	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$V_{GS} = 0$ to –10 V; $V_{DD} = -40$ V; $I_D = -200$ mA	–	3	–	ns
t_{off}	turn-off time	$V_{GS} = -10$ to 0 V; $V_{DD} = -40$ V; $I_D = -200$ mA	–	7	–	ns

P-channel enhancement mode vertical D-MOS transistor

BSS84

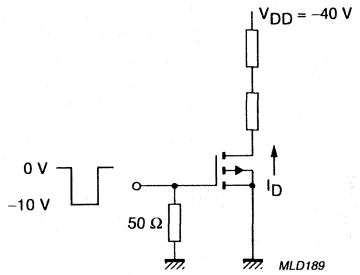


Fig.2 Switching time test circuit.

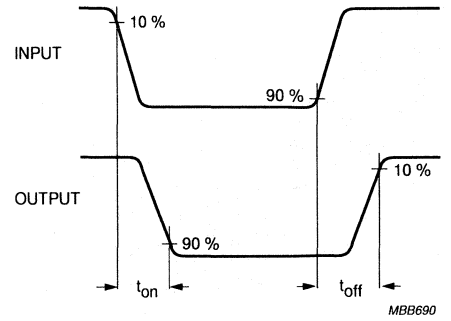


Fig.3 Input and output waveforms.

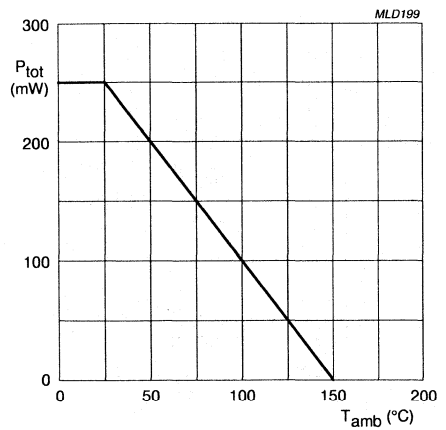
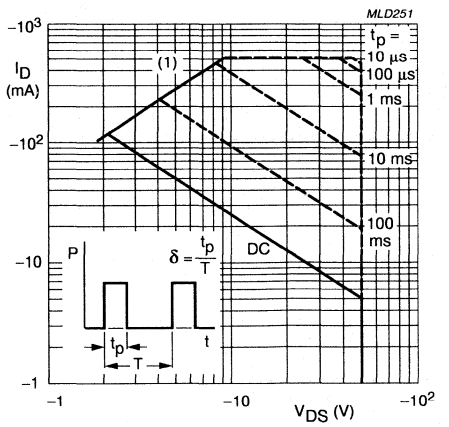


Fig.4 Power derating curve.

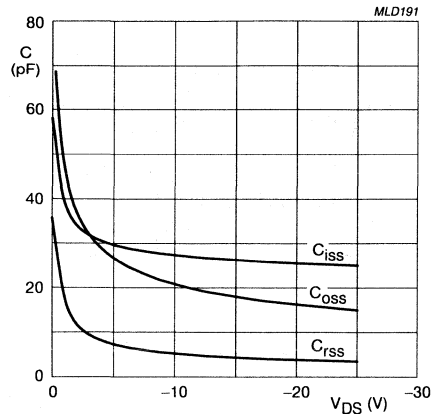


δ = 0.01.
T_{amb} = 25 °C.
(1) R_{DSon} limitation.

Fig.5 DC SOAR.

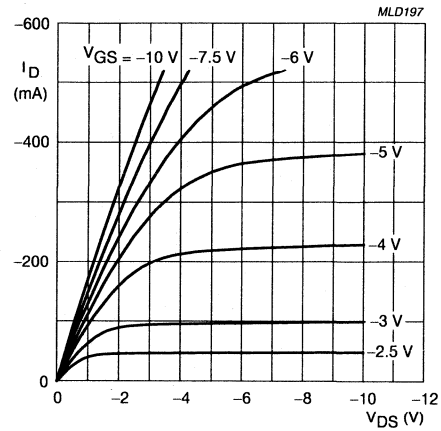
P-channel enhancement mode vertical D-MOS transistor

BSS84



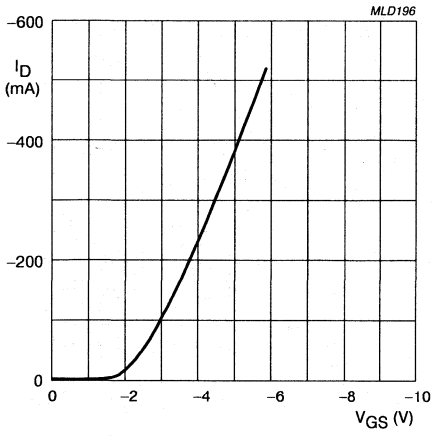
V_{GS} = 0; T_j = 25 °C; f = 1 MHz.

Fig.6 Capacitance as a function of drain source voltage; typical values.



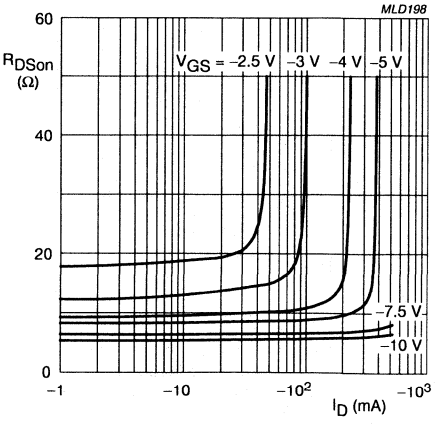
T_j = 25 °C.

Fig.7 Typical output characteristics.



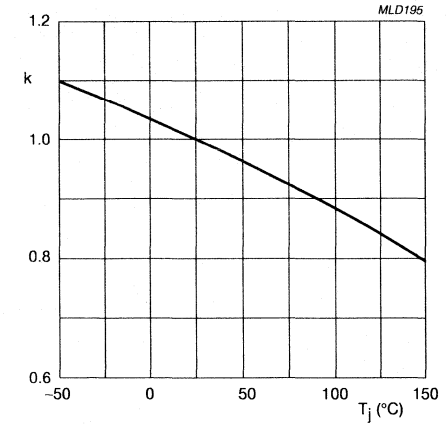
V_{DS} = −10 V; T_j = 25 °C.

Fig.8 Typical transfer characteristics.



T_j = 25 °C.

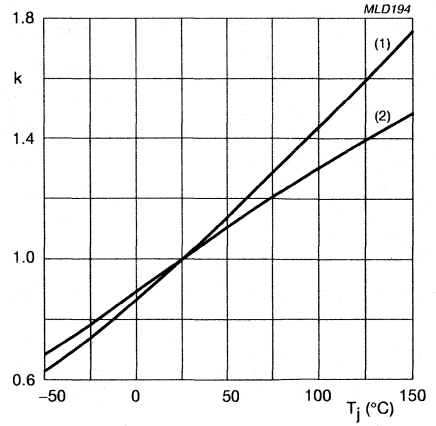
Fig.9 Drain-source on-state resistance as a function of drain current; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

$I_D = -1$ mA; $V_{DS} = V_{GS}$.

Fig.10 Temperature coefficient of gate-source threshold voltage.

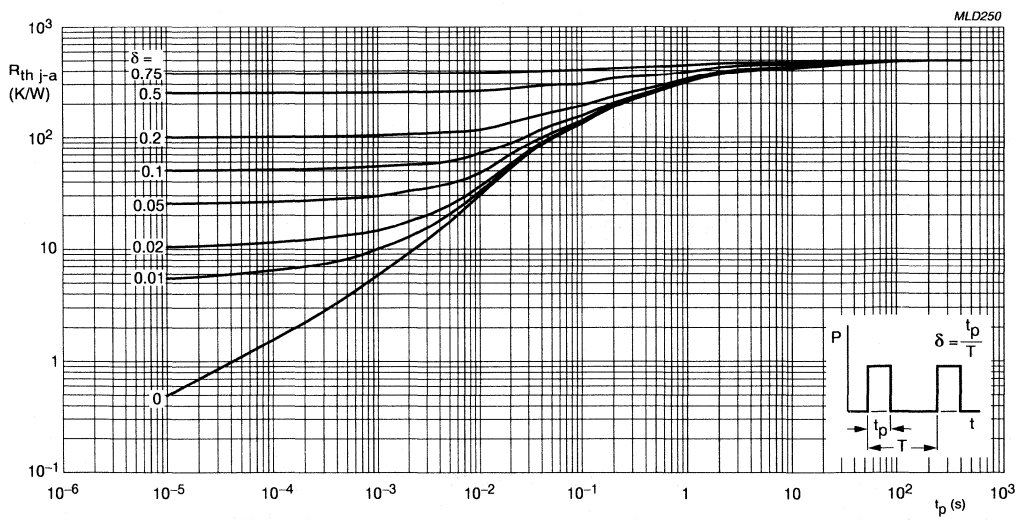


$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

(1) $I_D = -130$ mA; $V_{GS} = -10$ V.

(2) $I_D = -20$ mA; $V_{GS} = -2.4$ V.

Fig.11 Temperature coefficient of drain-source on-state resistance.



$T_{amb} = 25$ °C.

Fig.12 Thermal resistance from junction to ambient as a function of pulse time; typical values.

N-channel enhancement mode vertical D-MOS transistor

BSS87

DESCRIPTION

N-channel vertical D-MOS transistor in a SOT89 envelope. Designed primarily as a line current interrupter in telephone sets, it can also be applied in other applications such as in relays, line and high-speed transformer drivers etc.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.
- Low $R_{DS(on)}$

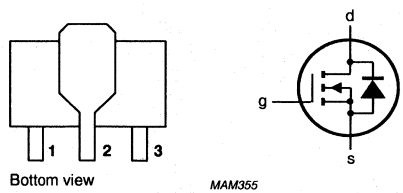
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	280	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source on-resistance				
I_D = 400 mA; V_{GS} = 10 V	$R_{DS(on)}$	max.	6	Ω
		typ.	4.5	Ω
Transfer admittance				
I_D = 400 mA; V_{DS} = 25 V	$\lvert Y_{fs} \rvert$	typ.	350	mS
		min.	140	mS

PINNING - SOT89

1 = source
2 = drain
3 = gate

PIN CONFIGURATION



marking: KA

Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BSS87

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	280	mA
Drain current (peak)	I_{DM}	max.	1.1	A
Total power dissipation up to T_{amb} = 25 °C (1)	P_{tot}	max.	1	W
Storage temperature range	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (1)	$R_{th\ j\text{-}a}$	=	125	K/W

Note

1. Transistor mounted on ceramic substrate area 2.5 cm^2, thickness 0.7 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage				
I_D = 250 µA; V_{GS} = 0	$V_{(BR)\ DSS}$	min.	200	V
Drain-source leakage current				
V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	200	nA
V_{DS} = 200 V; V_{GS} = 0	I_{DSS}	max.	60	µA
		typ.	100	nA
Gate-source leakage current				
V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate threshold voltage				
I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min.	0.8	V
		max.	2.8	V
Drain-source on-resistance				
I_D = 400 mA; V_{GS} = 10 V	$R_{DS(on)}$	max.	6	Ω
		typ.	4.5	Ω
Transfer admittance				
I_D = 400 mA; V_{DS} = 25 V	$\lvert Y_{fs} \rvert$	typ.	350	mS
		min.	140	mS
Input capacitance f = 1 MHz;				
V_{DS} = 25 V; V_{GS} = 0	C_{iss}	max.	60	pF
		typ.	45	pF
Output capacitance f = 1 MHz;				
V_{DS} = 25 V; V_{GS} = 0	C_{oss}	max.	25	pF
		typ.	15	pF

Feedback capacitance f = 1 MHz; V_{DS} = 25 V; V_{GS} = 0	C_{rss}	max.	10 pF
		typ.	3.5 pF
Switching times (see Figs 2 and 3)			
I_D = 250 mA; V_{DD} = 50 V;	t_{on}	typ.	5 ns
		max.	10 ns
V_{GS} = 0 to 10	t_{off}	typ.	15 ns
		max.	25 ns

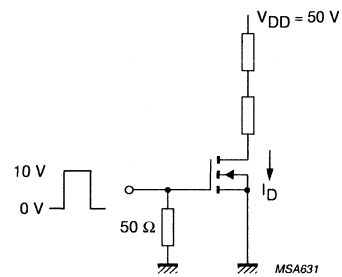


Fig.2 Switching times test circuit.

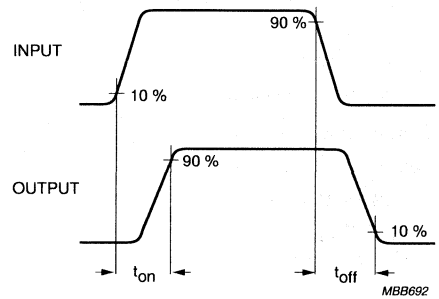


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistor

BSS89

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

APPLICATIONS

- Line current interruptor in telephone sets
- Relay, high-speed and line transformer drivers.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant package.

PINNING - TO-92 variant

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	d	drain
3	s	source

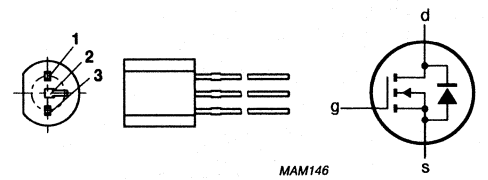


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–	200	V
V_{GSO}	gate-source voltage (DC)	open drain	–	–	±20	V
I_D	drain current (DC)		–	–	300	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	–	1	W
R_{DSon}	drain-source on-state resistance	I_D = 400 mA; V_{GS} = 10 V	–	4.5	6	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	I_D = 400 mA; V_{DS} = 25 V	140	350	–	mS

N-channel enhancement mode vertical D-MOS transistor

BSS89

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	200	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	300	mA
I_{DM}	peak drain current		–	1.2	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	1	W
T_{stg}	storage temperature		–55	+150	°C
T_j	junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	125	K/W

Note to the Limiting values and Thermal characteristics

1. Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for drain lead minimum 10 × 10 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 250 μA	200	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = V_{GS}$; I_D = 1 mA	0.8	–	2.8	V
I_{DSS}	drain-source leakage current	V_{DS} = 60 V; V_{GS} = 0	–	–	200	nA
		V_{DS} = 200 V; V_{GS} = 0	–	0.1	60	μA
I_{GSS}	gate leakage current	V_{DS} = 0; V_{GS} = ±20 V	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 400 mA	–	4.5	6	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	I_D = 400 mA; V_{DS} = 25 V	140	350	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	45	–	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	15	–	pF
C_{rss}	reverse transfer capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	3.5	–	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	V_{GS} = 0 to 10 V; V_{DD} = 50 V; I_D = 250 mA	–	5	–	ns
t_{off}	turn-off time	V_{GS} = 10 to 0 V; V_{DD} = 50 V; I_D = 250 mA	–	15	–	ns

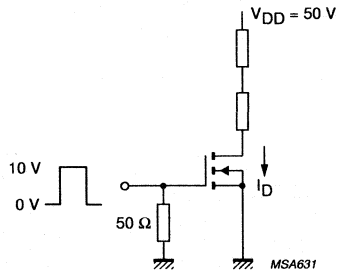


Fig.2 Switching time test circuit.

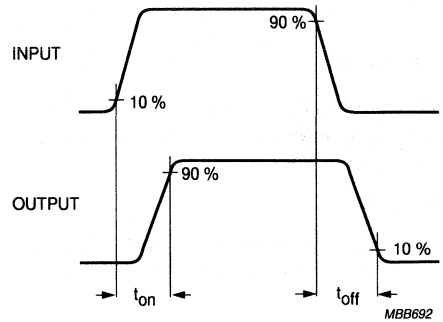


Fig.3 Input and output waveforms.

P-channel enhancement mode vertical D-MOS transistor

BSS92

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

APPLICATIONS

- Line current interrupter in telephony applications
- Relay, high speed and line transformer drivers.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a TO-92 (SOT54) variant package.

PINNING - TO-92 (SOT54) variant

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	d	drain
3	s	source

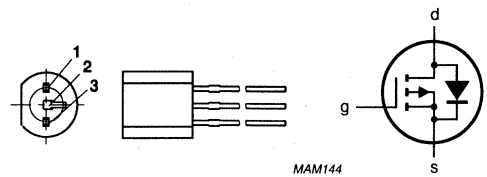


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–	–240	V
V_{GSO}	gate-source voltage (DC)	open drain	–	–	±20	V
I_D	drain current (DC)		–	–	–150	mA
R_{DSon}	drain-source on-state resistance	I_D = –100 mA; V_{GS} = –10 V	–	10	20	Ω
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	–	1	W
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = –25 V; I_D = –100 mA	60	200	–	mS

P-channel enhancement mode vertical D-MOS transistor

BSS92

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	−240	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	−150	mA
I_{DM}	peak drain current		–	−600	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	1	W
T_{stg}	storage temperature		−55	+150	°C
T_j	operating junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	125	K/W

Note to the Limiting values and Thermal characteristics

1. Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for drain lead minimum 10 mm × 10 mm.

CHARACTERISTICS

$T_j = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = -250$ µA	−240	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = V_{GS}$; $I_D = -1$ mA	−0.8	–	−2.8	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0$; $V_{DS} = -60$ V	–	–	−200	nA
		$V_{GS} = 0$; $V_{DS} = -200$ V	–	–	−60	µA
I_{GSS}	gate leakage current	$V_{DS} = 0$; $V_{GS} = \pm 20$ V	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = -10$ V; $I_D = -100$ mA	–	10	20	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	$V_{DS} = -25$ V; $I_D = -100$ mA	60	200	–	mS
C_{iss}	input capacitance	$V_{GS} = 0$; $V_{DS} = -25$ V; f = 1 MHz	–	65	–	pF
C_{oss}	output capacitance	$V_{GS} = 0$; $V_{DS} = -25$ V; f = 1 MHz	–	20	–	pF
C_{rss}	reverse transfer capacitance	$V_{GS} = 0$; $V_{DS} = -25$ V; f = 1 MHz	–	6	–	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$V_{GS} = 0$ to −10 V; $V_{DD} = -50$ V; $I_D = -250$ mA	–	5	–	ns
t_{off}	turn-off time	$V_{GS} = -10$ to 0 V; $V_{DD} = -50$ V; $I_D = -250$ mA	–	20	–	ns

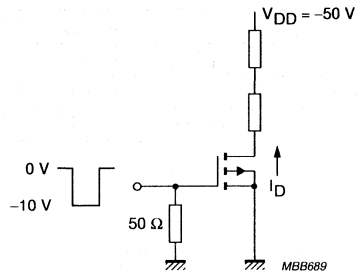


Fig.2 Switching times test circuit.

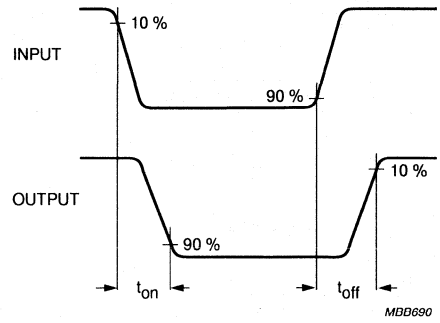


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistor

BSS123

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

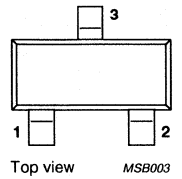
PINNING - SOT23

PIN	DESCRIPTION
1	gate
2	source
3	drain

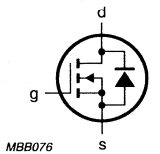
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		100	V
I_D	drain current	DC value	150	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 120 mA V_{GS} = 10 V	6	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	2.8	V

PIN CONFIGURATION



Top view MSB003



MBB076

Marking: SA.

Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BSS123

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	100	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	drain current	DC value	–	150	mA
I_{DM}	drain current	peak value	–	600	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
T_{stg}	storage temperature range		−65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	500	K/W

Note

1. Device mounted on a FR4 printboard.

N-channel enhancement mode vertical D-MOS transistor

BSS123

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA V_{GS} = 0	100	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 60 V V_{GS} = 0	–	–	10	nA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 120 mA V_{GS} = 10 V	–	3	6	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 120 mA V_{DS} = 25 V	80	140	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	24	40	pF
C_{oss}	output capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	15	25	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	4	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	4	10	ns
t_{off}	turn-off time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	10	20	ns

N-channel enhancement mode vertical D-MOS transistor

BSS123

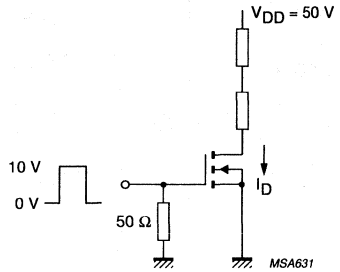


Fig.2 Switching time test circuit.

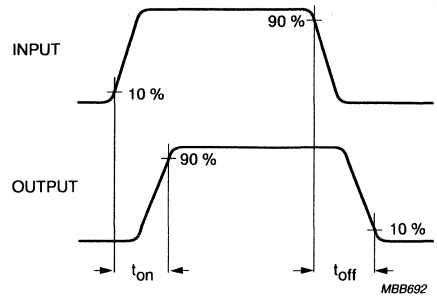


Fig.3 Input and output waveforms.

P-channel enhancement mode vertical D-MOS transistor

BSS192

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

APPLICATIONS

- Line current interrupter in telephone sets
- Relay, high-speed and line transformer drivers.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a SOT89 package.

PINNING - SOT89

PIN	SYMBOL	DESCRIPTION
1	s	source
2	d	drain
3	g	gate

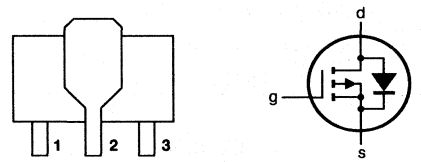


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Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		−240	V
V_{GSth}	gate-source threshold voltage	I_D = −1 mA; V_{GS} = V_{DS}	−2.8	V
I_D	drain current (DC)		−150	mA
R_{DSon}	drain-source on-state resistance	I_D = −100 mA; V_{GS} = −10 V	20	Ω

P-channel enhancement mode vertical D-MOS transistor

BSS192

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	−240	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	−150	mA
I_{DM}	peak drain current		–	−600	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	1	W
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	125	K/W

Note to the Limiting values and Thermal characteristics

1. Device mounted on a ceramic substrate; area 2.5 cm^2; thickness 0.7 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−240	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{GS} = V_{DS}$; I_D = −1 mA	−0.8	–	−2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −60 V	–	–	−200	nA
		V_{GS} = −0.2 V; V_{DS} = −200 V	–	−0.1	−60	μA
I_{GSS}	gate leakage current	V_{DS} = 0; V_{GS} = ±20 V	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = −10 V; I_D = −100 mA	–	10	20	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = −25 V; I_D = −200 mA	60	200	–	mS
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −25 V; f = 1 MHz	–	55	90	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −25 V; f = 1 MHz	–	20	30	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −25 V; f = 1 MHz	–	5	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	V_{GS} = 0 to −10 V; V_{DD} = −50 V; I_D = −250 mA	–	5	10	ns
t_{off}	turn-off time	V_{GS} = −10 to 0 V; V_{DD} = −50 V; I_D = −250 mA	–	20	30	ns

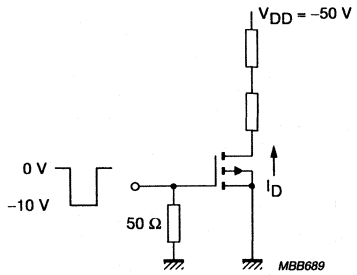


Fig.2 Switching times test circuit.

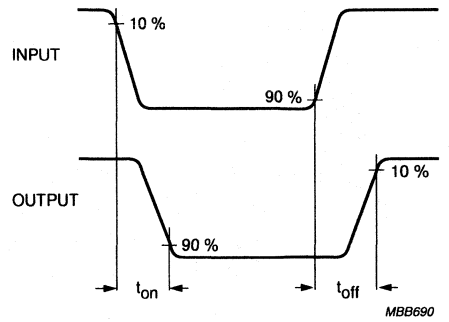


Fig.3 Input and output waveforms.

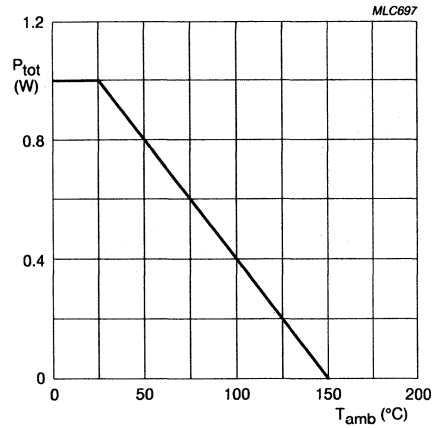
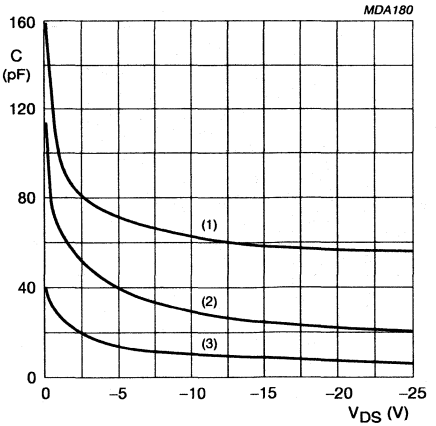


Fig.4 Power derating curve.

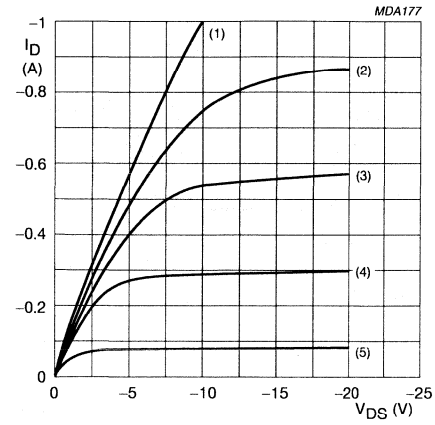


V_{GS} = 0; T_j = 25 °C; f = 1 MHz.
(1) C_{iss}.
(2) C_{oss}.
(3) C_{rss}.

Fig.5 Capacitance as a function of drain-source voltage; typical values.

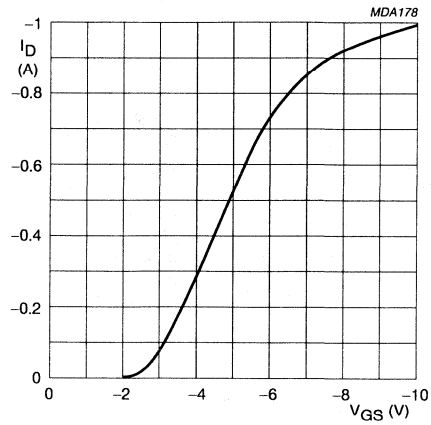
P-channel enhancement mode vertical D-MOS transistor

BSS192



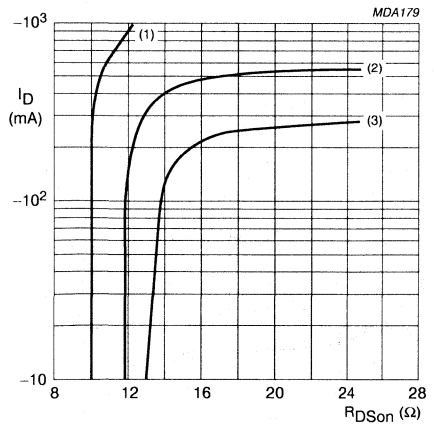
T_j = 25 °C.
(1) V_{GS} = 10 V.
(2) V_{GS} = 6 V.
(3) V_{GS} = 5 V.
(4) V_{GS} = 4 V.
(5) V_{GS} = 3 V.

Fig.6 Output characteristics; typical values.



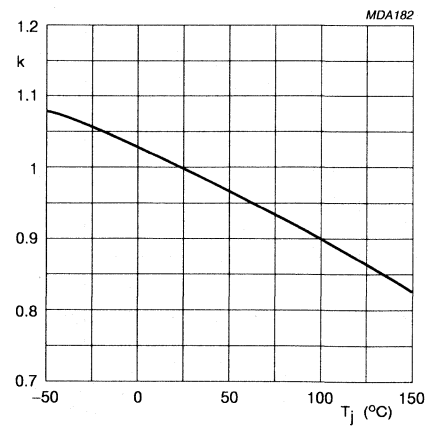
V_{DS} = −10 V; T_j = 25 °C.

Fig.7 Transfer characteristic; typical values.



T_j = 25 °C.
(1) V_{GS} = −10 V.
(2) V_{GS} = −5 V.
(3) V_{GS} = −4 V.

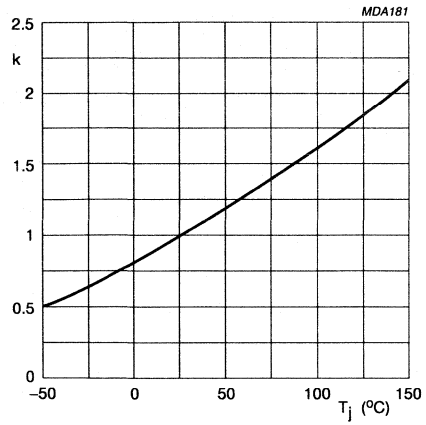
Fig.8 Drain current as a function of drain-source on-state resistance; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

V_{GSth} at I_D = −1 mA.

Fig.9 Temperature coefficient of gate-source threshold voltage; typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

$I_D = -200$ mA; $V_{GS} = -10$ V.

Fig.10 Temperature coefficient of drain-source on-state resistance; typical values.

N-channel vertical D-MOS transistor BST70A

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

FEATURES:

- Very low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

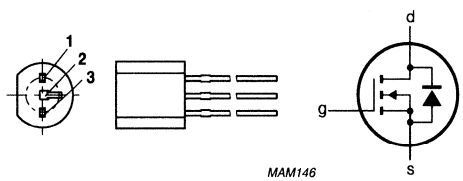
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (DC)	I_D	max.	0.5	A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance				
I_D = 500 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	2	Ω
		max.	4	Ω
Transfer admittance				
I_D = 500 mA; V_{DS} = 15 V	$\|Y_{fs}\|$	typ.	300	mS

PINNING - TO-92 VARIANT

1 = source
2 = gate
3 = drain

PIN CONFIGURATION



Note: Various pinout configurations available.

Fig.1 Simplified outline and symbol.

N-channel vertical D-MOS transistor BST70A

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (DC)	I_D	max.	0.5	A
Drain current (peak)	I_{DM}	max.	1.0	A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1	W
Storage temperature range	T_{stg}	− 65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm × 10 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage			
I_D = 10 μA; V_{GS} = 0	$V_{(BR)DS}$	min.	80 V
Drain-source leakage current			
V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	1 μA
Gate-source leakage current			
V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage			
I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance (see Fig.4)			
I_D = 500 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	2.0 Ω 4.0 Ω
Transfer admittance			
I_D = 500 mA; V_{DS} = 15 V	$\|Y_{fs}\|$	typ.	300 mS
Input capacitance at f = 1 MHz			
V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	45 pF 60 pF
Output capacitance at f = 1 MHz			
V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	30 pF 45 pF
Feedback capacitance at f = 1 MHz			
V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	8 pF 12 pF
Switching times (see Figs 2 and 3)			
I_D = 500 mA; V_{DS} = 50 V; V_{GS} = 0 to 10 V	t_{on} t_{off}	max. max.	10 ns 15 ns

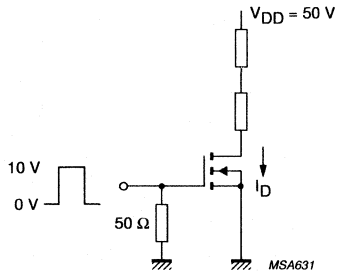


Fig.2 Switching times test circuit.

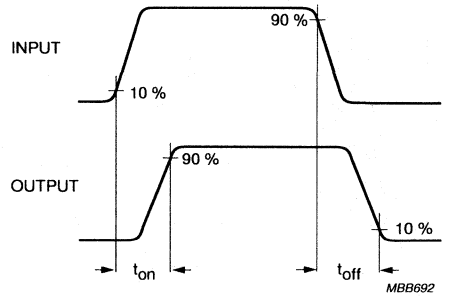


Fig.3 Input and output waveforms.

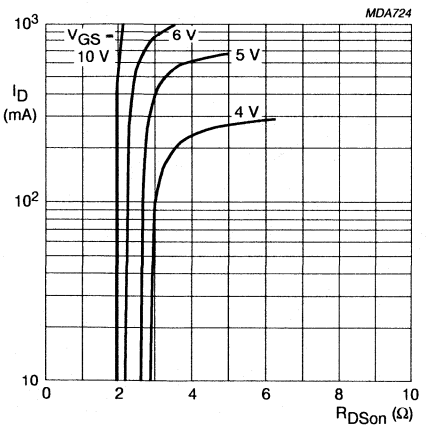


Fig.4 T_j = 25 °C; typical values.

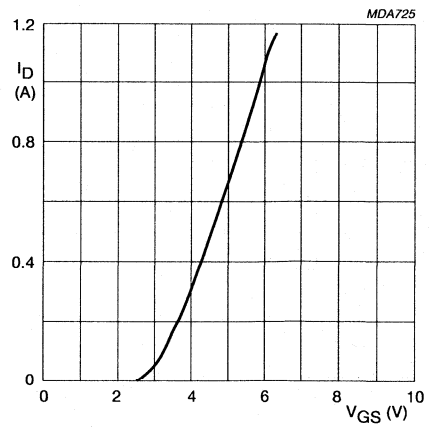


Fig.5 T_j = 25 °C; typical values at V_{DS} = 10 V.

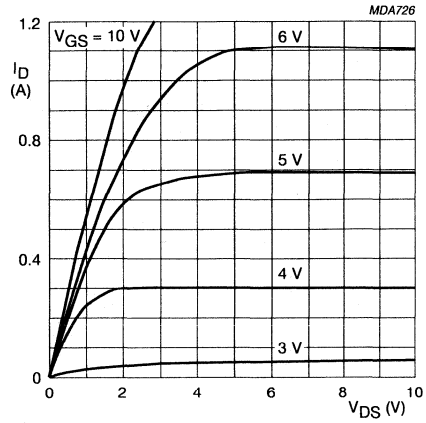


Fig.6 T_j = 25 °C; typical values.

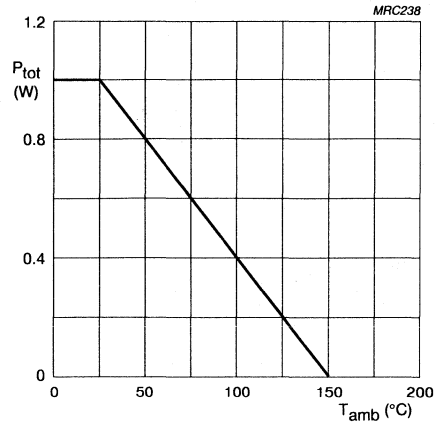


Fig.7 Power derating curve.

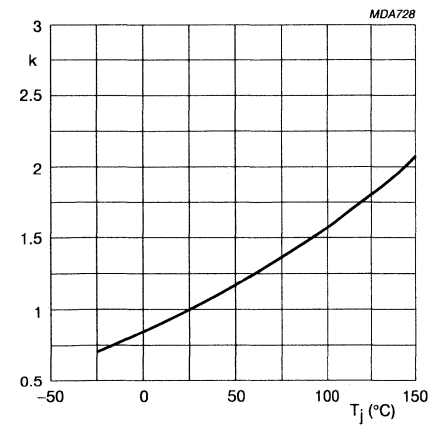


Fig.8

$$k = \frac{R_{DS\,(on)} \text{ at } T_j}{R_{DS\,(on)} \text{ at } 25\ °C};$$

typ. values at 500 mA/10 V.

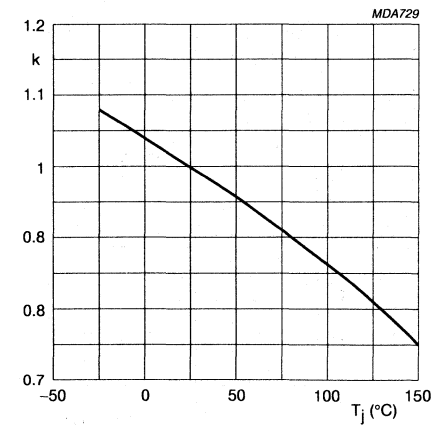


Fig.9

$$k = \frac{V_{GS\,(th)} \text{ at } T_j}{V_{GS\,(th)} \text{ at } 25\ °C};$$

$V_{GS(th)}$ at 1 mA; typical values.

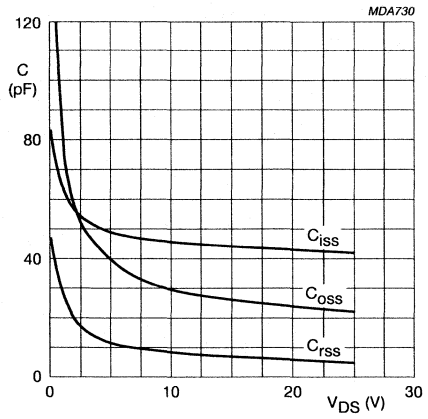


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-channel vertical D-MOS transistor — BST72A

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use in telephone ringer circuits and for application with relay, high-speed and line-transformer drivers.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

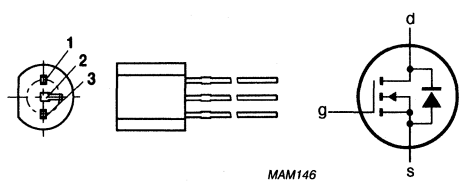
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80	V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	100	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Total power dissipation up to $T_{amb} = 25$ °C	P_{tot}	max.	0.83	W
Drain-source ON-resistance				
$I_D = 150$ mA; $V_{GS} = 5$ V	$R_{DS(on)}$	typ.	7	Ω
		max.	10	Ω
Transfer admittance				
$I_D = 200$ mA; $V_{DS} = 5$ V	$\lvert Y_{fs} \rvert$	typ.	150	mS

PINNING - TO-92 VARIANT

1 = source
2 = gate
3 = drain

PIN CONFIGURATION



Note: Various pinout configurations available.

Fig.1 Simplified outline and symbol.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80	V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	100	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Drain current (peak)	I_{DM}	max.	600	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	0.83	W
Storage temperature range	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	150	K/W

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage				
I_D = 10 μA; V_{GS} = 0	$V_{(BR)DS}$	min.	80	V
Drain-source leakage current				
V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	1.0	μA
Gate-source leakage current				
V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate threshold voltage				
I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min.	1.5	V
		max.	3.5	V
Drain-source ON-resistance (see Fig.4)				
I_D = 150 mA; V_{GS} = 5 V	$R_{DS(on)}$	typ.	7	Ω
		max.	10	Ω
Transfer admittance				
I_D = 200 mA; V_{DS} = 5 V	$\|Y_{fs}\|$	typ.	150	mS
Input capacitance at f = 1 MHz				
V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ.	15	pF
		max.	30	pF
Output capacitance at f = 1 MHz				
V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ.	13	pF
		max.	20	pF
Feedback capacitance at f = 1 MHz				
V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ.	3	pF
		max.	6	pF
Switching times (see Figs 2 and 3)				
I_D = 200 mA; V_{DS} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ.	4	ns
		max.	10	ns
	t_{off}	typ.	4	ns
		max.	10	ns

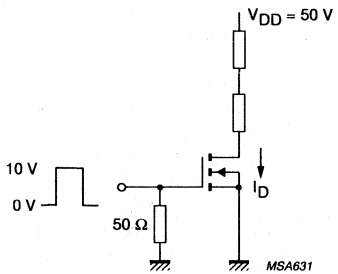


Fig.2 Switching times test circuit.

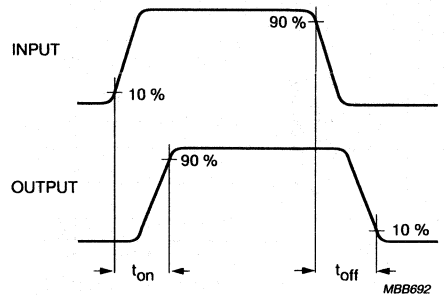


Fig.3 Input and output waveforms.

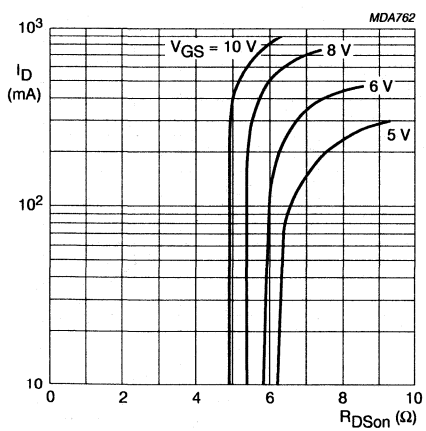


Fig.4 T_j = 25 °C; typical values.

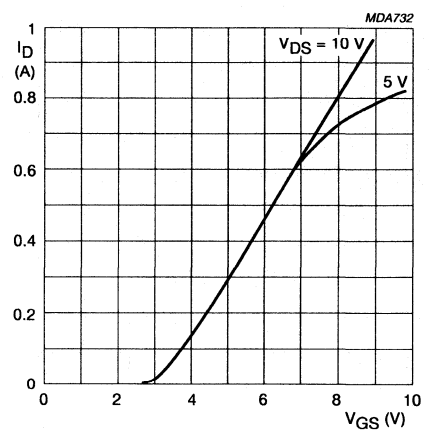


Fig.5 T_j = 25 °C; typical values.

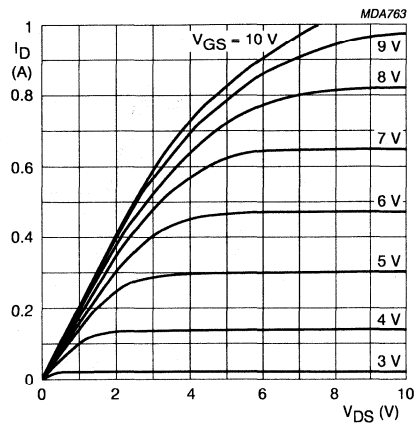


Fig.6 T_j = 25 °C; typical values.

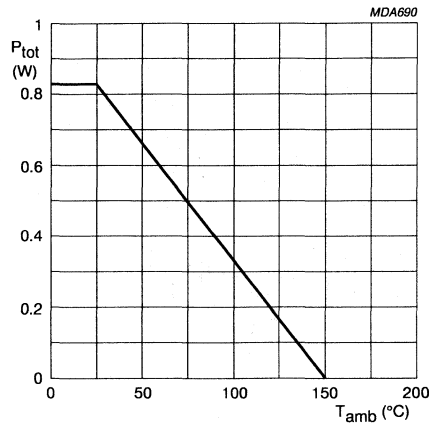


Fig.7 Power derating curve.

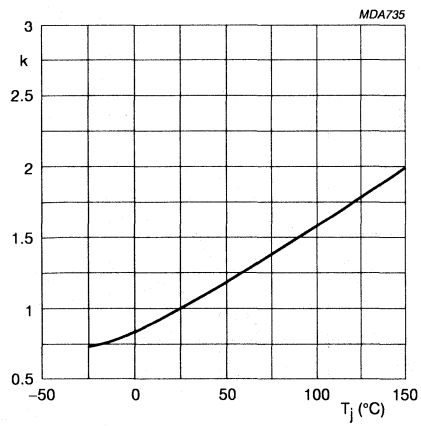


Fig.8

$$k = \frac{R_{DS\ on} \text{ at } T_j}{R_{DS\ on} \text{ at } 25\ °C};$$

typ. values at 150 mA/5 V.

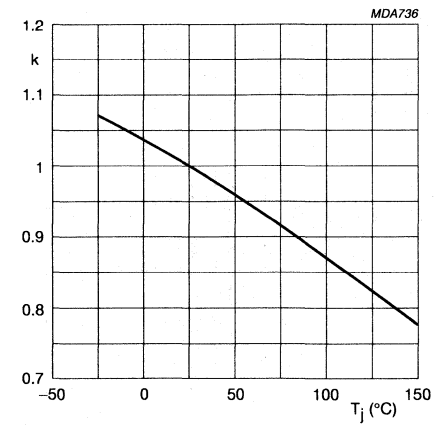


Fig.9

$$k = \frac{V_{GS\,(th)} \text{ at } T_j}{V_{GS\,(th)} \text{ at } 25\ °C};$$

$V_{GS(th)}$ at 1 mA; typical values.

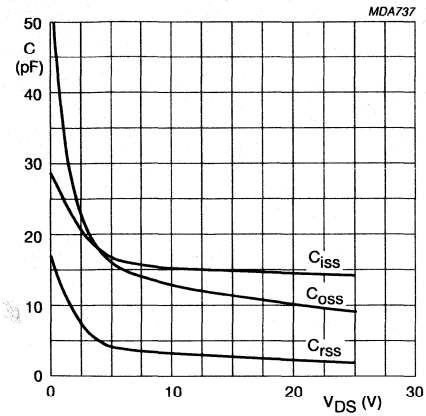


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-channel vertical D-MOS transistor | BST74A

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

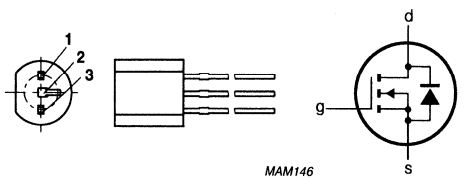
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (DC)	I_D	max.	250	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance				
I_D = 250 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	6	Ω
		max.	12	Ω
Transfer admittance				
I_D = 250 mA; V_{DS} = 15 V	$\|Y_{fs}\|$	typ.	250	mS

PINNING - TO-92 VARIANT

1 = source
2 = gate
3 = drain

PIN CONFIGURATION



Note: Various pinout configurations available.

Fig.1 Simplified outline and symbol.

N-channel vertical D-MOS transistor BST74A

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (DC)	I_D	max.	250	mA
Drain current (peak)	I_{DM}	max.	800	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1	W
Storage temperature range	T_{stg}		−65 to +150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for collector lead min. 10 mm × 10 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage				
I_D = 10 μA; V_{GS} = 0	$V_{(BR)DS}$	min.	200	V
Drain-source leakage current				
V_{DS} = 160 V; V_{GS} = 0	I_{DSS}	max.	10	μA
Gate-source leakage current				
V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate threshold voltage				
I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min.	0.8	V
		max.	2.8	V
Drain-source ON-resistance (see Fig.4)				
I_D = 250 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	6	Ω
		max.	12	Ω
Transfer admittance				
I_D = 250 mA; V_{DS} = 15 V	$\|Y_{fs}\|$	typ.	250	mS
Input capacitance at f = 1 MHz				
V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ.	70	pF
		max.	90	pF
Output capacitance at f = 1 MHz				
V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ.	20	pF
		max.	30	pF
Feedback capacitance at f = 1 MHz				
V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ.	5	pF
		max.	10	pF
Switching times (see Figs 2 and 3)				
I_D = 250 mA; V_{DS} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ.	4	ns
		max.	10	ns
	t_{off}	typ.	15	ns
		max.	25	ns

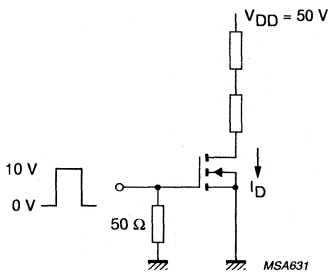


Fig.2 Switching times test circuit.

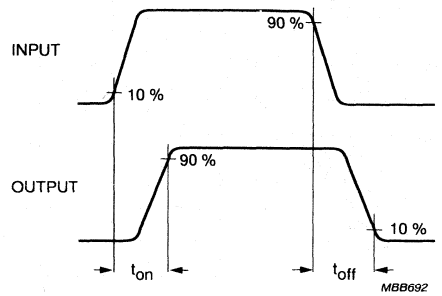


Fig.3 Input and output waveforms.

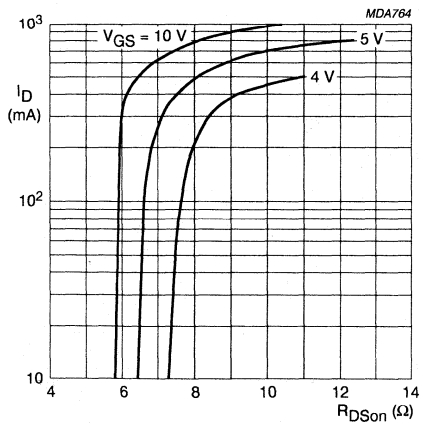


Fig.4 T_j = 25 °C; typical values.

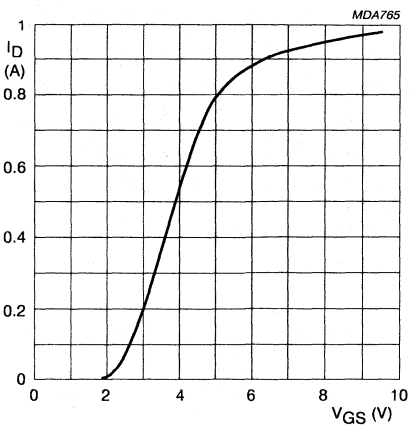


Fig.5 T_j = 25 °C; V_{DS} = 10 V; typical values.

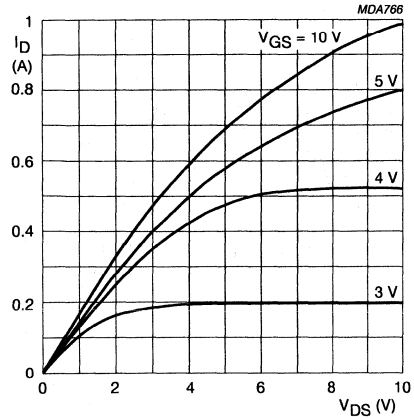


Fig.6 T_j = 25 °C; typical values.

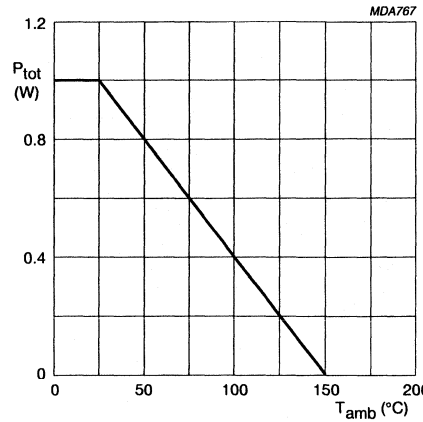


Fig.7 Power derating curve.

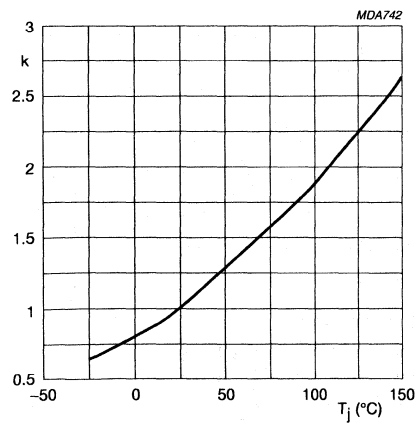


Fig.8

$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C};$$

at 400 mA/10 V; typical values.

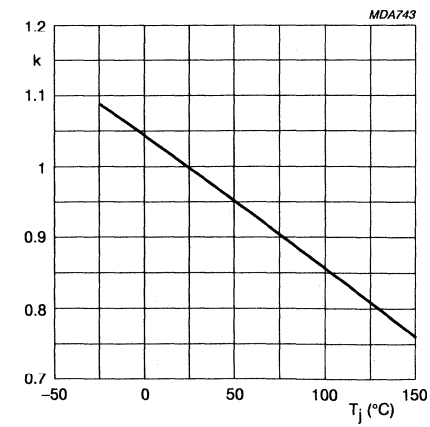


Fig.9

$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C};$$

$V_{GS(th)}$ at 1 mA; typical values.

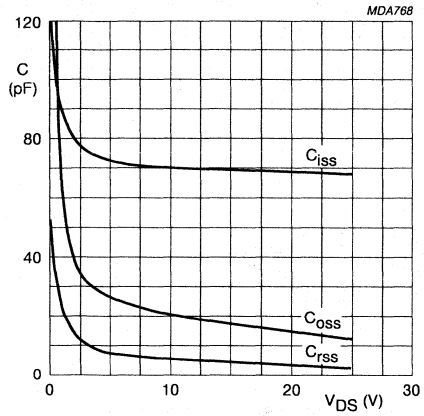


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-channel enhancement mode vertical D-MOS transistor

BST76A

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

APPLICATIONS

- Line current interrupter in telephone sets
- Relay, high-speed and line transformer drivers.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT54 (TO-92) variant package.

PINNING - SOT54 (TO-92) variant

PIN	SYMBOL	DESCRIPTION
1	s	source
2	g	gate
3	d	drain

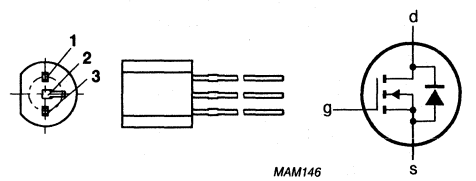


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	180	V
$V_{DS(SM)}$	drain-source voltage	non-repetitive peak; $t_p \leq 2$ mS	–	200	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	300	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	1	W
R_{DSon}	drain-source on-state resistance	$I_D = 15$ mA; $V_{GS} = 3$ V	7	10	Ω
$\|y_{fs}\|$	forward transfer admittance	$I_D = 300$ mA; $V_{DS} = 15$ V	250	–	mS

N-channel enhancement mode vertical D-MOS transistor

BST76A

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	180	V
$V_{DS(SM)}$	drain-source voltage	non-repetitive peak; $t_p \leq 2$ mS	–	200	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	300	mA
I_{DM}	peak drain current		–	800	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	1	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	125	K/W

Note to the Limiting values and Thermal characteristics

1. Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for drain lead minimum 10 mm × 10 mm.

CHARACTERISTICS

$T_j = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = 100$ µA	180	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = V_{GS}$; $I_D = 100$ µA	0.7	–	2.4	V
I_{DSS}	drain-source leakage current	$V_{DS} = 120$ V; $V_{GS} = 0$	–	–	10	µA
I_{GSS}	gate leakage current	$V_{DS} = 0$; $V_{GS} = \pm 20$ V	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 3$ V; $I_D = 15$ mA	–	7	10	Ω
		$V_{GS} = 10$ V; $I_D = 300$ mA	–	6	–	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	$I_D = 300$ mA; $V_{DS} = 15$ V	–	250	–	mS
C_{iss}	input capacitance	$V_{DS} = 10$ V; $V_{GS} = 0$; f = 1 MHz	–	50	65	pF
C_{oss}	output capacitance	$V_{DS} = 10$ V; $V_{GS} = 0$; f = 1 MHz	–	20	30	pF
C_{rss}	reverse transfer capacitance	$V_{DS} = 10$ V; $V_{GS} = 0$; f = 1 MHz	–	6	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$V_{GS} = 0$ to 10 V; $V_{DS} = 50$ V; $I_D = 300$ mA	–	–	10	ns
t_{off}	turn-off time	$V_{GS} = 10$ to 0 V; $V_{DS} = 50$ V; $I_D = 300$ mA	–	–	15	ns

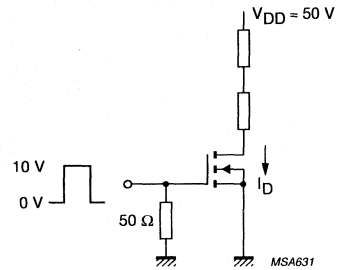


Fig.2 Switching times test circuit.

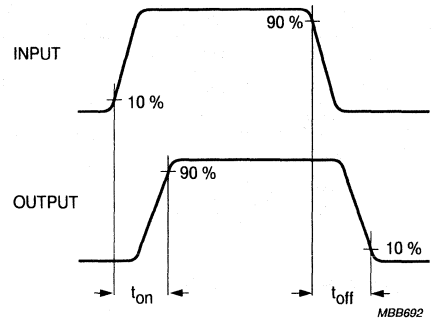


Fig.3 Input and output waveforms.

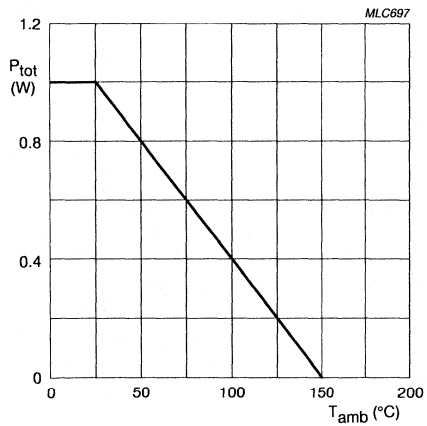
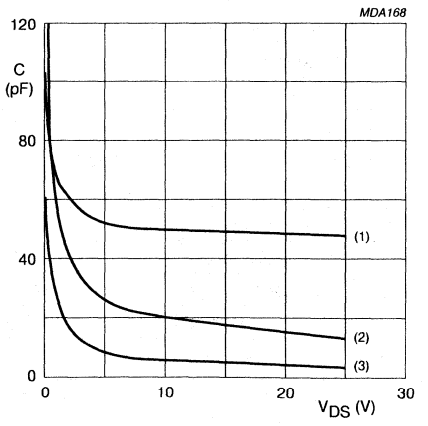
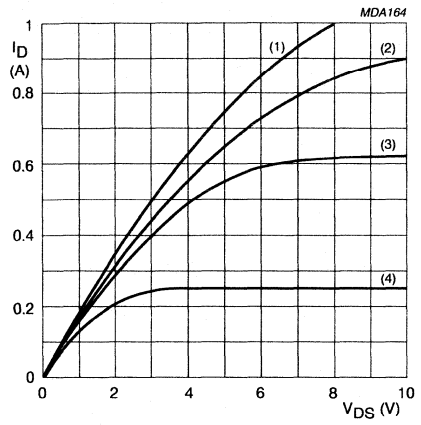


Fig.4 Power derating curve.



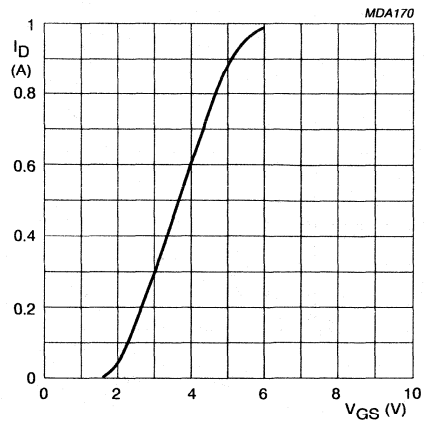
V_{GS} = 0; f = 1 MHz; T_j = 25 °C.
(1) C_{iss}.
(2) C_{oss}.
(3) C_{rss}.

Fig.5 Capacitance as a function of drain-source voltage; typical values.



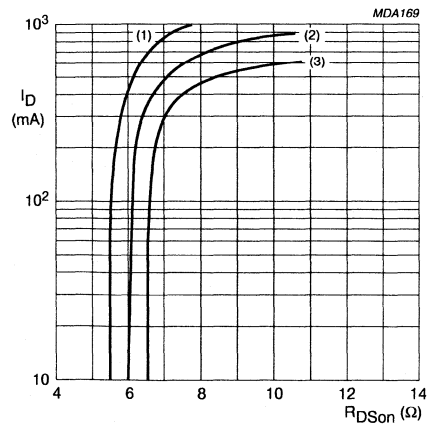
T_j = 25 °C.
(1) V_{GS} = 10 V.
(2) V_{GS} = 5 V.
(3) V_{GS} = 4 V.
(4) V_{GS} = 3 V.

Fig.6 Output characteristics; typical values.



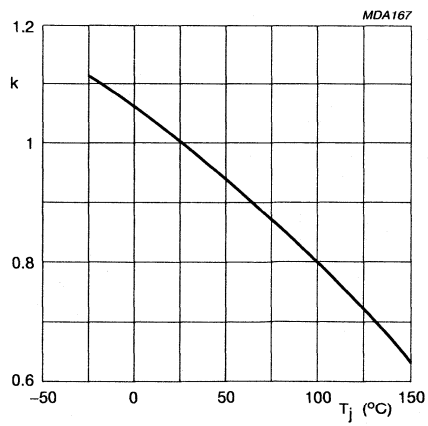
V_{DS} = 10 V; T_j = 25 °C.

Fig.7 Transfer characteristic; typical values.



T_j = 25 °C.
(1) V_{GS} = 10 V.
(2) V_{GS} = 5 V.
(3) V_{GS} = 4 V.

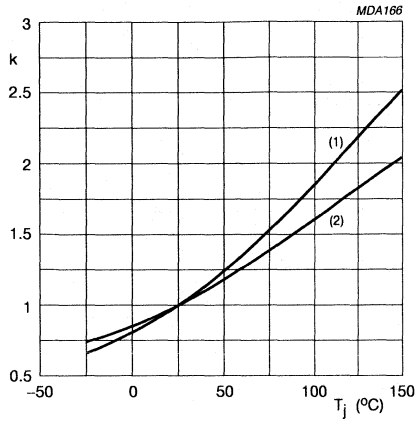
Fig.8 Drain current as a function of drain-source on-state resistance; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

V_{GSth} at 0.1 mA.

Fig.9 Temperature coefficient of gate-source threshold voltage; typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

(1) I_D = 300 mA; V_{GS} = 10 V.
(2) I_D = 15 mA; V_{GS} = 3 V.

Fig.10 Temperature coefficient of drain-source on-state resistance; typical values.

N-channel enhancement mode vertical D-MOS transistor

BST80

FEATURES

- Low drain-source on-state resistance
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

APPLICATIONS

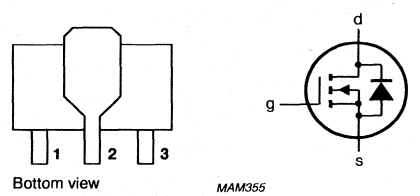
- Thin and thick film circuits
- Relay, high-speed and line transformer drivers.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT89 package.

PINNING - SOT89

PIN	SYMBOL	DESCRIPTION
1	s	source
2	d	drain
3	g	gate



Marking code: KM

Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	80	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	500	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	1	W
R_{DSon}	drain-source on-state resistance	I_D = 500 mA; V_{GS} = 10 V	2	3	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	I_D = 500 mA; V_{DS} = 15 V	300	–	mS

N-channel enhancement mode vertical D-MOS transistor

BST80

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	80	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	500	mA
I_{DM}	peak drain current		–	1	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	1	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	125	K/W

Note to the Limiting values and Thermal characteristics

1. Device mounted on a ceramic substrate; area 2.5 cm^2; thickness 0.7 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 µA	80	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.5	–	3.5	V
I_{DSS}	drain-source leakage current	V_{DS} = 60 V; V_{GS} = 0	–	–	1	µA
I_{GSS}	gate leakage current	V_{DS} = 0; V_{GS} = ±20 V	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 500 mA	–	2	3	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	I_D = 500 mA; V_{DS} = 15 V	–	300	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V; V_{GS} = 0; f = 1 MHz	–	45	60	pF
C_{oss}	output capacitance	V_{DS} = 10 V; V_{GS} = 0; f = 1 MHz	–	30	45	pF
C_{rss}	reverse transfer capacitance	V_{DS} = 10 V; V_{GS} = 0; f = 1 MHz	–	8	12	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	V_{GS} = 0 to 10 V; V_{DD} = 50 V; I_D = 500 mA	–	–	10	ns
t_{off}	turn-off time	V_{GS} = 10 to 0 V; V_{DD} = 50 V; I_D = 500 mA	–	–	15	ns

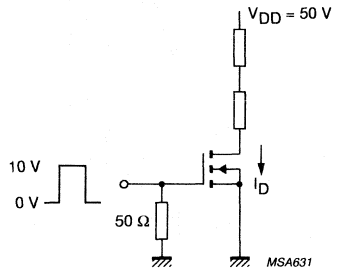


Fig.2 Switching times test circuit.

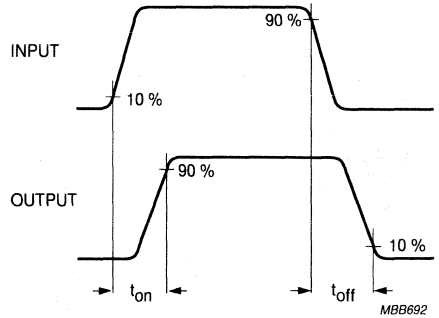


Fig.3 Input and output waveforms.

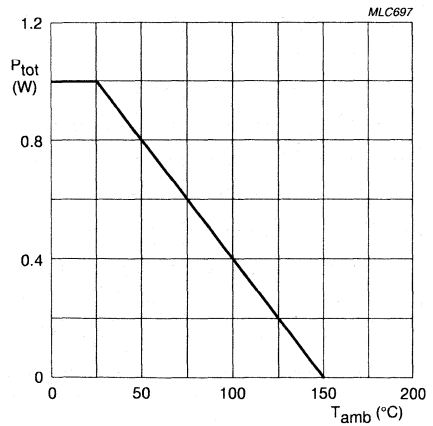
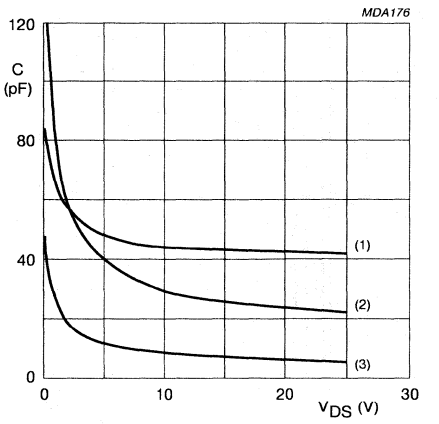


Fig.4 Power derating curve.



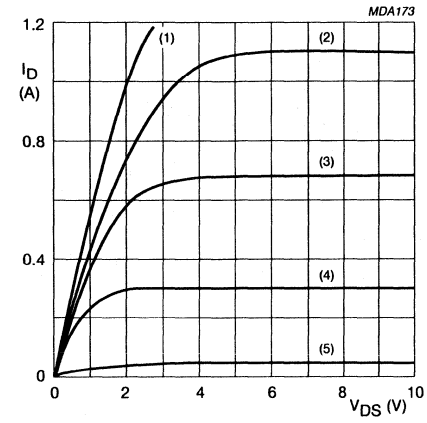
V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

(1) C_{iss}.

(2) C_{oss}.

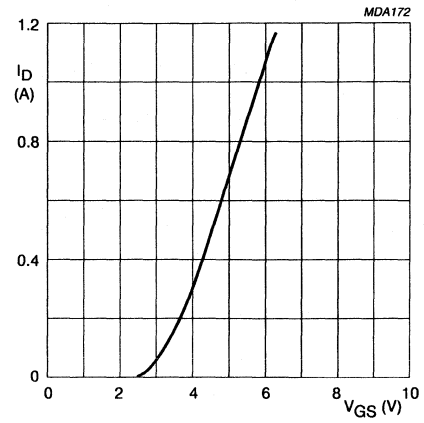
(3) C_{rss}.

Fig.5 Capacitance as a function of drain-source voltage; typical values.



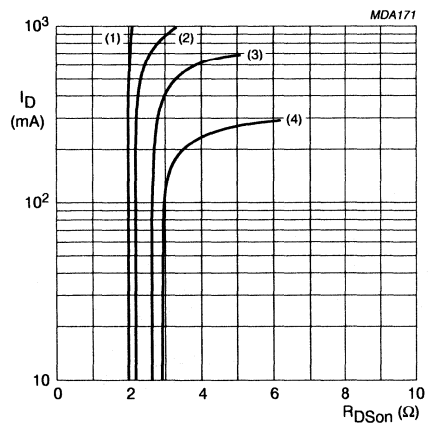
T_j = 25 °C.
(1) V_{GS} = 10 V.
(2) V_{GS} = 6 V.
(3) V_{GS} = 5 V.
(4) V_{GS} = 4 V.
(5) V_{GS} = 3 V.

Fig.6 Output characteristics; typical values.



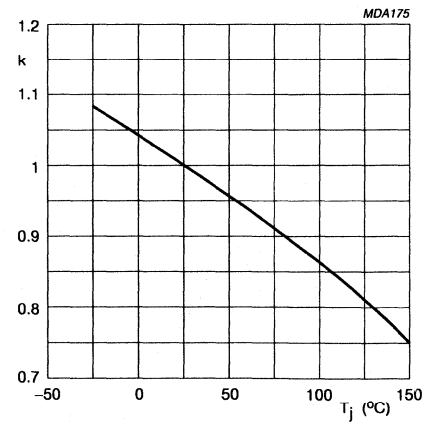
V_{DS} = 10 V; T_j = 25 °C.

Fig.7 Transfer characteristic; typical values.



T_j = 25 °C.
(1) V_{GS} = 10 V.
(2) V_{GS} = 6 V.
(3) V_{GS} = 5 V.
(4) V_{GS} = 4 V.

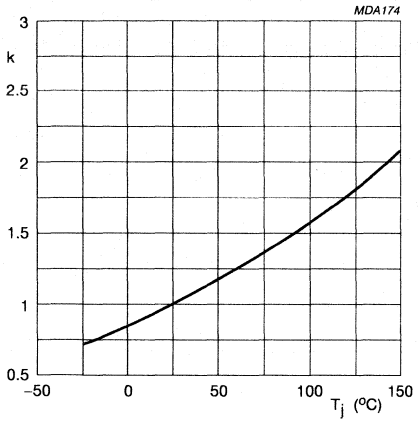
Fig.8 Drain current as a function of drain-source on-state resistance; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

V_{GSth} at 1 mA.

Fig.9 Temperature coefficient of gate-source threshold voltage; typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

I_D = 500 mA; V_{GS} = 10 V.

Fig.10 Temperature coefficient of drain-source on-state resistance; typical values.

N-channel enhancement mode vertical D-MOS transistor

BST82

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in SOT23 envelope and designed for use as Surface Mounted Device (SMD) in thin and thick-film circuits for telephone ringer and for application with relay, high-speed and line-transformer drivers.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown
- Low $R_{DS(on)}$

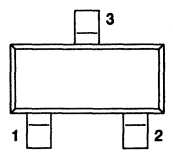
QUICK REFERENCE DATA

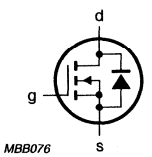
Drain-source voltage	V_{DS}	max.	80	V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	100	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	175	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Drain-source ON-resistance				
I_D = 150 mA; V_{GS} = 5 V	$R_{DS(on)}$	typ.	7	Ω
		max.	10	Ω
Transfer admittance				
I_D = 175 mA; V_{DS} = 5 V	$\lvert Y_{fs} \rvert$	typ.	150	mS

PINNING - SOT23

1 = gate
2 = source
3 = drain

PIN CONFIGURATION





Marking: 02p

Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BST82

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80	V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	100	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	175	mA
Drain current (peak)	I_{DM}	max.	600	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	300	mW
Storage temperature range	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	430	K/W

Note

1. Transistors mounted on a ceramic substrate of 7 mm x 5 mm x 0.7 mm.

N-channel enhancement mode vertical D-MOS transistor

BST82

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage				
I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	80	V
Drain-source leakage current				
V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	1.0	μA
Gate-source leakage current				
V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate-source cut-off voltage				
I_D = 1 mA; V_{DS} = V_{GS}	$V_{(P)GS}$	min.	1.5	V
		max.	3.5	V
Drain-source ON-resistance				
I_D = 150 mA; V_{GS} = 5 V	$R_{DS(on)}$	typ.	7	Ω
		max.	10	Ω
Transfer admittance				
I_D = 175 mA; V_{DS} = 5 V	$\lvert Y_{fs} \rvert$	typ.	150	mS
Input capacitance at f = 1 MHz				
V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ.	15	pF
		max.	30	pF
Output capacitance at f = 1 MHz				
V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ.	13	pF
		max.	20	pF
Feedback capacitance at f = 1 MHz				
V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ.	3	pF
		max.	6	pF
Switching times (see Figs 2 and 3)				
I_D = 175 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ.	4	ns
		max.	10	ns
	t_{off}	typ.	4	ns
		max.	10	ns

N-channel enhancement mode vertical D-MOS transistor

BST82

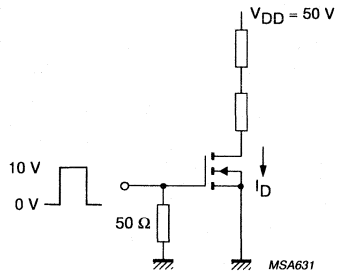


Fig.2 Switching times test circuit.

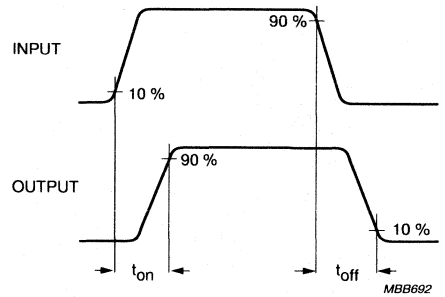


Fig.3 Input and output waveforms.

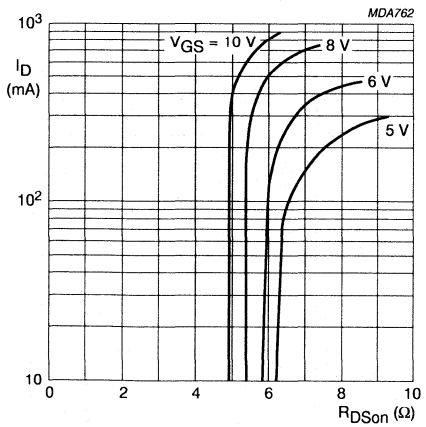


Fig.4 T_j = 25 °C; typical values.

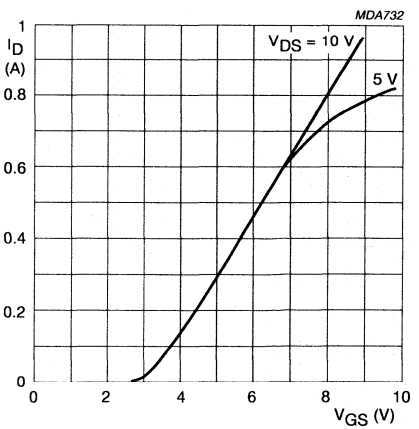


Fig.5 T_j = 25 °C; typical values.

N-channel enhancement mode vertical D-MOS transistor

BST82

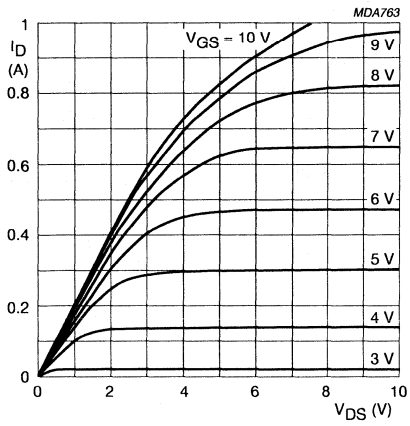


Fig.6 T_j = 25 °C; typical values.

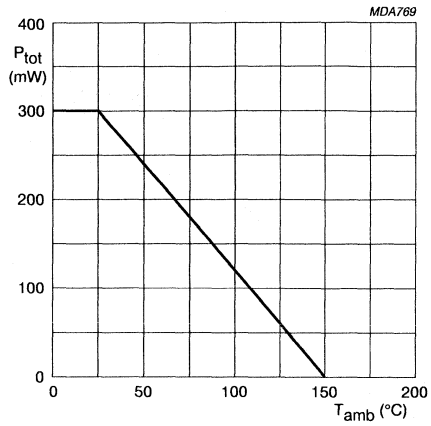


Fig.7 Power derating curve.

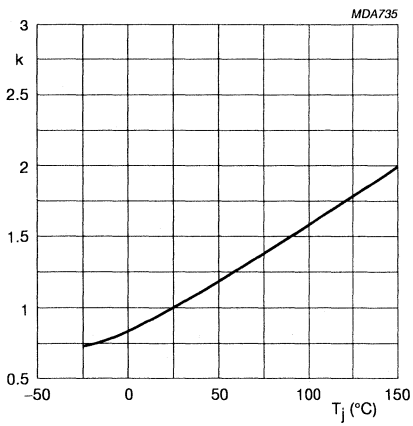


Fig.8

$$k = \frac{R_{DS\,(on)} \text{ at } T_j}{R_{DS\,(on)} \text{ at } 25\ °C};$$

typ. values at 150 mA/5 V.

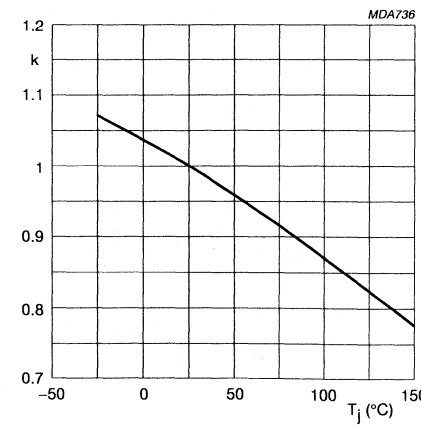


Fig.9

$$k = \frac{V_{GS\,(th)} \text{ at } T_j}{V_{GS\,(th)} \text{ at } 25\ °C};$$

$V_{GS(th)}$ at 1 mA; typical values.

N-channel enhancement mode vertical D-MOS transistor

BST82

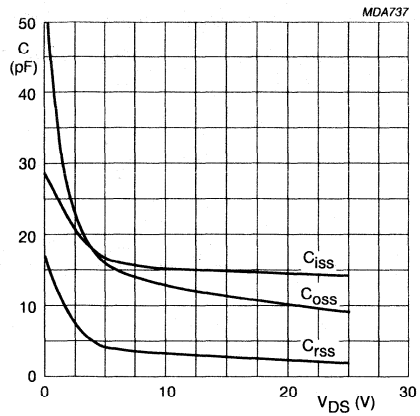


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-channel enhancement mode vertical D-MOS transistor

BST84

DESCRIPTION

N-channel vertical D-MOS transistor in SOT89 envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

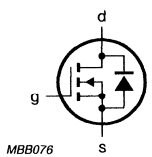
QUICK REFERENCE DATA

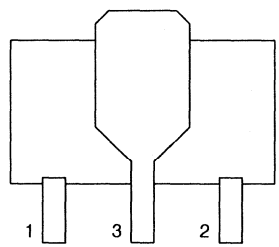
Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	250	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance				
I_D = 250 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	6	Ω
		max.	12	Ω
Transfer admittance				
I_D = 250 mA; V_{DS} = 15 V	$\lvert Y_{fs} \rvert$	typ.	250	mS

PINNING - SOT89

1 = source
2 = gate
3 = drain

PIN CONFIGURATION





Marking: KN

Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BST84

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	250	mA
Drain current (peak)	I_{DM}	max.	800	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1	W
Storage temperature range	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

Note

1. Transistor mounted on a ceramic substrate with area of 2.5 cm^2 and thickness of 0.7 mm.

N-channel enhancement mode vertical D-MOS transistor

BST84

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage				
I_D = 100 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200	V
Drain-source leakage current				
V_{DS} = 160 V; V_{GS} = 0	I_{DSS}	max.	10	μA
Gate-source leakage current				
V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate threshold voltage				
I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min.	0.8	V
		max.	2.8	V
Drain-source ON-resistance				
I_D = 250 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	6	Ω
		max.	12	Ω
Transfer admittance				
I_D = 250 mA; V_{DS} = 15 V	$\|Y_{fs}\|$	typ.	250	mS
Input capacitance at f = 1 MHz				
V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ.	70	pF
		max.	90	pF
Output capacitance at f = 1 MHz				
V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ.	20	pF
		max.	30	pF
Feedback capacitance at f = 1 MHz				
V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ.	5	pF
		max.	10	pF
Switching times (see Figs 2 and 3)				
I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ.	4	ns
		max.	10	ns
	t_{off}	typ.	15	ns
		max.	25	ns

N-channel enhancement mode vertical D-MOS transistor

BST84

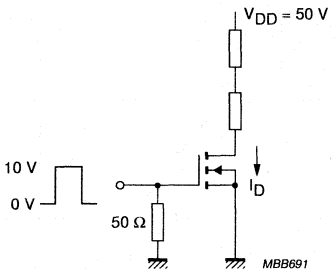


Fig.2 Switching times test circuit.

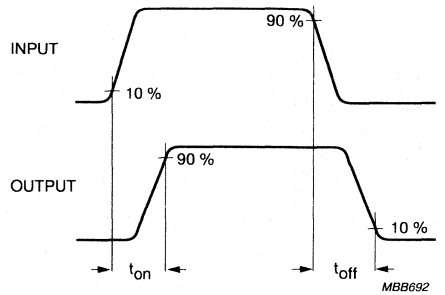


Fig.3 Input and output waveforms.

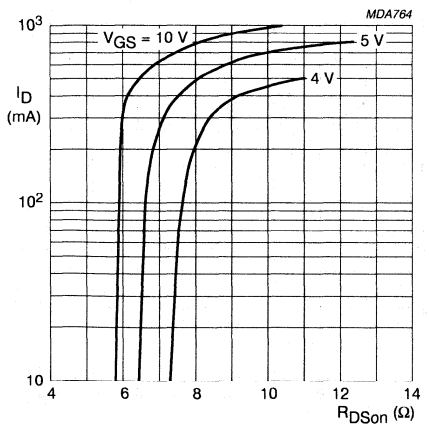


Fig.4 T_j = 25 °C; typical values.

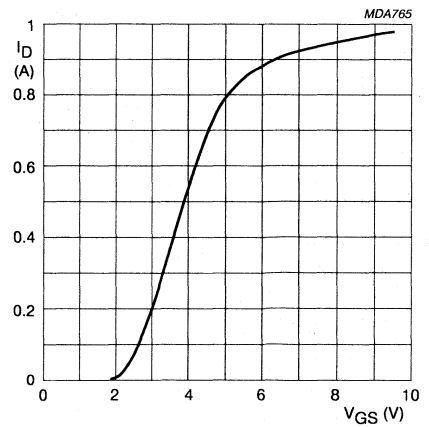


Fig.5 T_j = 25 °C; V_{DS} = 10 V; typical values.

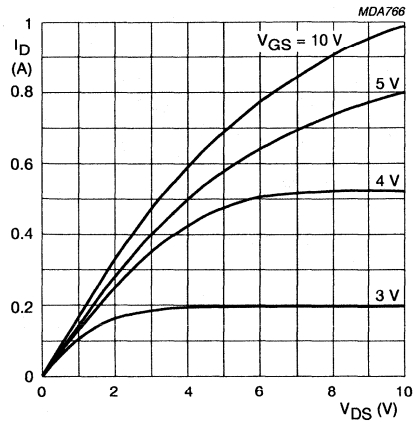


Fig.6 T_j = 25 °C; typical values.

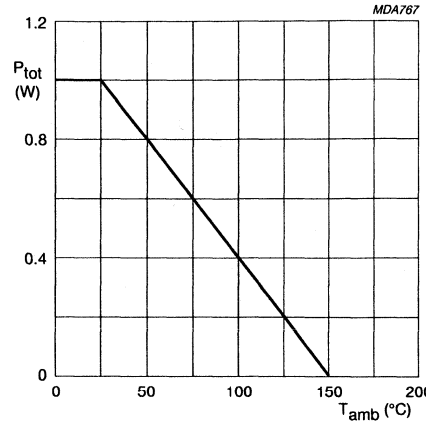


Fig.7 Power derating curve.

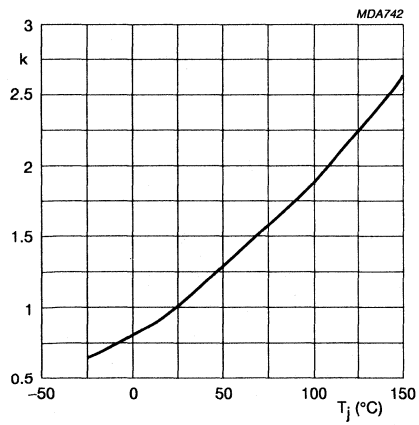


Fig.8

$$k = \frac{R_{DS\,(on)} \text{ at } T_j}{R_{DS\,(on)} \text{ at } 25\ °C};$$

at 400 mA/10 V; typical values.

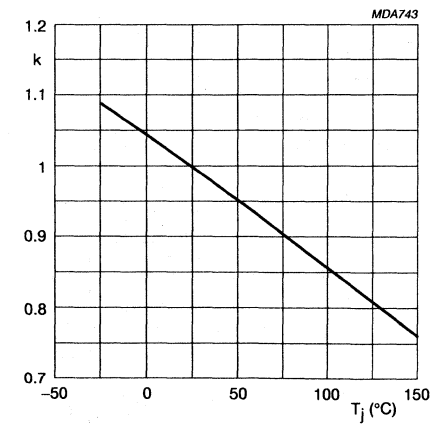


Fig.9

$$k = \frac{V_{GS\,(th)} \text{ at } T_j}{V_{GS\,(th)} \text{ at } 25\ °C};$$

$V_{GS(th)}$ at 1 mA; typical values.

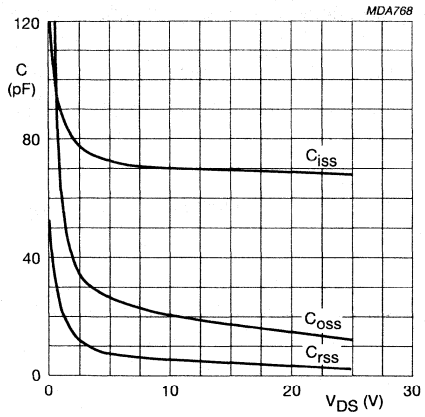


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-channel enhancement mode vertical D-MOS transistor

BST86

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in SOT89 envelope and designed for use as Surface Mounted Device (SMD) in thin and thick-film circuits for application with relay, high-speed and line-transformer drivers.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

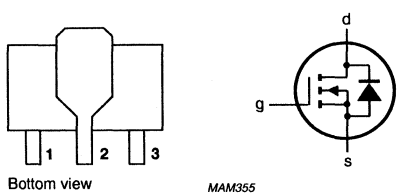
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	180	V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Total power dissipation up to $T_{amb} = 25$ °C	P_{tot}	max.	1	W
Drain-source ON-resistance				
$I_D = 15$ mA; $V_{GS} = 3$ V	$R_{DS(on)}$	typ.	7	Ω
		max.	10	Ω
Transfer admittance				
$I_D = 300$ mA; $V_{DS} = 15$ V	$\lvert Y_{fs} \rvert$	typ.	250	mS

PINNING - SOT89

1 = source
2 = drain
3 = gate

PIN CONFIGURATION



Marking: K0

Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BST86

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	180	V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Drain current (peak)	I_{DM}	max.	800	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1	W
Storage temperature range	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

Note

1. Transistor mounted on a ceramic substrate of 2.5 cm^2 and thickness of 0.7 mm.

N-channel enhancement mode vertical D-MOS transistor

BST86

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage				
I_D = 100 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	180	V
Drain-source leakage current				
V_{DS} = 120 V; V_{GS} = 0	I_{DSS}	max.	10	μA
Gate-source leakage current				
V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate threshold voltage				
I_D = 100 μA; V_{DS} = V_{GS}	$V_{GS(th)}$	min.	0.7	V
		max.	2.7	V
Drain-source ON-resistance				
I_D = 15 mA; V_{GS} = 3 V	$R_{DS(on)}$	typ.	7	Ω
		max.	10	Ω
I_D = 300 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	6	Ω
Transfer admittance				
I_D = 300 mA; V_{DS} = 15 V	$\|Y_{fs}\|$	typ.	250	mS
Input capacitance at f = 1 MHz				
V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ.	50	pF
		max.	65	pF
Output capacitance at f = 1 MHz				
V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ.	20	pF
		max.	30	pF
Feedback capacitance at f = 1 MHz				
V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ.	6	pF
		max.	10	pF
Switching times (see as 2 and 3)				
I_D = 300 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	max.	10	ns
	t_{off}	max.	15	ns

N-channel enhancement mode vertical D-MOS transistor

BST86

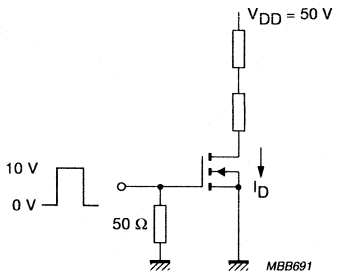


Fig.2 Switching times test circuit.

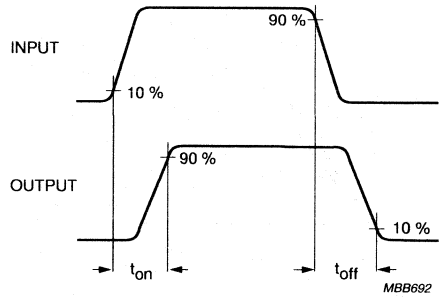
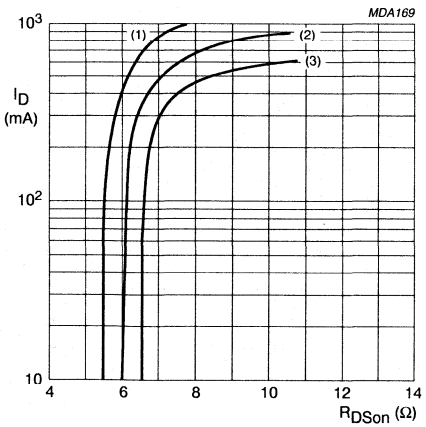


Fig.3 Input and output waveforms.



(1) V_{GS} = 10 V.
(2) V_{GS} = 5 V.
(3) V_{GS} = 4 V.

Fig.4 T_j = 25 °C; typical values.

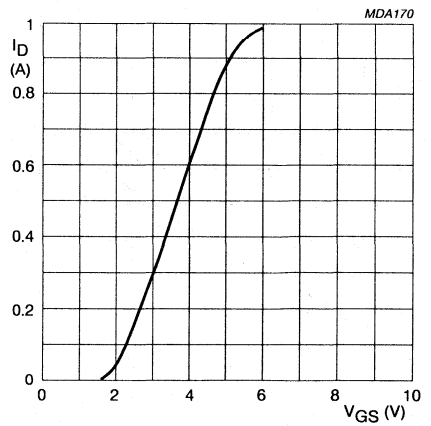
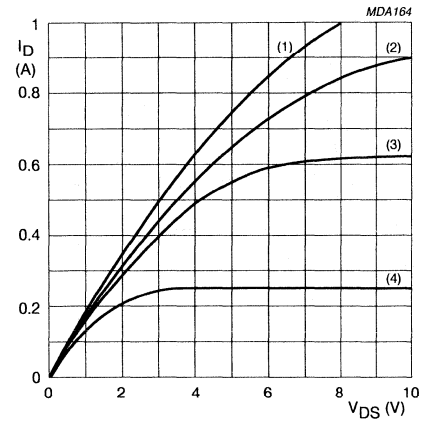


Fig.5 T_j = 25 °C; V_{DS} = 10 V; typ. values.



(1) V_{GS} = 10 V.
(2) V_{GS} = 5 V.
(3) V_{GS} = 4 V.
(4) V_{GS} = 3 V.

Fig.6 T_j = 25 °C; typical values.

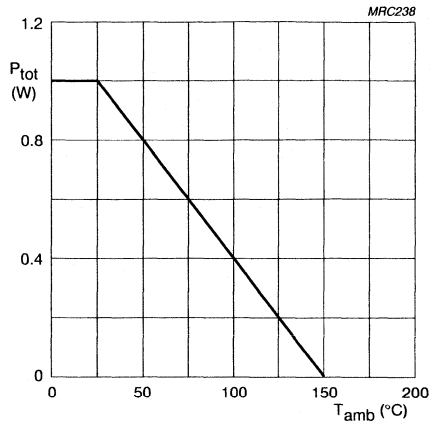
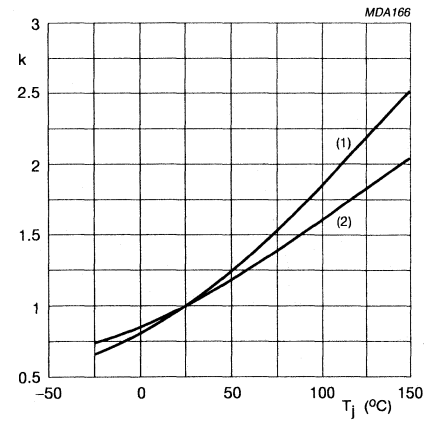


Fig.7 Power derating curve.



(1) I_D = 300 mA; V_{GS} = 10 V.
(2) I_D = 15 mA; V_{GS} = 3 V.

Fig.8

$$k = \frac{R_{DS\ on} \text{ at } T_j}{R_{DS\ on} \text{ at } 25\ °C};$$

typcial values.

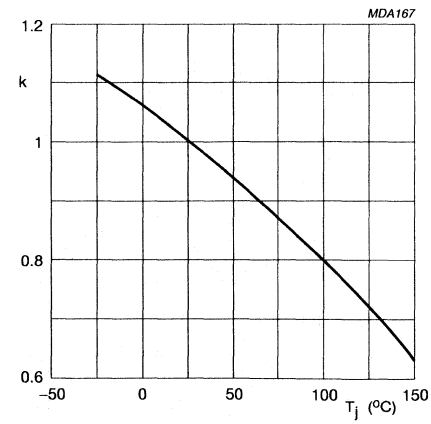
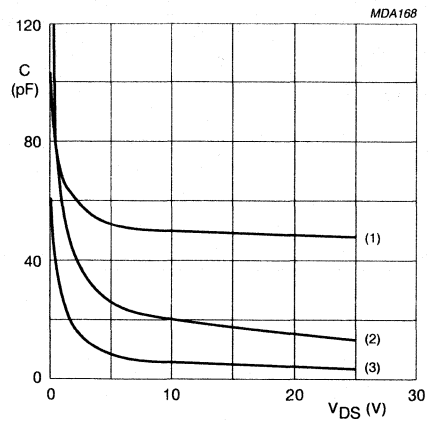


Fig.9

$$k = \frac{V_{GS\,(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C};$$

$V_{GS(th)}$ at 01. mA; typical values.



(1) C_{iss}.
(2) C_{oss}.
(3) C_{rss}.

Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

P-channel enhancement mode vertical D-MOS transistor

BST100

DESCRIPTION

P-channel vertical D-MOS transistor TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

FEATURES

- Very low $R_{DS(on)}$
- Direct interface to C-MOS
- High-speed switching
- No second breakdown

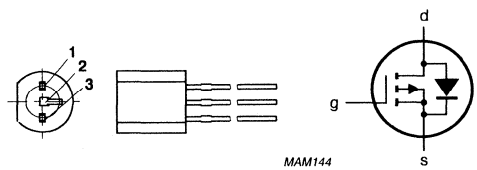
QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	0.3	A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance				
$-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$R_{DS(on)}$	typ.	4,5	Ω
		max.	6	Ω
Transfer admittance				
$-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert Y_{fs} \rvert$	typ.	200	mS

PINNING - TO-92 VARIANT

1 = source
2 = gate
3 = drain

PIN CONFIGURATION



Note: various pinout configurations available.

Fig.1 Simplified outline and symbol.

P-channel enhancement mode vertical D-MOS transistor

BST100

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	0.3	A
Drain current (peak)	$-I_{DM}$	max.	0.8	A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1	W
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

Note

1. Transistor mounted on printed-circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

P-channel enhancement mode vertical D-MOS transistor

BST100

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage				
$-I_D$ = 10 μA; V_{GS} = 0	$-V_{(BR)DSS}$	min.	60	V
Drain-source leakage current				
$-V_{DS}$ = 48 V; V_{GS} = 0	$-I_{DSS}$	max.	1	μA
Gate-source leakage current				
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	max.	100	nA
Gate threshold voltage				
$-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min.	1.5	V
		max.	3.5	V
Drain-source ON-resistance				
$-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$R_{DS(on)}$	typ.	4.5	Ω
		max.	6	Ω
Transfer admittance				
$-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\|Y_{fs}\|$	typ.	200	mS
Input capacitance at f = 1 MHz				
$-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ.	55	pF
		max.	70	pF
Output capacitance at f = 1 MHz				
$-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ.	30	pF
		max.	45	pF
Feedback capacitance at f = 1 MHz				
$-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ.	8	pF
		max.	12	pF
Switching times (see Figs 2 and 3)				
$-I_D$ = 200 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on}	typ.	4	ns
	t_{off}	typ.	20	ns

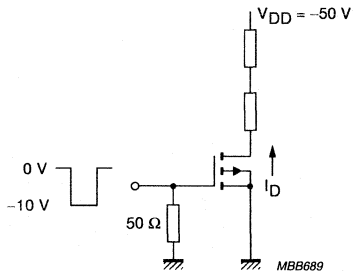


Fig.2 Switching times test circuit.

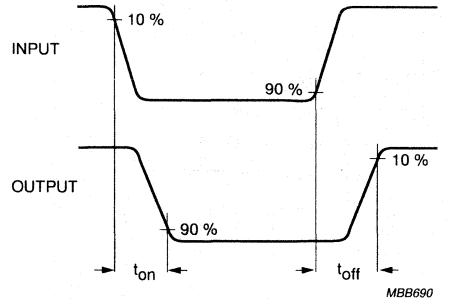


Fig.3 Input and output waveforms.

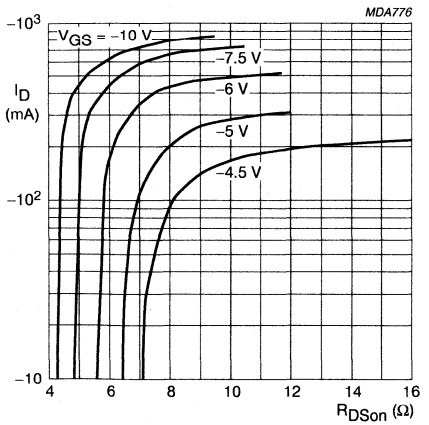


Fig.4 Drain current vs ON-resistance.
T_j = 25 °C; typical values.

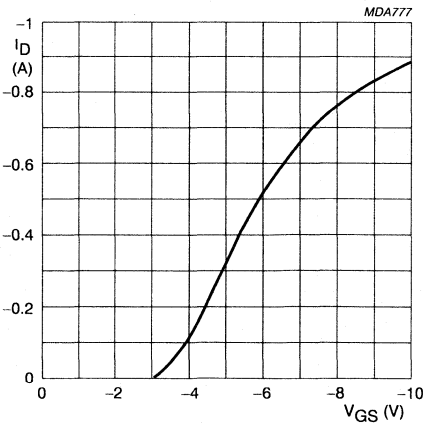


Fig.5 Transfer characteristics.
T_j = 25 °C; $-V_{DS}$ = 10 V; typical values.

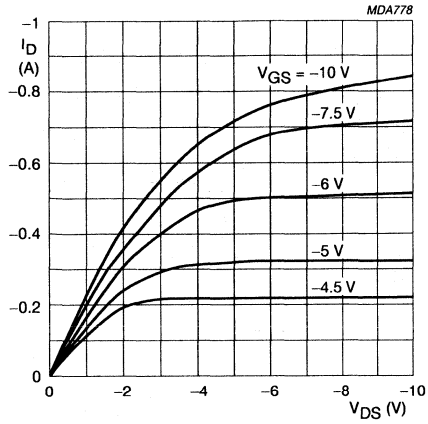


Fig.6 Output characteristics. T_j = 25 °C; typical values.

P-channel enhancement mode vertical D-MOS transistor

BST120

DESCRIPTION

P-channel vertical D-MOS transistor in SOT89 envelope and intended for use in relay, high-speed and line-transformer drivers, using SMD technology.

FEATURES

- Very low $R_{DS(on)}$
- Direct interface to C-MOS
- High-speed switching
- No second breakdown

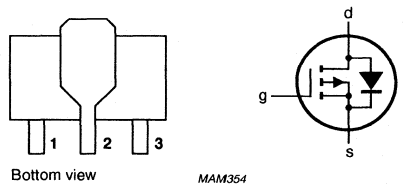
QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	0,3	A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance				
$-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$R_{DS(on)}$	typ.	4,5	Ω
		max.	6	Ω
Transfer admittance				
$-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\|Y_{fs}\|$	typ.	200	mS

PINNING - SOT89

1 = source
2 = drain
3 = gate

PIN CONFIGURATION



marking: LM

Fig.1 Simplified outline and symbol.

P-channel enhancement mode vertical D-MOS transistor

BST120

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.3 A
Drain current (peak)	$-I_{DM}$	max.	0.8 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

Note

1. Transistor mounted on ceramic substrate: area = 2,5 cm^2 and thickness = 0,7 mm.

P-channel enhancement mode vertical D-MOS transistor

BST120

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage				
$-I_D$ = 10 μA; V_{GS} = 0	$-V_{(BR)DSS}$	min.	60	V
Drain-source leakage current				
$-V_{DS}$ = 48 V; V_{GS} = 0	$-I_{DSS}$	max.	1	μA
Gate-source leakage current				
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	max.	100	nA
Gate threshold voltage				
$-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min.	1.5	V
		max.	3.5	V
Drain-source ON-resistance				
$-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$R_{DS(on)}$	typ.	4.5	Ω
		max.	6	Ω
Transfer admittance				
$-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\|Y_{fs}\|$	typ.	200	mS
Input capacitance at f = 1 MHz				
$-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ.	55	pF
		max.	70	pF
Output capacitance at f = 1 MHz				
$-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ.	30	pF
		max.	45	pF
Feedback capacitance at f = 1 MHz				
$-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ.	8	pF
		max.	12	pF
Switching times (see Figs 2 and 3)				
$-I_D$ = 200 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on}	typ.	4	ns
	t_{off}	typ.	20	ns

P-channel enhancement mode vertical D-MOS transistor

BST120

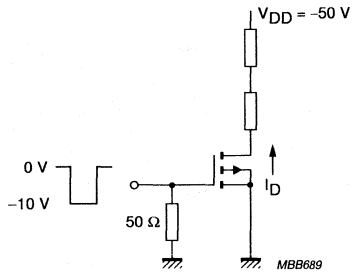


Fig.2 Switching times test circuit.

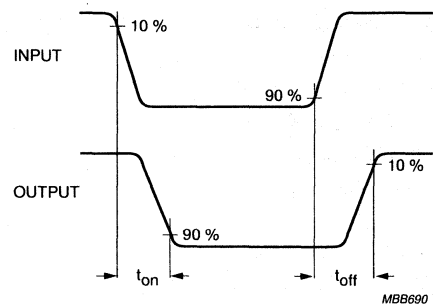


Fig.3 Input and output waveforms.

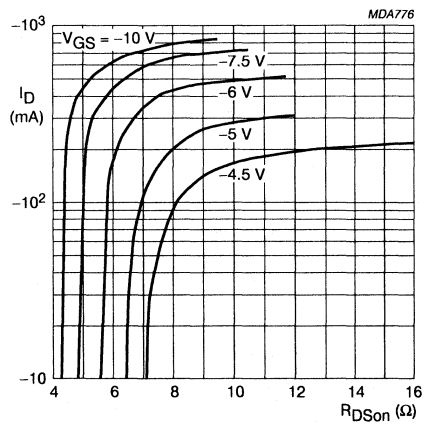


Fig.4 Drain current vs ON-resistance; T_j = 25 °C; typical values.

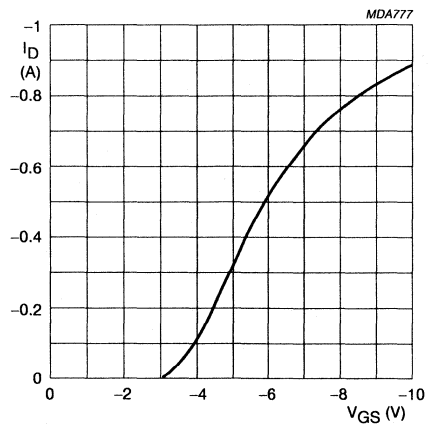


Fig.5 Transfer characteristics; T_j = 25 °C; $-V_{DS}$ = 10 V; typical values.

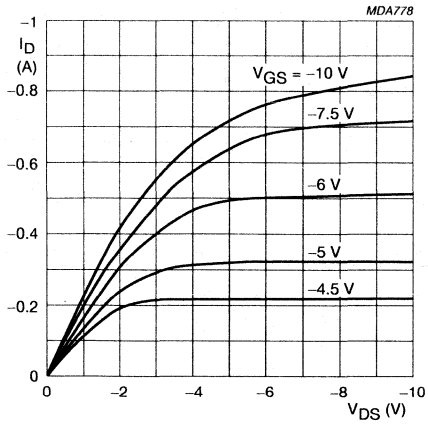


Fig.6 Output characteristics; T_j = 25 °C; typical values.

P-channel enhancement mode vertical D-MOS transistor

BST122

DESCRIPTION

P-channel vertical D-MOS transistor in SOT89 envelope and intended for use in relay, high-speed and line-transformer drivers, using SMD-technology.

FEATURES

- Very low $R_{DS(on)}$
- Direct interface to C-MOS, TTL
- High-speed switching
- No second breakdown

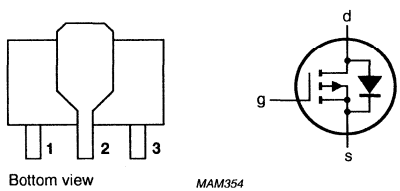
QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	0,25	A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance				
$-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$R_{DS(on)}$	max.	10	Ω
		typ.	7.5	Ω
Transfer admittance				
$-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\|Y_{fs}\|$	typ.	125	mS

PINNING - SOT89

1 = source
2 = drain
3 = gate

PIN CONFIGURATION



Marking: LN

Fig.1 Simplified outline and symbol.

P-channel enhancement mode vertical D-MOS transistor

BST122

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	0.25	A
Drain current (peak)	$-I_{DM}$	max.	0.5	A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Storage temperature range	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

Note

1. Transistor mounted on a ceramic substrate: area = 2,5 cm^2; thickness = 0,7 mm.

P-channel enhancement mode vertical D-MOS transistor

BST122

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage				
$-I_D$ = 10 μA; V_{GS} = 0	$-V_{(BR)DSS}$	min.	60	V
Drain-source leakage current				
$-V_{DS}$ = 48 V; V_{GS} = 0	$-I_{DSS}$	max.	1	μA
Gate-source leakage current				
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	max.	100	nA
Gate threshold voltage				
$-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min.	1.5	V
		max.	3.5	V
Drain-source ON-resistance				
$-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$R_{DS(on)}$	max.	10	Ω
		typ.	7.5	Ω
Transfer admittance				
$-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\|Y_{fs}\|$	typ.	125	mS
Input capacitance at f = 1 MHz				
$-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ.	30	pF
		max.	45	pF
Output capacitance at f = 1 MHz				
$-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ.	20	pF
		max.	30	pF
Feedback capacitance at f = 1 MHz				
$-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ.	5	pF
		max.	10	pF
Switching times (see Figs 2 and 3)				
$-I_D$ = 200 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on}	typ.	4	ns
	t_{off}	typ.	10	ns

P-channel enhancement mode vertical D-MOS transistor

BST122

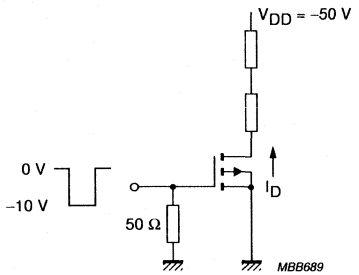


Fig.2 Switching times test circuit.

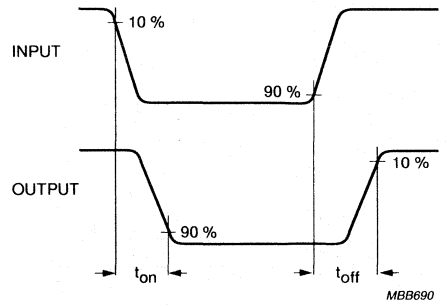


Fig.3 Input and output waveforms.

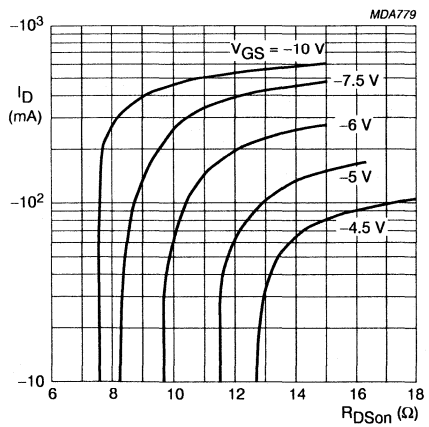


Fig.4 Drain current vs ON-resistance; T_j = 25 °C; typical values.

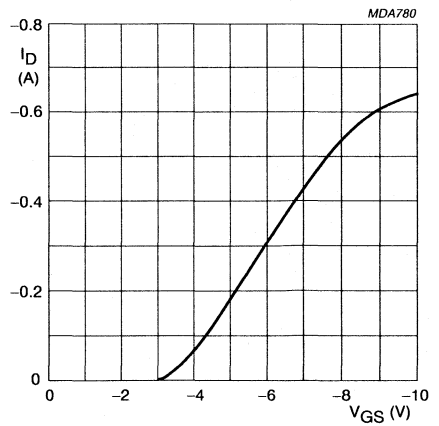


Fig.5 Transfer characteristics; T_j = 25 °C; $-V_{DS}$ = 10 V; typical values.

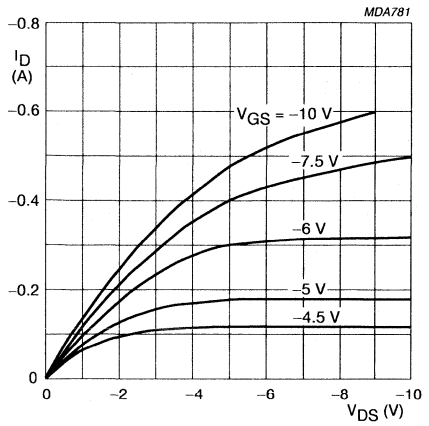


Fig.6 Output characteristics; T_j = 25 °C; typical values.

PowerMOS transistor Logic level TOPFET

BUK100-50DL

For maintenance only. Do not use for design-in.

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 3 pin plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

QUICK REFERENCE DATA

SYMBOL	PARAMETER		MAX.	UNIT
V_{DS}	Continuous drain source voltage		50	V
I_D	Continuous drain current		13.5	A
P_D	Total power dissipation		40	W
T_j	Continuous junction temperature		150	°C
$R_{DS(ON)}$	Drain-source on-state resistance		125	mΩ
I_{ISL}	Input supply current	V_{IS} = 5 V	650	µA

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Lower operating input current permits direct drive by micro-controller
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

FUNCTIONAL BLOCK DIAGRAM

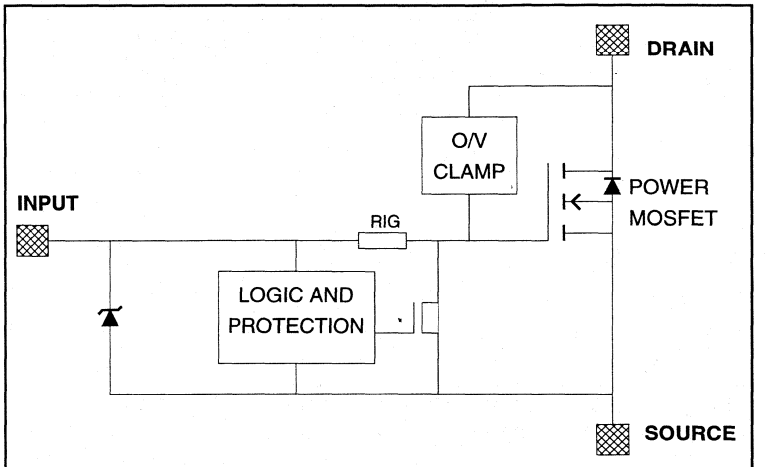
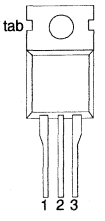


Fig.1. Elements of the TOPFET.

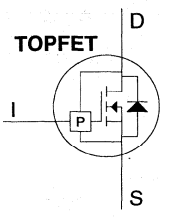
PINNING - TO220AB

PIN	DESCRIPTION
1	input
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Continuous drain source voltage[1]	-	-	50	V
V_{IS}	Continuous input voltage	-	0	6	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; $V_{IS} = 5$ V	-	13.5	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; $V_{IS} = 5$ V	-	8.5	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; $V_{IS} = 5$ V	-	54	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	40	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	4	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	$V_{IS} = 5$ V	-	50	V
	Short circuit load protection[4]				
$V_{DDP(P)}$	Protected drain source supply voltage[5]	$V_{IS} = 5$ V	-	24	V
P_{DSM}	Instantaneous overload dissipation	$T_{mb} = 25$ °C	-	0.6	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	$V_{IS} = 0$ V	-	15	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; $I_{DM} = 15$ A; $V_{DD} \leq 20$ V; inductive load	-	200	mJ
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 95$ °C; $I_{DM} = 8$ A; $V_{DD} \leq 20$ V; f = 250 Hz	-	20	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

5 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than $V_{DDP(P)}$ maximum.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	2.5	3.1	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 1 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V	-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance[1]	V_{IS} = 5 V; I_{DM} = 7.5 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	85	125	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[2]	T_{mb} = 25 °C; L ≤ 10 µH; R_L = 10 mΩ				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 5 V	-	0.2	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 5 V	-	0.8	-	ms
$I_{D(SC)}$	Drain current[3]	V_{DD} = 13 V; V_{IS} = 5 V	-	25	-	A
$I_{DM(SC)}$	Peak drain current[4]	V_{IS} = 5 V; V_{DD} = 13 V	-	60	-	A
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 5 V; from $I_D \geq 1$ A[5]	150	-	-	°C

TRANSFER CHARACTERISTIC

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 7.5 A $t_p \leq 300$ µs; $\delta \leq 0.01$	5	9	-	S

1 Continuous input voltage. The specified pulse width is for the drain current.

2 Refer to OVERLOAD PROTECTION LIMITING VALUES.

3 Continuous drain-source supply voltage. Pulsed input voltage.

4 Continuous input voltage. Momentary short circuit load connection. (The higher peak current is due to the effect of capacitance Cgd).

5 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA		1.0	1.5	2.0	V
I_{IS}	Input supply current	normal operation;	V_{IS} = 5 V	100	200	350	µA
			V_{IS} = 4 V	-	160	270	µA
V_{ISR}	Protection reset voltage[1]		T_j = 25 °C	2.0	2.6	3.5	V
			T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	protection latched;	V_{IS} = 5 V	-	330	650	µA
			V_{IS} = 3.5 V	-	240	430	µA
$V_{(BR)IS}$	Input breakdown voltage	I_I = 10 mA		6	-	-	V
R_{IG}	Input series resistance		T_j = 25 °C	-	33	-	kΩ
	to gate of power MOSFET		T_j = 150 °C	-	50	-	kΩ

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω . Refer to waveform figure and test circuit.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	8	-	µs
t_r	Rise time	resistive load R_L = 4 Ω	-	40	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	40	-	µs
t_f	Fall time	resistive load R_L = 4 Ω	-	35	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq 25$ °C; V_{IS} = 0 V	-	15	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDO}	Forward voltage	I_S = 15 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

1 The input voltage below which the overload protection circuits will be reset.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

NVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

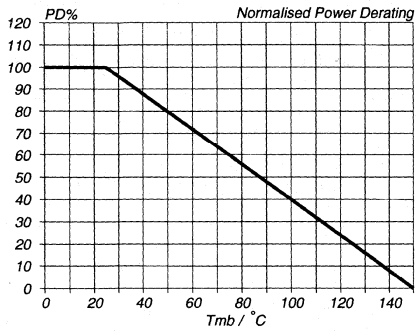


Fig.2. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

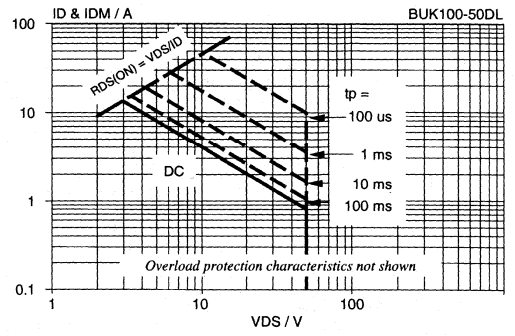


Fig.4. Safe operating area. $T_{mb} = 25\ ^\circ C$
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

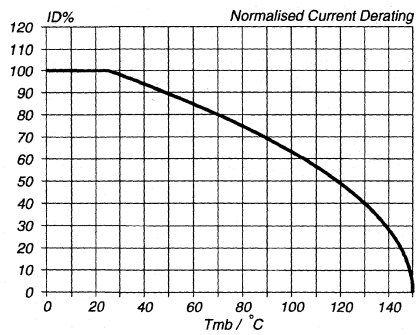


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

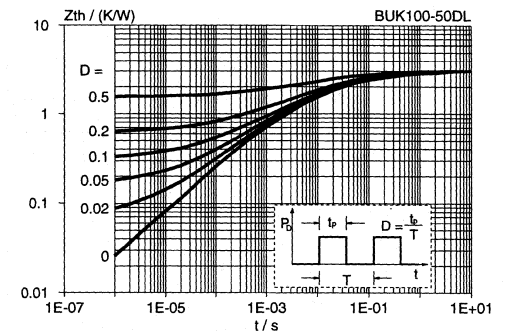


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

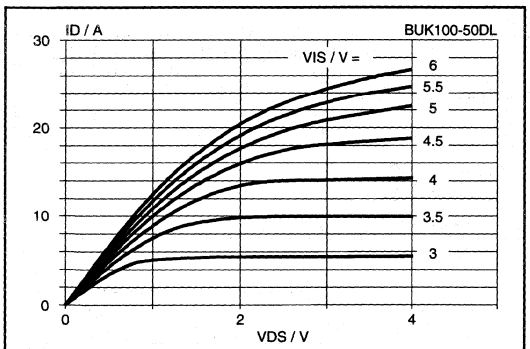


Fig.6. Typical on-state characteristics, T_j = 25 ˚C. ID = f(V_{DS}); parameter V_{IS}; t_p = 2 ms

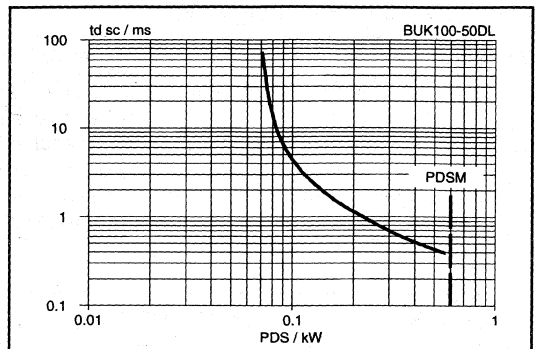


Fig.9. Typical overload protection characteristics. $t_{d\,sc}$ = f(P_{DS}); conditions: $V_{IS} \geq$ 4 V; T_j = 25 ˚C.

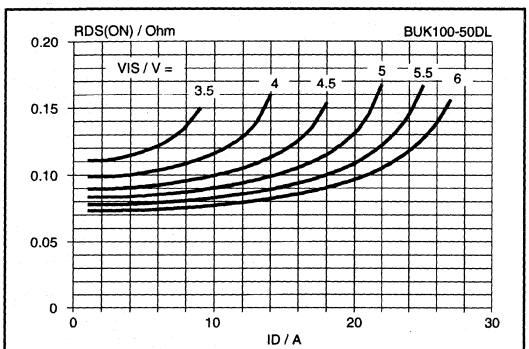


Fig.7. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)}$ = f(I_D); parameter V_{IS}; t_p = 2 ms

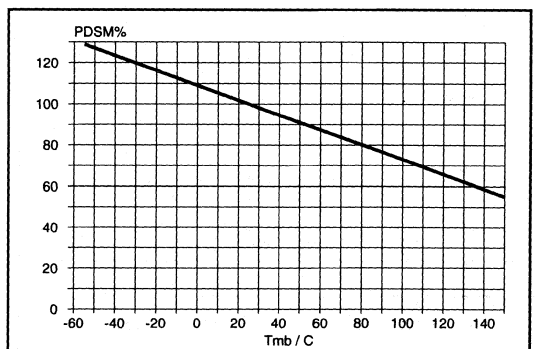


Fig.10. Normalised limiting overload dissipation. P_{DSM}% =100·P_{DSM}/P_{DSM}(25 ˚C) = f(T_{mb})

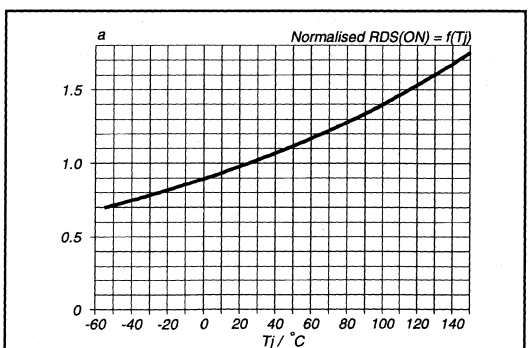


Fig.8. Normalised drain-source on-state resistance. a = $R_{DS(ON)}$/$R_{DS(ON)}$25 ˚C = f(T_j); I_D = 7.5 A; V_{IS} = 5 V

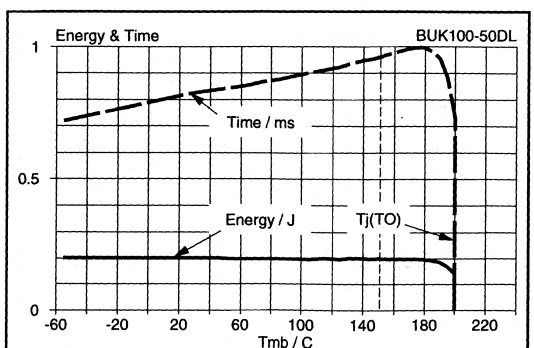


Fig.11. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; V_{IS} = 5 V; SC load = 30 mΩ

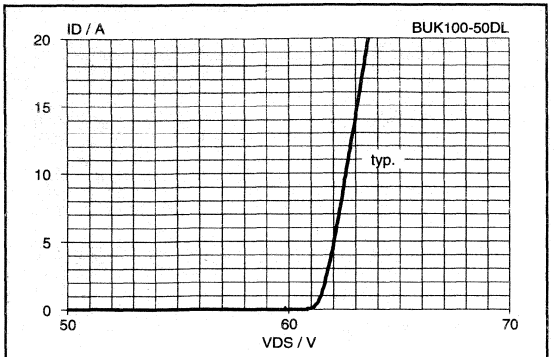


Fig.12. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: $V_{IS} = 0$ V; $t_p \leq 50$ µs

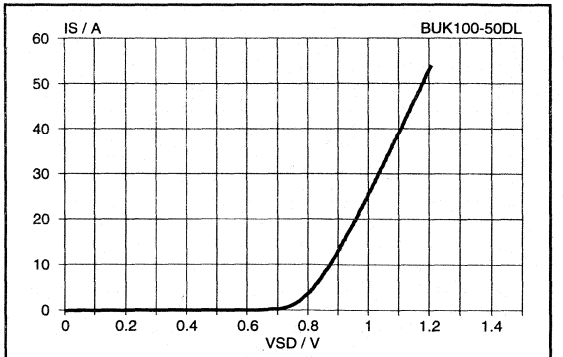


Fig.15. Typical reverse diode current, $T_j = 25$ °C. $I_S = f(V_{SDS})$; conditions: $V_{IS} = 0$ V; $t_p = 250$ µs

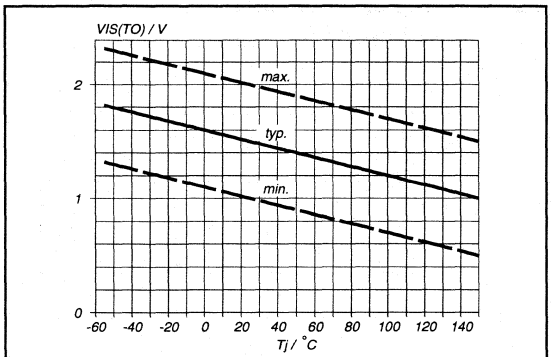


Fig.13. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = 5$ V

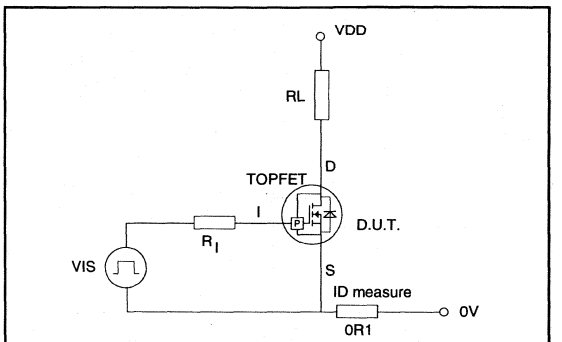


Fig.16. Test circuit for resistive load switching times.

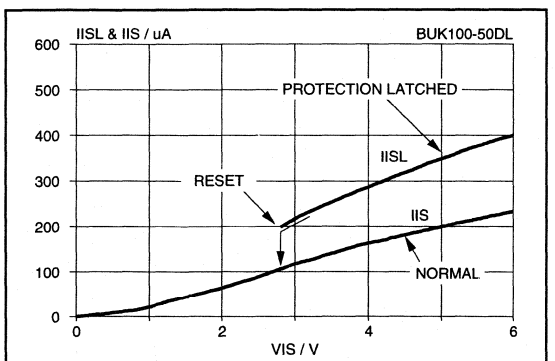


Fig.14. Typical DC input characteristics, $T_j = 25$ °C. I_{ISL} & $I_{IS} = f(V_{IS})$; protection latched & normal operation

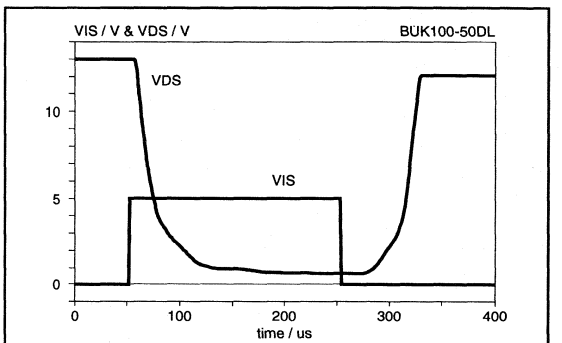


Fig.17. Typical switching waveforms, resistive load. $V_{DD} = 13$ V; $R_L = 4\ \Omega$; $R_I = 50\ \Omega$, $T_j = 25$ °C.

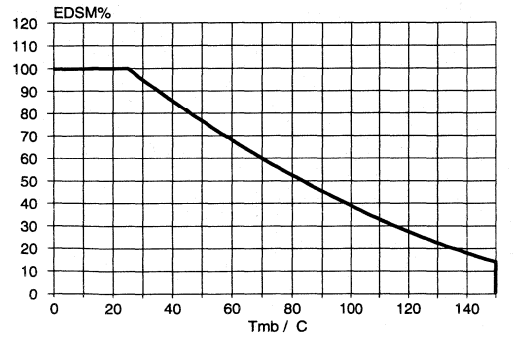


Fig.18. Normalised limiting clamping energy. $E_{DSM}\% = f(T_{mb})$; conditions: I_D = 15 A; V_{IS} = 5 V

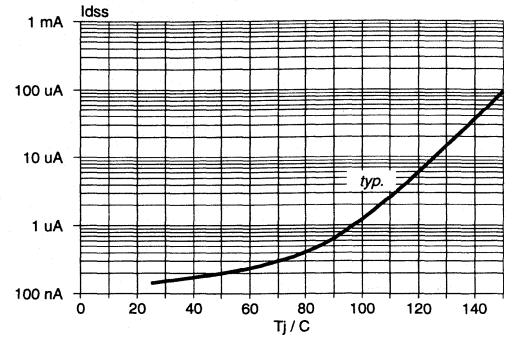


Fig.20. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

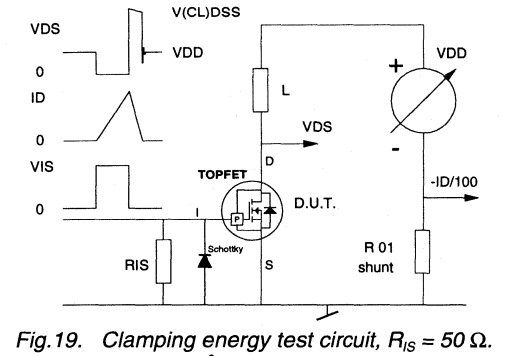


Fig.19. Clamping energy test circuit, R_{IS} = 50 Ω.

$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$$

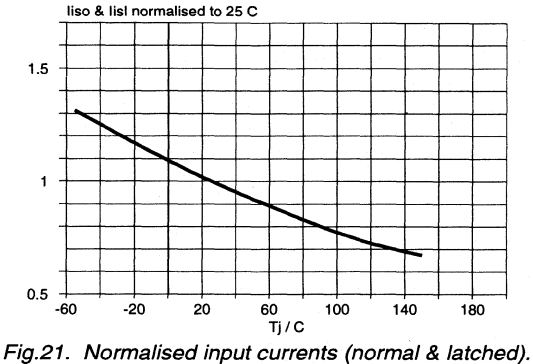


Fig.21. Normalised input currents (normal & latched). $I_{ISO}/I_{ISO}25^{\circ}C$ & $I_{ISL}/I_{ISL}25^{\circ}C = f(T_j)$; V_{IS} = 5 V

PowerMOS transistor Logic level TOPFET

BUK100-50GL

For maintenance only. Do not use for design-in.

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 3 pin plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Low operating input current
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	13.5	A
P_D	Total power dissipation	40	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{IS} = 5 V	125	mΩ

FUNCTIONAL BLOCK DIAGRAM

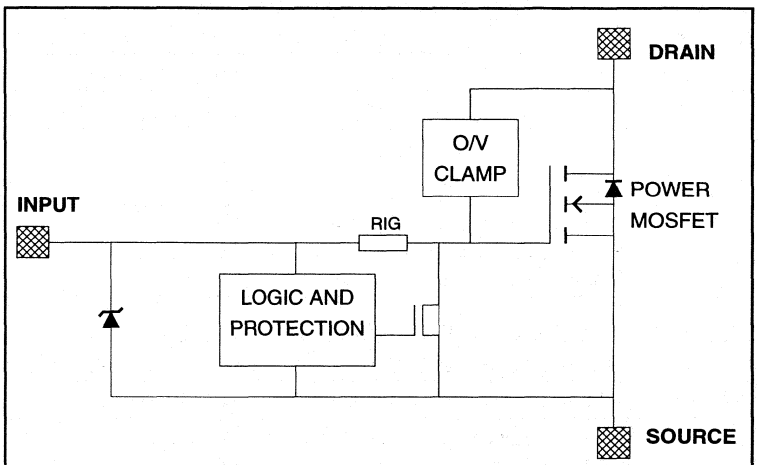
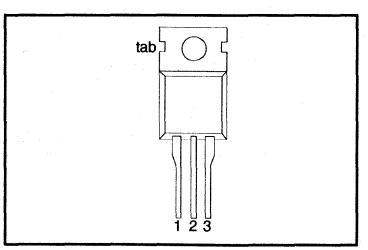


Fig.1. Elements of the TOPFET.

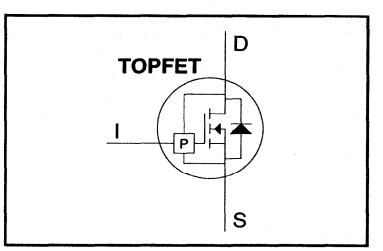
PINNING - TO220AB

PIN	DESCRIPTION
1	input
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Continuous off-state drain source voltage[1]	V_{IS} = 0 V	-	50	V
V_{IS}	Continuous input voltage	-	0	6	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; V_{IS} = 5 V	-	13.5	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; V_{IS} = 5 V	-	8.5	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; V_{IS} = 5 V	-	54	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	40	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	4	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 5 V	-	50	V
	Short circuit load protection				
$V_{DDP(P)}$	Protected drain source supply voltage[4]	V_{IS} = 5 V	-	35	V
P_{DSM}	Instantaneous overload dissipation	T_{mb} = 25 °C	-	0.6	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	V_{IS} = 0 V	-	15	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; I_{DM} = 15 A; $V_{DD} \leq 20$ V; inductive load	-	200	mJ
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 95$ °C; I_{DM} = 4 A; $V_{DD} \leq 20$ V; f = 250 Hz	-	20	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	2.5	3.1	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 1 A; $t_p \le 300\ \mu s$; $\delta \le 0.01$	-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V	-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{IS} = 5 V; I_{DM} = 7.5 A; $t_p \le 300\ \mu s$; $\delta \le 0.01$	-	85	125	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	T_{mb} = 25 °C; L ≤ 10 µH				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 5 V	-	0.2	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 5 V	-	0.8	-	ms
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 5 V; from $I_D \ge 1$ A[2]	150	-	-	°C

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA	1.0	1.5	2.0	V
I_{IS}	Input supply current	V_{IS} = 5 V; normal operation	-	0.2	0.35	mA
V_{ISR}	Protection reset voltage[3]		2.0	2.6	3.5	V
V_{ISR}	Protection reset voltage	T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	V_{IS} = 5 V; protection latched	0.5	1.2	2.0	mA
$V_{(BR)IS}$	Input clamp voltage	I_I = 10 mA	6	-	-	V
R_{IG}	Input series resistance	to gate of power MOSFET	-	4	-	kΩ

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum. Refer to OVERLOAD PROTECTION LIMITING VALUES.

2 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

3 The input voltage below which the overload protection circuits will be reset.

TRANSFER CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 7.5 A $t_p \leq$ 300 µs; $\delta \leq 0.01$	5	9	-	S
$I_{D(SC)}$	Drain current[1]	V_{DS} = 13 V; V_{IS} = 5 V	-	25	-	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω. Refer to waveform figures and test circuits.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	1.5	-	µs
t_r	Rise time	resistive load R_L = 4 Ω	-	8	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	6	-	µs
t_f	Fall time	resistive load R_L = 4 Ω	-	4.5	-	µs
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	1.5	-	µs
t_r	Rise time	inductive load I_{DM} = 3 A	-	1	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	10	-	µs
t_f	Fall time	inductive load I_{DM} = 3 A	-	0.5	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq$ 25 °C; V_{IS} = 0 V	-	13.5	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	I_S = 15 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

1 During overload before short circuit load protection operates.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

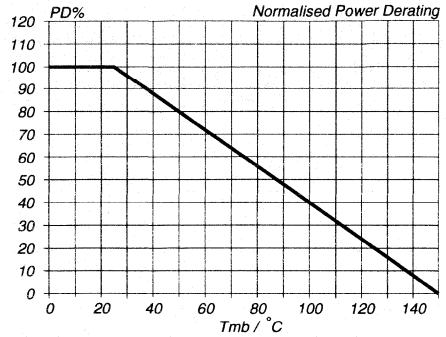


Fig.2. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

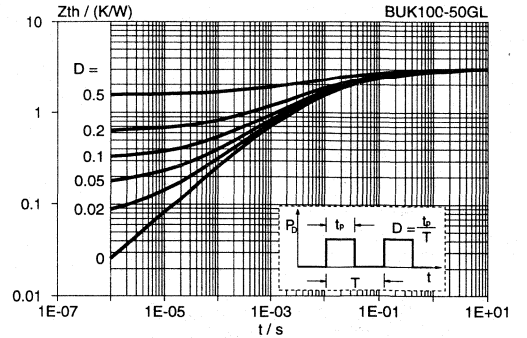


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

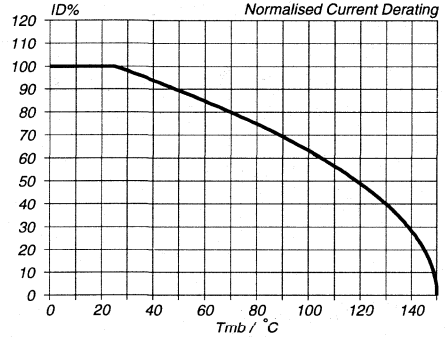


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

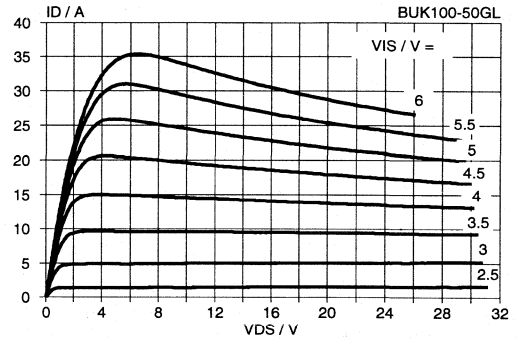


Fig.6. Typical output characteristics, $T_j = 25$ °C.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250$ µs & $t_p < t_{d\,sc}$

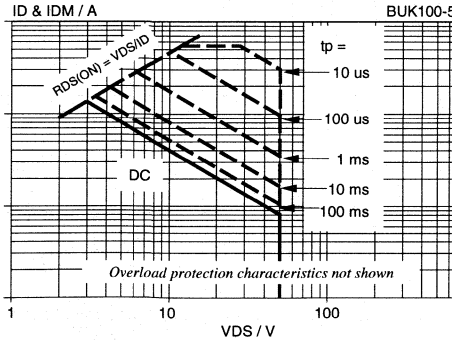


Fig.4. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

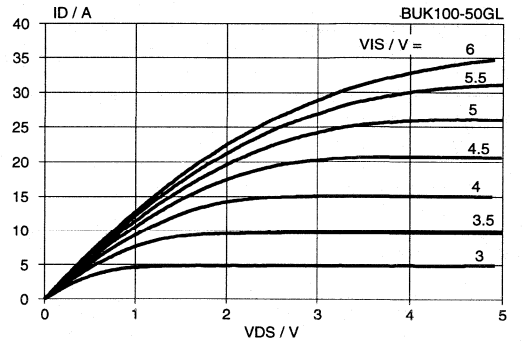


Fig.7. Typical on-state characteristics, $T_j = 25$ °C.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250$ µs

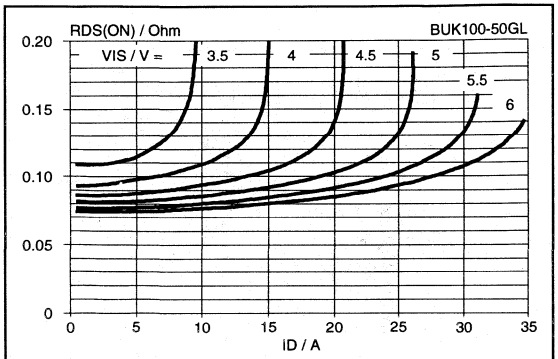


Fig.8. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

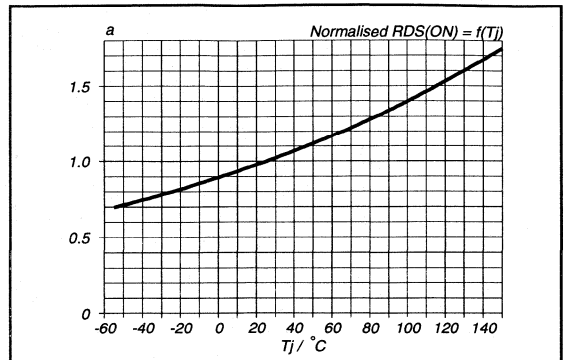


Fig.11. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25$ °C = $f(T_j)$; I_D = 7.5 A; V_{IS} = 5 V

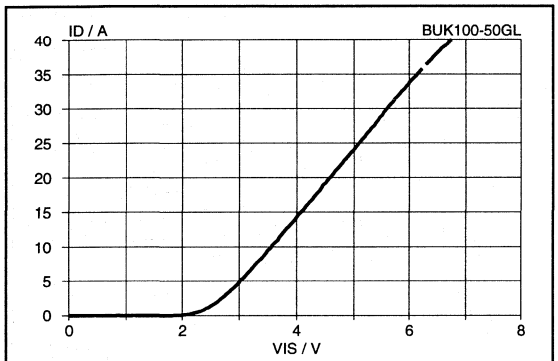


Fig.9. Typical transfer characteristics, T_j = 25 °C. $I_D = f(V_{IS})$; conditions: V_{DS} = 10 V; t_p = 250 µs

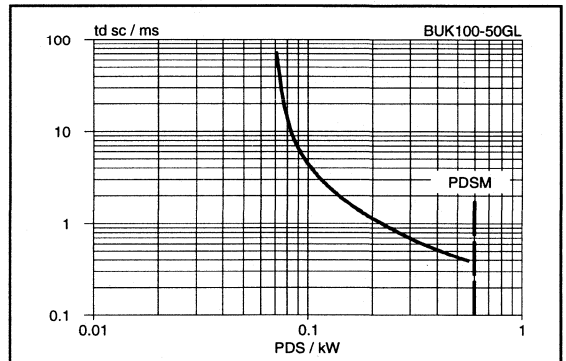


Fig.12. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{IS} \geq 4$ V; T_j = 25 °C.

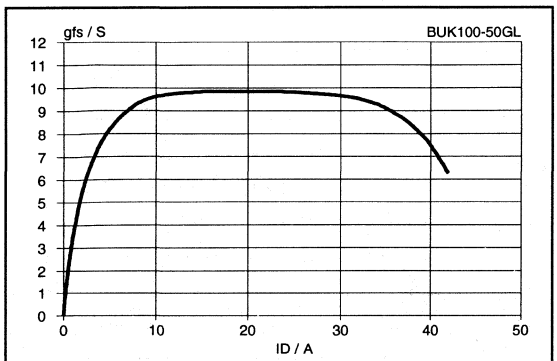


Fig.10. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V; t_p = 250 µs

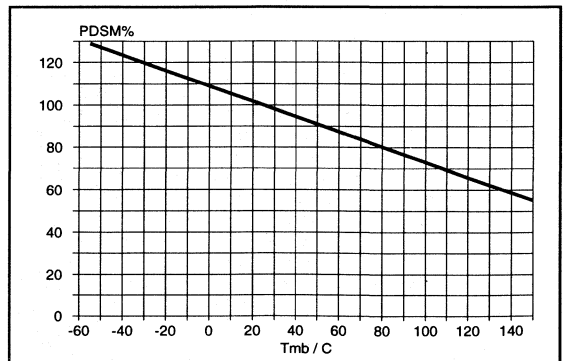


Fig.13. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ °C) = f(T_{mb})$

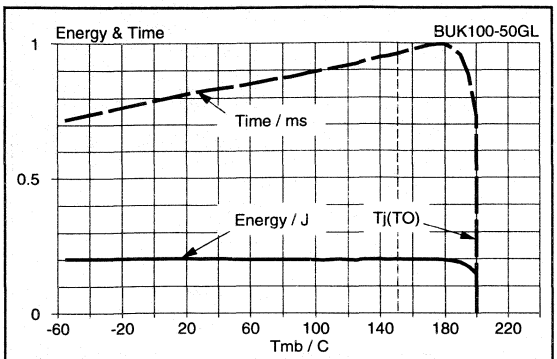


Fig.14. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; V_{IS} = 5 V; SC load = 30 mΩ

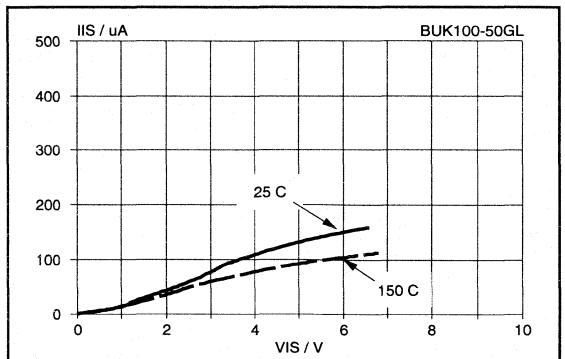


Fig.17. Typical DC input characteristics. $I_{IS} = f(V_{IS})$; normal operation, parameter: T_j

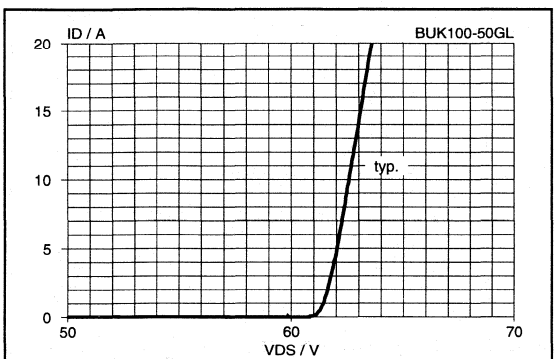


Fig.15. Typical clamping characteristics, 25 ˚C. $I_D = f(V_{DS})$; conditions: V_{IS} = 0 V; $t_p \leq 50$ µs

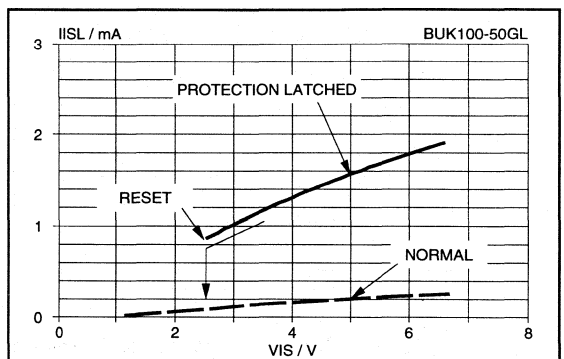


Fig.18. Typical DC input characteristics, T_j = 25 ˚C. $I_{ISL} = f(V_{IS})$; overload protection operated ⇒ I_D = 0 A

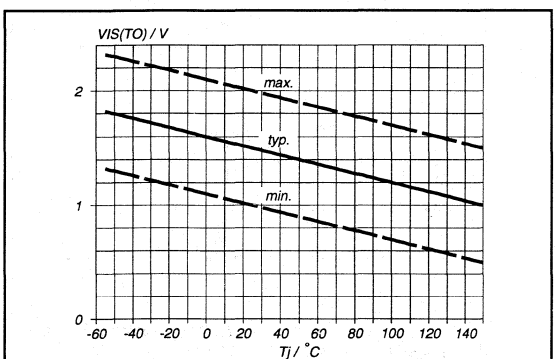


Fig.16. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

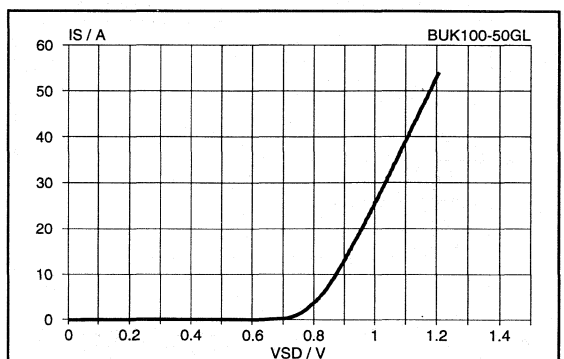


Fig.19. Typical reverse diode current, T_j = 25 ˚C. $I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V; t_p = 250 µs

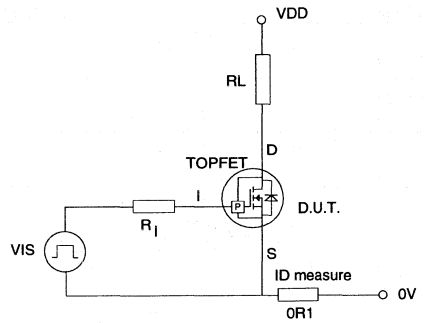


Fig.20. Test circuit for resistive load switching times.

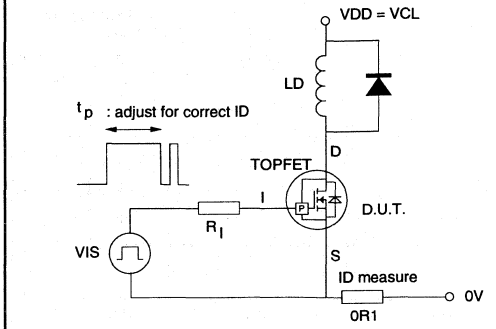


Fig.23. Test circuit for inductive load switching times.

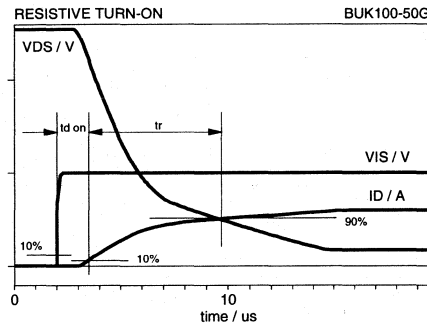


Fig.21. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 4 Ω; R_I = 50 Ω, T_j = 25 °C.

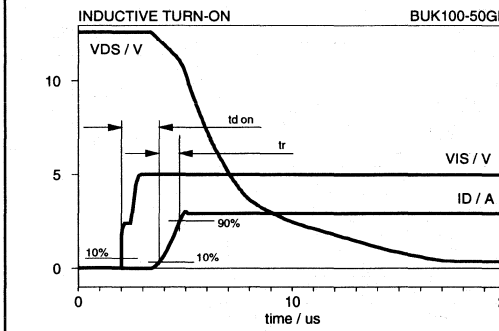


Fig.24. Typical switching waveforms, inductive load. V_{DD} = 13 V; I_D = 3 A; R_I = 50 Ω, T_j = 25 °C.

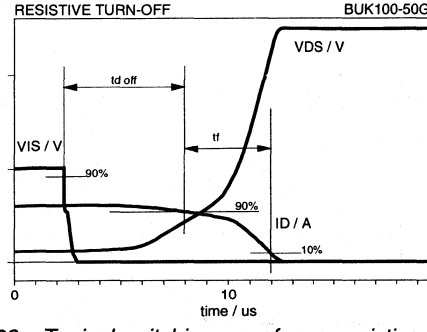


Fig.22. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 4 Ω; R_I = 50 Ω, T_j = 25 °C.

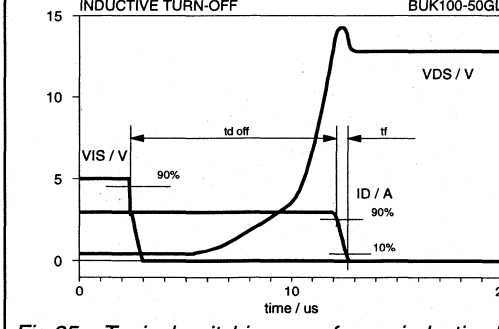


Fig.25. Typical switching waveforms, inductive load. V_{DD} = 13 V; I_D = 3 A; R_I = 50 Ω, T_j = 25 °C.

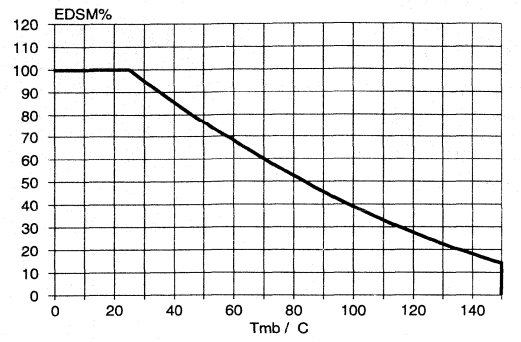


Fig.26. Normalised limiting clamping energy. $E_{DSM}\% = f(T_{mb})$; conditions: I_D = 15 A; V_{IS} = 5 V

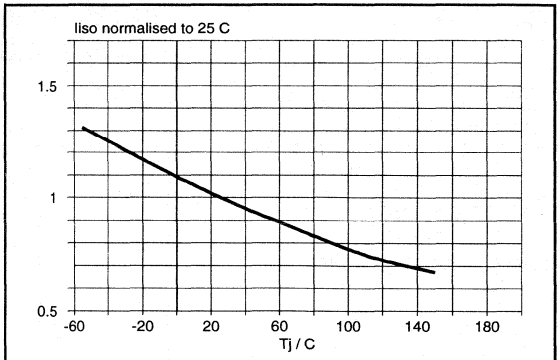


Fig.29. Normalised input current (normal operation). $I_{IS}/I_{IS}25\ ^{\circ}C = f(T_j)$; V_{IS} = 5 V

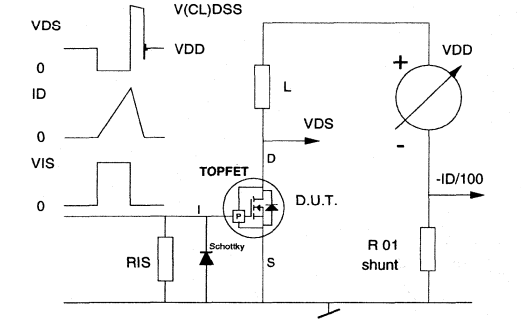


Fig.27. Clamping energy test circuit, R_{IS} = 50 Ω.
$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$

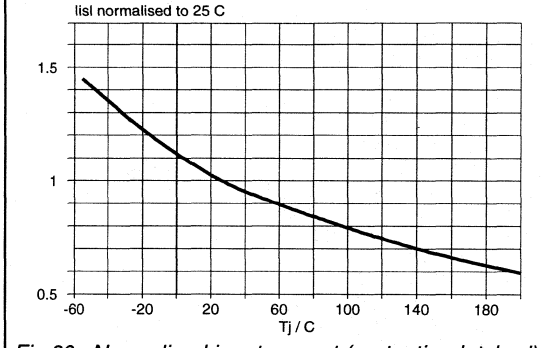


Fig.30. Normalised input current (protection latched). $I_{ISL}/I_{ISL}25\ ^{\circ}C = f(T_j)$; V_{IS} = 5 V

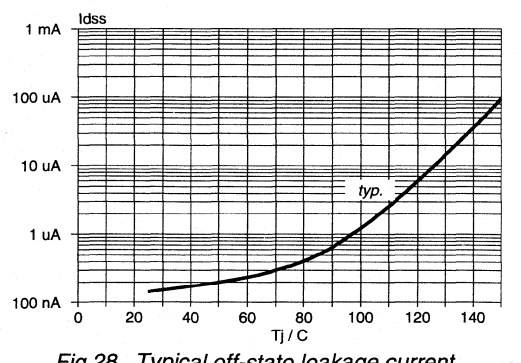


Fig.28. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

PowerMOS transistor Logic level TOPFET

BUK101-50DL

For maintenance only. Do not use for design-in.

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 3 pin plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Lower operating input current permits direct drive by micro-controller
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER		MAX.	UNIT
V_{DS}	Continuous drain source voltage		50	V
I_D	Continuous drain current		26	A
P_D	Total power dissipation		75	W
T_j	Continuous junction temperature		150	°C
$R_{DS(ON)}$	Drain-source on-state resistance		60	mΩ
I_{ISL}	Input supply current	V_{IS} = 5 V	650	µA

FUNCTIONAL BLOCK DIAGRAM

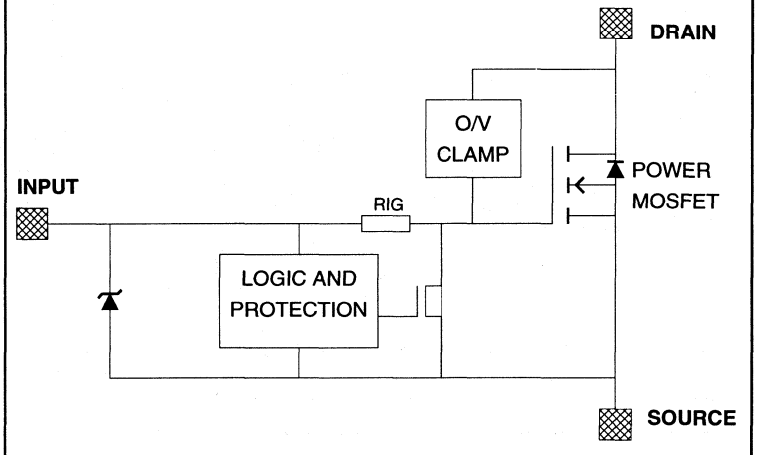
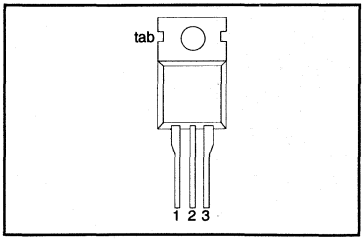


Fig.1. Elements of the TOPFET.

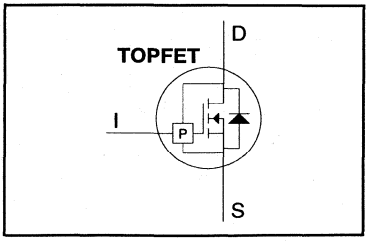
PINNING - TO220AB

PIN	DESCRIPTION
1	input
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Continuous drain source voltage[1]	-	-	50	V
V_{IS}	Continuous input voltage	-	0	6	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; $V_{IS} = 5$ V	-	26	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; $V_{IS} = 5$ V	-	16	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; $V_{IS} = 5$ V	-	100	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	75	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	4	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	$V_{IS} = 5$ V	-	50	V
	Short circuit load protection[4]				
$V_{DDP(P)}$	Protected drain source supply voltage[5]	$V_{IS} = 5$ V	-	20	V
P_{DSM}	Instantaneous overload dissipation	$T_{mb} = 25$ °C	-	1.3	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	$V_{IS} = 0$ V	-	26	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; $I_{DM} = 26$ A; $V_{DD} \leq 20$ V; inductive load	-	625	mJ
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 95$ °C; $I_{DM} = 8$ A; $V_{DD} \leq 20$ V; f = 250 Hz	-	40	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

5 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than $V_{DDP(P)}$ maximum.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	1.3	1.67	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 2 A; $t_p \le 300$ µs; $\delta \le 0.01$	-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V	-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance[1]	V_{IS} = 5 V; I_{DM} = 13 A; $t_p \le 300$ µs; $\delta \le 0.01$	-	45	60	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[2]	T_{mb} = 25 °C; L ≤ 10 µH; R_L = 10 mΩ				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 5 V	-	0.4	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 5 V	-	0.8	-	ms
$I_{D(SC)}$	Drain current[3]	V_{DD} = 13 V; V_{IS} = 5 V	-	45	-	A
$I_{DM(SC)}$	Peak drain current[4]	V_{IS} = 5 V; V_{DD} = 13 V	-	105	-	A
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 5 V; from $I_D \ge 1$ A[5]	150	-	-	°C

TRANSFER CHARACTERISTIC

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 13 A $t_p \le 300$ µs; $\delta \le 0.01$	10	16	-	S

1 Continuous input voltage. The specified pulse width is for the drain current.

2 Refer to OVERLOAD PROTECTION LIMITING VALUES.

3 Continuous drain-source supply voltage. Pulsed input voltage.

4 Continuous input voltage. Momentary short circuit load connection. (The higher peak current is due to the effect of capacitance Cgd).

5 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA		1.0	1.5	2.0	V
I_{IS}	Input supply current	normal operation;	V_{IS} = 5 V	100	200	350	µA
			V_{IS} = 4 V	-	160	270	µA
V_{ISR}	Protection reset voltage[1]		T_j = 25 °C	2.0	2.6	3.5	V
			T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	protection latched;	V_{IS} = 5 V	-	330	650	µA
			V_{IS} = 3.5 V	-	240	430	µA
$V_{(BR)IS}$	Input breakdown voltage	I_I = 10 mA		6	-	-	V
R_{IG}	Input series resistance		T_j = 25 °C	-	33	-	kΩ
	to gate of power MOSFET		T_j = 150 °C	-	50	-	kΩ

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω. Refer to waveform figure and test circuit.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	17	-	µs
t_r	Rise time	resistive load R_L = 2.1 Ω	-	75	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	60	-	µs
t_f	Fall time	resistive load R_L = 2.1 Ω	-	70	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq 25$ °C; V_{IS} = 0 V	-	26	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDO}	Forward voltage	I_S = 26 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

1 The input voltage below which the overload protection circuits will be reset.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

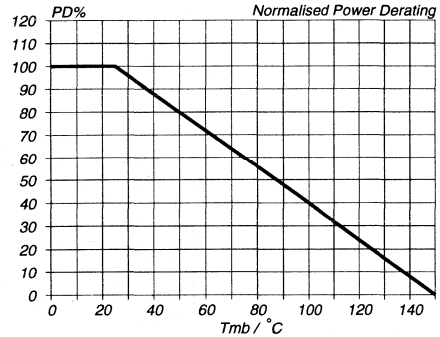


Fig.2. Normalised power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

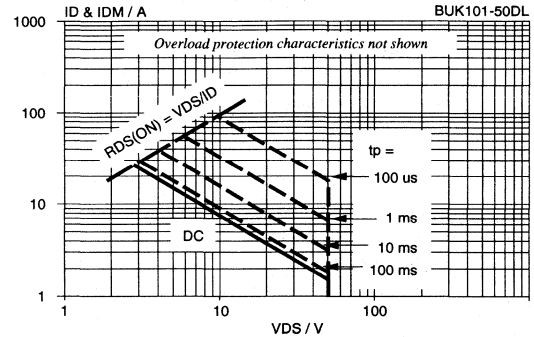


Fig.4. Safe operating area. T_{mb} = 25 °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

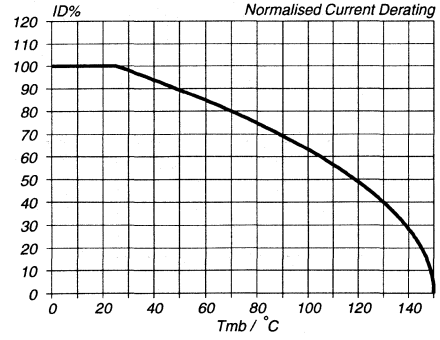


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: V_{IS} = 5 V

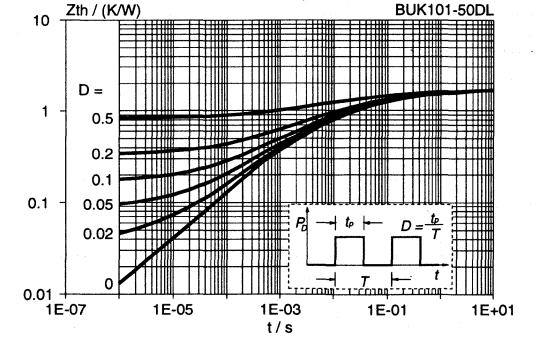


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

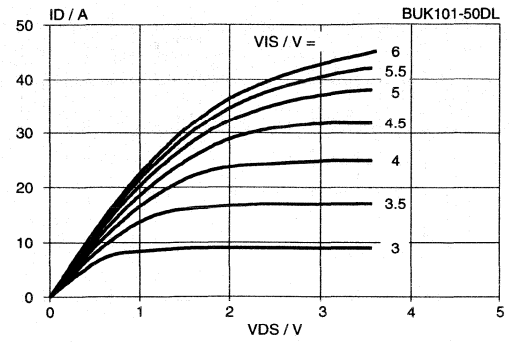


Fig.6. Typical on-state characteristics, T_j = 25 ˚C. ID = f(V_{DS}); parameter V_{IS}; t_p = 2 ms

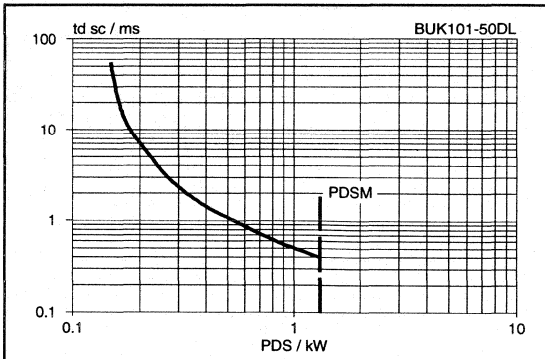


Fig.9. Typical overload protection characteristics. $t_{d\,sc}$ = f(P_{DS}); conditions: $V_{IS} \geq$ 4 V; T_j = 25 ˚C.

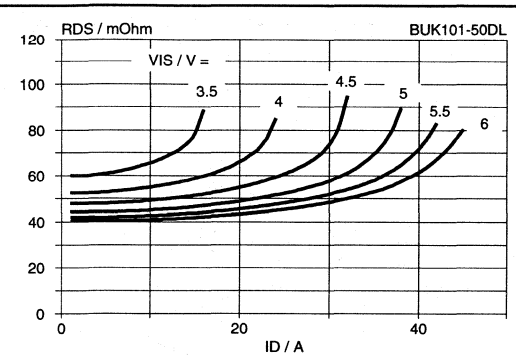


Fig.7. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)}$ = f(I_D); parameter V_{IS}; t_p = 2 ms

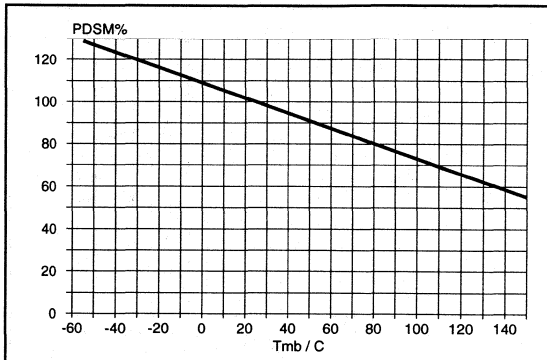


Fig.10. Normalised limiting overload dissipation. P_{DSM}% =100·P_{DSM}/P_{DSM}(25 ˚C) = f(T_{mb})

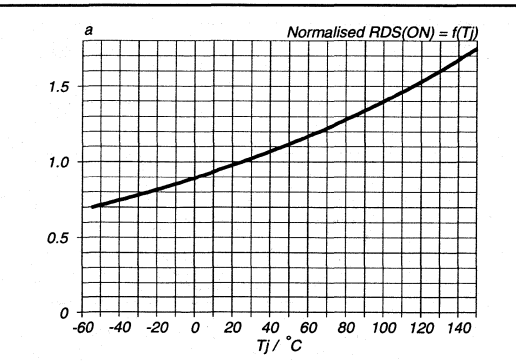


Fig.8. Normalised drain-source on-state resistance. a = $R_{DS(ON)}$/$R_{DS(ON)}$25 ˚C = f(T_j); I_D = 13 A; V_{IS} = 5 V

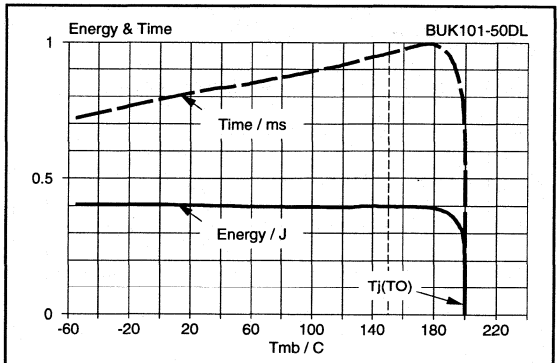


Fig.11. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; V_{IS} = 5 V; SC load = 30 mΩ

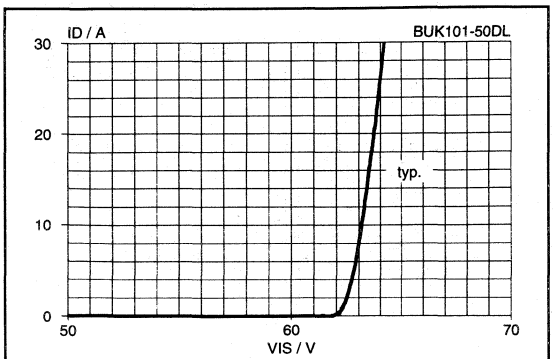


Fig.12. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: $V_{IS} = 0$ V; $t_p \leq 50$ µs

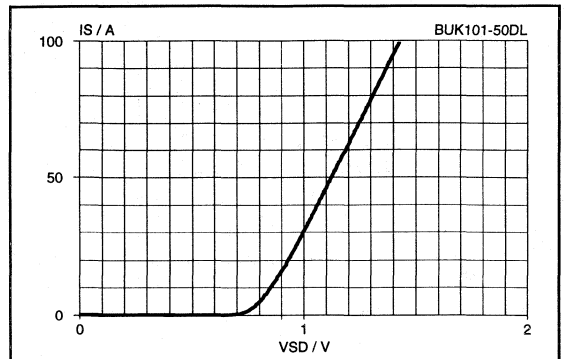


Fig.15. Typical reverse diode current, $T_j = 25$ °C. $I_S = f(V_{SDS})$; conditions: $V_{IS} = 0$ V

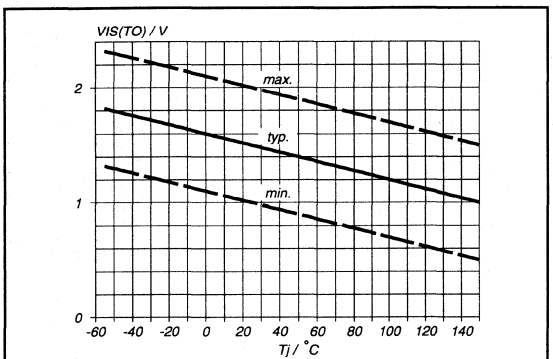


Fig.13. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = 5$ V

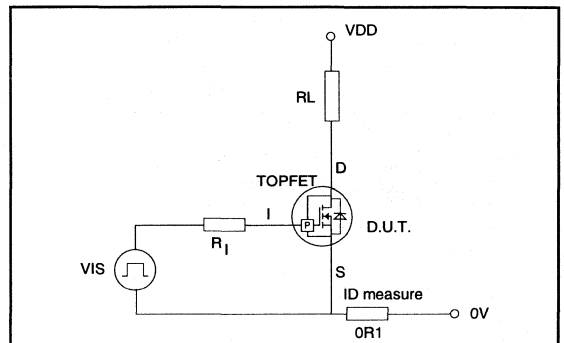


Fig.16. Test circuit for resistive load switching times.

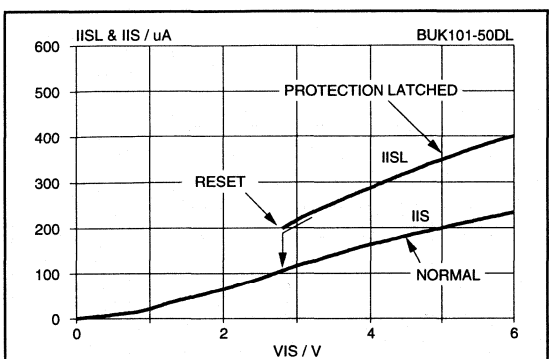


Fig.14. Typical DC input characteristics, $T_j = 25$ °C. I_{ISL} & $I_{IS} = f(V_{IS})$; protection latched & normal operation

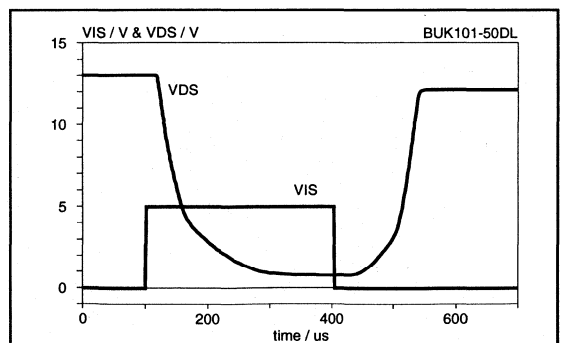


Fig.17. Typical switching waveforms, resistive load. $V_{DD} = 13$ V; $R_L = 2.1$ Ω; $R_I = 50$ Ω, $T_j = 25$ °C.

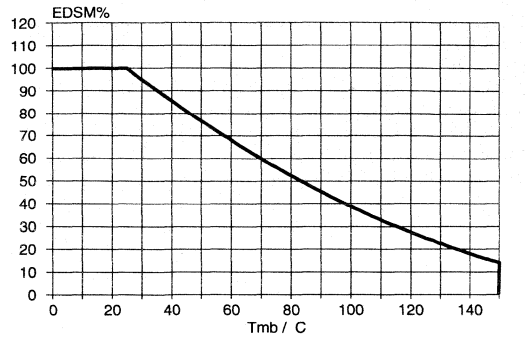


Fig.18. Normalised clamping energy rating. $E_{DSM}\% = f(T_{mb})$; conditions: I_D = 26 A; V_{IS} = 5 V

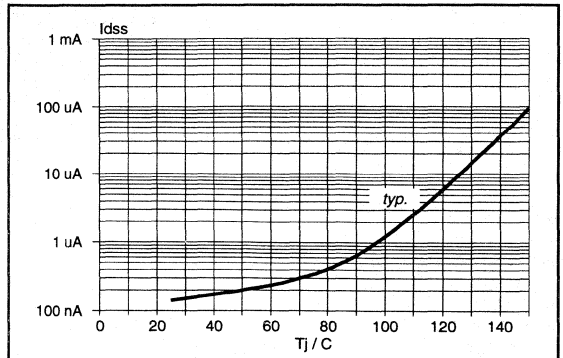


Fig.20. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

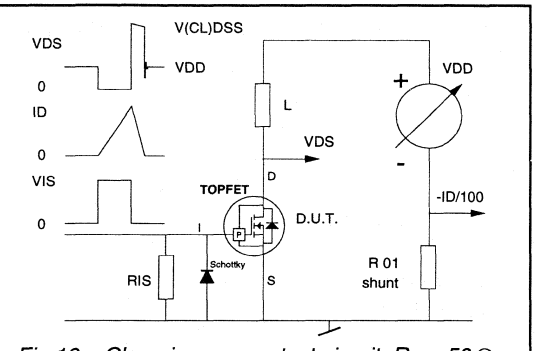


Fig.19. Clamping energy test circuit, R_{IS} = 50 Ω.

$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$$

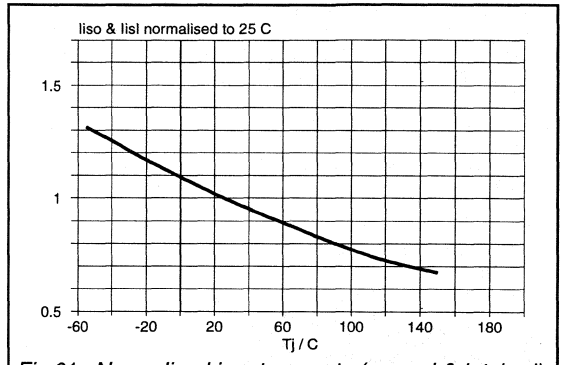


Fig.21. Normalised input currents (normal & latched). $I_{ISO}/I_{ISO}25^{\circ}C$ & $I_{ISL}/I_{ISL}25^{\circ}C = f(T_j)$; V_{IS} = 5 V

PowerMOS transistor Logic level TOPFET

BUK101-50GL

For maintenance only. Do not use for design-in.

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 3 pin plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Low operating input current
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	26	A
P_D	Total power dissipation	75	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{IS} = 5 V	60	mΩ

FUNCTIONAL BLOCK DIAGRAM

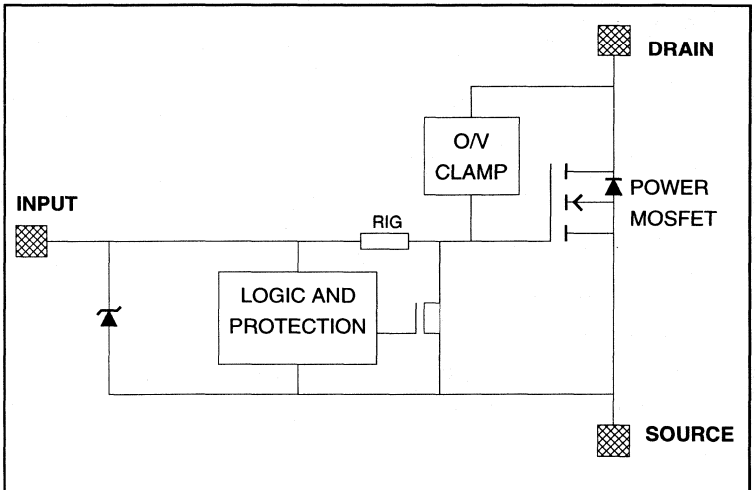
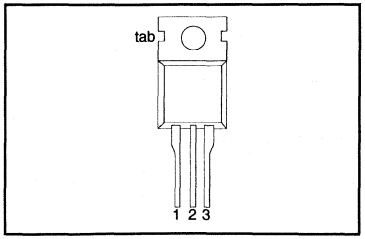


Fig.1. Elements of the TOPFET.

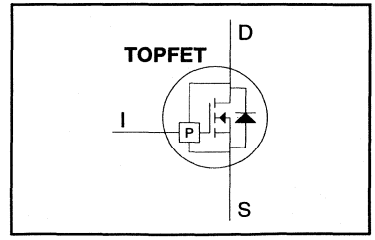
PINNING - TO220AB

PIN	DESCRIPTION
1	input
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Continuous off-state drain source voltage	V_{IS} = 0 V	-	50	V
V_{IS}	Continuous input voltage	-	0	6	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; V_{IS} = 5 V	-	26	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; V_{IS} = 5 V	-	16	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; V_{IS} = 5 V	-	100	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	75	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[1]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[2]	for valid protection	4	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 5 V	-	50	V
	Short circuit load protection				
$V_{DDP(P)}$	Protected drain source supply voltage[3]	V_{IS} = 5 V	-	35	V
P_{DSM}	Instantaneous overload dissipation	T_{mb} = 25 °C	-	1.3	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	V_{IS} = 0 V	-	26	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; I_{DM} = 26 A; $V_{DD} \leq 20$ V; inductive load	-	625	mJ
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 95$ °C; I_{DM} = 8 A; $V_{DD} \leq 20$ V; f = 250 Hz	-	40	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

2 The input voltage for which the overload protection circuits are functional.

3 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	1.3	1.67	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 2 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V	-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{IS} = 5 V; I_{DM} = 13 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	45	60	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	T_{mb} = 25 °C; L ≤ 10 µH				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 5 V	-	0.4	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 5 V	-	0.8	-	ms
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 5 V; from $I_D \geq 1$ A[2]	150	-	-	°C

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA	1.0	1.5	2.0	V
I_{IS}	Input supply current	V_{IS} = 5 V; normal operation	-	0.2	0.35	mA
V_{ISR}	Protection reset voltage[3]		2.0	2.6	3.5	V
V_{ISR}	Protection reset voltage	T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	V_{IS} = 5 V; protection latched	0.5	1.2	2.0	mA
$V_{(BR)IS}$	Input clamp voltage	I_I = 10 mA	6	7	-	V
R_{IG}	Input series resistance	to gate of power MOSFET	-	4	-	kΩ

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum. Refer to OVERLOAD PROTECTION LIMITING VALUES.

2 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

3 The input voltage below which the overload protection circuits will be reset.

TRANSFER CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 13 A $t_p \leq$ 300 µs; $\delta \leq 0.01$	10	16	-	S
$I_{D(SC)}$	Drain current[1]	V_{DS} = 13 V; V_{IS} = 5 V	-	40	-	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω. Refer to waveform figures and test circuits.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	2.5	-	µs
t_r	Rise time	resistive load R_L = 2.1 Ω	-	15	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	10	-	µs
t_f	Fall time	resistive load R_L = 2.1 Ω	-	7	-	µs
$t_{d\,on}$	Turn-on delay time	V_{DD} = 10 V; V_{IS} = 5 V	-	2	-	µs
t_r	Rise time	inductive load I_{DM} = 6 A	-	4	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 10 V; V_{IS} = 0 V	-	15	-	µs
t_f	Fall time	inductive load I_{DM} = 6 A	-	1	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq$ 25 °C	-	26	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	I_S = 26 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

1 During overload before short circuit load protection operates.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

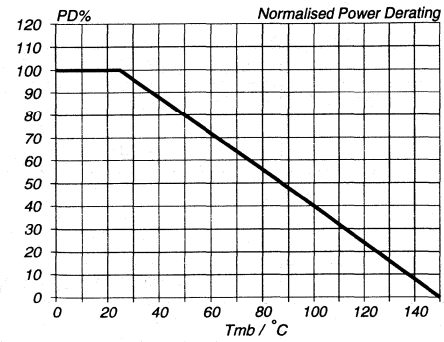


Fig.2. Normalised power dissipation.
$P_D\% = 100 \cdot P_D / P_D(25\ ^\circ C) = f(T_{mb})$

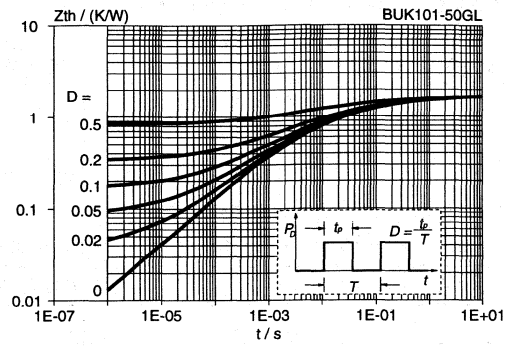


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

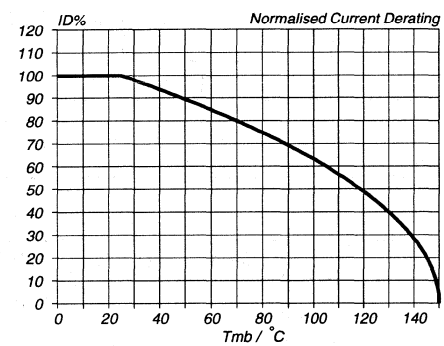


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D / I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

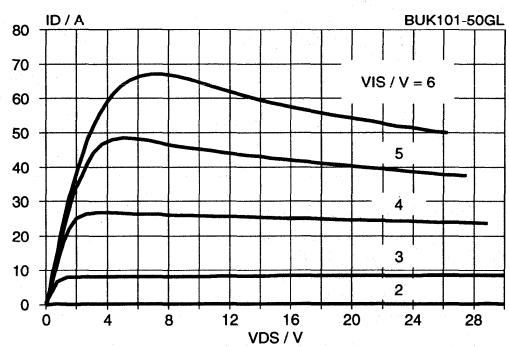


Fig.6. Typical output characteristics, $T_j = 25$ °C.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$ & $t_p < t_{d\,sc}$

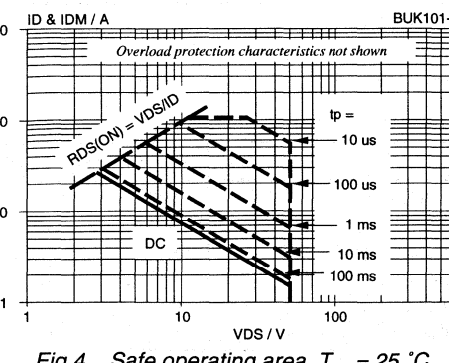


Fig.4. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

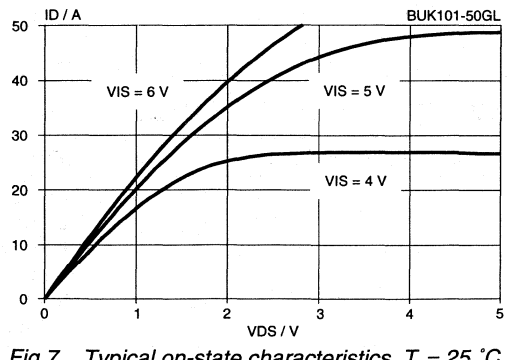


Fig.7. Typical on-state characteristics, $T_j = 25$ °C.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$

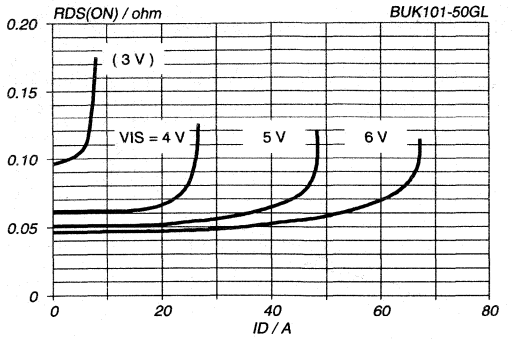


Fig.8. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

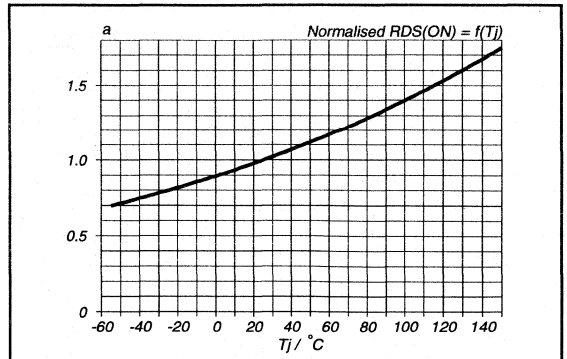


Fig.11. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}$25 °C = $f(T_j)$; I_D = 13 A; V_{IS} = 5 V

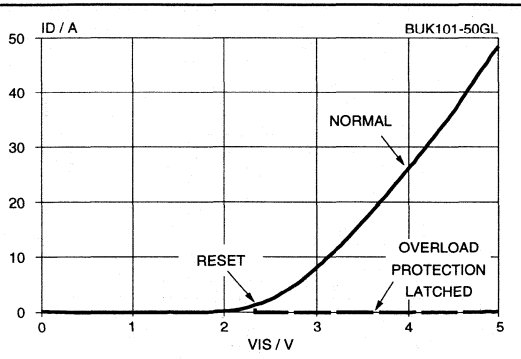


Fig.9. Typical transfer characteristics, T_j = 25 °C. $I_D = f(V_{IS})$; conditions: V_{DS} = 10 V; t_p = 250 µs

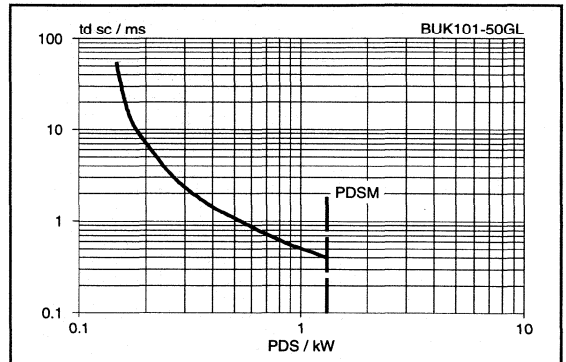


Fig.12. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{IS} \geq 4$ V; T_j = 25 °C.

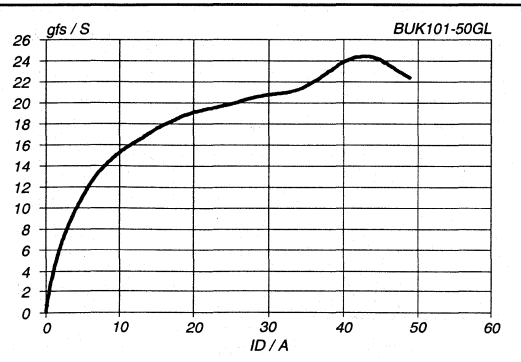


Fig.10. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V; t_p = 250 µs

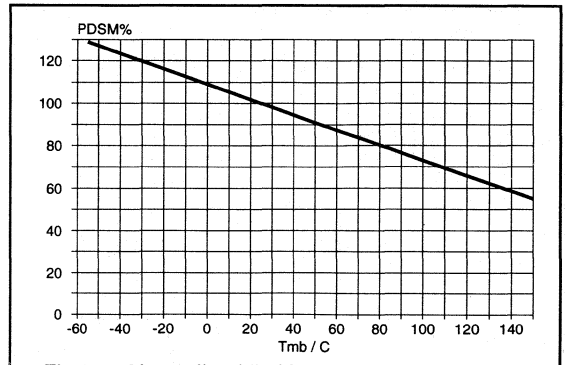


Fig.13. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ °C) = f(T_{mb})$

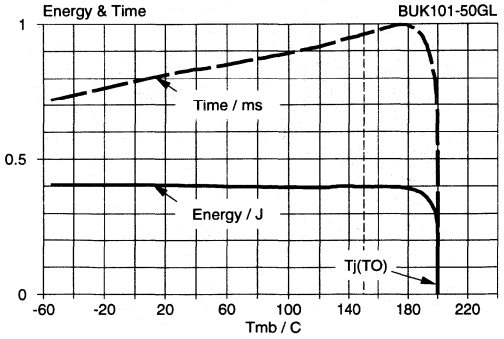


Fig.14. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; V_{IS} = 5 V; SC load = 30 mΩ

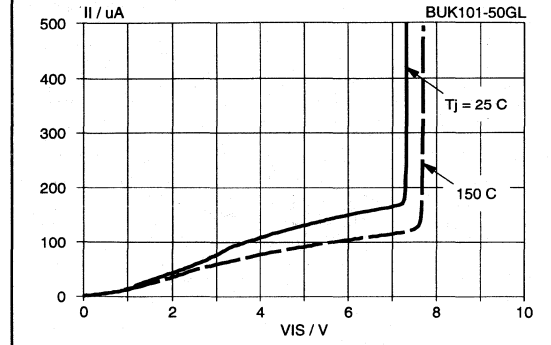


Fig.17. Typical DC input characteristics. $I_I = f(V_{IS})$; normal operation; parameter: T_j

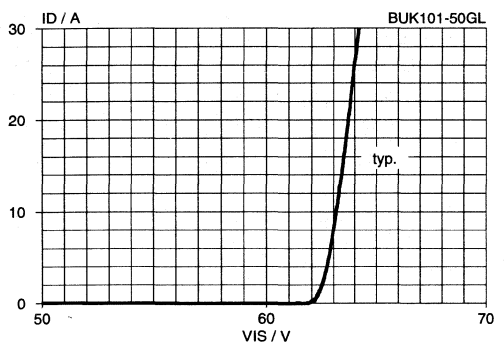


Fig.15. Typical clamping characteristics, 25 ˚C. $I_D = f(V_{DS})$; conditions: V_{IS} = 0 V; $t_p \leq 50$ µs

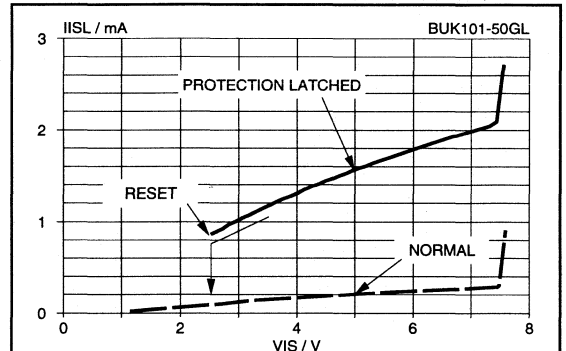


Fig.18. Typical DC input characteristics, T_j = 25 ˚C. $I_{ISL} = f(V_{IS})$; overload protection operated ⇒ I_D = 0 A

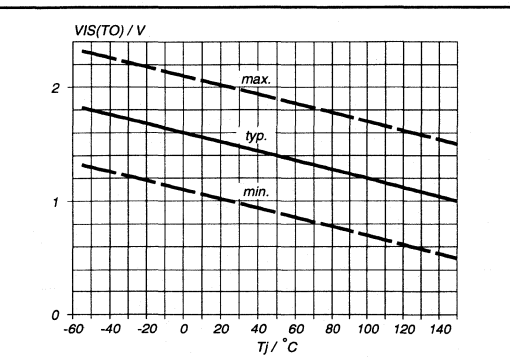


Fig.16. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

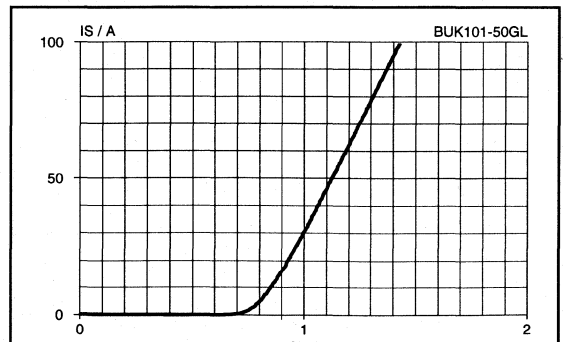


Fig.19. Typical reverse diode current, T_j = 25 ˚C. $I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V

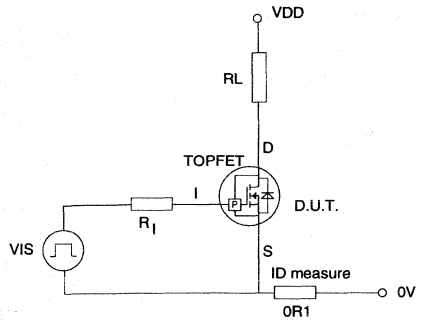


Fig.20. Test circuit for resistive load switching times.

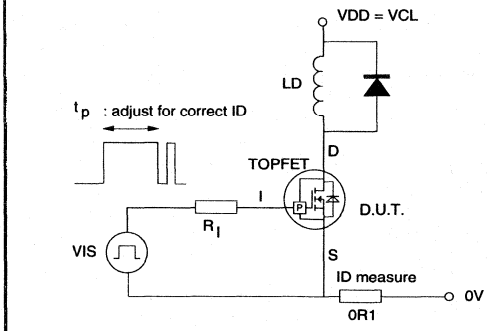


Fig.23. Test circuit for inductive load switching times.

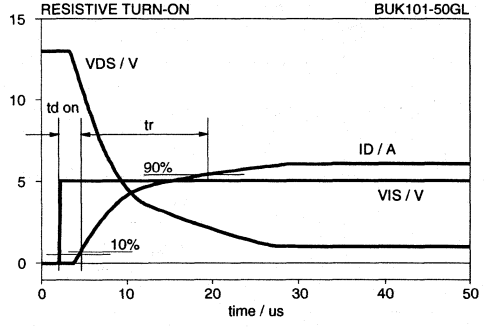


Fig.21. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 2.1 Ω; R_I = 50 Ω, T_j = 25 °C.

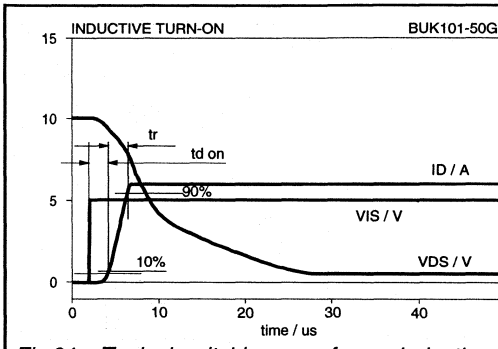


Fig.24. Typical switching waveforms, inductive load. V_{DD} = 10 V; I_D = 6 A; R_I = 50 Ω, T_j = 25 °C.

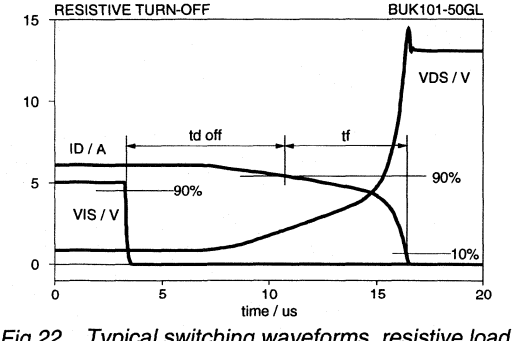


Fig.22. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 2.1 Ω; R_I = 50 Ω, T_j = 25 °C.

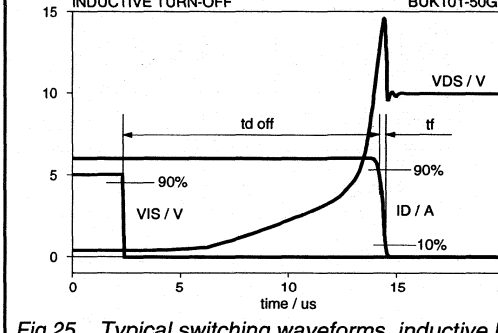


Fig.25. Typical switching waveforms, inductive load. V_{DD} = 10 V; I_D = 6 A; R_I = 50 Ω, T_j = 25 °C.

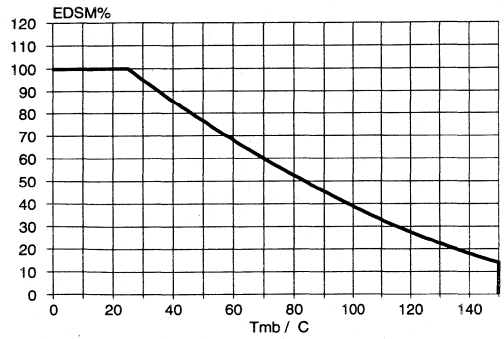


Fig.26. Normalised clamping energy rating. $E_{DSM}\% = f(T_{mb})$; conditions: I_D = 26 A; V_{IS} = 5 V

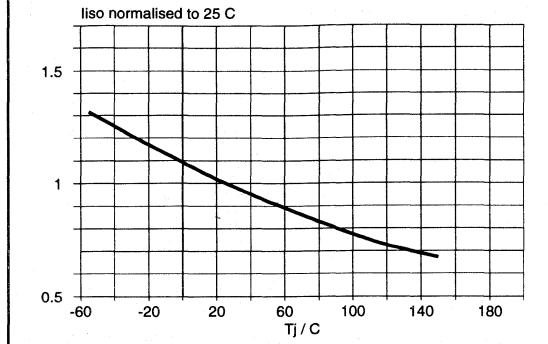


Fig.29. Normalised input current (normal operation). $I_{IS}/I_{IS}25\ ^{\circ}C = f(T_j)$; V_{IS} = 5 V

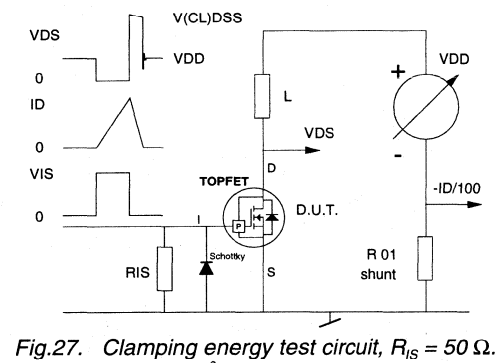


Fig.27. Clamping energy test circuit, R_{IS} = 50 Ω.

$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$$

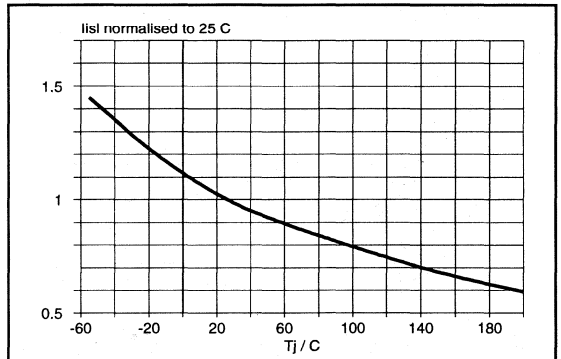


Fig.30. Normalised input current (protection latched). $I_{ISL}/I_{ISL}25\ ^{\circ}C = f(T_j)$; V_{IS} = 5 V

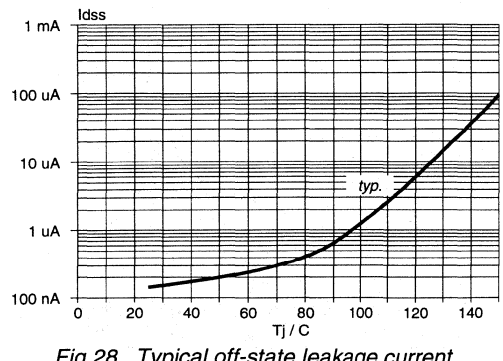


Fig.28. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

PowerMOS transistor Logic level TOPFET

BUK102-50DL

For maintenance only. Do not use for design-in.

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 3 pin plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Lower operating input current permits direct drive by micro-controller
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER		MAX.	UNIT
V_{DS}	Continuous drain source voltage		50	V
I_D	Continuous drain current		45	A
P_D	Total power dissipation		125	W
T_j	Continuous junction temperature		150	°C
$R_{DS(ON)}$	Drain-source on-state resistance		35	mΩ
I_{ISL}	Input supply current	V_{IS} = 5 V	650	µA

FUNCTIONAL BLOCK DIAGRAM

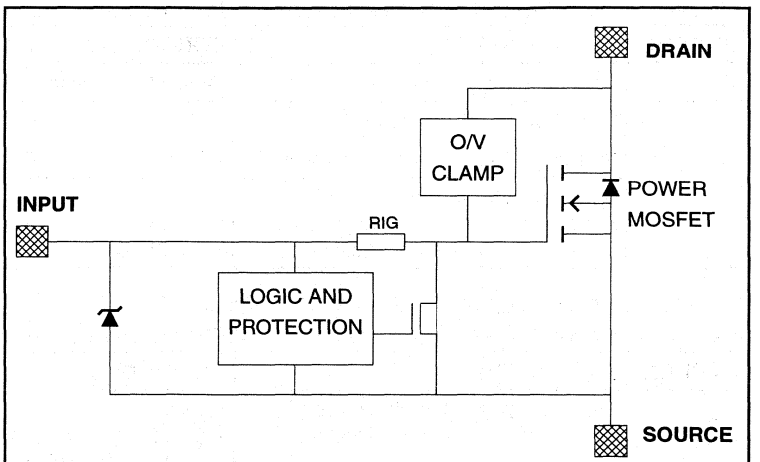
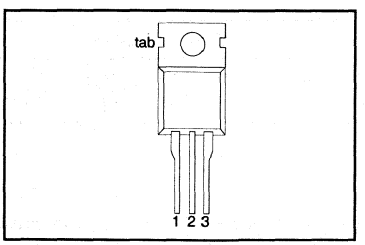


Fig.1. Elements of the TOPFET.

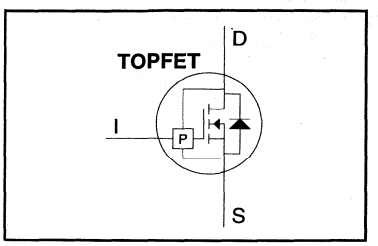
PINNING - TO220AB

PIN	DESCRIPTION
1	input
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Continuous drain source voltage[1]	-	-	50	V
V_{IS}	Continuous input voltage	-	0	6	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; $V_{IS} = 5$ V	-	45	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; $V_{IS} = 5$ V	-	28	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; $V_{IS} = 5$ V	-	180	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	125	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	4	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	$V_{IS} = 5$ V	-	50	V
	Short circuit load protection[4]				
$V_{DDP(P)}$	Protected drain source supply voltage[5]	$V_{IS} = 5$ V	-	16	V
P_{DSM}	Instantaneous overload dissipation	$T_{mb} = 25$ °C	-	2.1	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	$V_{IS} = 0$ V	-	45	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; $I_{DM} = 25$ A; $V_{DD} \leq 20$ V; inductive load	-	1	J
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 85$ °C; $I_{DM} = 16$ A; $V_{DD} \leq 20$ V; f = 250 Hz	-	80	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

5 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than $V_{DDP(P)}$ maximum.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	0.8	1	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 4 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V	-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance[1]	V_{IS} = 5 V; I_{DM} = 25 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	30	35	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[2]	T_{mb} = 25 °C; L ≤ 10 µH; R_L = 10 mΩ				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 5 V	-	1.1	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 5 V	-	0.8	-	ms
$I_{D(SC)}$	Drain current[3]	V_{DD} = 13 V; V_{IS} = 5 V	-	75	-	A
$I_{DM(SC)}$	Peak drain current[4]	V_{IS} = 5 V; V_{DD} = 13 V	-	200	-	A
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 5 V; from $I_D \geq 2$ A[5]	150	-	-	°C

TRANSFER CHARACTERISTIC

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 25 A $t_p \leq 300$ µs; $\delta \leq 0.01$	17	28	-	S

1 Continuous input voltage. The specified pulse width is for the drain current.

2 Refer to OVERLOAD PROTECTION LIMITING VALUES.

3 Continuous drain-source supply voltage. Pulsed input voltage.

4 Continuous input voltage. Momentary short circuit load connection. (The higher peak current is due to the effect of capacitance Cgd).

5 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA		1.0	1.5	2.0	V
I_{IS}	Input supply current	normal operation;	V_{IS} = 5 V	100	200	350	µA
			V_{IS} = 4 V	-	160	270	µA
V_{ISR}	Protection reset voltage[1]		T_j = 25 °C	2.0	2.6	3.5	V
			T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	protection latched;	V_{IS} = 5 V	-	330	650	µA
			V_{IS} = 3.5 V	-	240	430	µA
$V_{(BR)IS}$	Input breakdown voltage	I_I = 10 mA		6	-	-	V
R_{IG}	Input series resistance		T_j = 25 °C	-	33	-	kΩ
	to gate of power MOSFET		T_j = 150 °C	-	50	-	kΩ

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω. Refer to waveform figure and test circuit.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	30	-	µs
t_r	Rise time	resistive load R_L = 2.1 Ω	-	150	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	120	-	µs
t_f	Fall time	resistive load R_L = 2.1 Ω	-	120	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq 25$ °C; V_{IS} = 0 V	-	45	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDO}	Forward voltage	I_S = 45 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

1 The input voltage below which the overload protection circuits will be reset.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

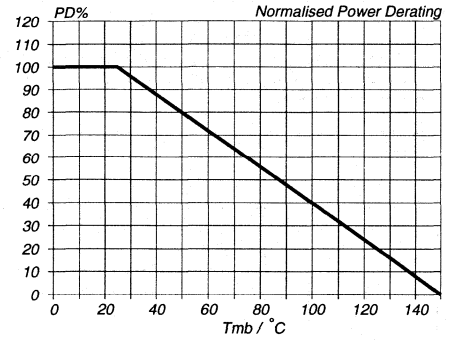


Fig.2. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

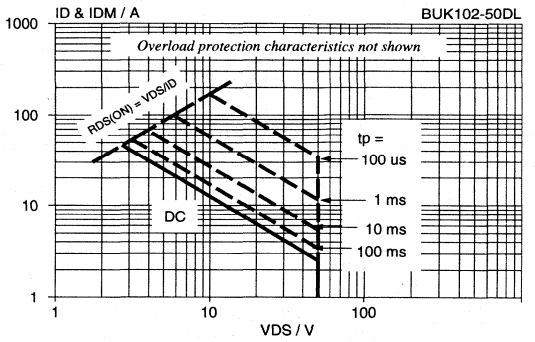


Fig.4. Safe operating area. $T_{mb} = 25\ ^\circ C$
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

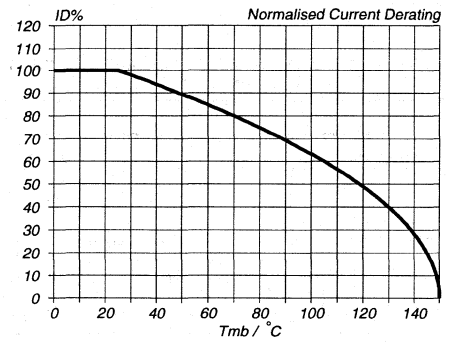


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

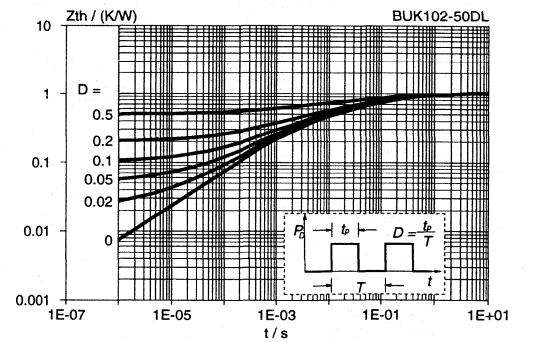


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

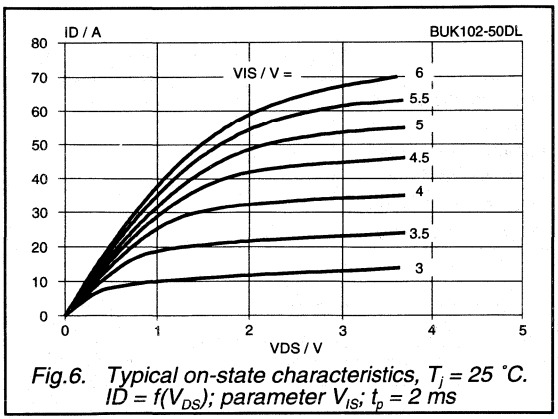


Fig.6. Typical on-state characteristics, T_j = 25 ˚C. ID = f(V_{DS}); parameter V_{IS}; t_p = 2 ms

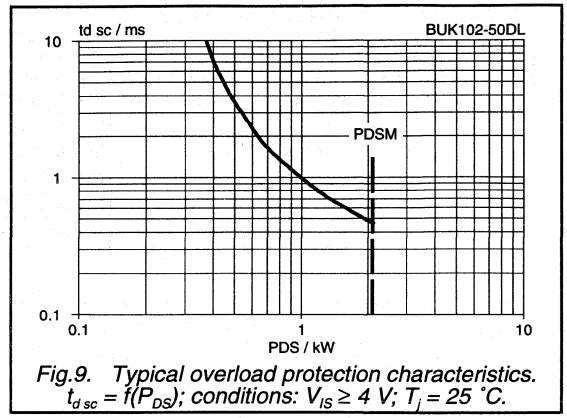


Fig.9. Typical overload protection characteristics. $t_{d\,sc}$ = f(P_{DS}); conditions: $V_{IS} \geq 4$ V; T_j = 25 ˚C.

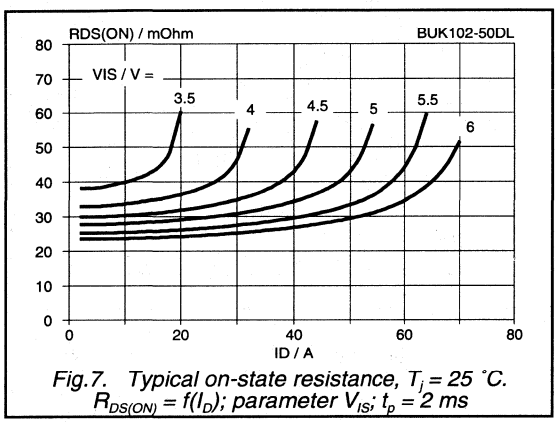


Fig.7. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)}$ = f(I_D); parameter V_{IS}; t_p = 2 ms

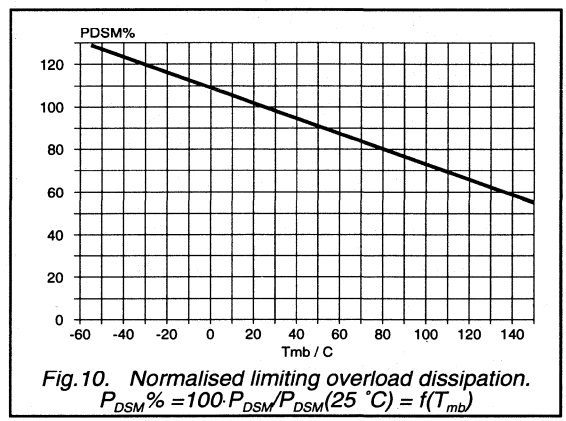


Fig.10. Normalised limiting overload dissipation. P_{DSM}% =100·P_{DSM}/P_{DSM}(25 ˚C) = f(T_{mb})

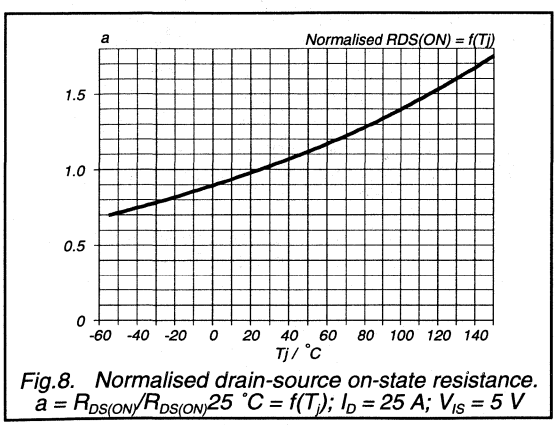


Fig.8. Normalised drain-source on-state resistance. a = $R_{DS(ON)}$/$R_{DS(ON)}$25 ˚C = f(T_j); I_D = 25 A; V_{IS} = 5 V

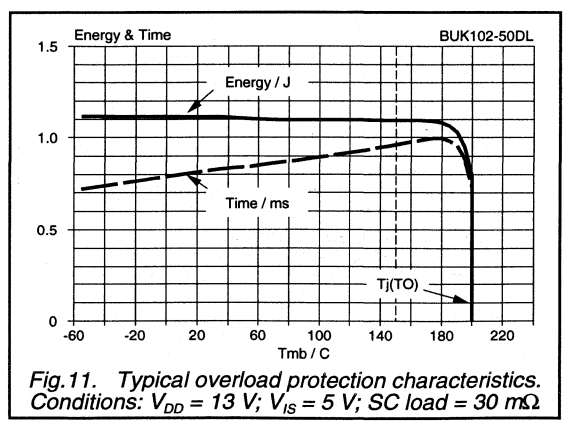


Fig.11. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; V_{IS} = 5 V; SC load = 30 mΩ

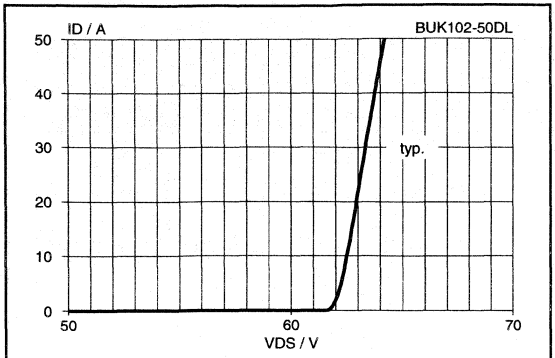


Fig.12. Typical clamping characteristics, 25 ˚C. $I_D = f(V_{DS})$; conditions: $V_{IS} = 0$ V; $t_p \leq 50$ µs

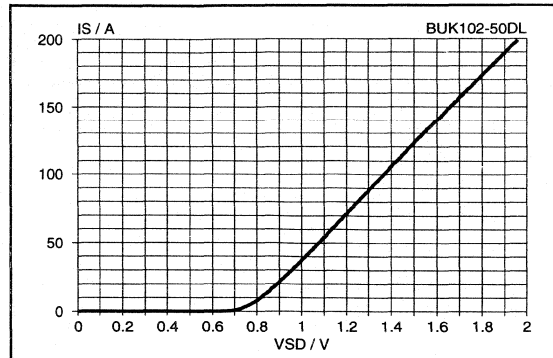


Fig.15. Typical reverse diode current, $T_j = 25$ ˚C. $I_S = f(V_{SDS})$; conditions: $V_{IS} = 0$ V; $t_p = 250$ µs

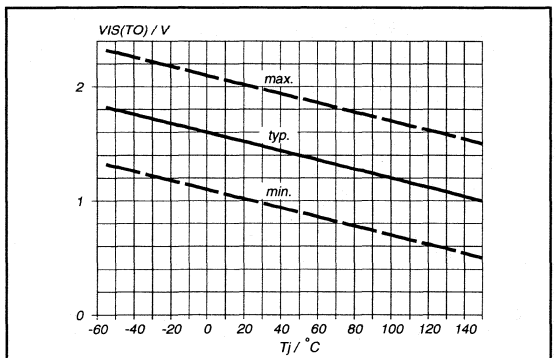


Fig.13. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = 5$ V

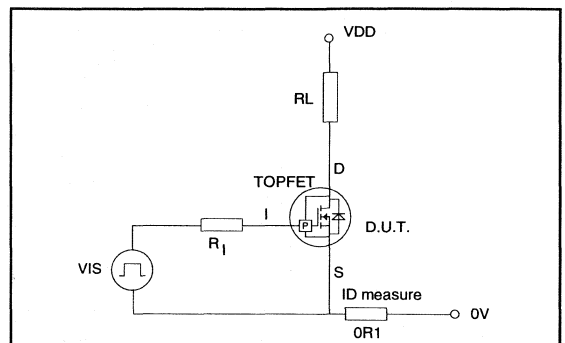


Fig.16. Test circuit for resistive load switching times.

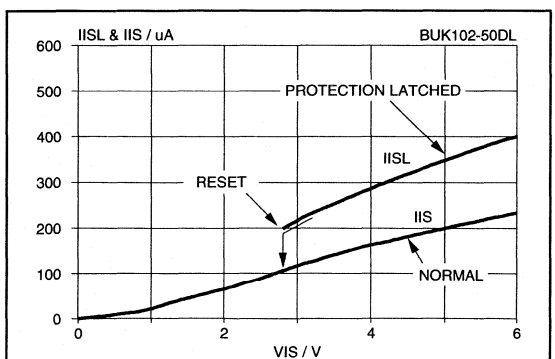


Fig.14. Typical DC input characteristics, $T_j = 25$ ˚C. I_{ISL} & $I_{IS} = f(V_{IS})$; protection latched & normal operation

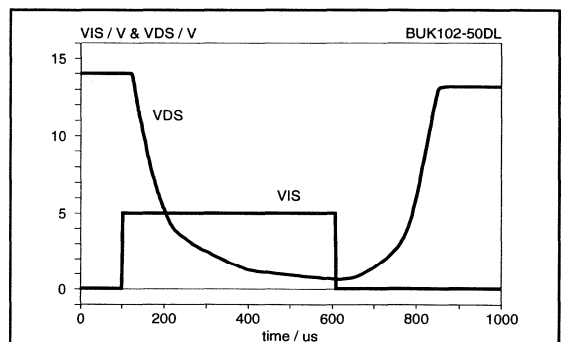


Fig.17. Typical switching waveforms, resistive load. $V_{DD} = 13$ V; $R_L = 1.1$ Ω; $R_I = 50$ Ω, $T_j = 25$ ˚C.

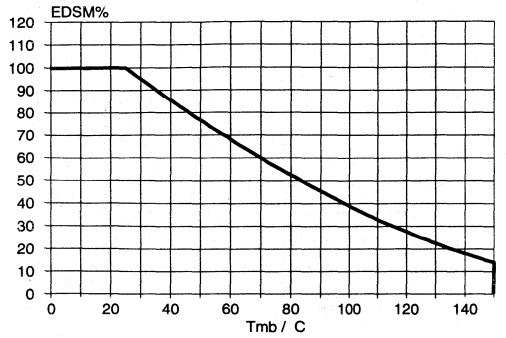


Fig.18. Normalised limiting clamping energy. $E_{DSM}\% = f(T_{mb})$; conditions: I_D = 25 A; V_{IS} = 10 V

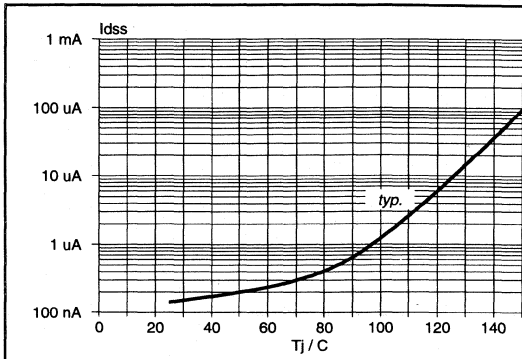


Fig.20. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

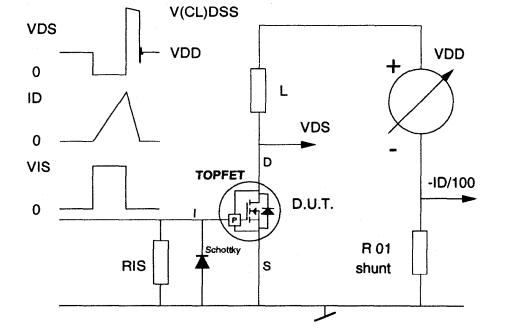


Fig.19. Clamping energy test circuit, R_{IS} = 50 Ω.
$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$$

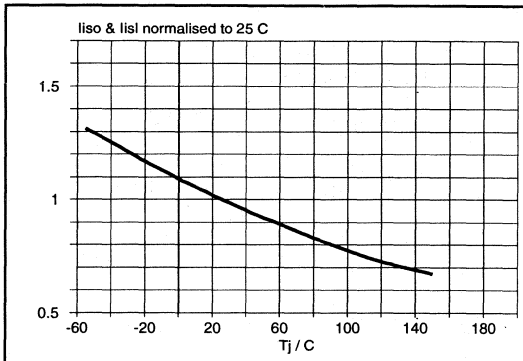


Fig.21. Normalised input currents (normal & latched). $I_{ISO}/I_{ISO}25^{\circ}C$ & $I_{ISL}/I_{ISL}25^{\circ}C = f(T_j)$; V_{IS} = 5 V

PowerMOS transistor Logic level TOPFET

BUK102-50GL

For maintenance only. Do not use for design-in.

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 3 pin plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V input level
- Low threshold voltage also allows 5 V control
- Control of power MOSFET and supply of overload protection circuits derived from input
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	45	A
P_D	Total power dissipation	125	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{IS} = 5 V	35	mΩ

FUNCTIONAL BLOCK DIAGRAM

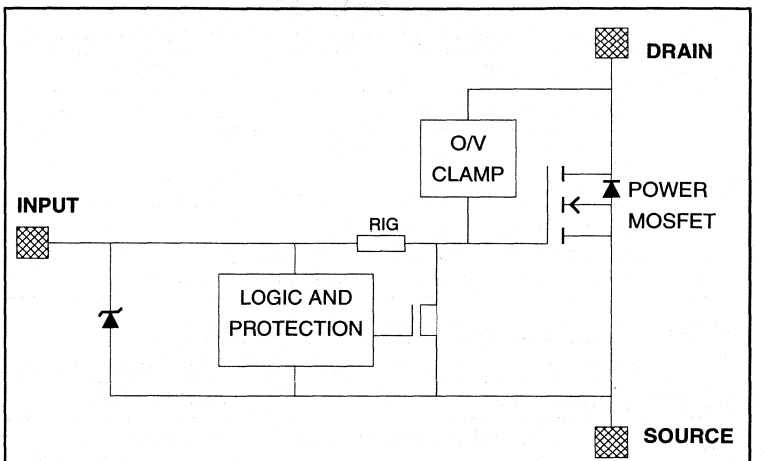
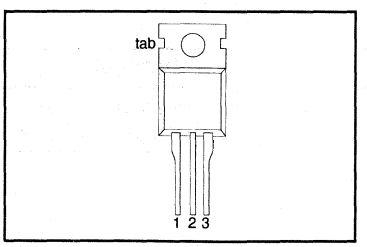


Fig.1. Elements of the TOPFET.

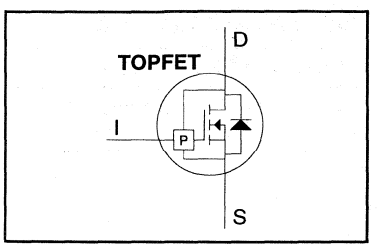
PINNING - TO220AB

PIN	DESCRIPTION
1	input
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Continuous off-state drain source voltage[1]	V_{IS} = 0 V	-	50	V
V_{IS}	Continuous input voltage	-	0	6	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; V_{IS} = 5 V	-	45	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; V_{IS} = 5 V	-	28	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; V_{IS} = 5 V	-	180	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	125	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	4	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 5 V	-	50	V
	Short circuit load protection				
$V_{DDP(P)}$	Protected drain source supply voltage[4]	V_{IS} = 5 V	-	24	V
P_{DSM}	Instantaneous overload dissipation	T_{mb} = 25 °C	-	2.1	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	V_{IS} = 0 V	-	45	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; I_{DM} = 25 A; $V_{DD} \leq 25$ V; inductive load	-	1	J
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 85$ °C; I_{DM} = 16 A; $V_{DD} \leq 20$ V; f = 250 Hz	-	80	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	0.8	1.0	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 2 A; $t_p \le 300$ µs; $\delta \le 0.01$	-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V	-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	I_{DM} = 25 A; V_{IS} = 5 V; $t_p \le 300$ µs; $\delta \le 0.01$	-	30	35	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	T_{mb} = 25 °C; L ≤ 10 µH				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 5 V	-	1.1	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 5 V	-	0.8	-	ms
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 5 V; from $I_D \ge 2$ A[2]	150	-	-	°C

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA	1.0	1.5	2.0	V
I_{IS}	Input supply current	V_{IS} = 5 V; normal operation	-	0.2	0.35	mA
V_{ISR}	Protection reset voltage[3]		2.0	2.6	3.5	V
V_{ISR}	Protection reset voltage	T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	V_{IS} = 5 V; protection latched	2	3.8	10	mA
$V_{(BR)IS}$	Input clamp voltage	I_I = 10 mA	6	-	-	V
R_{IG}	Input series resistance	to gate of power MOSFET	-	1.5	-	kΩ

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum. Refer to OVERLOAD PROTECTION LIMITING VALUES.

2 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

3 The input voltage below which the overload protection circuits will be reset.

TRANSFER CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 25 A $t_p \leq$ 300 µs; $\delta \leq 0.01$	17	28	-	S
$I_{D(SC)}$	Drain current[1]	V_{DS} = 13 V; V_{IS} = 5 V	-	60	-	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω. Refer to waveform figures and test circuits.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	2	-	µs
t_r	Rise time	resistive load R_L = 1.1 Ω	-	8	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	8	-	µs
t_f	Fall time	resistive load R_L = 1.1 Ω	-	8	-	µs
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	3.7	-	µs
t_r	Rise time	inductive load I_{DM} = 11 A	-	3.7	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	13	-	µs
t_f	Fall time	inductive load I_{DM} = 11 A	-	1.4	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq$ 25 °C; V_{IS} = 0 V	-	50	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	I_S = 50 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

1 During overload before short circuit load protection operates.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

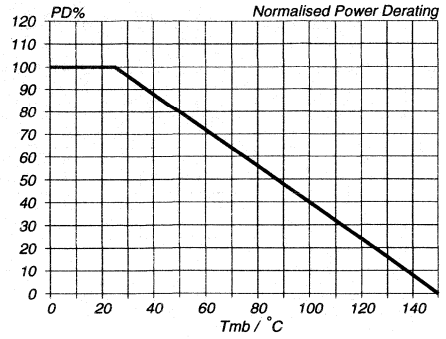


Fig.2. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

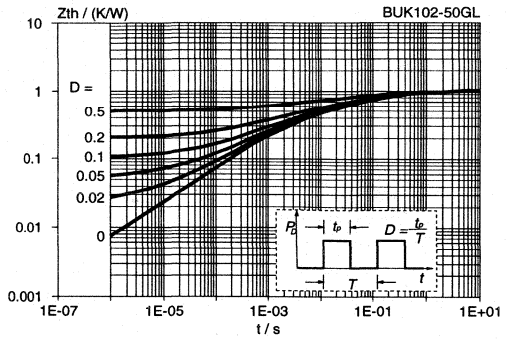


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; *parameter* $D = t_p/T$

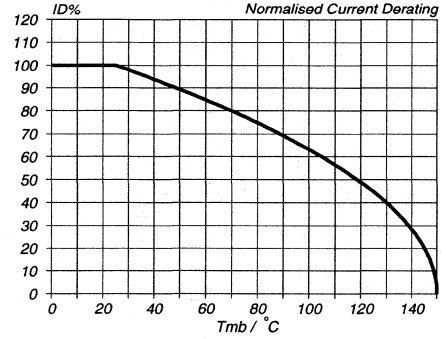


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; *conditions:* $V_{IS} = 5$ V

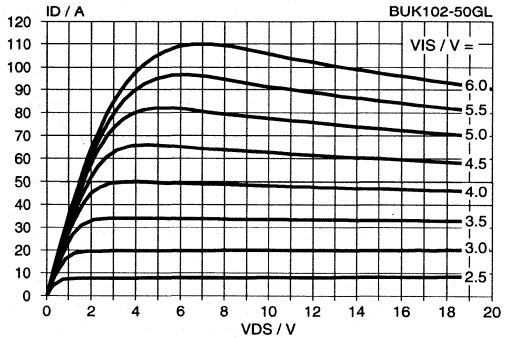


Fig.6. Typical output characteristics, $T_j = 25\ ^\circ C$.
$ID = f(V_{DS})$; *parameter* V_{IS}; $t_p = 250\ \mu s$ & $t_p < t_{d\,sc}$

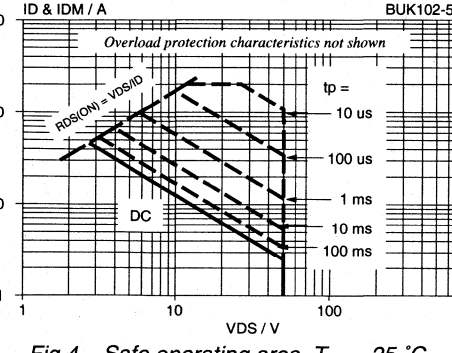


Fig.4. Safe operating area. $T_{mb} = 25\ ^\circ C$
I_D & $I_{DM} = f(V_{DS})$; I_{DM} *single pulse; parameter* t_p

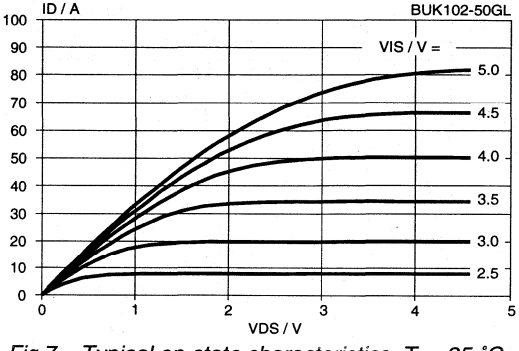


Fig.7. Typical on-state characteristics, $T_j = 25\ ^\circ C$.
$ID = f(V_{DS})$; *parameter* V_{IS}; $t_p = 250\ \mu s$

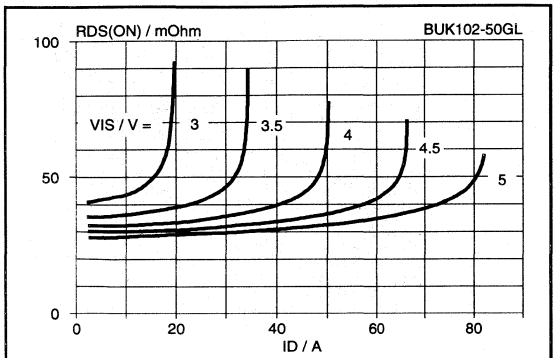


Fig.8. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

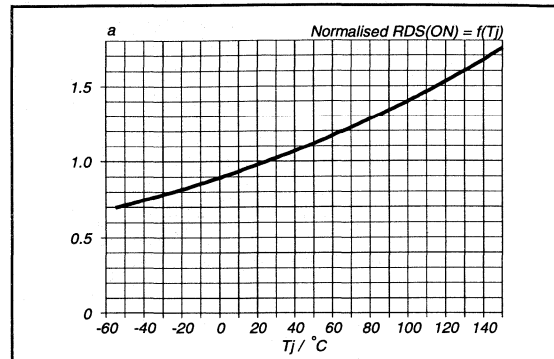


Fig.11. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25\ °C = f(T_j)$; I_D = 25 A; V_{IS} = 5 V

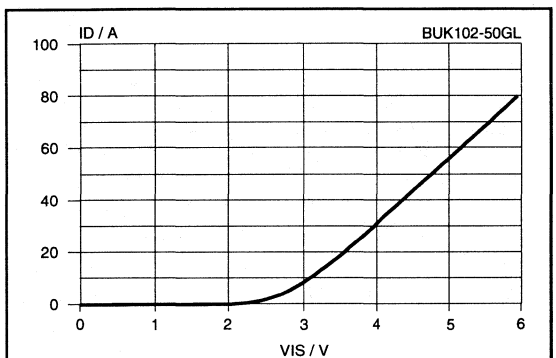


Fig.9. Typical transfer characteristics, T_j = 25 °C. $I_D = f(V_{IS})$; conditions: V_{DS} = 10 V; t_p = 250 µs

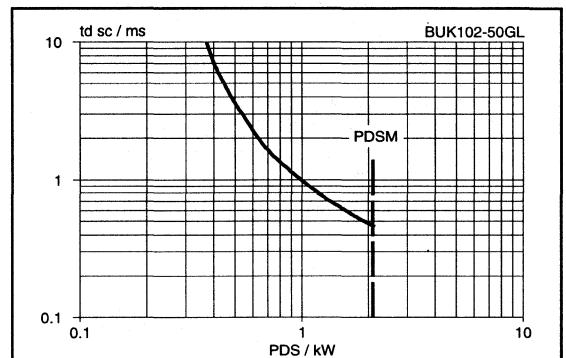


Fig.12. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{IS} \geq 4$ V; T_j = 25 °C.

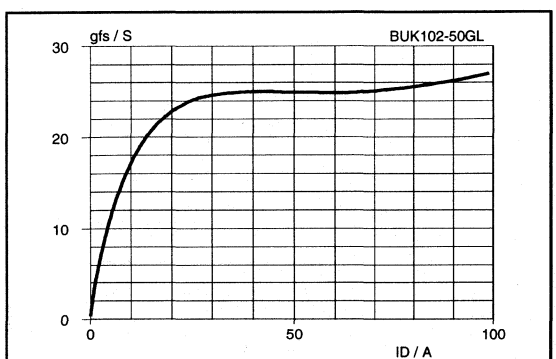


Fig.10. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V; t_p = 250 µs

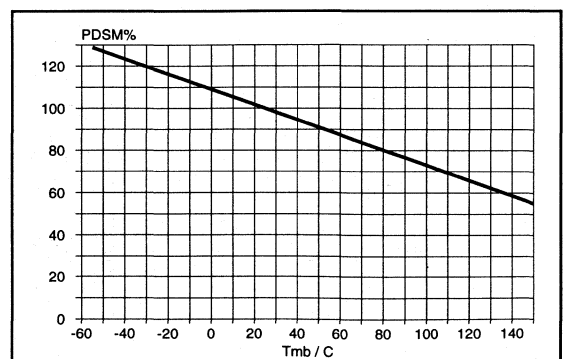


Fig.13. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ °C) = f(T_{mb})$

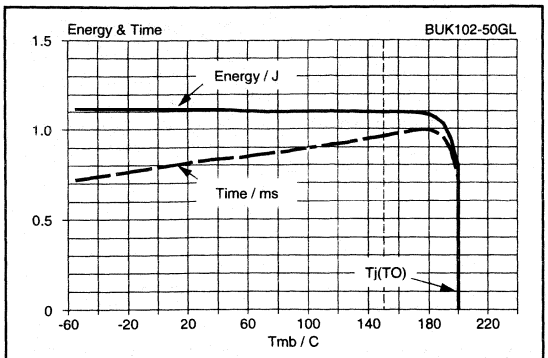


Fig.14. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; V_{IS} = 5 V; SC load = 30 mΩ

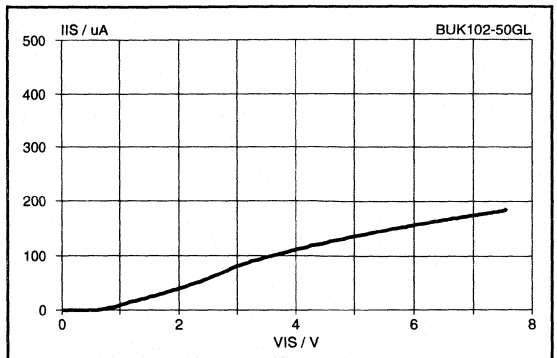


Fig.17. Typical DC input characteristics, T_j = 25 ˚C. $I_{IS} = f(V_{IS})$; normal operation

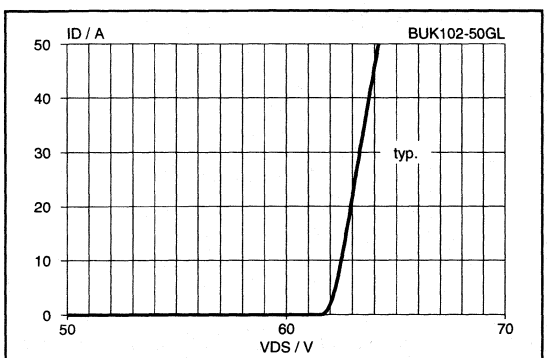


Fig.15. Typical clamping characteristics, 25 ˚C. $I_D = f(V_{DS})$; conditions: V_{IS} = 0 V; $t_p \leq 50$ µs

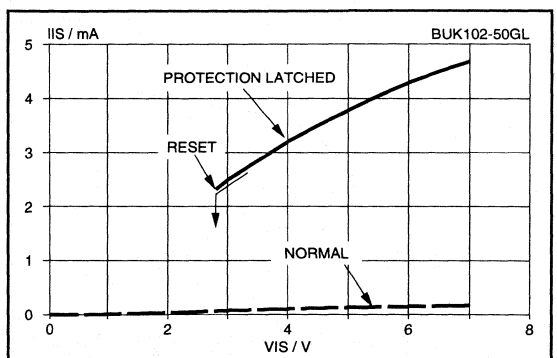


Fig.18. Typical DC input characteristics, T_j = 25 ˚C. $I_{ISL} = f(V_{IS})$; overload protection operated ⇒ I_D = 0 A

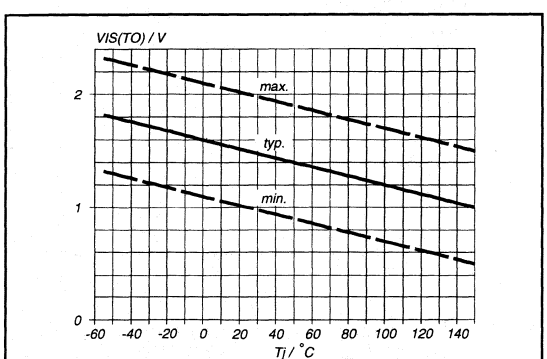


Fig.16. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

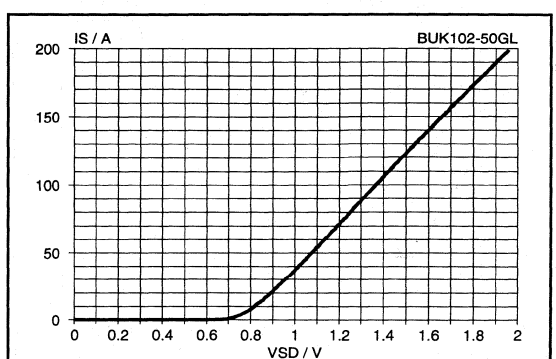


Fig.19. Typical reverse diode current, T_j = 25 ˚C. $I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V; t_p = 250 µs

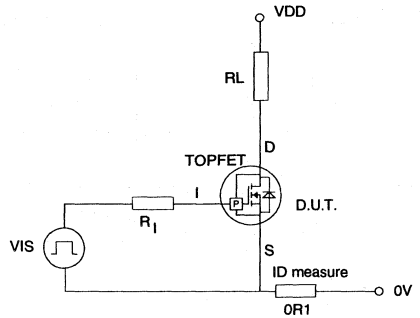


Fig.20. Test circuit for resistive load switching times.

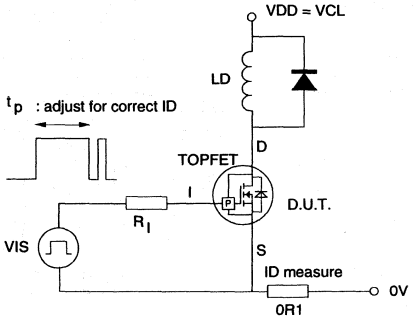


Fig.23. Test circuit for inductive load switching times.

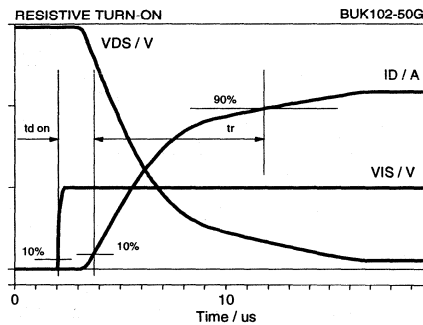


Fig.21. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 1.1 Ω; R_I = 50 Ω, T_j = 25 °C.

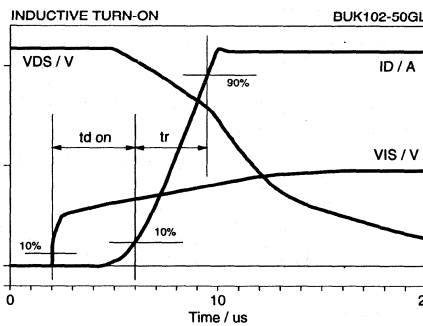


Fig.24. Typical switching waveforms, inductive load. V_{DD} = 13 V; I_D = 11 A; R_I = 50 Ω, T_j = 25 °C.

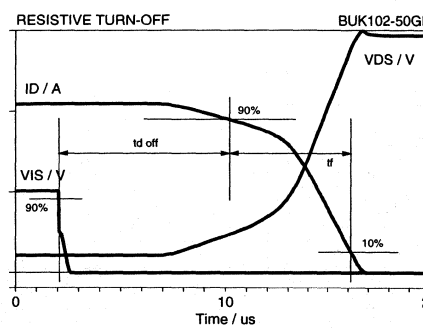


Fig.22. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 1.1 Ω; R_I = 50 Ω, T_j = 25 °C.

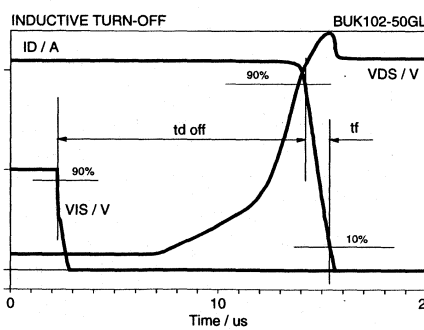


Fig.25. Typical switching waveforms, inductive load. V_{DD} = 13 V; I_D = 11 A; R_I = 50 Ω, T_j = 25 °C.

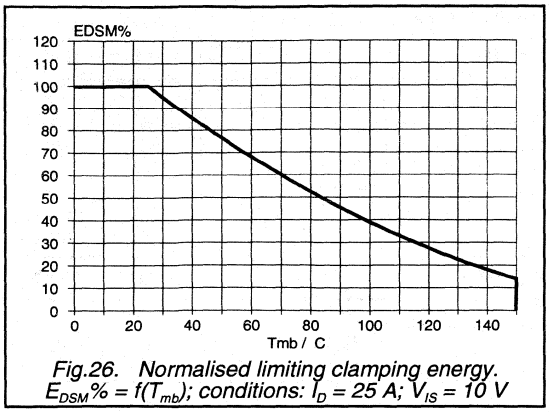


Fig.26. Normalised limiting clamping energy. $E_{DSM}\% = f(T_{mb})$; conditions: I_D = 25 A; V_{IS} = 10 V

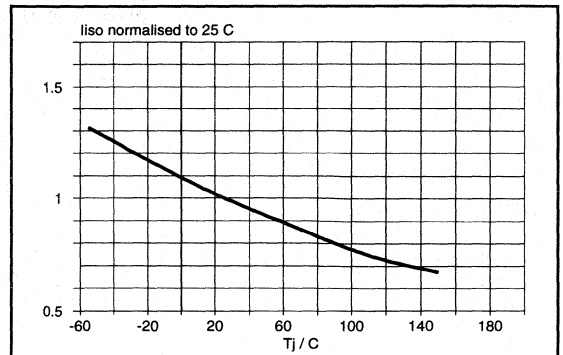


Fig.29. Normalised input current (normal operation). I_{IS}/I_{ISS}25 °C = $f(T_j)$; V_{IS} = 5 V

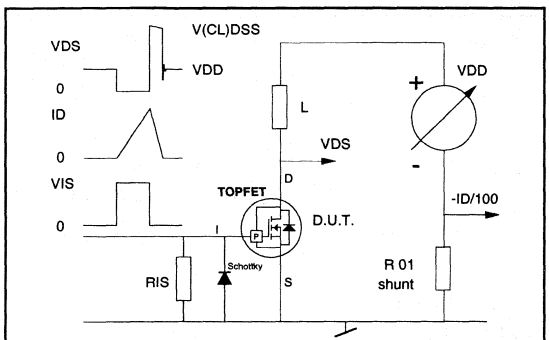


Fig.27. Clamping energy test circuit, R_{IS} = 50 Ω.

$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$$

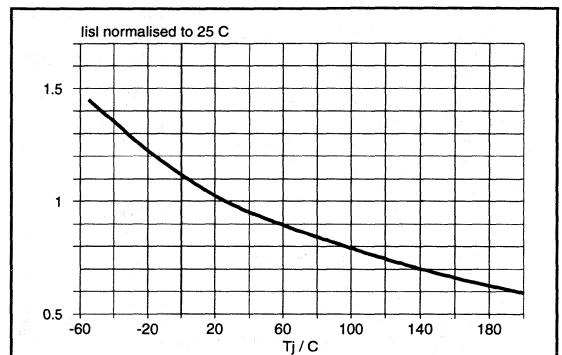


Fig.30. Normalised input current (protection latched). I_{ISL}/I_{ISL}25 °C = $f(T_j)$; V_{IS} = 5 V

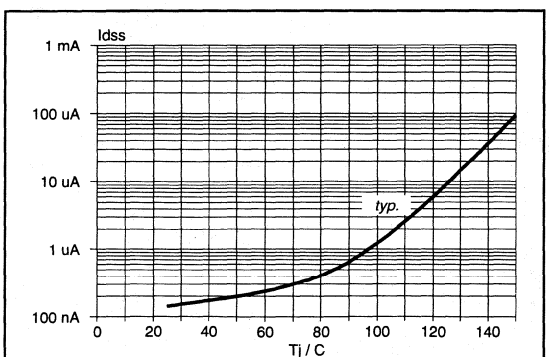


Fig.28. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

PowerMOS transistor
Logic level TOPFET

BUK104-50L/S
BUK104-50LP/SP

For maintenance only. Do not use for design-in.

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 5 pin plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	15	A
P_{tot}	Total power dissipation	40	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance		
	V_{IS} = 5 V	125	mΩ
	V_{IS} = 7 V	100	mΩ
SYMBOL	**PARAMETER**	**NOM.**	**UNIT**
V_{PSN}	Protection supply voltage		
	BUK104-50L	5	V
	BUK104-50S	10	V

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Logic and protection supply from separate pin
- Low operating supply current
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by protection supply
- Protection circuit condition indicated by flag pin
- 5 V logic compatible input level
- Separate input pin for higher frequency drive
- ESD protection on input, flag and protection supply pins
- Over voltage clamping for turn off of inductive loads
- Both linear and switching operation are possible

FUNCTIONAL BLOCK DIAGRAM

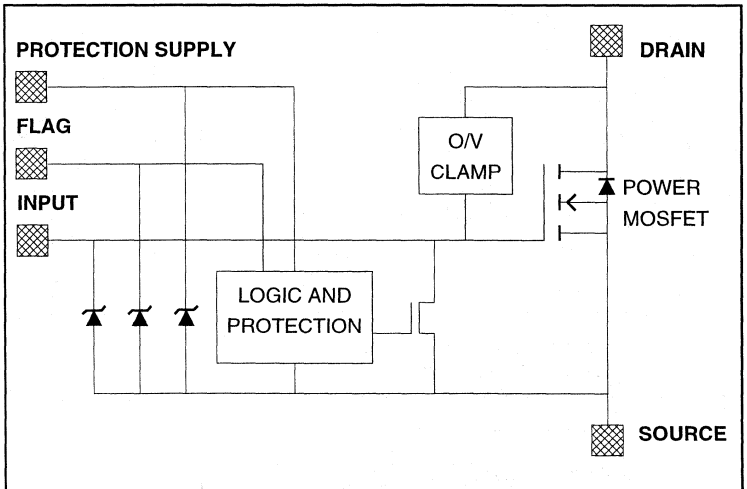


Fig.1. Elements of the TOPFET.

PINNING - SOT263

PIN	DESCRIPTION
1	input
2	flag
3	drain
4	protection supply
5	source
tab	drain

PIN CONFIGURATION

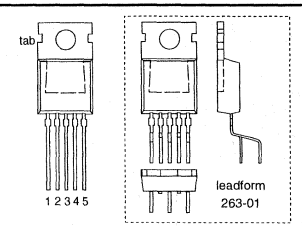


Fig. 2. Type numbers ending with suffix P refer to leadform 263-01.

SYMBOL

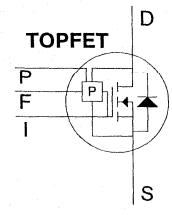


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
	Voltages					
V_{DSS}	Continuous off-state drain source voltage[1]	V_{IS} = 0 V	-	50		V
V_{IS}	Continuous input voltage	-	0	11		V
V_{FS}	Continuous flag voltage	-	0	11		V
V_{PS}	Continuous supply voltage	-	0	11		V
	Currents	V_{IS} =	-	7	5	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C	-	15	13	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C	-	9.5	8.5	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C	-	60	54	A
	Thermal					
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	40		W
T_{stg}	Storage temperature	-	-55	150		°C
T_j	Junction temperature[2]	continuous	-	150		°C
T_{sold}	Lead temperature	during soldering	-	250		°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply connected, TOPFET can protect itself from two types of overload - over temperature and short circuit load.

An n-MOS transistor turns on between the input and source to quickly discharge the power MOSFET gate capacitance.

For internal overload protection to remain latched while the control circuit is high, external series input resistance must be provided. Refer to INPUT CHARACTERISTICS.

SYMBOL	PARAMETER	CONDITIONS	MIN.		MAX.	UNIT
		V_{IS} =	7	5	-	V
V_{PSP}	Protection supply voltage[3]	for valid protection				
		BUK104-50L	4.4	4	-	V
		BUK104-50S	5.4	5	-	V
	Over temperature protection	$V_{PS} = V_{PSN}$				
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 10 V; $R_I \geq 2$ kΩ	-		50	V
		V_{IS} = 5 V; $R_I \geq 1$ kΩ	-		50	V
	Short circuit load protection	$V_{PS} = V_{PSN}$; L ≤ 10 µH				
$V_{DDP(P)}$	Protected drain source supply voltage[4]	V_{IS} = 10 V; $R_I \geq 2$ kΩ	-		25	V
		V_{IS} = 5 V; $R_I \geq 1$ kΩ	-		45	V
P_{DSM}	Instantaneous overload dissipation		-		0.8	kW

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The minimum supply voltage required for correct operation of the overload protection circuits.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DRRM}	Repetitive peak clamping drain current	$R_{IS} \geq 100\ \Omega$[1]	-	15	A
E_{DSM}	Non-repetitive inductive turn-off energy[2]	$I_{DM} = 15$ A; $R_{IS} \geq 100\ \Omega$	-	200	mJ
E_{DRM}	Repetitive inductive turn-off energy	$R_{IS} \geq 100\ \Omega$; $T_{mb} \leq 95$ °C; $I_{DM} = 4$ A; $V_{DD} \leq 20$ V; f = 250 Hz	-	20	mJ
I_{DIRM}	Repetitive peak drain to input current[3]	$R_{IS} = 0\ \Omega$; $t_p \leq 1$ ms	-	50	mA

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} = 25$ °C; $V_{IS} = V_{PS} = V_{FS} = 0$ V	-	15	A

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	2.5	3.1	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

$T_{mb} = 25$ °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSR}$	Drain-source clamping voltage	$R_{IS} = 100\ \Omega$; $I_D = 10$ mA		50	-	65	V
$V_{(CL)DSR}$	Drain-source clamping voltage	$R_{IS} = 100\ \Omega$; $I_{DM} = 1$ A; $t_p \leq 300\ \mu$s; $\delta \leq 0.01$		50	-	70	V
I_{DSS}	Zero input voltage drain current	$V_{DS} = 12$ V; $V_{IS} = 0$ V		-	0.5	10	µA
I_{DSR}	Drain source leakage current	$V_{DS} = 50$ V; $R_{IS} = 100\ \Omega$;		-	1	20	µA
I_{DSR}	Drain source leakage current	$V_{DS} = 40$ V; $R_{IS} = 100\ \Omega$; $T_j = 125$ °C		-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	$I_{DM} = 7.5$ A; $t_p \leq 300\ \mu$s; $\delta \leq 0.01$	$V_{IS} = 7$ V	-	75	100	mΩ
			$V_{IS} = 5$ V	-	95	125	mΩ

1 The input pin must be connected to the source pin by a specified external resistance to allow the power MOSFET gate source voltage to become sufficiently positive for active clamping. Refer to INPUT CHARACTERISTICS.

2 While the protection supply voltage is connected, during overvoltage clamping it is possible that the overload protection may operate at energies close to the limiting value. Refer to OVERLOAD PROTECTION CHARACTERISTICS.

3 Shorting the input to source with low resistance inhibits the internal overvoltage protection by preventing the power MOSFET gate source voltage becoming positive.

OVERLOAD PROTECTION CHARACTERISTICS

With adequate protection supply voltage TOPFET detects when one of the overload thresholds is exceeded.

Provided there is adequate input series resistance it switches off and remains latched off until reset by the protection supply pin.

Refer also to OVERLOAD PROTECTION LIMITING VALUES and INPUT CHARACTERISTICS.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	$V_{PS} = V_{PSN}$[2]; $T_{mb} = 25$ °C; $L \leq 10$ µH; $R_I \geq 2$ kΩ				
$E_{DS(TO)}$	Overload threshold energy	$V_{DD} = 13$ V; $V_{IS} = 10$ V	-	150	-	mJ
$t_{d\,sc}$	Response time	$V_{DD} = 13$ V; $V_{IS} = 10$ V	-	375	-	µs
	Over temperature protection	$V_{PS} = V_{PSN}$; $R_I \geq 2$ kΩ				
$T_{j(TO)}$	Threshold junction temperature	from $I_D \geq 0.65$ A[3]	150	-	-	°C

TRANSFER CHARACTERISTICS

$T_{mb} = 25$ °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 10$ V; $I_{DM} = 7.5$ A $t_p \leq 300$ µs; $\delta \leq 0.01$	5	9	-	S
I_D	Drain current[4]	$V_{DS} = 13$ V; $V_{IS} = 5$ V	-	25	-	A
		$V_{IS} = 10$ V		40	-	A

PROTECTION SUPPLY CHARACTERISTICS

$T_{mb} = 25$ °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Protection supply					
I_{PS}, I_{PSL}	Protection supply current	normal operation or protection latched				
		BUK104-50L $V_{PS} = 5$ V	-	0.2	0.35	mA
		BUK104-50S $V_{PS} = 10$ V	-	0.4	1.0	mA
V_{PSR}	Protection reset voltage[5]		1.5	2.5	3.5	V
		$T_j = 150$ °C	1.0	-	-	V
$V_{(CL)PS}$	Protection clamp voltage	$I_P = 1.35$ mA	11	13	-	V

REVERSE DIODE CHARACTERISTICS

$T_{mb} = 25$ °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	$I_S = 15$ A; $V_{IS} = V_{PS} = V_{FS} = 0$ V; $t_p = 300$ µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[6]	-	-	-	-

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum.

2 At the appropriate nominal protection supply voltage for each type. Refer to QUICK REFERENCE DATA.

3 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

4 During overload condition. Refer also to OVERLOAD PROTECTION LIMITING VALUES and CHARACTERISTICS.

5 The supply voltage below which the overload protection circuits will be reset.

6 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
	Normal operation						
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA		1.0	1.5	2.0	V
			T_{mb} = 150 °C	0.5	-	-	V
I_{IS}	Input current	V_{IS} = 10 V		-	10	100	nA
$V_{(CL)IS}$	Input clamp voltage	I_I = 1 mA		11	13	-	V
	Overload protection latched						
R_{ISL}	Input resistance[1]	V_{PS} = 5 V	I_I = 5 mA;	-	55	-	Ω
			T_{mb} = 150 °C	-	95	-	Ω
		V_{PS} = 10 V	I_I = 5 mA;	-	35	-	Ω
			T_{mb} = 150 °C	-	60	-	Ω
	Application information						
	External input resistances for	(see figure 29)					
R_{IS}	internal overvoltage clamping[2]	R_I = ∞ Ω;	V_{DS} > 30 V	100	-	-	Ω
R_I	internal overload protection[3]	R_{IS} = ∞ Ω;	V_{II} = 5 V	1	-	-	kΩ
			V_{II} = 10 V	2	-	-	kΩ

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C; R_I = 50 Ω; R_{IS} = 50 Ω (see figure 29); resistive load R_L = 10 Ω. For waveforms see figure 28.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 15 V; V_{IS}: 0 V ⇒ 10 V	-	8	-	ns
t_r	Rise time		-	13	-	ns
$t_{d\,off}$	Turn-off delay time	V_{DD} = 15 V; V_{IS}: 10 V ⇒ 0 V	-	100	-	ns
t_f	Fall time		-	45	-	ns

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{iss}	Input capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	415	600	pF
C_{oss}	Output capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	275	400	pF
C_{rss}	Reverse transfer capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	55	80	pF
C_{pso}	Protection supply pin capacitance	V_{PS} = 10 V	-	30	-	pF
C_{fso}	Flag pin capacitance	V_{FS} = 10 V; V_{PS} = 0 V	-	20	-	pF

1 The resistance of the internal transistor which discharges the power MOSFET gate capacitance when overload protection operates.
The external drive circuit should be such that the input voltage does not exceed $V_{IS(TO)}$ minimum when the overload protection has operated. Refer also to figure for latched input characteristics.

2 Applications using a lower value for R_{IS} would require external overvoltage protection.

3 For applications requiring a lower value for R_I, an external overload protection strategy is possible using the flag pin to 'tell' the control circuit to switch off the input.

FLAG DESCRIPTION

The flag pin provides a means to detect the presence of the protection supply and indicate the state of the overload detectors. The flag is the open drain of an n-MOS transistor and requires an external pull-up resistor[1]. It is suitable for both 5 V and 10 V logic. Flag may be used to implement an external protection strategy[2] for applications which require low input drive impedance.

TRUTH TABLE

CONDITION	DESCRIPTION	FLAG
NORMAL	Normal operation and adequate protection supply voltage	LOGIC LOW
OVER TEMP.	Over temperature detected	LOGIC HIGH
SHORT CIRCUIT	Overload condition detected	LOGIC HIGH
SUPPLY FAULT	Inadequate protection supply voltage	LOGIC HIGH

FLAG CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Flag 'low'	normal operation				
V_{FS}	Flag voltage	I_F = 1.6 mA	-	0.15	0.4	V
I_{FSS}	Flag saturation current	V_{FS} = 10 V	-	15	-	mA
	Flag 'high'	overload or fault				
I_{FS}	Flag leakage current	V_{FS} = 10 V	-	-	10	µA
V_{PSF}	Protection supply threshold voltage	V_{FF} = 5 V; R_F = 3 kΩ;				
		BUK104-50L	2.5	3.3	4	V
		BUK104-50S	3.3	4.2	5	V
$V_{(CL)FS}$	Flag clamping voltage	I_F = 1 mA; V_{PS} = 0 V	11	13	-	V
	Application information					
R_F	Suitable external pull-up resistance	V_{FF} =5 V	1	10	50	kΩ
		V_{FF} =10 V	2	20	100	kΩ

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

1 Even if the flag pin is not used, it is recommended that it is connected to the protection supply via a pull-up resistor. It should not be left floating.

2 Low pass filtering of the flag signal may be advisable to prevent false tripping.

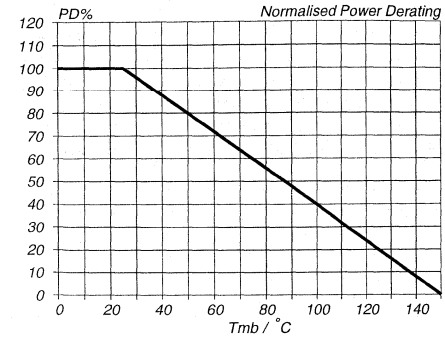


Fig.4. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

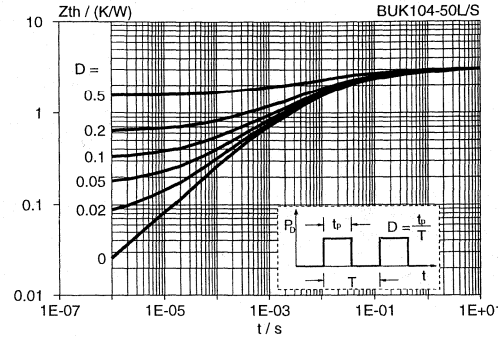


Fig.7. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

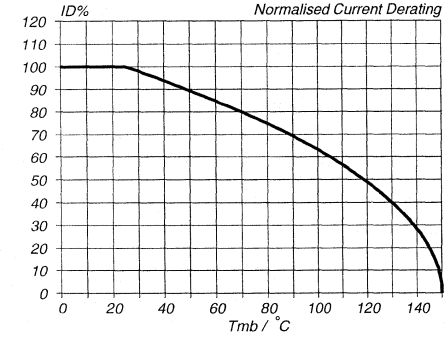


Fig.5. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

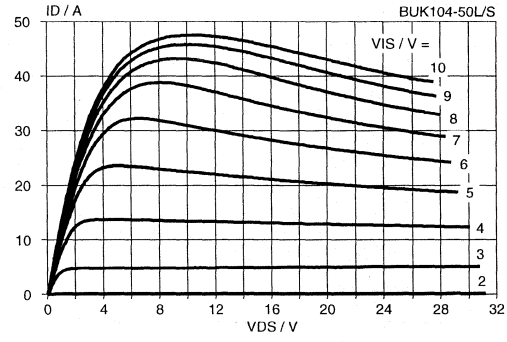


Fig.8. Typical output characteristics, $T_j = 25\ ^\circ C$.
ID = $f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$ & $t_p < t_{d\,sc}$

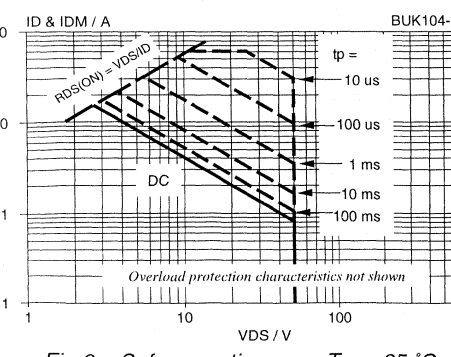


Fig.6. Safe operating area. $T_{mb} = 25\ ^\circ C$
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

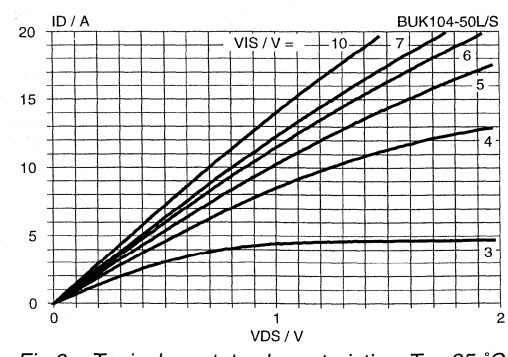


Fig.9. Typical on-state characteristics, $T_j = 25\ ^\circ C$.
$I_D = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$

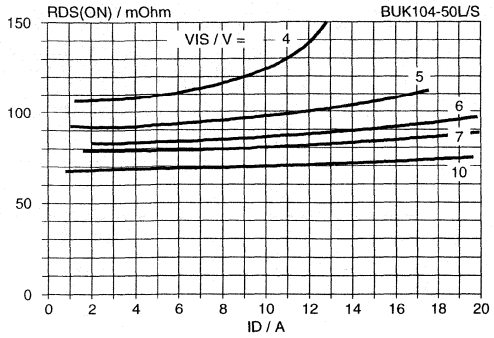


Fig.10. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

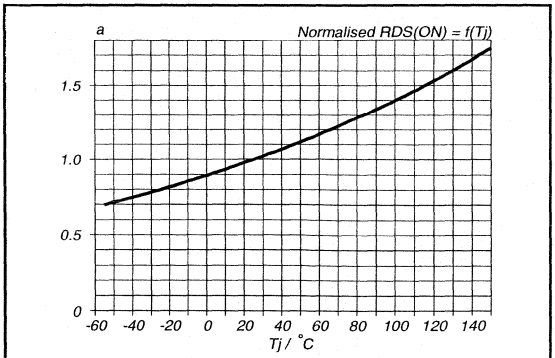


Fig.13. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25\ ˚C = f(T_j)$; I_D = 7.5 A; $V_{IS} \geq 5$ V

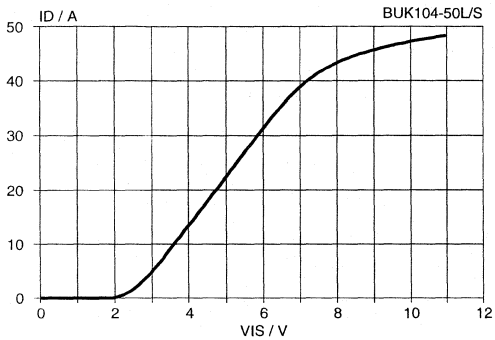


Fig.11. Typical transfer characteristics, T_j = 25 ˚C. $I_D = f(V_{IS})$; conditions: V_{DS} = 10 V; t_p = 250 µs

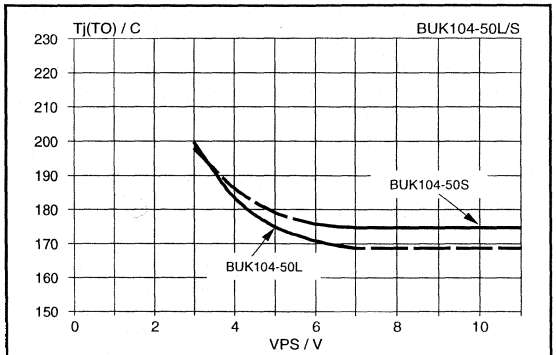


Fig.14. Typical over temperature protection threshold $T_{j(TO)} = f(V_{PS})$; conditions: V_{DS} > 0.1 V

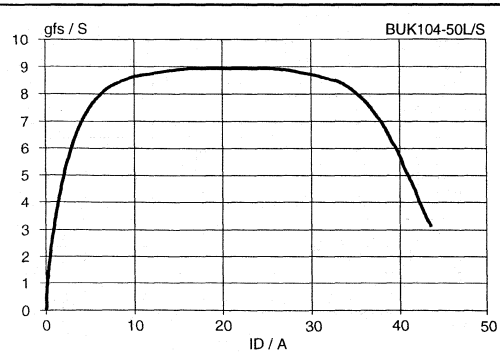


Fig.12. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V; t_p = 250 µs

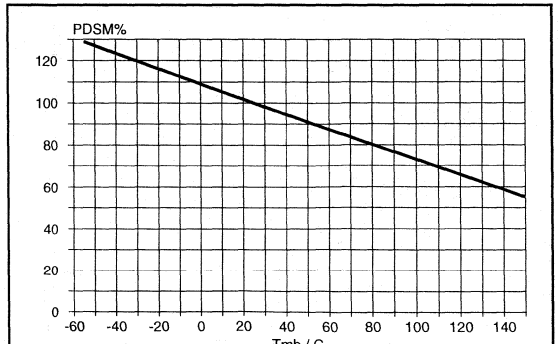


Fig.15. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ ˚C) = f(T_{mb})$

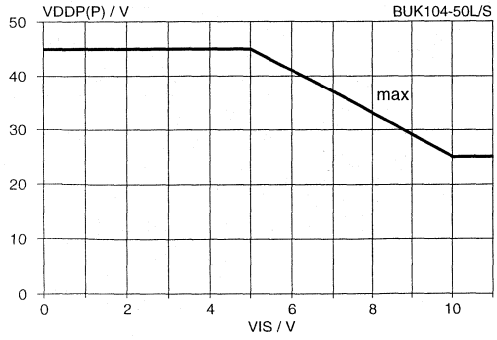


Fig.16. Maximum drain source supply voltage for SC load protection. $V_{DDP(P)} = f(V_{IS})$; $T_{mb} \leq 150$ ˚C

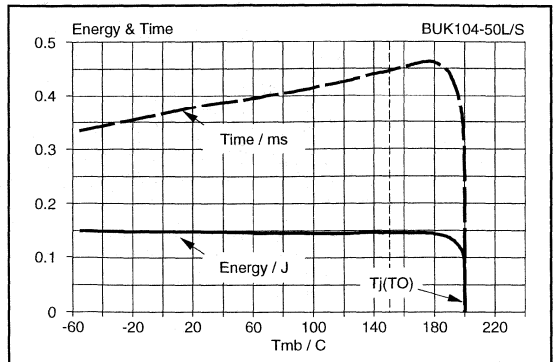


Fig.19. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; $V_{PS} = V_{PSN}$, V_{IS} = 7 V; SC load

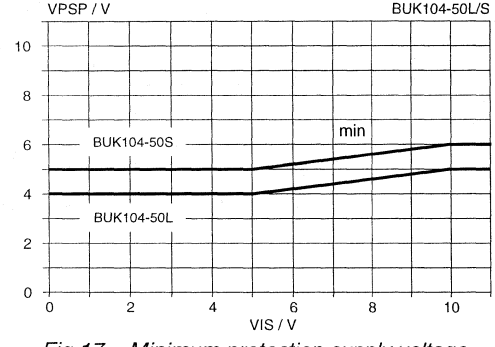


Fig.17. Minimum protection supply voltage for SC load protection. $V_{PSP} = f(V_{IS})$; $T_{mb} \geq 25$ ˚C

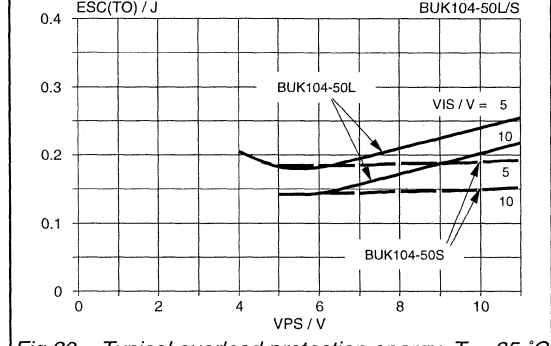


Fig.20. Typical overload protection energy, T_j = 25 ˚C $E_{SC(TO)} = f(V_{PS})$; conditions: V_{DS} = 13 V, parameter V_{IS}

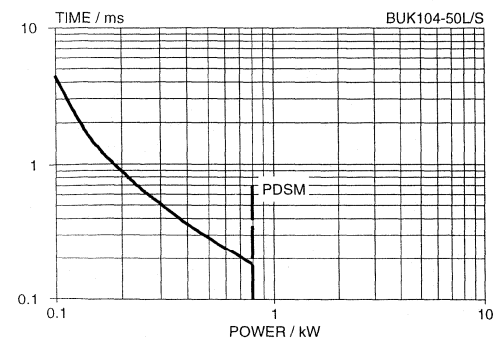


Fig.18. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{PS} \geq V_{PSP}$; $V_{IS} \geq 5$ V

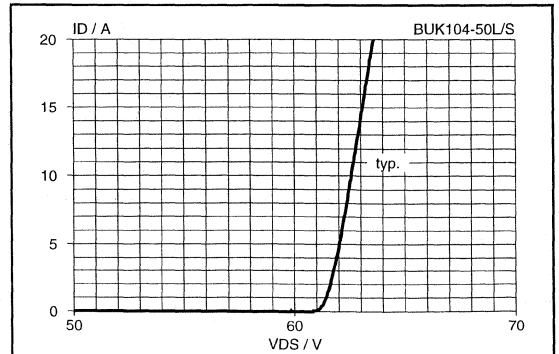


Fig.21. Typical clamping characteristics, 25 ˚C. $I_D = f(V_{DS})$; conditions: R_{IS} = 100 Ω; $t_p \leq 50$ µs

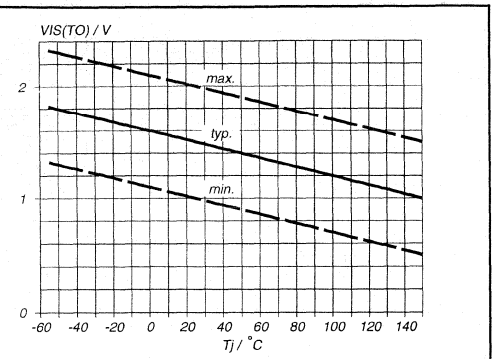


Fig.22. Input threshold voltage.
$V_{IS(TO)} = f(T_j)$; *conditions:* $I_D = 1$ *mA;* $V_{DS} = 5$ *V*

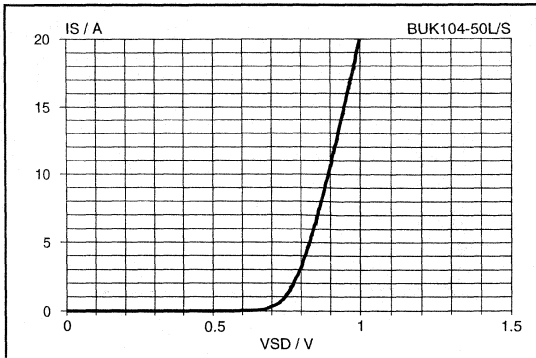


Fig.25. Typical reverse diode current, $T_j = 25$ *°C.*
$I_S = f(V_{SDS})$; *conditions:* $V_{IS} = 0$ *V;* $t_p = 250$ *µs*

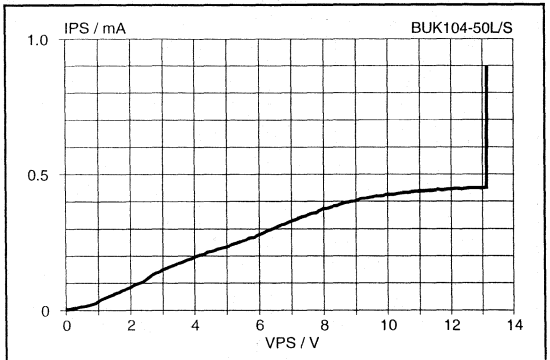


Fig.23. Typical DC protection supply characteristics.
$I_{PS} = f(V_{PS})$; *normal or overload operation;* $T_j = 25$ *°C*

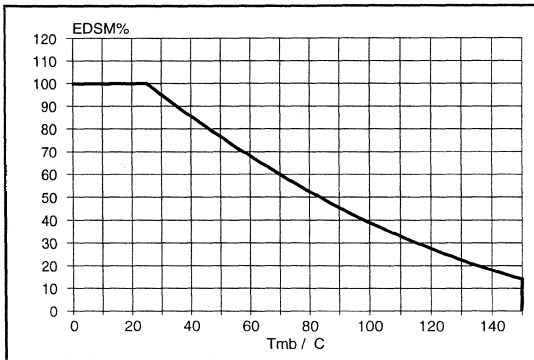


Fig.26. Normalised limiting clamping energy.
$E_{DSM}\% = f(T_{mb})$; *conditions:* $I_D = 15$ *A*

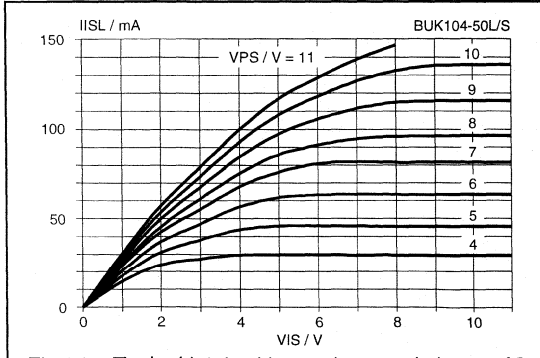


Fig.24. Typical latched input characteristics, 25 °C.
$I_{ISL} = f(V_{IS})$; *after overload protection latched*

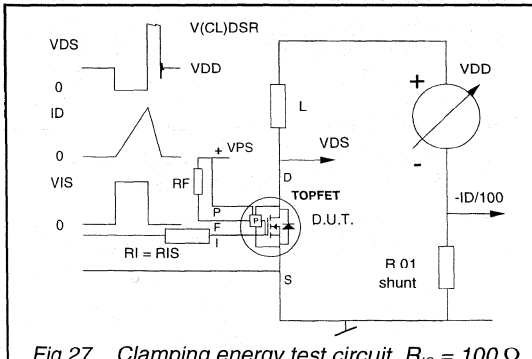


Fig.27. Clamping energy test circuit, $R_{IS} = 100\ \Omega$.
$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSR}/(V_{(CL)DSR} - V_{DD})$

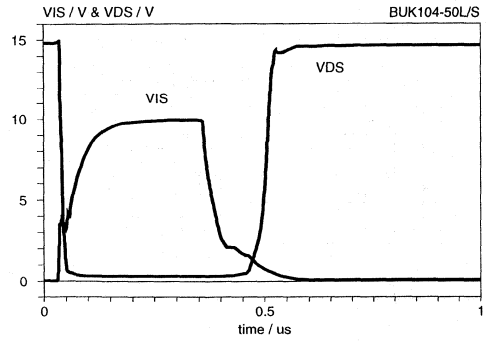


Fig.28. Typical resistive load switching waveforms $R_I = R_{IS} = 50\ \Omega$; $R_L = 10\ \Omega$; $V_{DD} = 15$ V; $T_j = 25$ °C

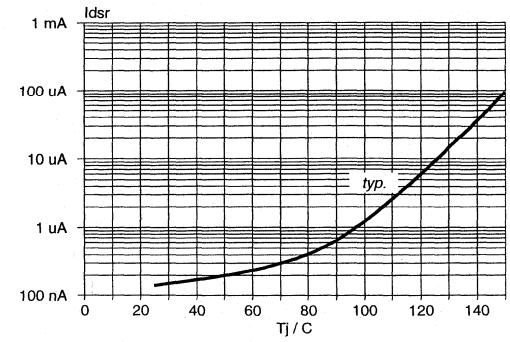


Fig.31. Typical off-state leakage current. $I_{DSR} = f(T_j)$; Conditions: $V_{DS} = 40$ V; $R_{IS} = 100\ \Omega$.

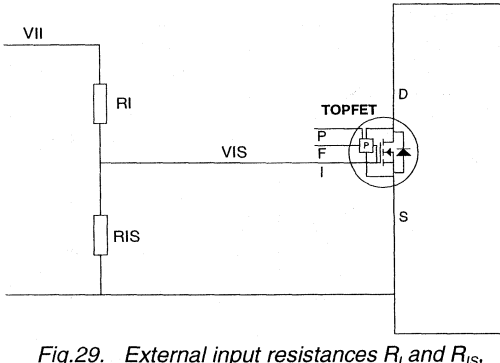


Fig.29. External input resistances R_I and R_{IS}, generator voltage V_{II} and input voltage V_{IS}.

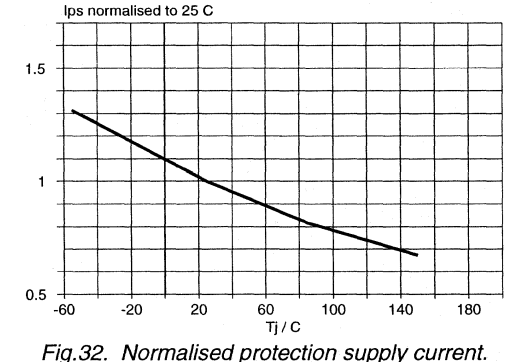


Fig.32. Normalised protection supply current. $I_{PS}/I_{PS}25$ °C $= f(T_j)$; $V_{PS} = V_{PSN}$

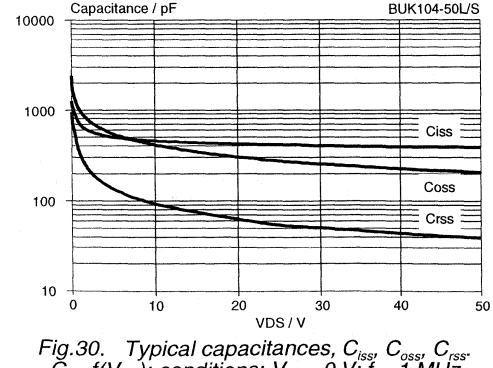


Fig.30. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: $V_{IS} = 0$ V; $f = 1$ MHz

PowerMOS transistor
Logic level TOPFET

BUK106-50L/S
BUK106-50LP/SP

For maintenance only. Do not use for design-in.

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 5 pin plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	50	A
P_{tot}	Total power dissipation	125	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance		
	V_{IS} = 5 V	35	mΩ
	V_{IS} = 8 V	28	mΩ
SYMBOL	**PARAMETER**	**NOM.**	**UNIT**
V_{PSN}	Protection supply voltage		
	BUK106-50L	5	V
	BUK106-50S	10	V

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Logic and protection supply from separate pin
- Low operating supply current
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by protection supply
- Protection circuit condition indicated by flag pin
- 5 V logic compatible input level
- Separate input pin for higher frequency drive
- ESD protection on input, flag and protection supply pins
- Over voltage clamping for turn off of inductive loads
- Both linear and switching operation are possible

FUNCTIONAL BLOCK DIAGRAM

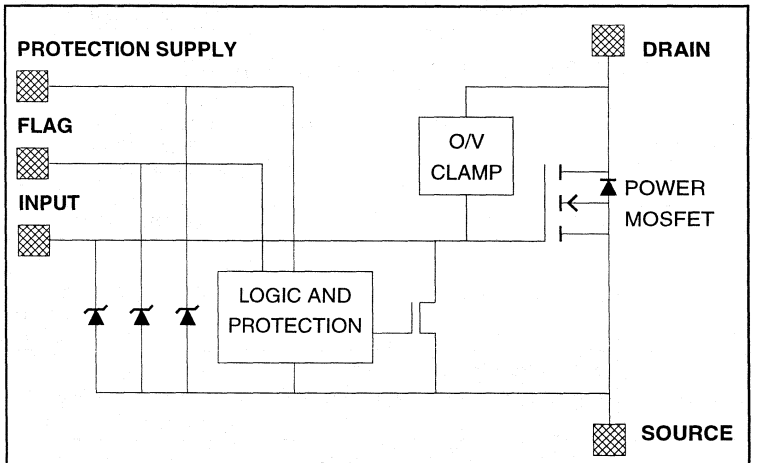


Fig.1. Elements of the TOPFET.

PINNING - SOT263

PIN	DESCRIPTION
1	input
2	flag
3	drain
4	protection supply
5	source
tab	drain

PIN CONFIGURATION

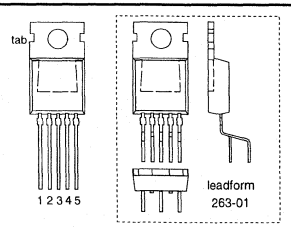


Fig. 2. Type numbers ending with suffix P refer to leadform 263-01.

SYMBOL

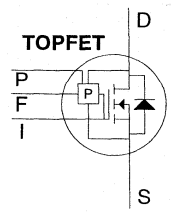


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
	Voltages					
V_{DSS}	Continuous off-state drain source voltage[1]	V_{IS} = 0 V	-	50		V
V_{IS}	Continuous input voltage	-	0	11		V
V_{FS}	Continuous flag voltage	-	0	11		V
V_{PS}	Continuous supply voltage	-	0	11		V
	Currents	V_{IS} =	-	8	5	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C	-	50	45	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C	-	31	28	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C	-	200	180	A
	Thermal					
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125		W
T_{stg}	Storage temperature	-	-55	150		°C
T_j	Junction temperature[2]	continuous	-	150		°C
T_{sold}	Lead temperature	during soldering	-	250		°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply connected, TOPFET can protect itself from two types of overload - over temperature and short circuit load.

An n-MOS transistor turns on between the input and source to quickly discharge the power MOSFET gate capacitance.

For internal overload protection to remain latched while the control circuit is high, external series input resistance must be provided. Refer to INPUT CHARACTERISTICS.

SYMBOL	PARAMETER	CONDITIONS	MIN.		MAX.	UNIT
		V_{IS} =	8	5	-	V
V_{PSP}	Protection supply voltage[3]	for valid protection				
		BUK106-50L	4.4	4	-	V
		BUK106-50S	5.4	5	-	V
	Over temperature protection	$V_{PS} = V_{PSN}$				
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 10 V; $R_I \geq 2$ kΩ	-		50	V
		V_{IS} = 5 V; $R_I \geq 1$ kΩ	-		50	V
	Short circuit load protection	$V_{PS} = V_{PSN}$; L ≤ 10 µH				
$V_{DDP(P)}$	Protected drain source supply voltage[4]	V_{IS} = 10 V; $R_I \geq 2$ kΩ	-		24	V
		V_{IS} = 5 V; $R_I \geq 1$ kΩ	-		45	V
P_{DSM}	Instantaneous overload dissipation		-		4	kW

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The minimum supply voltage required for correct operation of the overload protection circuits.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DRRM}	Repetitive peak clamping drain current	$R_{IS} \geq 100\ \Omega$[1]	-	50	A
E_{DSM}	Non-repetitive inductive turn-off energy[2]	$I_{DM} = 27$ A; $R_{IS} \geq 100\ \Omega$	-	1	J
E_{DRM}	Repetitive inductive turn-off energy	$R_{IS} \geq 100\ \Omega$; $T_{mb} \leq 85$ °C; $I_{DM} = 16$ A; $V_{DD} \leq 20$ V; f = 250 Hz	-	80	mJ
I_{DIRM}	Repetitive peak drain to input current[3]	$R_{IS} = 0\ \Omega$; $t_p \leq 1$ ms	-	50	mA

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} = 25$ °C; $V_{IS} = V_{PS} = V_{FS} = 0$ V	-	50	A

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	0.8	1.0	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

$T_{mb} = 25$ °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSR}$	Drain-source clamping voltage	$R_{IS} = 100\ \Omega$; $I_D = 10$ mA		50	-	65	V
$V_{(CL)DSR}$	Drain-source clamping voltage	$R_{IS} = 100\ \Omega$; $I_{DM} = 1$ A; $t_p \leq 300\ \mu$s; $\delta \leq 0.01$		50	-	70	V
I_{DSS}	Zero input voltage drain current	$V_{DS} = 12$ V; $V_{IS} = 0$ V		-	0.5	10	µA
I_{DSR}	Drain source leakage current	$V_{DS} = 50$ V; $R_{IS} = 100\ \Omega$;		-	1	20	µA
I_{DSR}	Drain source leakage current	$V_{DS} = 40$ V; $R_{IS} = 100\ \Omega$; $T_j = 125$ °C		-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	$I_{DM} = 25$ A; $t_p \leq 300\ \mu$s; $\delta \leq 0.01$	$V_{IS} = 8$ V	-	22	28	mΩ
			$V_{IS} = 5$ V	-	28	35	mΩ

1 The input pin must be connected to the source pin by a specified external resistance to allow the power MOSFET gate source voltage to become sufficiently positive for active clamping. Refer to INPUT CHARACTERISTICS.

2 While the protection supply voltage is connected, during overvoltage clamping it is possible that the overload protection may operate at energies close to the limiting value. Refer to OVERLOAD PROTECTION CHARACTERISTICS.

3 Shorting the input to source with low resistance inhibits the internal overvoltage protection by preventing the power MOSFET gate source voltage becoming positive.

OVERLOAD PROTECTION CHARACTERISTICS

With adequate protection supply voltage TOPFET detects when one of the overload thresholds is exceeded.

Provided there is adequate input series resistance it switches off and remains latched off until reset by the protection supply pin.

Refer also to OVERLOAD PROTECTION LIMITING VALUES and INPUT CHARACTERISTICS.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	$V_{PS} = V_{PSN}$[2]; $T_{mb} = 25$ °C; $L \leq 10$ µH				
$E_{DS(TO)}$	Overload threshold energy	$V_{DD} = 13$ V; $V_{IS} = 10$ V	-	550	-	mJ
$t_{d\,sc}$	Response time	$V_{DD} = 13$ V; $V_{IS} = 10$ V	-	0.4	-	ms
	Over temperature protection	$V_{PS} = V_{PSN}$				
$T_{j(TO)}$	Threshold junction temperature	from $I_D \geq 2.5$ A[3]	150	-	-	°C

TRANSFER CHARACTERISTICS

$T_{mb} = 25$ °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 12$ V; $I_{DM} = 25$ A $t_p \leq 300$ µs; $\delta \leq 0.01$	17	28	-	S
I_D	Drain current[4]	$V_{DS} = 13$ V; $V_{IS} = 5$ V	-	80	-	A
		$V_{IS} = 10$ V		160	-	A

PROTECTION SUPPLY CHARACTERISTICS

$T_{mb} = 25$ °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Protection supply					
I_{PS}, I_{PSL}	Protection supply current	normal operation or protection latched				
		BUK106-50L $V_{PS} = 5$ V	-	0.2	0.35	mA
		BUK106-50S $V_{PS} = 10$ V	-	0.4	1.0	mA
V_{PSR}	Protection reset voltage[5]		1.5	2.5	3.5	V
		$T_j = 150$ °C	1.0	-	-	V
$V_{(CL)PS}$	Protection clamp voltage	$I_P = 1.35$ mA	11	13	-	V

REVERSE DIODE CHARACTERISTICS

$T_{mb} = 25$ °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	$I_S = 20$ A; $V_{IS} = V_{PS} = V_{FS} = 0$ V; $t_p = 300$ µs	-	0.9	1.2	V
t_{rr}	Reverse recovery time	not applicable[6]	-	-	-	-

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum.

2 At the appropriate nominal protection supply voltage for each type. Refer to QUICK REFERENCE DATA.

3 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

4 During overload condition. Refer also to OVERLOAD PROTECTION LIMITING VALUES and CHARACTERISTICS.

5 The supply voltage below which the overload protection circuits will be reset.

6 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
	Normal operation						
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA		1.0	1.5	2.0	V
			T_{mb} = 150 °C	0.5	-	-	V
I_{IS}	Input current	V_{IS} = 10 V		-	10	100	nA
$V_{(CL)IS}$	Input clamp voltage	I_I = 1 mA		11	13	-	V
	Overload protection latched						
R_{ISL}	Input resistance[1]	V_{PS} = 5 V	I_I = 5 mA;	-	55	-	Ω
			T_{mb} = 150 °C	-	95	-	Ω
		V_{PS} = 10 V	I_I = 5 mA;	-	35	-	Ω
			T_{mb} = 150 °C	-	60	-	Ω
	Application information						
	External input resistances for	(see figure 29)					
R_{IS}	internal overvoltage clamping[2]	R_I = ∞ Ω;	V_{DS} > 30 V	100	-	-	Ω
R_I	internal overload protection[3]	R_{IS} = ∞ Ω;	V_{II} = 5 V	1	-	-	kΩ
			V_{II} = 10 V	2	-	-	kΩ

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C; R_I = 50 Ω; R_{IS} = 50 Ω (see figure 29); resistive load R_L = 10 Ω. For waveforms see figure 28.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 15 V; V_{IS}: 0 V ⇒ 10 V	-	10	-	ns
t_r	Rise time		-	35	-	ns
$t_{d\,off}$	Turn-off delay time	V_{DD} = 15 V; V_{IS}: 10 V ⇒ 0 V	-	280	-	ns
t_f	Fall time		-	120	-	ns

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{iss}	Input capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	1250	1800	pF
C_{oss}	Output capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	650	1000	pF
C_{rss}	Reverse transfer capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	150	250	pF
C_{pso}	Protection supply pin capacitance	V_{PS} = 10 V	-	30	-	pF
C_{fso}	Flag pin capacitance	V_{FS} = 10 V; V_{PS} = 0 V	-	20	-	pF

1 The resistance of the internal transistor which discharges the power MOSFET gate capacitance when overload protection operates.
The external drive circuit should be such that the input voltage does not exceed $V_{IS(TO)}$ minimum when the overload protection has operated. Refer also to figure for latched input characteristics.

2 Applications using a lower value for R_{IS} would require external overvoltage protection.

3 For applications requiring a lower value for R_I, an external overload protection strategy is possible using the flag pin to 'tell' the control circuit to switch off the input.

FLAG DESCRIPTION

The flag pin provides a means to detect the presence of the protection supply and indicate the state of the overload detectors. The flag is the open drain of an n-MOS transistor and requires an external pull-up resistor[1]. It is suitable for both 5 V and 10 V logic. Flag may be used to implement an external protection strategy[2] for applications which require low input drive impedance.

TRUTH TABLE

CONDITION	DESCRIPTION	FLAG
NORMAL	Normal operation and adequate protection supply voltage	LOGIC LOW
OVER TEMP.	Over temperature detected	LOGIC HIGH
SHORT CIRCUIT	Overload condition detected	LOGIC HIGH
SUPPLY FAULT	Inadequate protection supply voltage	LOGIC HIGH

FLAG CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Flag 'low'	normal operation				
V_{FS}	Flag voltage	I_F = 1.6 mA	-	0.15	0.4	V
I_{FSS}	Flag saturation current	V_{FS} = 10 V	-	15	-	mA
	Flag 'high'	overload or fault				
I_{FS}	Flag leakage current	V_{FS} = 10 V	-	-	10	µA
V_{PSF}	Protection supply threshold voltage	V_{FF} = 5 V; R_F = 3 kΩ;				
		BUK106-50L	2.5	3.3	4	V
		BUK106-50S	3.3	4.2	5	V
$V_{(CL)FS}$	Flag clamping voltage	I_F = 1 mA; V_{PS} = 0 V	11	13	-	V
	Application information					
R_F	Suitable external pull-up resistance	V_{FF} =5 V	1	10	50	kΩ
		V_{FF} =10 V	2	20	100	kΩ

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

1 Even if the flag pin is not used, it is recommended that it is connected to the protection supply via a pull-up resistor. It should not be left floating.

2 Low pass filtering of the flag signal may be advisable to prevent false tripping.

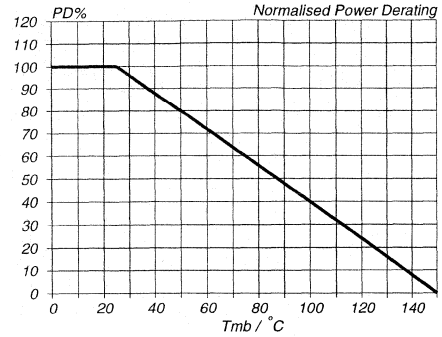


Fig.4. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

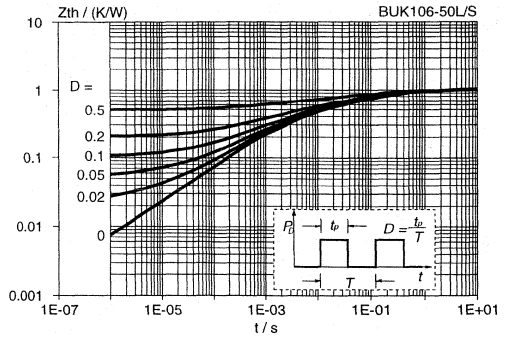


Fig.7. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

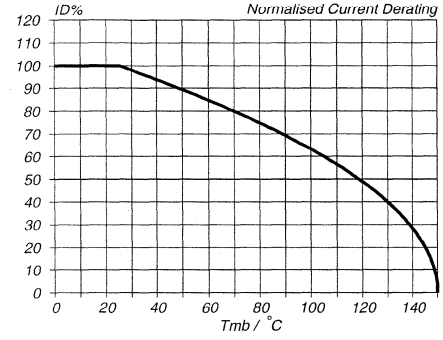


Fig.5. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

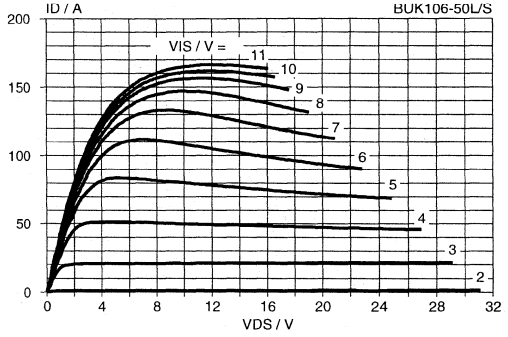


Fig.8. Typical output characteristics, $T_j = 25$ °C.
ID = $f(V_{DS})$; parameter V_{IS}; $t_p = 250$ µs & $t_p < t_{d\,sc}$

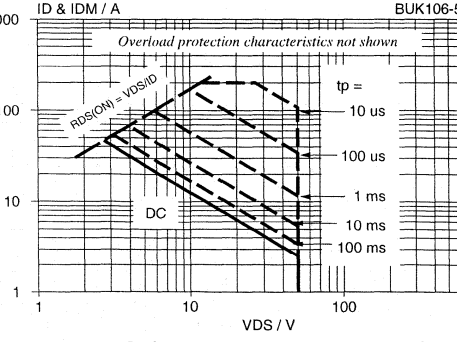


Fig.6. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

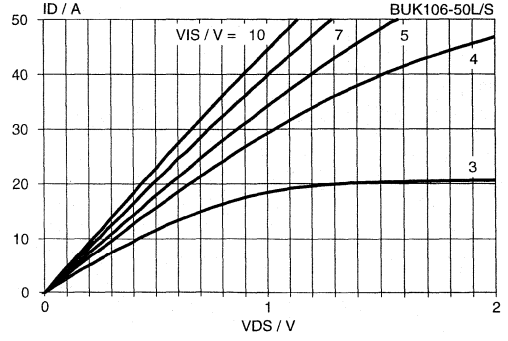


Fig.9. Typical on-state characteristics, $T_j = 25$ °C.
$I_D = f(V_{DS})$; parameter V_{IS}; $t_p = 250$ µs

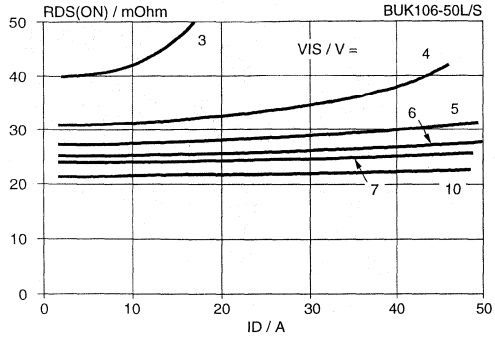


Fig.10. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

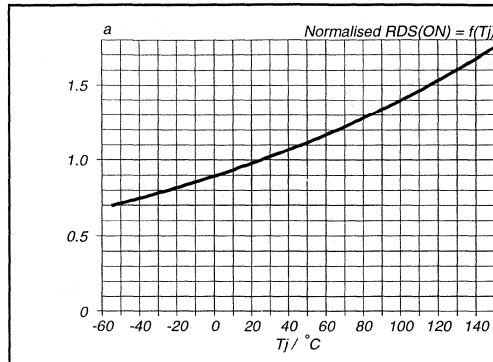


Fig.13. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25\ ^{\circ}C = f(T_j)$; I_D = 25 A; $V_{IS} \geq$ 5 V

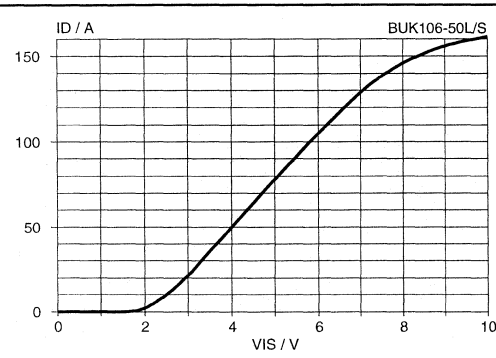


Fig.11. Typical transfer characteristics, T_j = 25 ˚C. $I_D = f(V_{IS})$; conditions: V_{DS} = 12 V; t_p = 250 µs

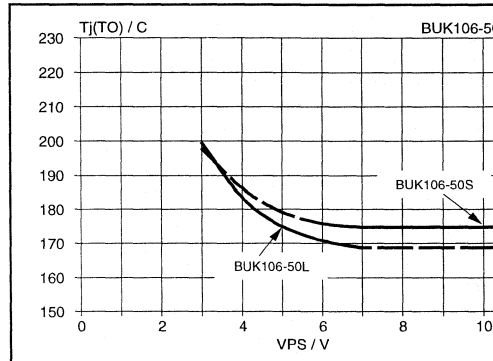


Fig.14. Typical over temperature protection threshold $T_{j(TO)} = f(V_{PS})$; conditions: V_{DS} > 0.1 V

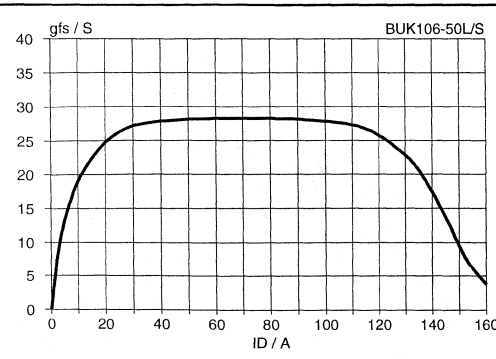


Fig.12. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 12 V; t_p = 250 µs

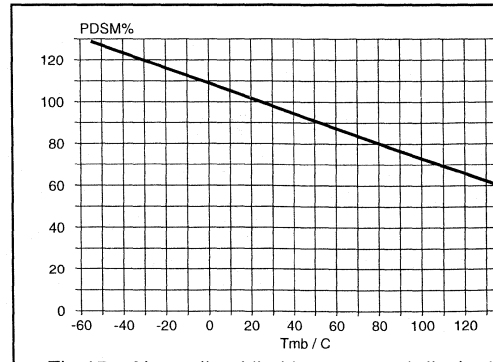


Fig.15. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ ^{\circ}C) = f(T_{mb})$

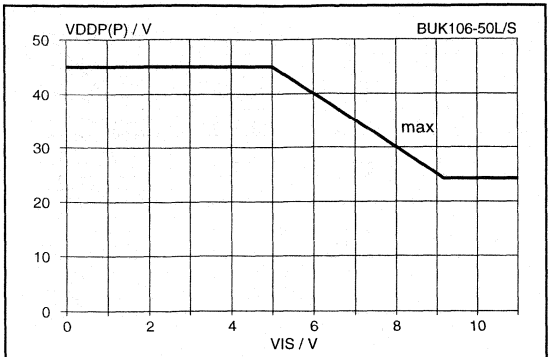


Fig.16. Maximum drain source supply voltage for SC load protection. $V_{DDP(P)} = f(V_{IS})$; $T_{mb} \leq 150$ °C

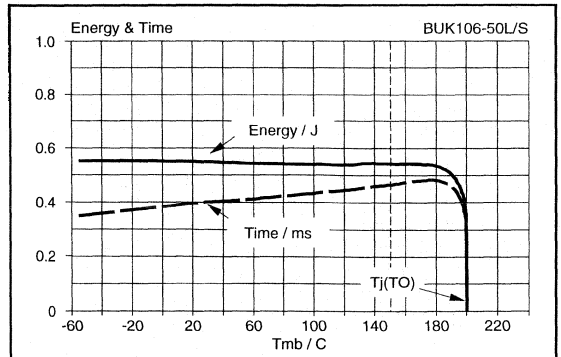


Fig.19. Typical overload protection characteristics. Conditions: $V_{DD} = 13$ V; $V_{PS} = V_{PSN}$, $V_{IS} = 8$ V; SC load

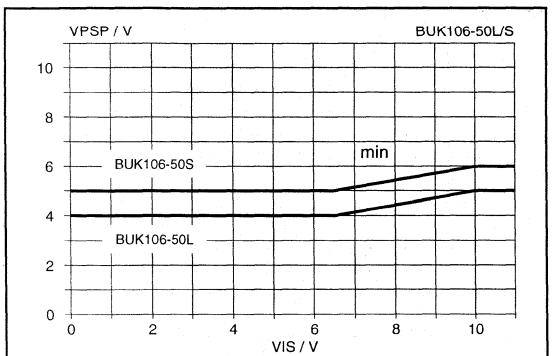


Fig.17. Minimum protection supply voltage for SC load protection. $V_{PSP} = f(V_{IS})$; $T_{mb} \geq 25$ °C

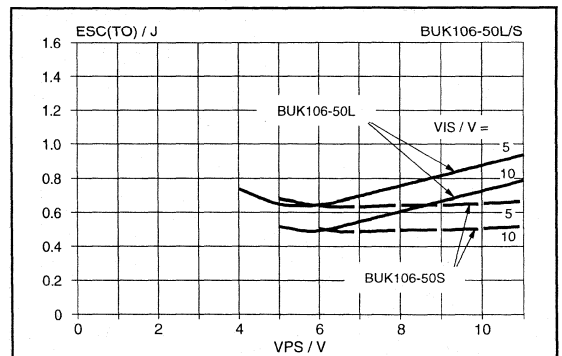


Fig.20. Typical overload protection energy, $T_j = 25$ °C $E_{SC(TO)} = f(V_{PS})$; conditions: $V_{DS} = 13$ V, parameter V_{IS}

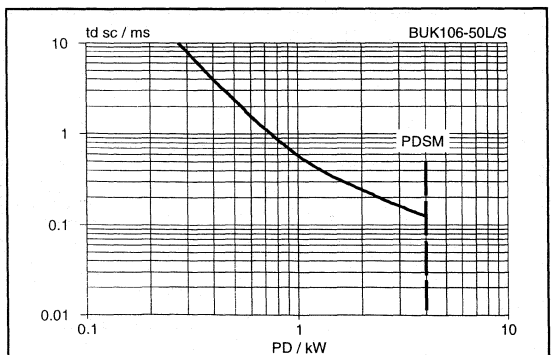


Fig.18. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{PS} \geq V_{PSP}$; $V_{IS} \geq 5$ V

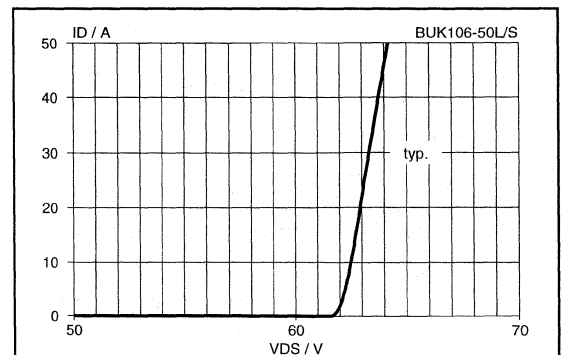


Fig.21. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: $R_{IS} = 100\ \Omega$; $t_p \leq 50\ \mu s$

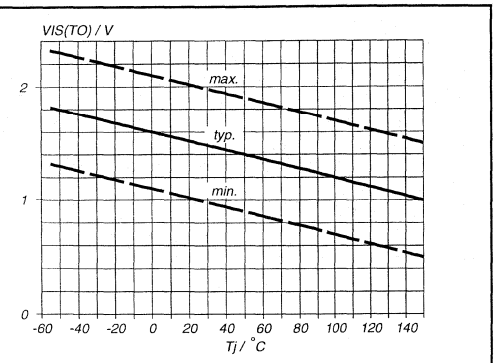


Fig.22. Input threshold voltage.
$V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

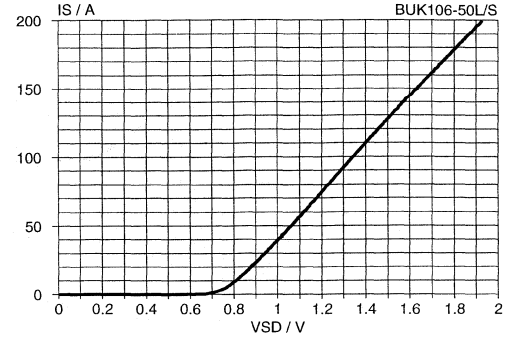


Fig.25. Typical reverse diode current, T_j = 25 °C.
$I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V; t_p = 250 µs

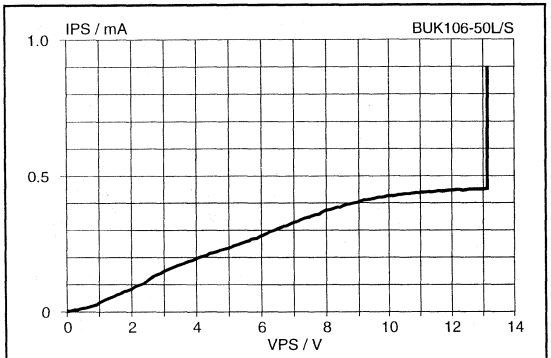


Fig.23. Typical DC protection supply characteristics.
$I_{PS} = f(V_{PS})$; normal or overload operation; T_j = 25 °C

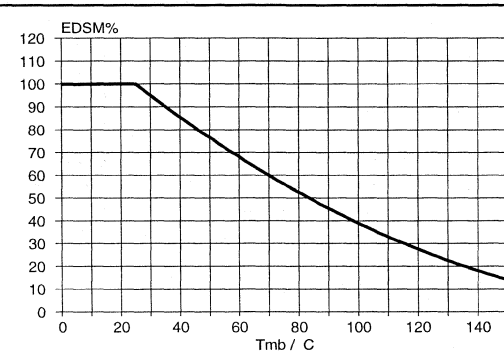


Fig.26. Normalised limiting clamping energy.
E_{DSM}% = $f(T_{mb})$; conditions: I_D = 27 A

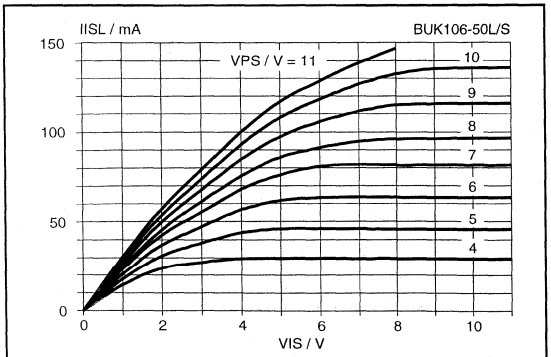


Fig.24. Typical latched input characteristics, 25 °C.
$I_{ISL} = f(V_{IS})$; after overload protection latched

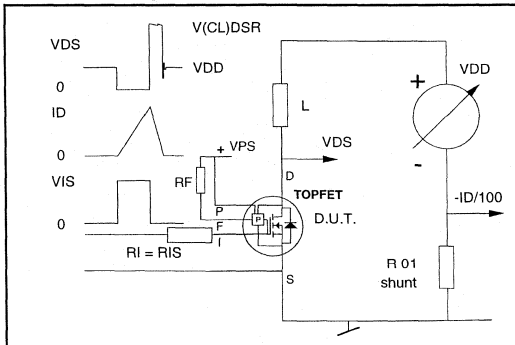


Fig.27. Clamping energy test circuit, R_{IS} = 100 Ω.
$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSR}/(V_{(CL)DSR} - V_{DD})$

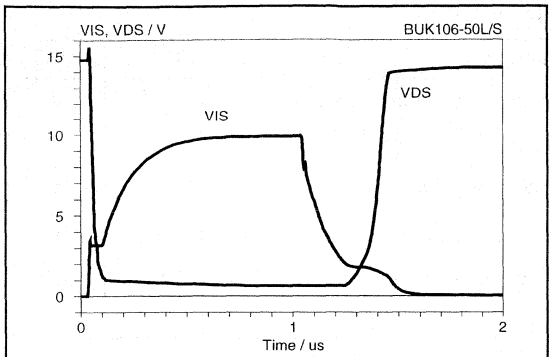


Fig.28. Typical resistive load switching waveforms $R_I = R_{IS} = 50\ \Omega$; $R_L = 10\ \Omega$; $V_{DD} = 15$ V; $T_j = 25$ ˚C

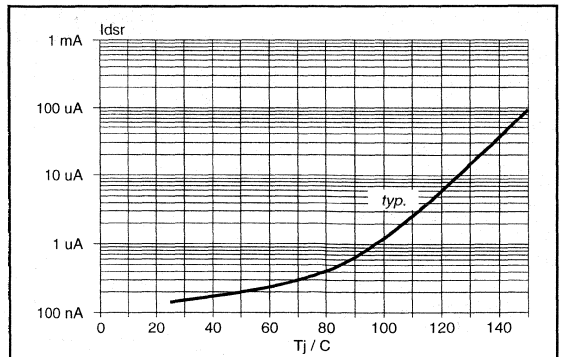


Fig.31. Typical off-state leakage current. $I_{DSR} = f(T_j)$; Conditions: $V_{DS} = 40$ V; $R_{IS} = 100\ \Omega$.

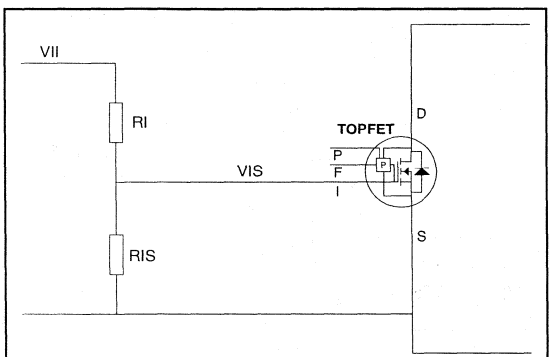


Fig.29. External input resistances R_I and R_{IS}, generator voltage V_{II} and input voltage V_{IS}.

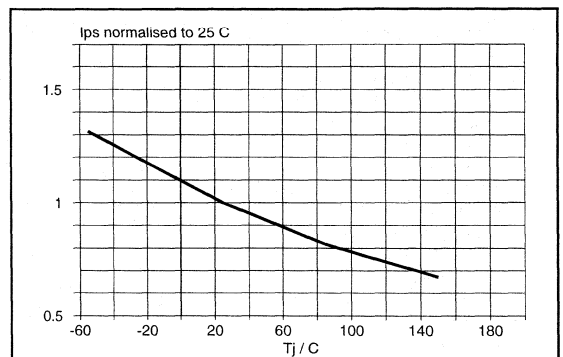


Fig.32. Normalised protection supply current. $I_{PS}/I_{PS}25\ ^{\circ}C = f(T_j)$; $V_{PS} = V_{PSN}$

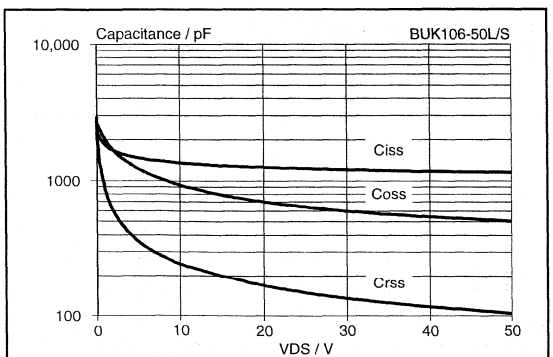


Fig.30. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: $V_{IS} = 0$ V; $f = 1$ MHz

PowerMOS transistor Logic level TOPFET

BUK107-50DL

For maintenance only. Do not use for design-in.

DESCRIPTION

Monolithic overload protected logic level power MOSFET in a surface mount plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- small motors
- solenoids

FEATURES

- Vertical power DMOS output stage
- Overload protected up to 85˚C ambient
- Overload protection by current limiting and overtemperature sensing
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Low operating input current permits direct drive by micro-controller
- ESD protection on all pins
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	0.7	A
P_D	Total power dissipation	1.8	W
T_j	Continuous junction temperature	150	˚C
$R_{DS(ON)}$	Drain-source on-state resistance	200	mΩ

FUNCTIONAL BLOCK DIAGRAM

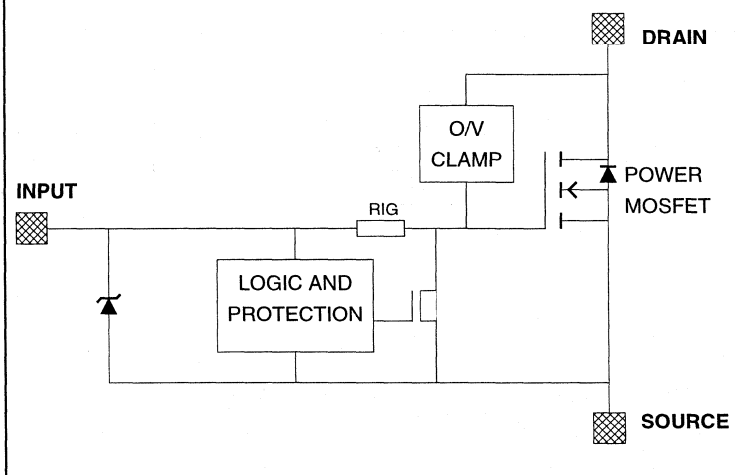
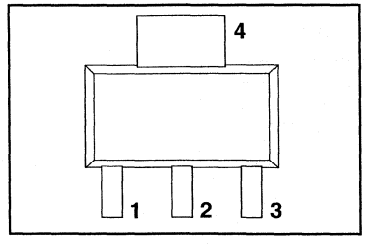


Fig.1. Elements of the TOPFET.

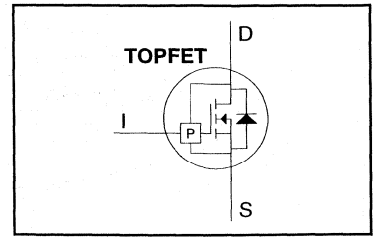
PINNING - SOT223

PIN	DESCRIPTION
1	input
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Continuous drain source voltage[1]	-	-	50	V
I_D	Continuous drain current[2]	-	-	self limiting	A
I_I	Continuous input current	clamping	-	3	mA
I_{IRM}	Non-repetitive peak input current	$t_p \leq 1$ ms	-	10	mA
P_D	Total power dissipation	$T_{amb} = 25$ °C	-	1.8	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature	normal operation[3]	-	150	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{DSM}	Non-repetitive clamping energy	$T_b \leq 25$ °C; $I_{DM} < I_{D(lim)}$; inductive load	-	100	mJ
E_{DRM}	Repetitive clamping energy	$T_b \leq 75$ °C; $I_{DM} = 50$ mA; f = 250 Hz	-	4	mJ

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from short circuit loads.
Overload protection operates by means of drain current limiting and activating the overtemperature protection.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDP}	Protected drain source supply voltage	$V_{IS} = 5$ V	-	35	V
		$V_{IS} = 4$ V	-	16	V

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off to protect itself when there is an overload fault condition.
It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Overload protection					
$I_{D(lim)}$	Drain current limiting	$V_{IS} = 5$ V	0.7	1.1	1.5	A
	Overtemperature protection	only in drain current limiting				
$T_{j(TO)}$	Threshold junction temperature	$V_{IS} = 5$ V	100	130	160	°C

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 Refer to OVERLOAD PROTECTION CHARACTERISTICS.

3 **Not** in an overload condition with drain current limiting.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}sp}$	Junction to solder point		-	12	18	K/W
$R_{th\ j\text{-}b}$	Junction to board[1]	Mounted on any PCB	-	40	-	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	Mounted on PCB of fig. 19	-	-	70	K/W

STATIC CHARACTERISTICS

T_b = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	55	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 200 mA; $t_p \le 300\ \mu s$; $\delta \le 0.01$	-	56	70	V
I_{DSS}	Off-state drain current	V_{DS} = 45 V; V_{IS} = 0 V	-	0.5	2	µA
I_{DSS}	Off-state drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Off-state drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 100 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance[2]	V_{IS} = 5 V; I_{DM} = 100 mA; $t_p \le 300\ \mu s$; $\delta \le 0.01$	-	150	200	mΩ

INPUT CHARACTERISTICS

T_b = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA		1.7	2.2	2.7	V
I_{IS}	Input supply current	normal operation;	V_{IS} = 5 V	-	330	450	µA
			V_{IS} = 4 V	-	170	270	µA
I_{ISL}	Input supply current	protection latched;	V_{IS} = 5 V	-	500	650	µA
			V_{IS} = 3.5 V	-	250	400	µA
V_{ISR}	Protection latch reset voltage[3]			1	2.2	3.5	V
$V_{(CL)IS}$	Input clamping voltage	I_I = 1.5 mA		6	7.5	-	V
R_{IG}	Input series resistance	to gate of power MOSFET		-	33	-	kΩ

SWITCHING CHARACTERISTICS

T_{amb} = 25 °C; resistive load R_L = 50 Ω; adjust V_{DD} to obtain I_D = 250 mA; refer to test circuit and waveforms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\ on}$	Turn-on delay time	V_{IS} = 0 V to V_{IS} = 5 V	-	8	-	µs
t_r	Rise time		-	30	-	µs
$t_{d\ off}$	Turn-off delay time	V_{IS} = 5 V to V_{IS} = 0 V	-	3	-	µs
t_f	Fall time		-	6	-	µs

1 Temperature measured 1.3 mm from tab.

2 Continuous input voltage. The specified pulse width is for the drain current.

3 The input voltage below which the overload protection circuits will be reset.

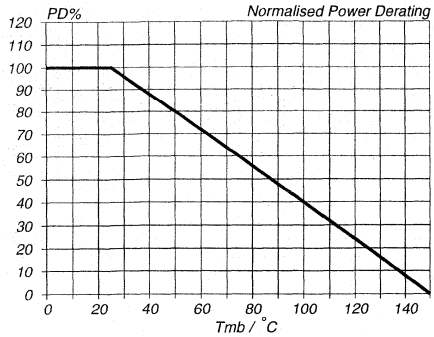


Fig.2. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

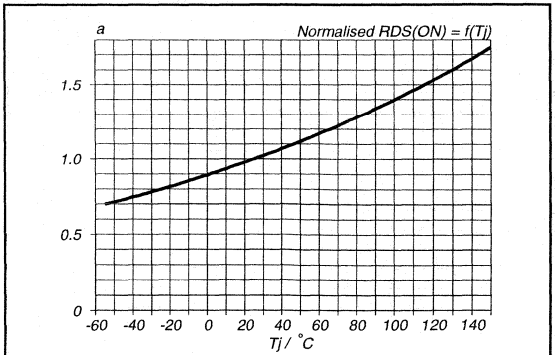


Fig.5. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25\ ^\circ C = f(T_j)$; I_D = 100 mA; V_{IS} = 5 V

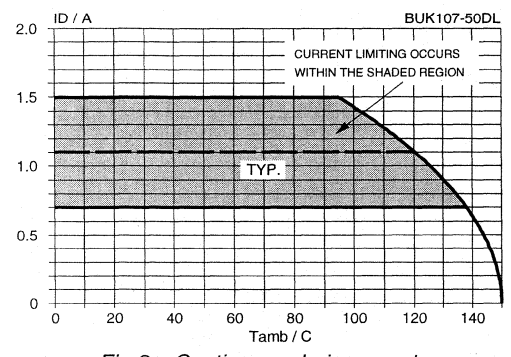


Fig.3. Continuous drain current. $I_D = f(T_{amb})$; condition: V_{IS} = 5 V

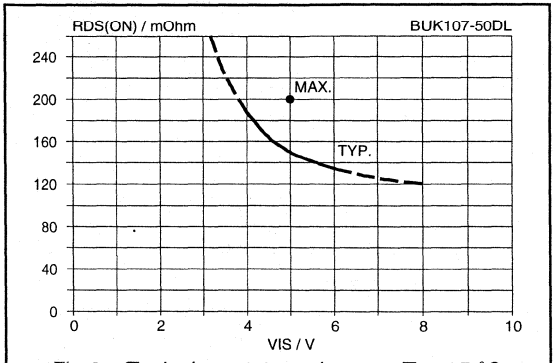


Fig.6. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(V_{IS})$; conditions: I_D = 100 mA, t_p = 300 µs

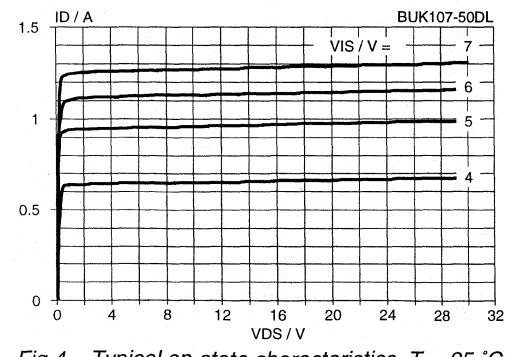


Fig.4. Typical on-state characteristics, T_j = 25 °C. $I_D = f(V_{DS})$; parameter V_{IS}; t_p = 300 µs

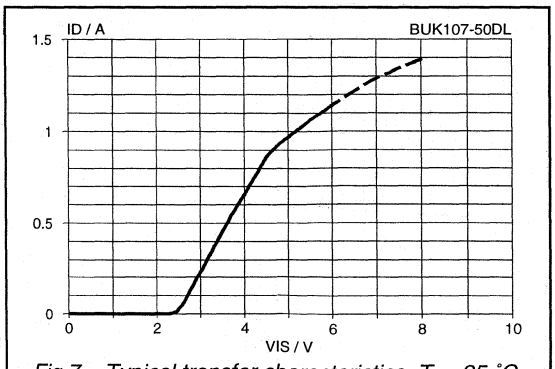


Fig.7. Typical transfer characteristics, T_j = 25 °C. $I_D = f(V_{IS})$; conditions: V_{DS} = 10 V, t_p = 300 µs

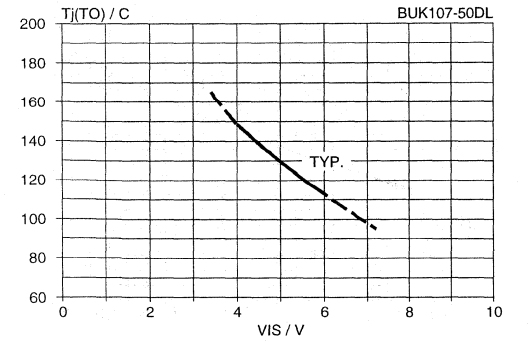


Fig.8. Typical overtemperature protection threshold.
$T_{j(TO)} = f(V_{IS})$; condition: V_{DS} = 10 V

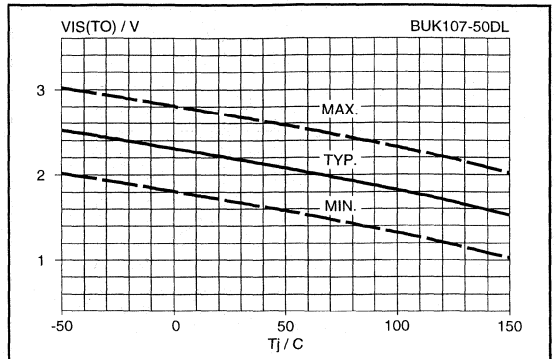


Fig.11. Input threshold voltage.
$V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

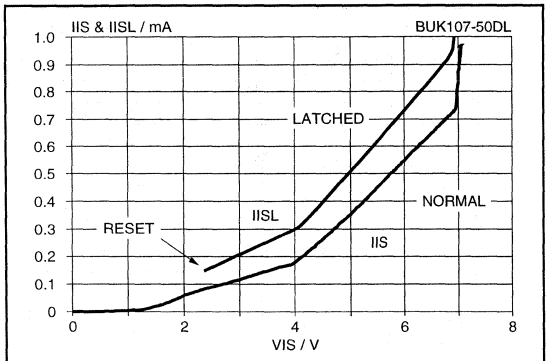


Fig.9. Typical DC input characteristics, T_j = 25 ˚C.
I_{IS} & $I_{ISL} = f(V_{IS})$; normal operation & protection latched

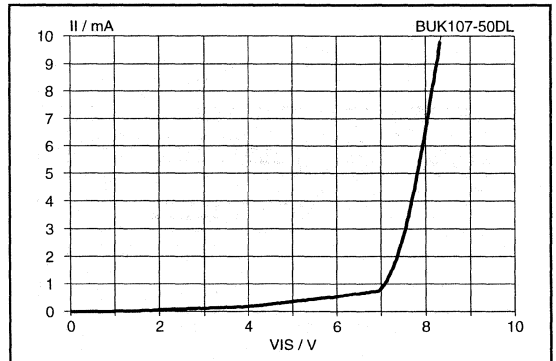


Fig.12. Typical input clamping characteristic.
$I_I = f(V_{IS})$; normal operation, T_j = 25 ˚C.

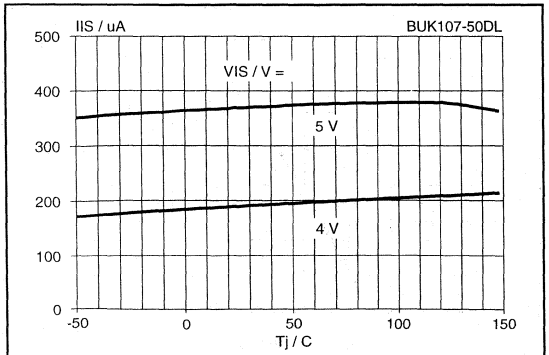


Fig.10. Typical DC input current.
$I_{IS} = f(T_j)$; parameter V_{IS}; normal operation

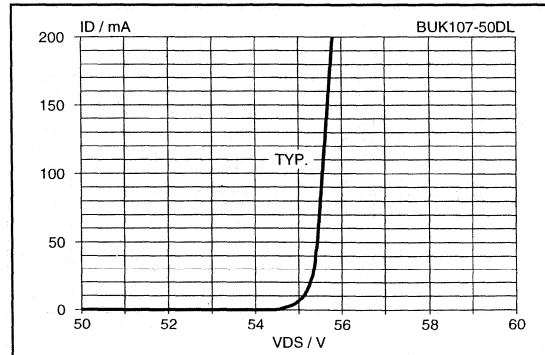


Fig.13. Overvoltage clamping characteristic, 25 ˚C.
$I_D = f(V_{DS})$; conditions: V_{IS} = 0 V; $t_p \leq 300$ µs

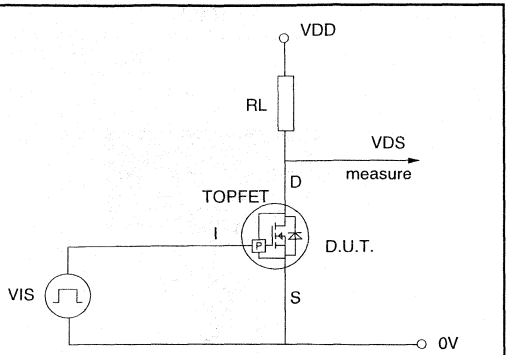


Fig.14. Test circuit for resistive load switching times. V_{IS} = 5 V

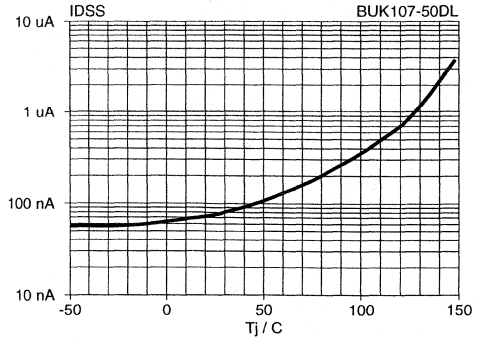


Fig.16. Typical drain source leakage current $I_{DSS} = f(T_j)$; conditions: V_{DS} = 40 V; V_{IS} = 0 V.

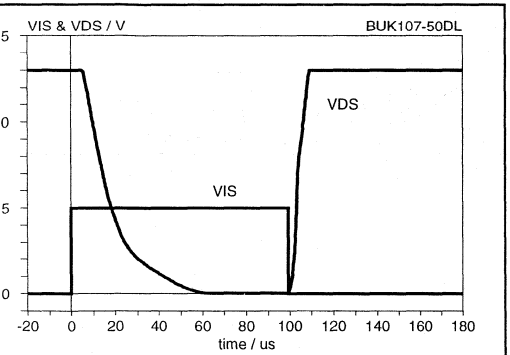


Fig.15. Typical switching waveforms, resistive load . R_L = 50 Ω; adjust V_{DD} to obtain I_D = 250 mA; T_j = 25˚C

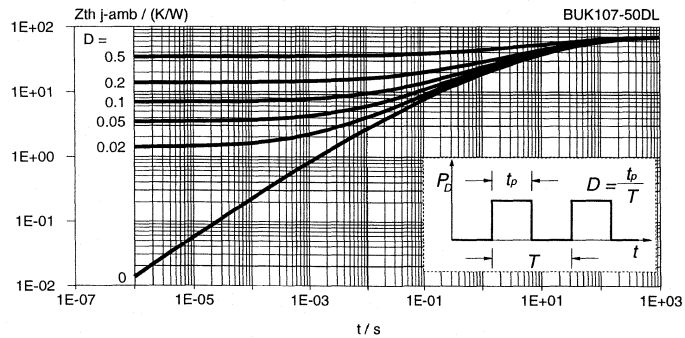


Fig.17. Transient thermal impedance, TOPFET mounted on PCB of fig 19. $Z_{th\ j\text{-}amb} = f(t)$; parameter $D = t_p/T$

MOUNTING INSTRUCTIONS

Dimensions in mm.

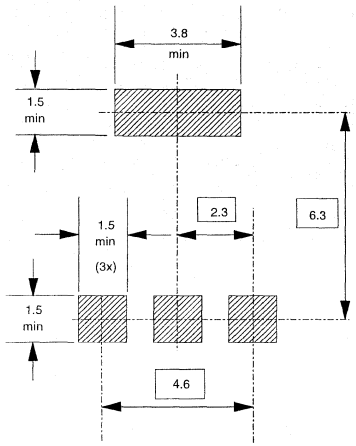


Fig.18. Soldering pattern for surface mounting.

PRINTED CIRCUIT BOARD

Dimensions in mm.

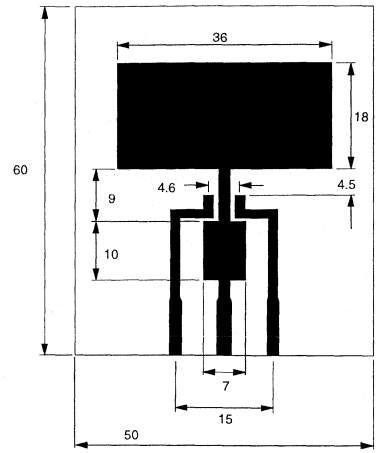


Fig.19. PCB for thermal resistance and power rating. PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).

PowerMOS transistor Logic level TOPFET

BUK107-50GL

For maintenance only. Do not use for design-in.

DESCRIPTION

Monolithic overload protected logic level power MOSFET in a surface mount plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- small motors
- solenoids

FEATURES

- Vertical power DMOS output stage
- Overload protected up to 85˚C ambient
- Overload protection by current limiting and overtemperature sensing
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Low operating input current
- ESD protection on all pins
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	0.5	A
P_D	Total power dissipation	1.8	W
T_j	Continuous junction temperature	150	˚C
$R_{DS(ON)}$	Drain-source on-state resistance	200	mΩ

FUNCTIONAL BLOCK DIAGRAM

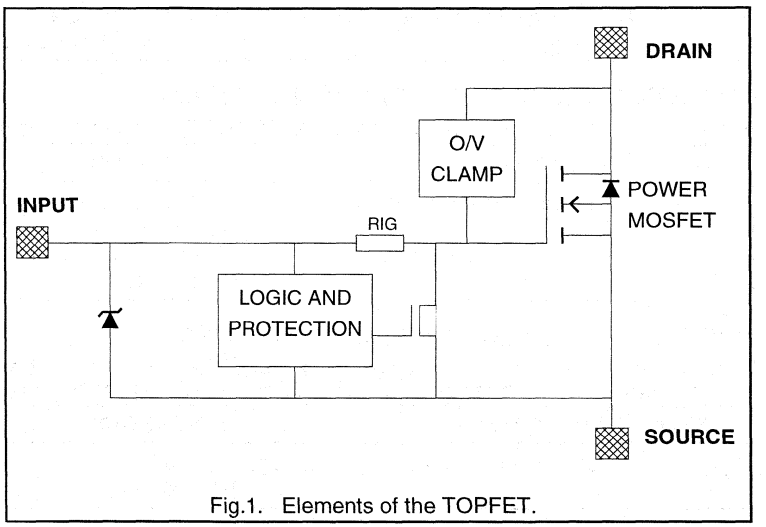
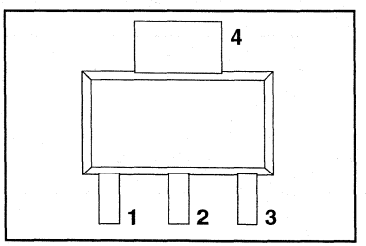


Fig.1. Elements of the TOPFET.

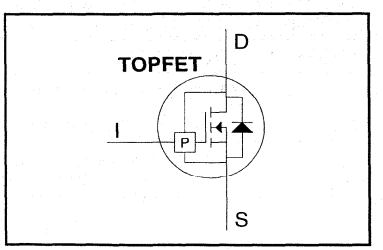
PINNING - SOT223

PIN	DESCRIPTION
1	input
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Continuous drain source voltage[1]	-	-	50	V
I_D	Continuous drain current[2]	-	-	self limiting	A
I_I	Continuous input current	clamping	-	3	mA
I_{IRM}	Non-repetitive peak input current	$t_p \leq 1$ ms	-	10	mA
P_D	Total power dissipation	$T_{amb} = 25$ °C	-	1.8	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature	normal operation[3]	-	150	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{DSM}	Non-repetitive clamping energy	$T_b \leq 25$ °C; $I_{DM} < I_{D(lim)}$; inductive load	-	100	mJ
E_{DRM}	Repetitive clamping energy	$T_b \leq 75$ °C; $I_{DM} = 50$ mA; f = 250 Hz	-	4	mJ

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from short circuit loads.
Overload protection operates by means of drain current limiting and activating the overtemperature protection.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDP}	Protected drain source supply voltage	$V_{IS} = 5$ V	-	35	V
		$V_{IS} = 4$ V	-	16	V

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off to protect itself when there is an overload fault condition.
It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Overload protection					
$I_{D(lim)}$	Drain current limiting	$V_{IS} = 5$ V	0.5	1.1	1.5	A
	Overtemperature protection	only in drain current limiting				
$T_{j(TO)}$	Threshold junction temperature	$V_{IS} = 5$ V	100	130	160	°C

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 Refer to OVERLOAD PROTECTION CHARACTERISTICS.

3 **Not** in an overload condition with drain current limiting.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}sp}$	Junction to solder point		-	12	18	K/W
$R_{th\ j\text{-}b}$	Junction to board[1]	Mounted on any PCB	-	40	-	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	Mounted on PCB of fig. 19	-	-	70	K/W

STATIC CHARACTERISTICS

T_b = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	55	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 200 mA; $t_p \leq 300\ \mu s$; $\delta \leq 0.01$	-	56	70	V
I_{DSS}	Off-state drain current	V_{DS} = 45 V; V_{IS} = 0 V	-	0.5	2	µA
I_{DSS}	Off-state drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Off-state drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 100 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{IS} = 5 V; I_{DM} = 100 mA; $t_p \leq 300\ \mu s$; $\delta \leq 0.01$	-	150	200	mΩ

INPUT CHARACTERISTICS

T_b = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA		1.7	2.2	2.7	V
I_{IS}	Input supply current	normal operation;	V_{IS} = 5 V	-	330	450	µA
			V_{IS} = 4 V	-	170	270	µA
I_{ISL}	Input supply current	protection latched;	V_{IS} = 5 V	-	1.45	2	mA
			V_{IS} = 3.5 V	-	0.95	1.3	mA
V_{ISR}	Protection latch reset voltage[2]			1	2.7	3.5	V
$V_{(CL)IS}$	Input clamping voltage	I_I = 1.5 mA		6	7.5	-	V
R_{IG}	Input series resistance	to gate of power MOSFET		-	4.5	-	kΩ

1 Temperature measured 1.3 mm from tab.

2 The input voltage below which the overload protection circuits will be reset.

SWITCHING CHARACTERISTICS

T_{amb} = 25 °C; resistive load R_L = 50 Ω; adjust V_{DD} to obtain I_D = 250 mA; refer to test circuit and waveforms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{IS} = 0 V to V_{IS} = 5 V	-	0.9	-	µs
t_r	Rise time		-	3.5	-	µs
$t_{d\,off}$	Turn-off delay time	V_{IS} = 5 V to V_{IS} = 0 V	-	2.8	-	µs
t_f	Fall time		-	9.0	-	µs

T_{amb} = 25 °C; resistive load R_L = 10 kΩ; V_{DD} = 12.5 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{IS} = 0 V to V_{IS} = 5 V	-	0.8	-	µs
t_r	Rise time		-	2.3	-	µs
$t_{d\,off}$	Turn-off delay time	V_{IS} = 5 V to V_{IS} = 0 V	-	7.5	-	µs
t_f	Fall time		-	12.5	-	µs

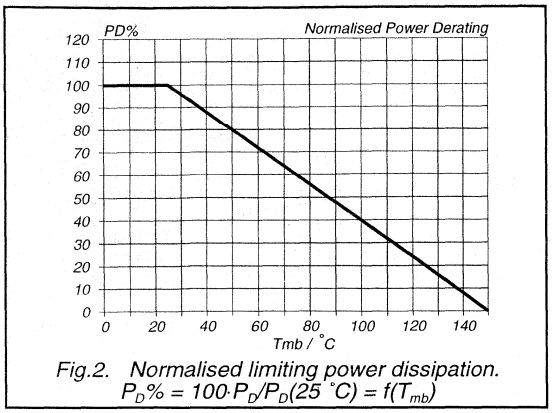


Fig.2. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

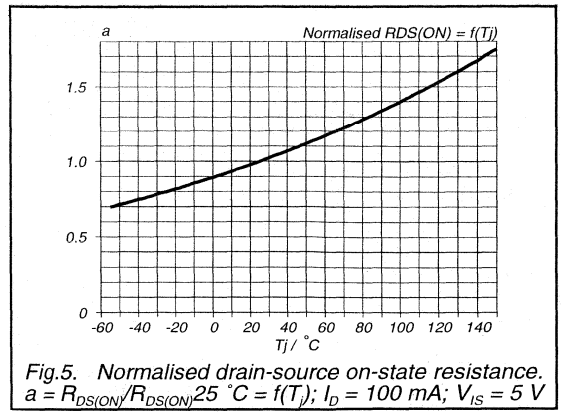


Fig.5. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25\ ^\circ C = f(T_j)$; I_D = 100 mA; V_{IS} = 5 V

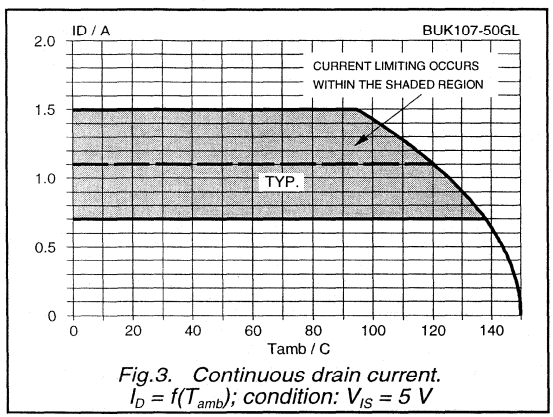


Fig.3. Continuous drain current. $I_D = f(T_{amb})$; condition: V_{IS} = 5 V

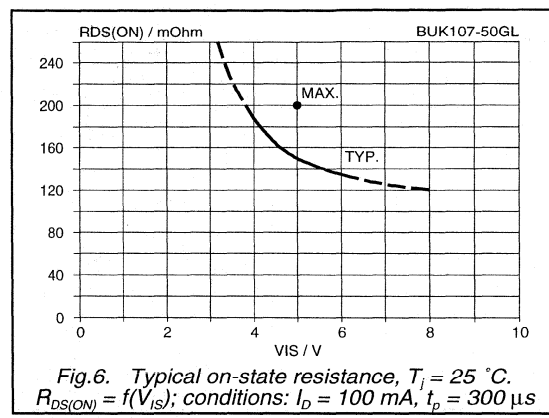


Fig.6. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(V_{IS})$; conditions: I_D = 100 mA, t_p = 300 µs

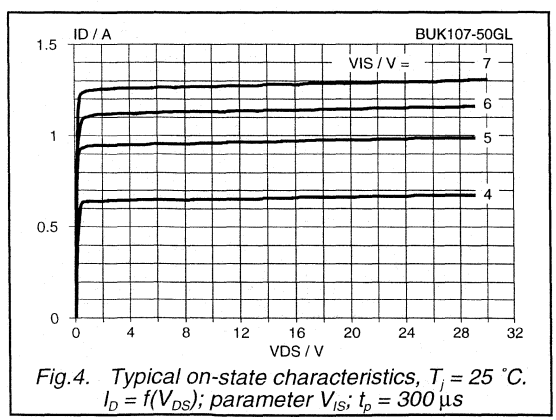


Fig.4. Typical on-state characteristics, T_j = 25 °C. $I_D = f(V_{DS})$; parameter V_{IS}; t_p = 300 µs

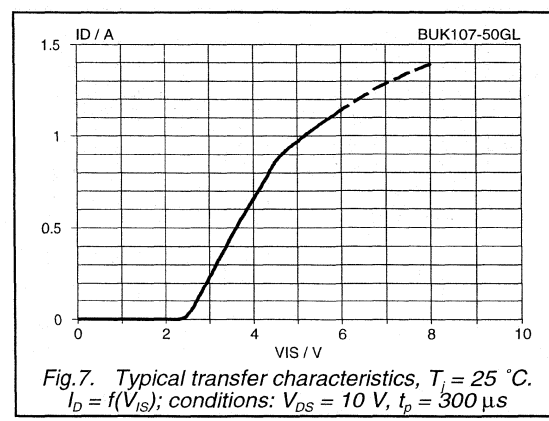


Fig.7. Typical transfer characteristics, T_j = 25 °C. $I_D = f(V_{IS})$; conditions: V_{DS} = 10 V, t_p = 300 µs

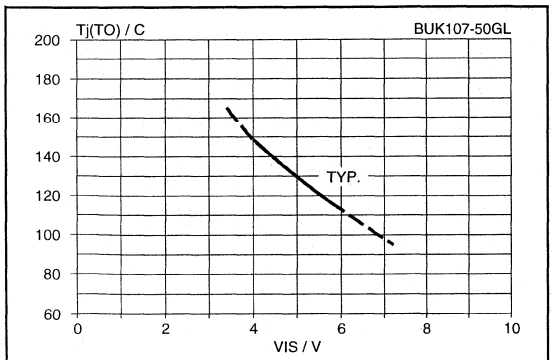


Fig.8. Typical overtemperature protection threshold. $T_{j(TO)} = f(V_{IS})$; condition: V_{DS} = 10 V

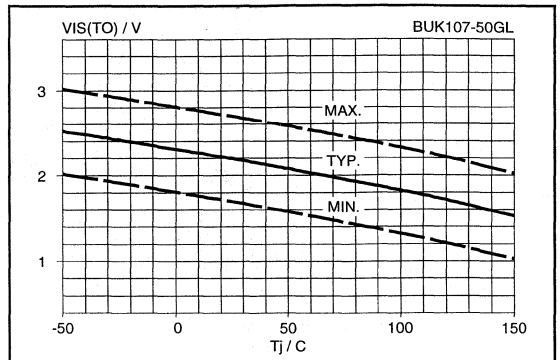


Fig.11. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

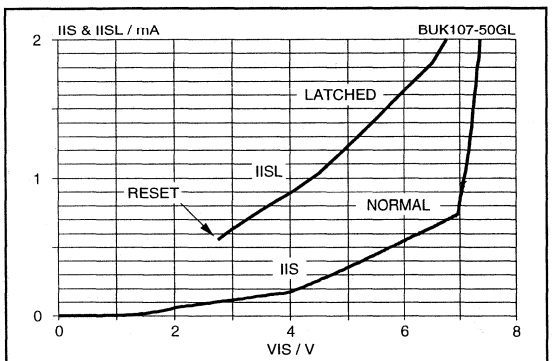


Fig.9. Typical DC input characteristics, T_j = 25 ˚C. I_{IS} & $I_{ISL} = f(V_{IS})$; normal operation & protection latched

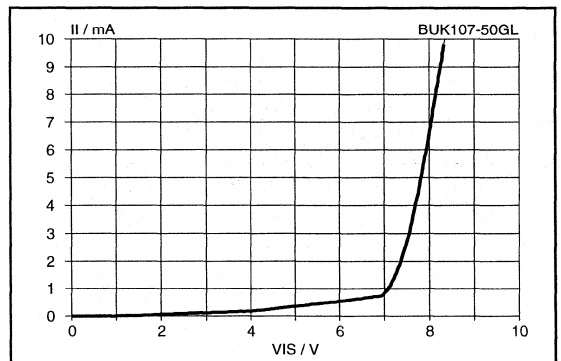


Fig.12. Typical input clamping characteristic. $I_I = f(V_{IS})$; normal operation, T_j = 25 ˚C.

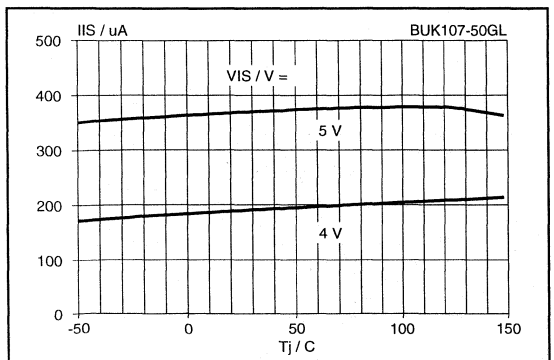


Fig.10. Typical DC input current. $I_{IS} = f(T_j)$; parameter V_{IS}; normal operation

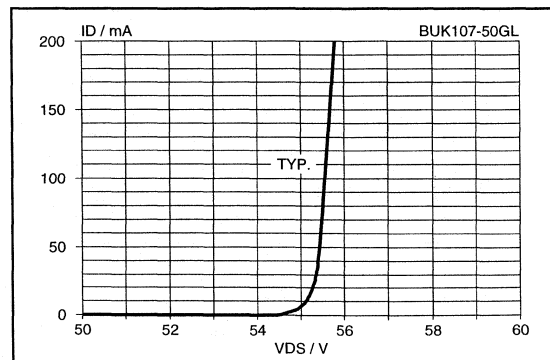


Fig.13. Overvoltage clamping characteristic, 25 ˚C. $I_D = f(V_{DS})$; conditions: V_{IS} = 0 V; $t_p \leq 300$ µs

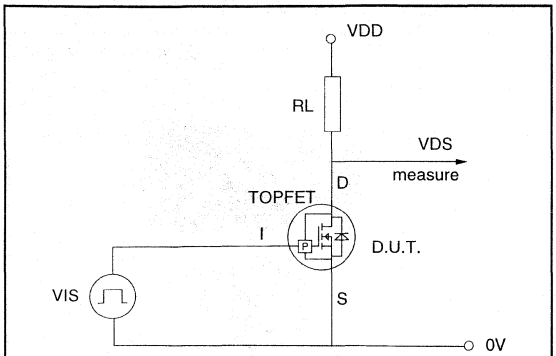


Fig.14. Test circuit for resistive load switching times. V_{IS} = 5 V

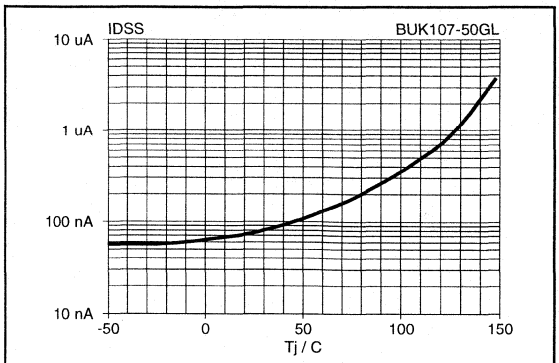


Fig.16. Typical drain source leakage current $I_{DSS} = f(T_j)$; conditions: V_{DS} = 40 V; V_{IS} = 0 V.

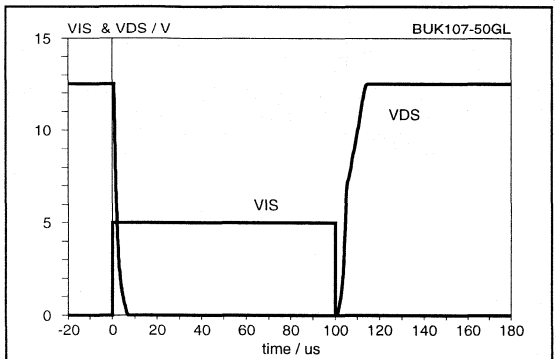


Fig.15. Typical switching waveforms, resistive load . R_L = 50 Ω; adjust V_{DD} to obtain I_D = 250 mA; T_j = 25˚C

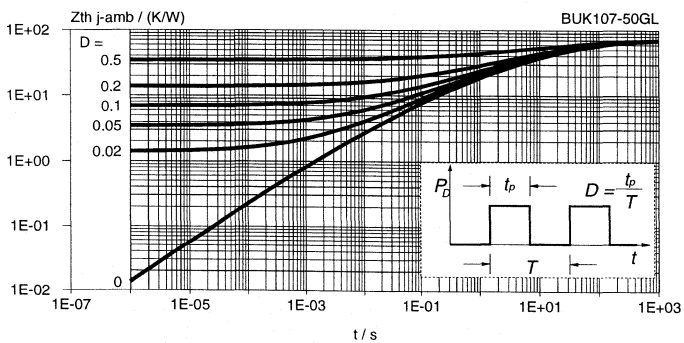


Fig.17. Transient thermal impedance, TOPFET mounted on PCB of fig 19. $Z_{th\ j\text{-}amb} = f(t)$; parameter $D = t_p/T$

MOUNTING INSTRUCTIONS

Dimensions in mm.

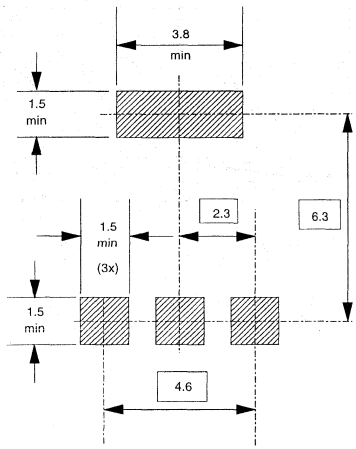


Fig.18. Soldering pattern for surface mounting.

PRINTED CIRCUIT BOARD

Dimensions in mm.

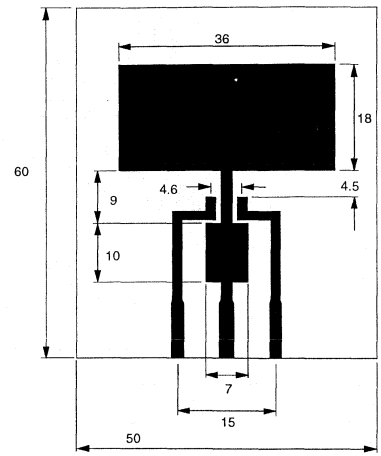


Fig.19. PCB for thermal resistance and power rating. PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).

PowerMOS transistor Logic level TOPFET

BUK108-50DL

For maintenance only. Do not use for design-in.

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 3 pin plastic surface mount envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Lower operating input current permits direct drive by micro-controller
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER		MAX.	UNIT
V_{DS}	Continuous drain source voltage		50	V
I_D	Continuous drain current		13.5	A
P_D	Total power dissipation		40	W
T_j	Continuous junction temperature		150	°C
$R_{DS(ON)}$	Drain-source on-state resistance		125	mΩ
I_{ISL}	Input supply current	V_{IS} = 5 V	650	μA

FUNCTIONAL BLOCK DIAGRAM

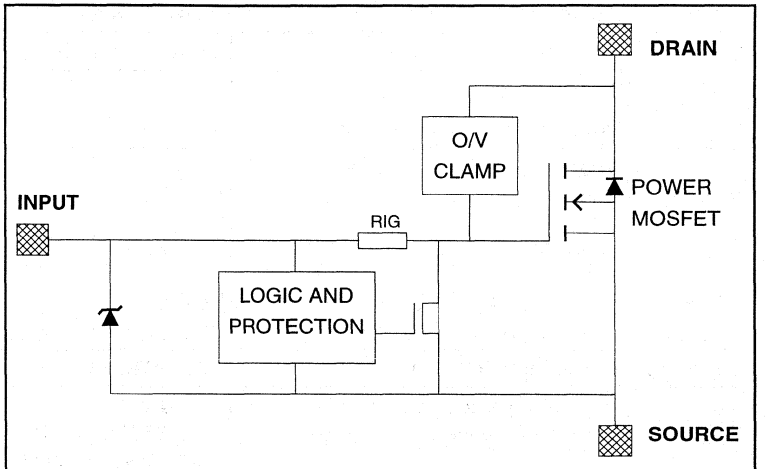
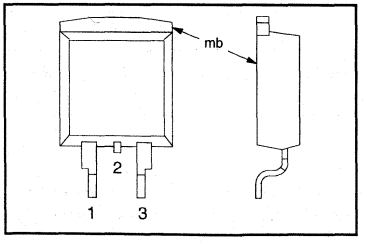


Fig.1. Elements of the TOPFET.

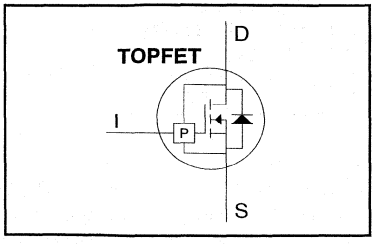
PINNING - SOT404

PIN	DESCRIPTION
1	input
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Continuous drain source voltage[1]	-	-	50	V
V_{IS}	Continuous input voltage	-	0	6	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; $V_{IS} = 5$ V	-	13.5	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; $V_{IS} = 5$ V	-	8.5	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; $V_{IS} = 5$ V	-	54	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	40	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	4	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	$V_{IS} = 5$ V	-	50	V
	Short circuit load protection[4]				
$V_{DDP(P)}$	Protected drain source supply voltage[5]	$V_{IS} = 5$ V	-	24	V
P_{DSM}	Instantaneous overload dissipation	$T_{mb} = 25$ °C	-	0.6	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	$V_{IS} = 0$ V	-	15	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; $I_{DM} = 15$ A; $V_{DD} \leq 20$ V; inductive load	-	200	mJ
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 95$ °C; $I_{DM} = 8$ A; $V_{DD} \leq 20$ V; f = 250 Hz	-	20	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

5 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than $V_{DDP(P)}$ maximum.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	2.5	3.1	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	minimum footprint FR4 PCB (see fig. 23)	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 1 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V	-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance[1]	V_{IS} = 5 V; I_{DM} = 7.5 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	85	125	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[2]	T_{mb} = 25 °C; L ≤ 10 µH; R_L = 10 mΩ				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 5 V	-	0.2	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 5 V	-	0.8	-	ms
$I_{D(SC)}$	Drain current[3]	V_{DD} = 13 V; V_{IS} = 5 V	-	25	-	A
$I_{DM(SC)}$	Peak drain current[4]	V_{IS} = 5 V; V_{DD} = 13 V	-	60	-	A
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 5 V; from $I_D \geq 0.5$ A[5]	150	-	-	°C

TRANSFER CHARACTERISTIC

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 7.5 A $t_p \leq 300$ µs; $\delta \leq 0.01$	5	9	-	S

1 Continuous input voltage. The specified pulse width is for the drain current.

2 Refer to OVERLOAD PROTECTION LIMITING VALUES.

3 Continuous drain-source supply voltage. Pulsed input voltage.

4 Continuous input voltage. Momentary short circuit load connection. (The higher peak current is due to the effect of capacitance Cgd).

5 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA		1.0	1.5	2.0	V
I_{IS}	Input supply current	normal operation;	V_{IS} = 5 V	100	200	350	µA
			V_{IS} = 4 V	-	160	270	µA
V_{ISR}	Protection reset voltage[1]		T_j = 25 °C	2.0	2.6	3.5	V
			T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	protection latched;	V_{IS} = 5 V	-	330	650	µA
			V_{IS} = 3.5 V	-	240	430	µA
$V_{(BR)IS}$	Input breakdown voltage	I_I = 10 mA		6	-	-	V
R_{IG}	Input series resistance		T_j = 25 °C	-	33	-	kΩ
	to gate of power MOSFET		T_j = 150 °C	-	50	-	kΩ

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω. Refer to waveform figure and test circuit.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	8	-	µs
t_r	Rise time	resistive load R_L = 4 Ω	-	40	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	40	-	µs
t_f	Fall time	resistive load R_L = 4 Ω	-	35	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq$ 25 °C; V_{IS} = 0 V	-	15	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDO}	Forward voltage	I_S = 15 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from upper edge of tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

1 The input voltage below which the overload protection circuits will be reset.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

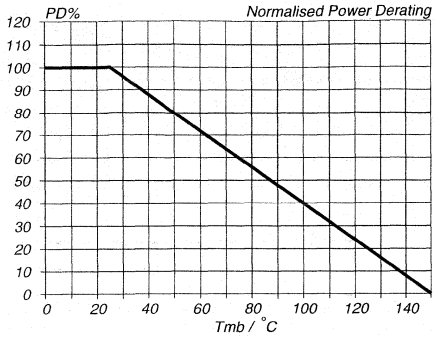


Fig.2. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

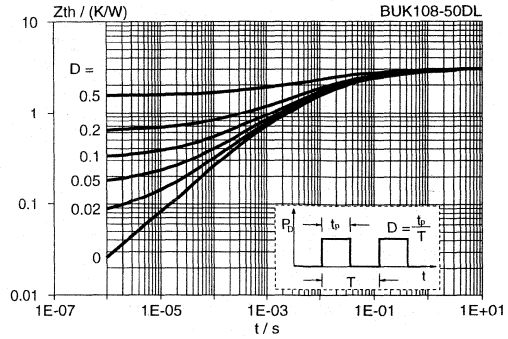


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

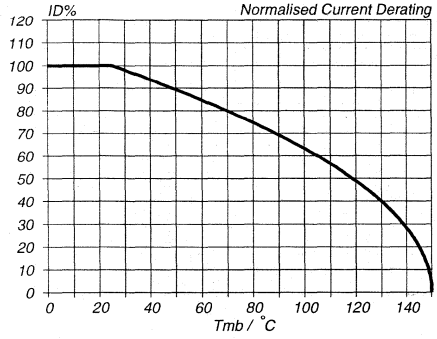


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

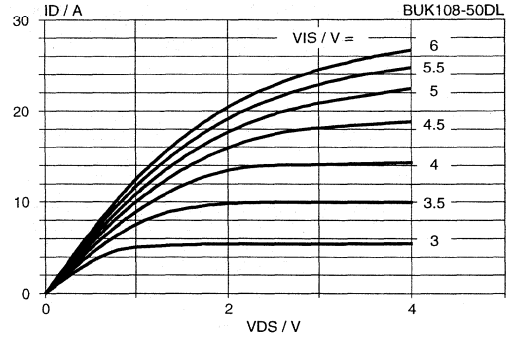


Fig.6. Typical on-state characteristics, $T_j = 25\ ^\circ C$.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 2$ ms

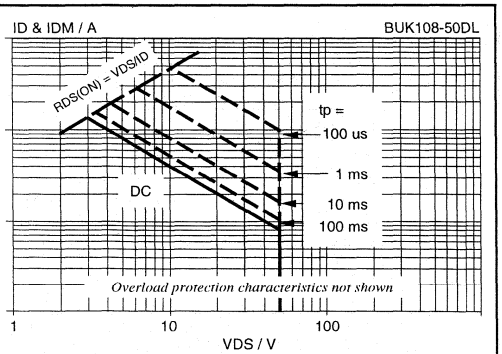


Fig.4. Safe operating area. $T_{mb} = 25\ ^\circ C$
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

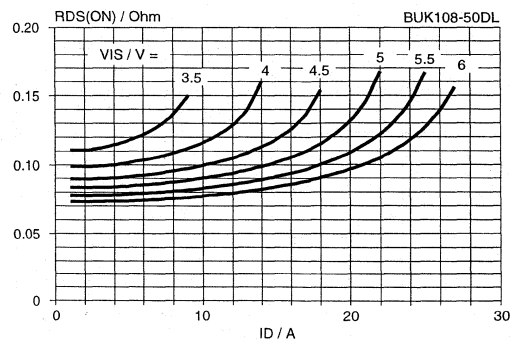


Fig.7. Typical on-state resistance, $T_j = 25\ ^\circ C$.
$R_{DS(ON)} = f(I_D)$; parameter V_{IS}; $t_p = 2$ ms

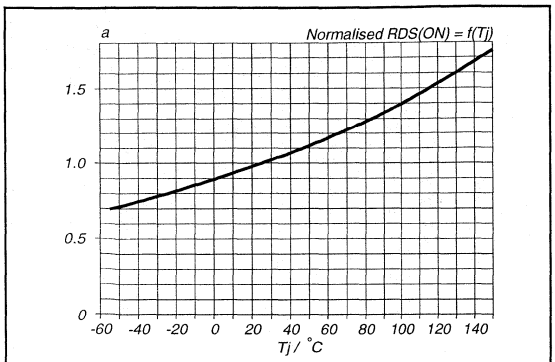


Fig.8. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 7.5 A; V_{IS} = 5 V

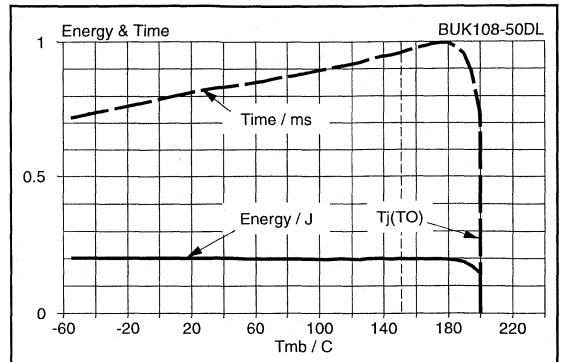


Fig.11. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; V_{IS} = 5 V; SC load = 30 mΩ

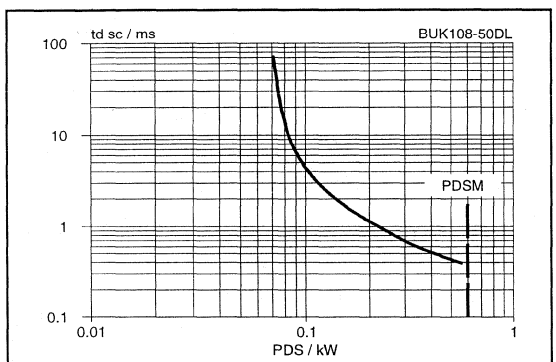


Fig.9. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{IS} \geq 4$ V; T_j = 25 °C.

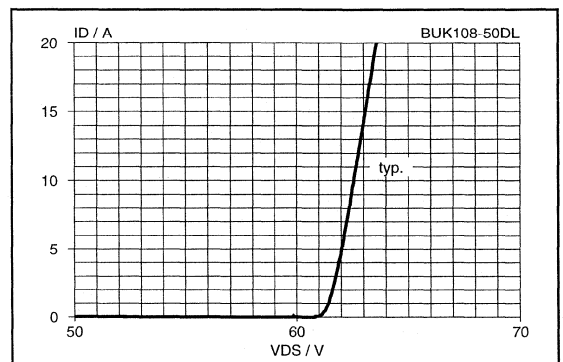


Fig.12. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: V_{IS} = 0 V; $t_p \leq 50$ µs

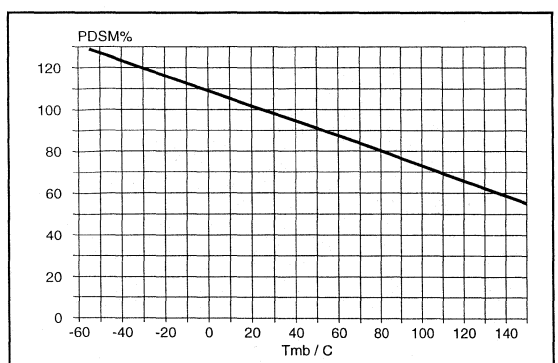


Fig.10. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM(25\,°C)} = f(T_{mb})$

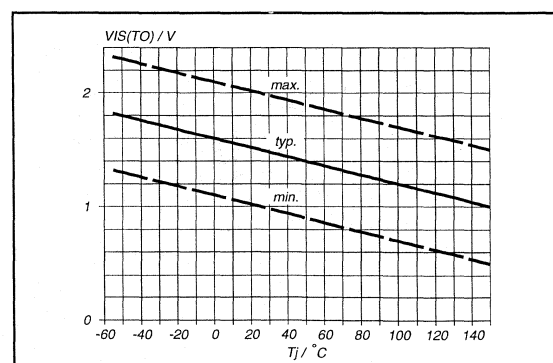


Fig.13. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

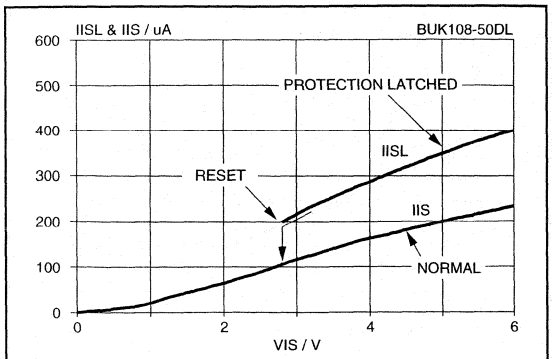


Fig.14. Typical DC input characteristics, T_j = 25 ˚C. I_{ISL} & I_{IS} = f(V_{IS}); protection latched & normal operation

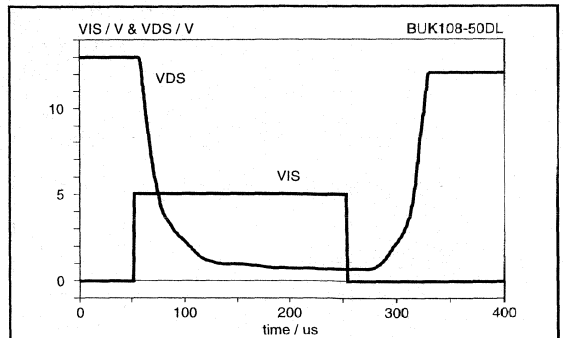


Fig.17. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 4 Ω; R_I = 50 Ω, T_j = 25 ˚C.

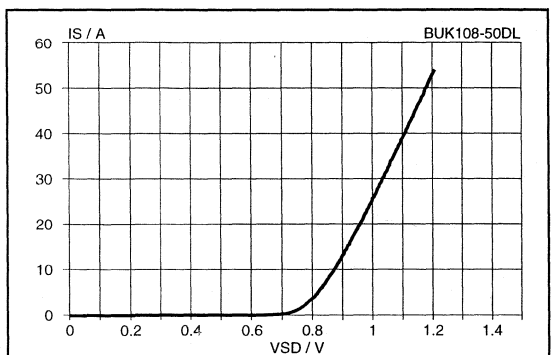


Fig.15. Typical reverse diode current, T_j = 25 ˚C. I_S = f(V_{SDS}); conditions: V_{IS} = 0 V; t_p = 250 µs

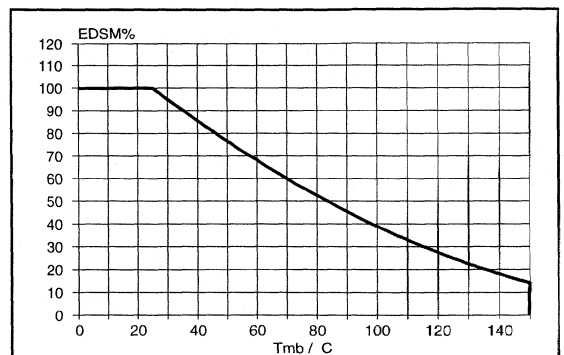


Fig.18. Normalised limiting clamping energy. E_{DSM}% = f(T_{mb}); conditions: I_D = 15 A; V_{IS} = 5 V

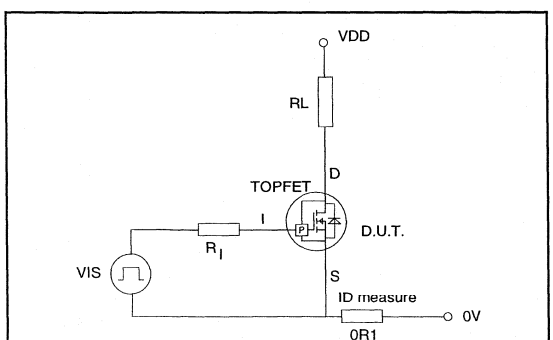


Fig.16. Test circuit for resistive load switching times.

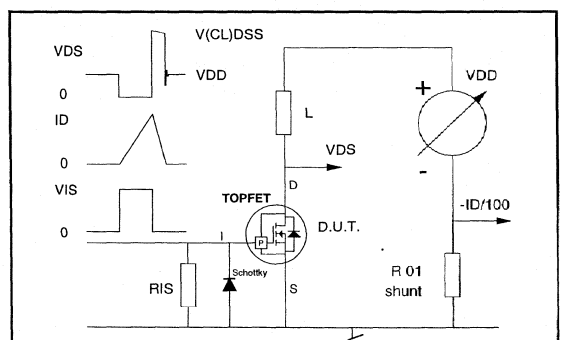


Fig.19. Clamping energy test circuit, R_{IS} = 50 Ω.

$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$$

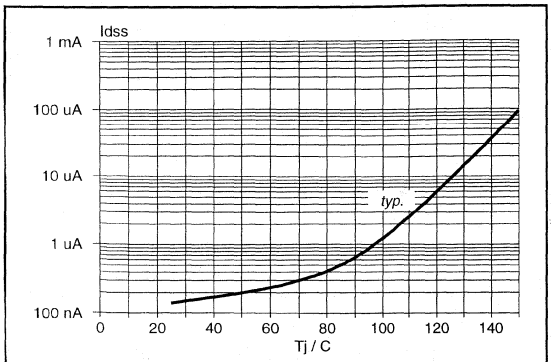


Fig.20. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

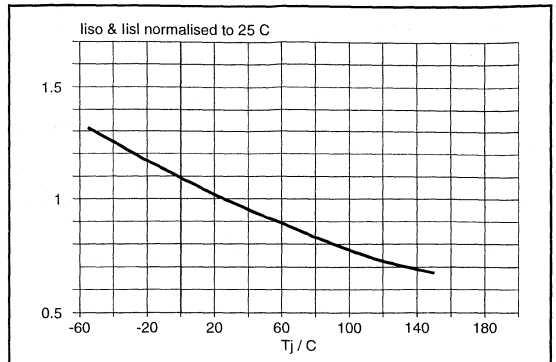


Fig.21. Normalised input currents (normal & latched). $I_{ISO}/I_{ISO}25^{\circ}C$ & $I_{ISL}/I_{ISL}25^{\circ}C = f(T_j)$; V_{IS} = 5 V

PowerMOS transistor Logic level TOPFET

BUK108-50GL

For maintenance only. Do not use for design-in.

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 3 pin plastic surface mount envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Low operating input current
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	13.5	A
P_D	Total power dissipation	40	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{IS} = 5 V	125	mΩ

FUNCTIONAL BLOCK DIAGRAM

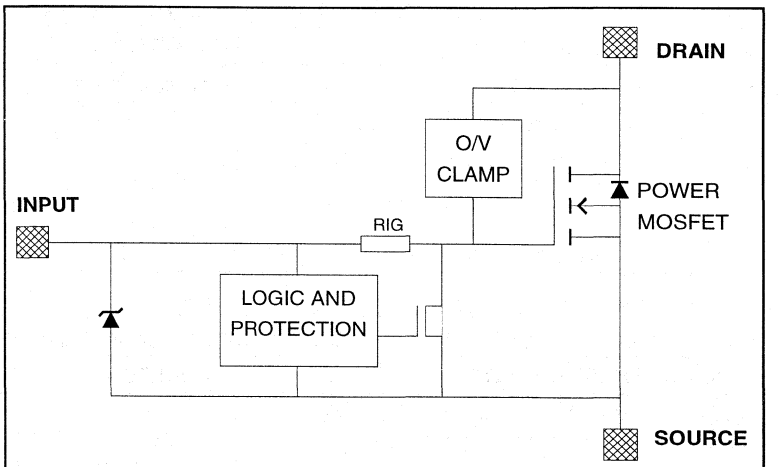
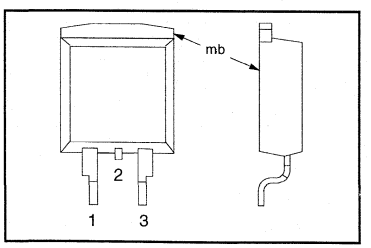


Fig.1. Elements of the TOPFET.

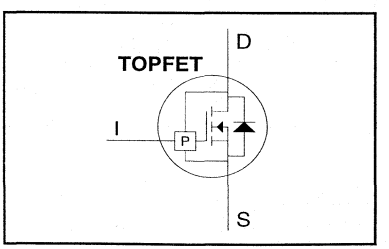
PINNING - SOT404

PIN	DESCRIPTION
1	input
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Continuous off-state drain source voltage[1]	V_{IS} = 0 V	-	50	V
V_{IS}	Continuous input voltage	-	0	6	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; V_{IS} = 5 V	-	13.5	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; V_{IS} = 5 V	-	8.5	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; V_{IS} = 5 V	-	54	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	40	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	4	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 5 V	-	50	V
	Short circuit load protection				
$V_{DDP(P)}$	Protected drain source supply voltage[4]	V_{IS} = 5 V	-	35	V
P_{DSM}	Instantaneous overload dissipation	T_{mb} = 25 °C	-	0.6	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	V_{IS} = 0 V	-	15	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; I_{DM} = 15 A; $V_{DD} \leq 20$ V; inductive load	-	200	mJ
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 95$ °C; I_{DM} = 4 A; $V_{DD} \leq 20$ V; f = 250 Hz	-	20	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	2.5	3.1	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	minimum footprint FR4 PCB (see fig. 32)	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 1 A; $t_p \leq 300\ \mu s$; $\delta \leq 0.01$	-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V	-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{IS} = 5 V; I_{DM} = 7.5 A; $t_p \leq 300\ \mu s$; $\delta \leq 0.01$	-	85	125	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	T_{mb} = 25 °C; L ≤ 10 µH				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 5 V	-	0.2	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 5 V	-	0.8	-	ms
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 5 V; from $I_D \geq 0.5$ A[2]	150	-	-	°C

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA	1.0	1.5	2.0	V
I_{IS}	Input supply current	V_{IS} = 5 V; normal operation	-	0.2	0.35	mA
V_{ISR}	Protection reset voltage[3]		2.0	2.6	3.5	V
V_{ISR}	Protection reset voltage	T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	V_{IS} = 5 V; protection latched	0.5	1.2	2.0	mA
$V_{(BR)IS}$	Input clamp voltage	I_I = 10 mA	6	-	-	V
R_{IG}	Input series resistance	to gate of power MOSFET	-	4	-	kΩ

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum. Refer to OVERLOAD PROTECTION LIMITING VALUES.

2 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

3 The input voltage below which the overload protection circuits will be reset.

TRANSFER CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 7.5 A $t_p \leq 300$ µs; $\delta \leq 0.01$	5	9	-	S
$I_{D(SC)}$	Drain current[1]	V_{DS} = 13 V; V_{IS} = 5 V	-	25	-	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_i = 50 Ω. Refer to waveform figures and test circuits.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	1.5	-	µs
t_r	Rise time	resistive load R_L = 4 Ω	-	8	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	6	-	µs
t_f	Fall time	resistive load R_L = 4 Ω	-	4.5	-	µs
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	1.5	-	µs
t_r	Rise time	inductive load I_{DM} = 3 A	-	1	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	10	-	µs
t_f	Fall time	inductive load I_{DM} = 3 A	-	0.5	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq 25$ °C; V_{IS} = 0 V	-	13.5	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	I_S = 15 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from upper edge of tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

1 During overload before short circuit load protection operates.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

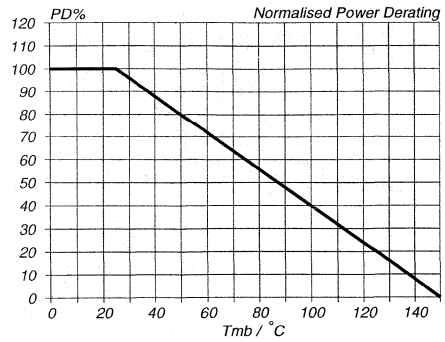


Fig.2. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

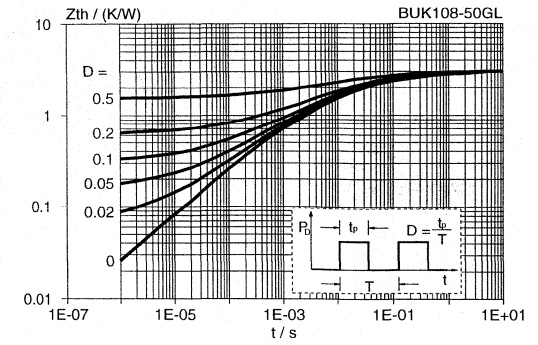


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

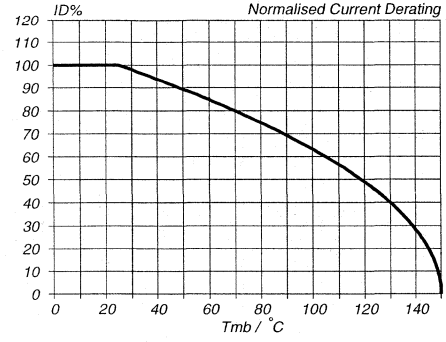


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

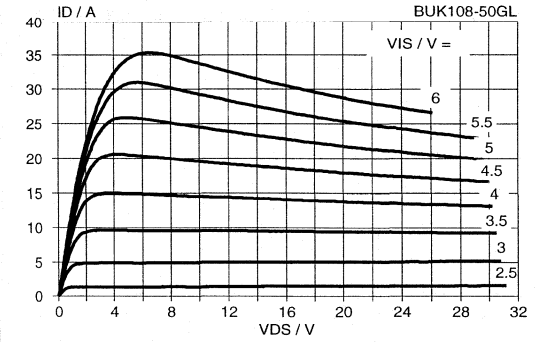


Fig.6. Typical output characteristics, $T_j = 25\ ^\circ C$.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$ & $t_p < t_{d\,sc}$

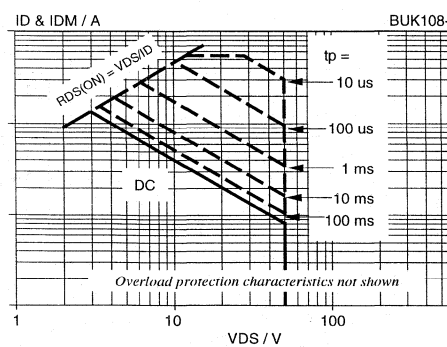


Fig.4. Safe operating area. $T_{mb} = 25\ ^\circ C$
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

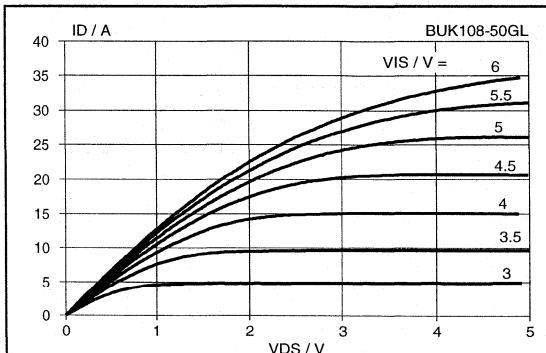


Fig.7. Typical on-state characteristics, $T_j = 25\ ^\circ C$.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$

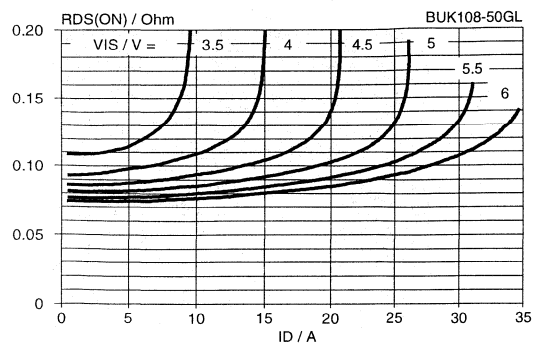


Fig.8. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

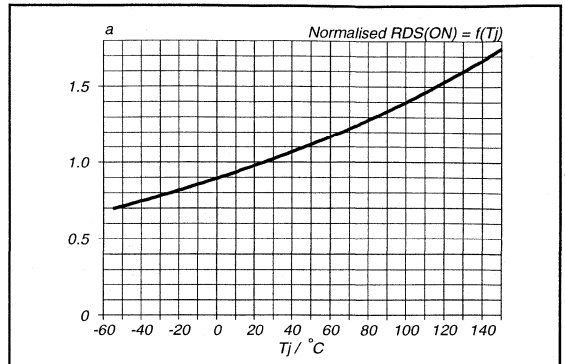


Fig.11. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25$ ˚C $= f(T_j)$; I_D = 7.5 A; V_{IS} = 5 V

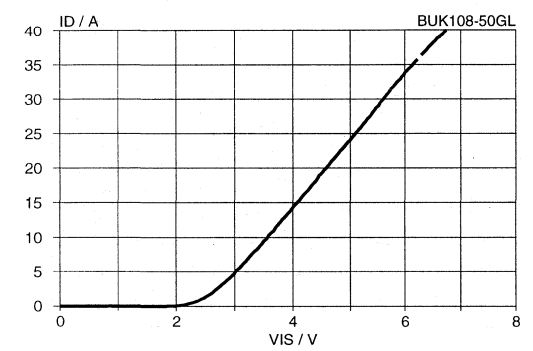


Fig.9. Typical transfer characteristics, T_j = 25 ˚C. $I_D = f(V_{IS})$; conditions: V_{DS} = 10 V; t_p = 250 µs

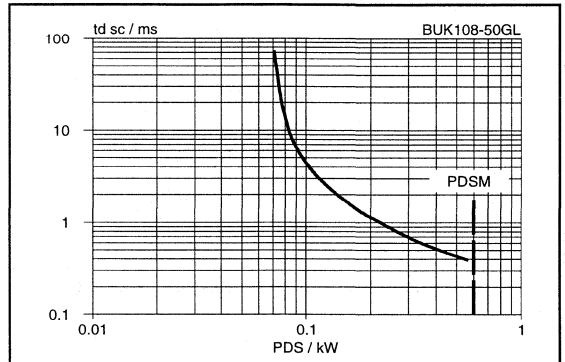


Fig.12. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{IS} \geq 4$ V; T_j = 25 ˚C.

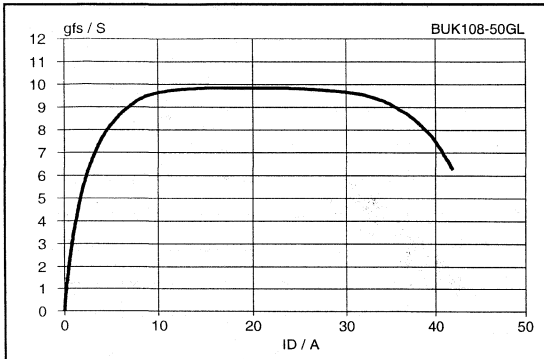


Fig.10. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V; t_p = 250 µs

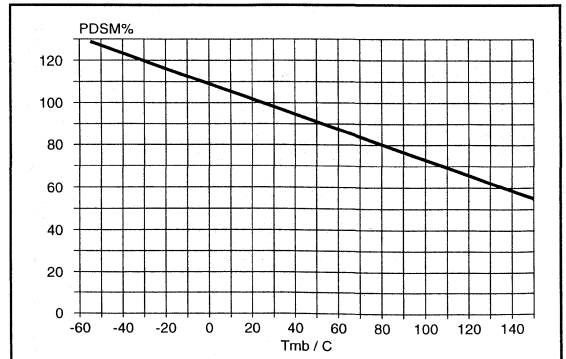


Fig.13. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ ^\circ C) = f(T_{mb})$

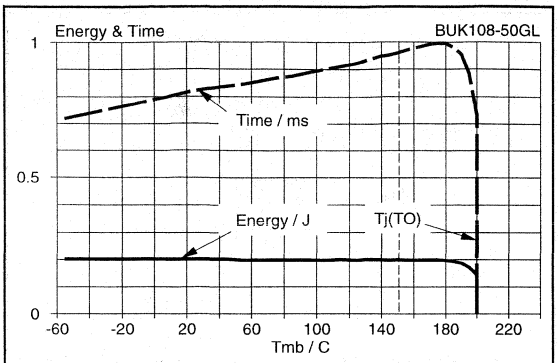


Fig.14. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; V_{IS} = 5 V; SC load = 30 mΩ

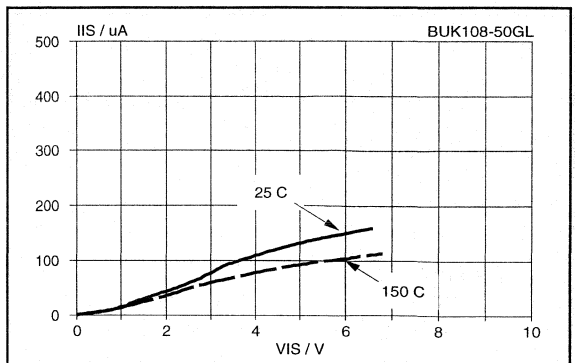


Fig.17. Typical DC input characteristics. $I_{IS} = f(V_{IS})$; normal operation, parameter: T_j

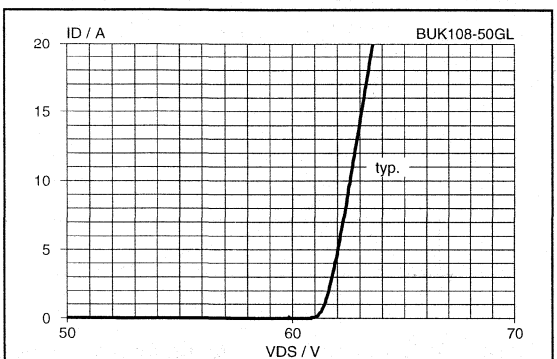


Fig.15. Typical clamping characteristics, 25 ˚C. $I_D = f(V_{DS})$; conditions: V_{IS} = 0 V; $t_p \leq 50$ µs

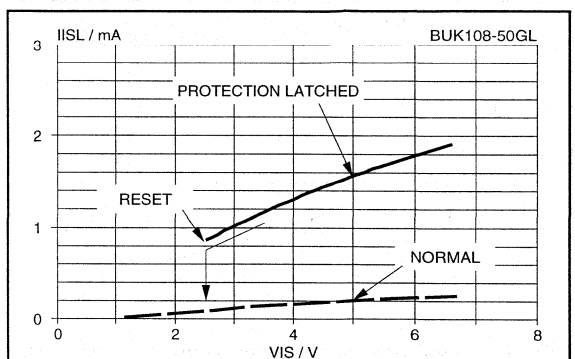


Fig.18. Typical DC input characteristics, T_j = 25 ˚C. $I_{ISL} = f(V_{IS})$; overload protection operated ⇒ I_D = 0 A

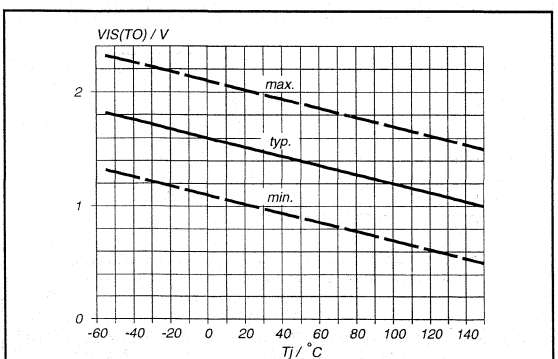


Fig.16. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

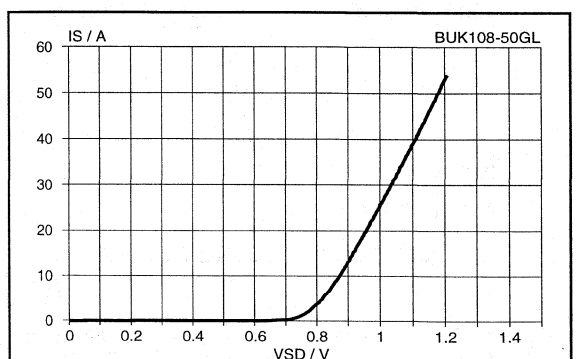


Fig.19. Typical reverse diode current, T_j = 25 ˚C. $I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V; t_p = 250 µs

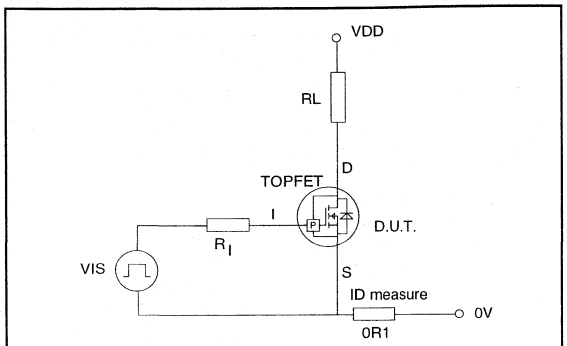


Fig.20. Test circuit for resistive load switching times.

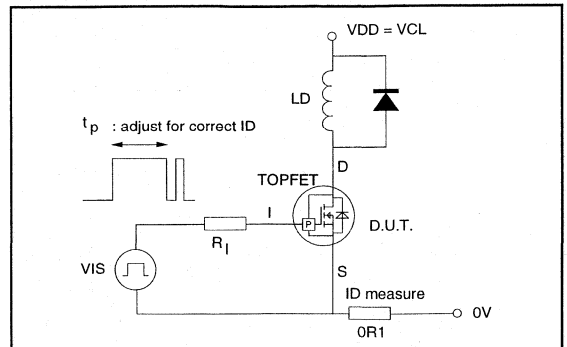


Fig.23. Test circuit for inductive load switching times.

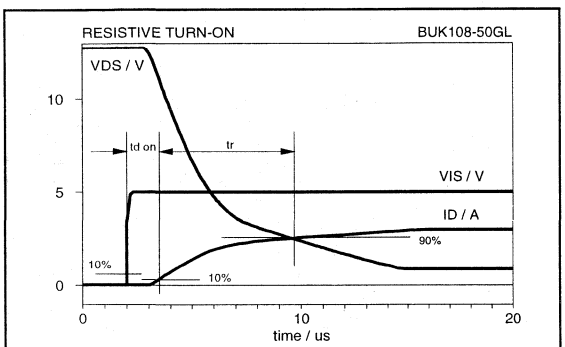


Fig.21. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 4 Ω; R_I = 50 Ω, T_j = 25 ˚C.

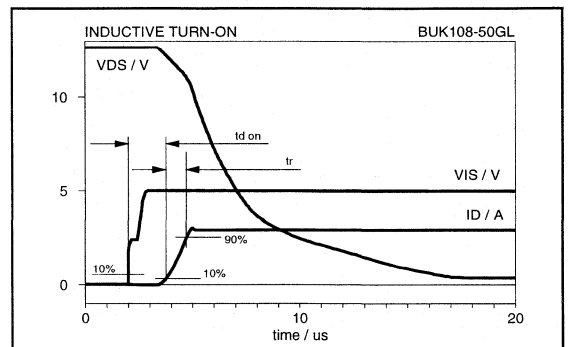


Fig.24. Typical switching waveforms, inductive load. V_{DD} = 13 V; I_D = 3 A; R_I = 50 Ω, T_j = 25 ˚C.

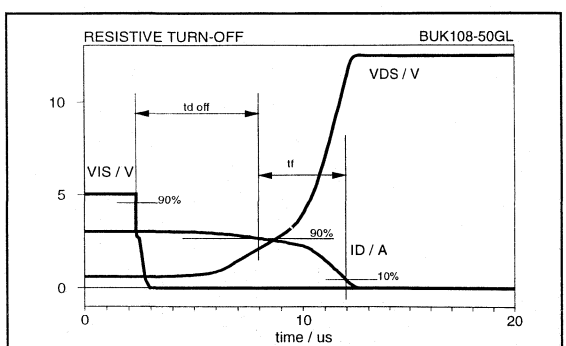


Fig.22. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 4 Ω; R_I = 50 Ω, T_j = 25 ˚C.

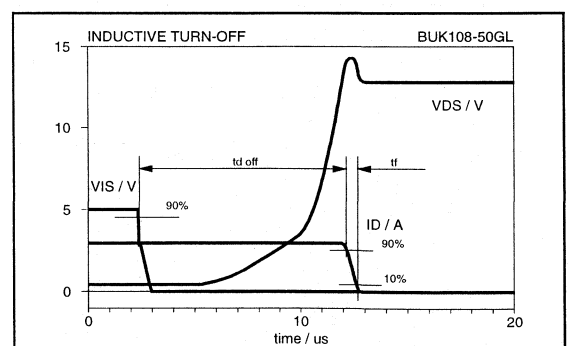


Fig.25. Typical switching waveforms, inductive load. V_{DD} = 13 V; I_D = 3 A; R_I = 50 Ω, T_j = 25 ˚C.

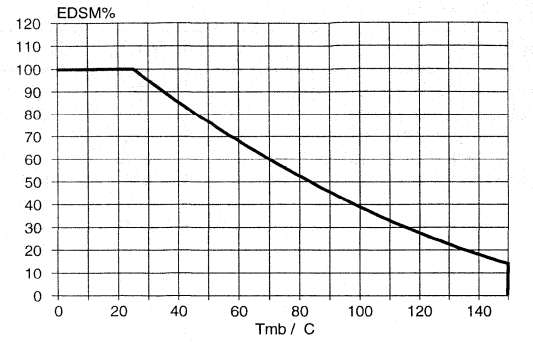


Fig.26. Normalised limiting clamping energy. $E_{DSM}\% = f(T_{mb})$; conditions: I_D = 15 A; V_{IS} = 5 V

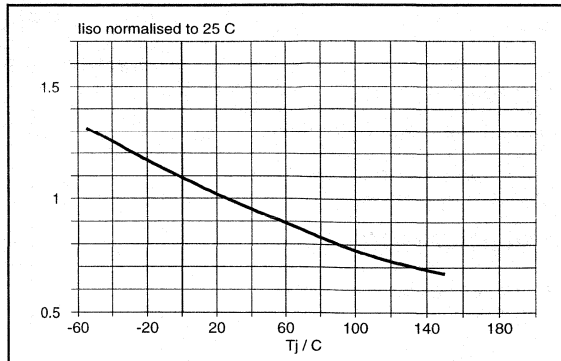


Fig.29. Normalised input current (normal operation). $I_{IS}/I_{IS}25\ ^{\circ}C = f(T_j)$; V_{IS} = 5 V

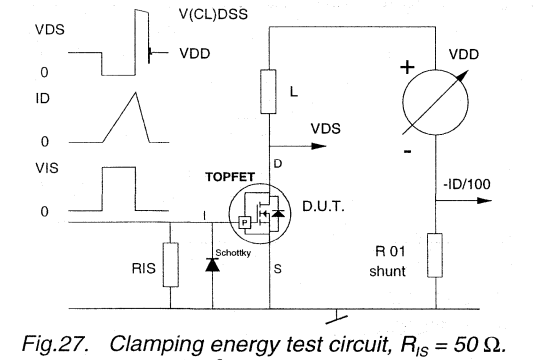


Fig.27. Clamping energy test circuit, R_{IS} = 50 Ω.
$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$

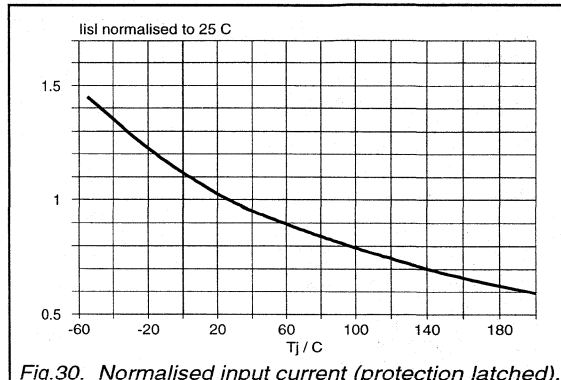


Fig.30. Normalised input current (protection latched). $I_{ISL}/I_{ISL}25\ ^{\circ}C = f(T_j)$; V_{IS} = 5 V

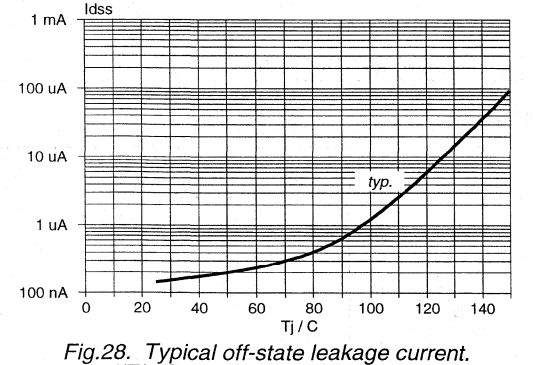


Fig.28. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

PowerMOS transistor Logic level TOPFET

BUK109-50DL

For maintenance only. Do not use for design-in.

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 3 pin plastic surface mount envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Lower operating input current permits direct drive by micro-controller
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER		MAX.	UNIT
V_{DS}	Continuous drain source voltage		50	V
I_D	Continuous drain current		26	A
P_D	Total power dissipation		75	W
T_j	Continuous junction temperature		150	°C
$R_{DS(ON)}$	Drain-source on-state resistance		60	mΩ
I_{ISL}	Input supply current	V_{IS} = 5 V	650	µA

FUNCTIONAL BLOCK DIAGRAM

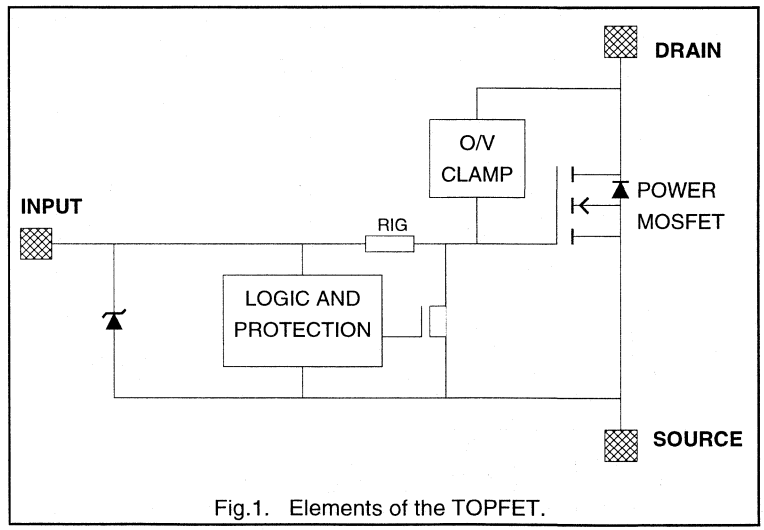
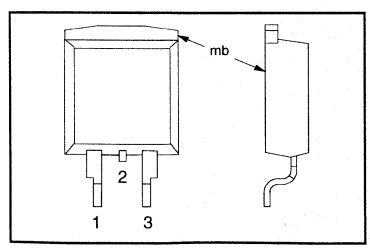


Fig.1. Elements of the TOPFET.

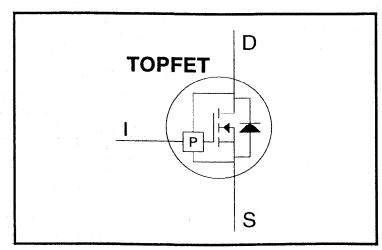
PINNING - SOT404

PIN	DESCRIPTION
1	input
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Continuous drain source voltage[1]	-	-	50	V
V_{IS}	Continuous input voltage	-	0	6	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; $V_{IS} = 5$ V	-	26	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; $V_{IS} = 5$ V	-	16	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; $V_{IS} = 5$ V	-	100	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	75	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	4	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	$V_{IS} = 5$ V	-	50	V
	Short circuit load protection[4]				
$V_{DDP(P)}$	Protected drain source supply voltage[5]	$V_{IS} = 5$ V	-	20	V
P_{DSM}	Instantaneous overload dissipation	$T_{mb} = 25$ °C	-	1.3	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	$V_{IS} = 0$ V	-	26	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; $I_{DM} = 26$ A; $V_{DD} \leq 20$ V; inductive load	-	625	mJ
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 95$ °C; $I_{DM} = 8$ A; $V_{DD} \leq 20$ V; f = 250 Hz	-	40	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

5 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than $V_{DDP(P)}$ maximum.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	1.3	1.67	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	minimum footprint FR4 PCB (see fig. 23)	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 2 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V	-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance[1]	V_{IS} = 5 V; I_{DM} = 13 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	45	60	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[2]	T_{mb} = 25 °C; L ≤ 10 µH; R_L = 10 mΩ				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 5 V	-	0.4	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 5 V	-	0.8	-	ms
$I_{D(SC)}$	Drain current[3]	V_{DD} = 13 V; V_{IS} = 5 V	-	45	-	A
$I_{DM(SC)}$	Peak drain current[4]	V_{IS} = 5 V; V_{DD} = 13 V	-	105	-	A
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 5 V; from $I_D \geq 1$ A[5]	150	-	-	°C

TRANSFER CHARACTERISTIC

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 13 A $t_p \leq 300$ µs; $\delta \leq 0.01$	10	16	-	S

1 Continuous input voltage. The specified pulse width is for the drain current.

2 Refer to OVERLOAD PROTECTION LIMITING VALUES.

3 Continuous drain-source supply voltage. Pulsed input voltage.

4 Continuous input voltage. Momentary short circuit load connection. (The higher peak current is due to the effect of capacitance Cgd).

5 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA		1.0	1.5	2.0	V
I_{IS}	Input supply current	normal operation;	V_{IS} = 5 V	100	200	350	µA
			V_{IS} = 4 V	-	160	270	µA
V_{ISR}	Protection reset voltage[1]		T_j = 25 °C	2.0	2.6	3.5	V
			T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	protection latched;	V_{IS} = 5 V	-	330	650	µA
			V_{IS} = 3.5 V	-	240	430	µA
$V_{(BR)IS}$	Input breakdown voltage	I_I = 10 mA		6	-	-	V
R_{IG}	Input series resistance		T_j = 25 °C	-	33	-	kΩ
	to gate of power MOSFET		T_j = 150 °C	-	50	-	kΩ

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω. Refer to waveform figure and test circuit.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	17	-	µs
t_r	Rise time	resistive load R_L = 2.1 Ω	-	75	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	60	-	µs
t_f	Fall time	resistive load R_L = 2.1 Ω	-	70	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq 25$ °C; V_{IS} = 0 V	-	26	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDO}	Forward voltage	I_S = 26 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from upper edge of tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

1 The input voltage below which the overload protection circuits will be reset.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

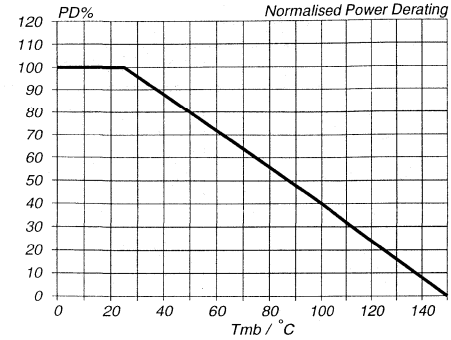


Fig.2. Normalised power dissipation.
$P_D\% = 100 \cdot P_D / P_D(25\ ^\circ C) = f(T_{mb})$

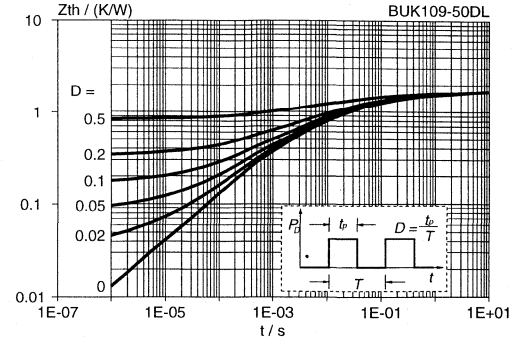


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; *parameter* $D = t_p/T$

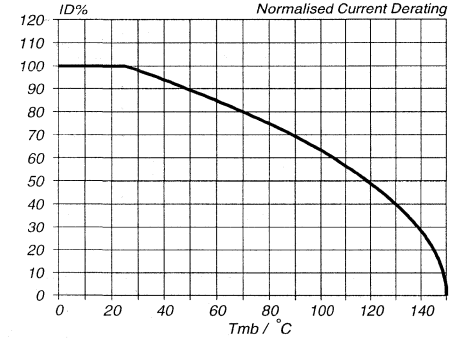


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D / I_D(25\ ^\circ C) = f(T_{mb})$; *conditions:* $V_{IS} = 5$ V

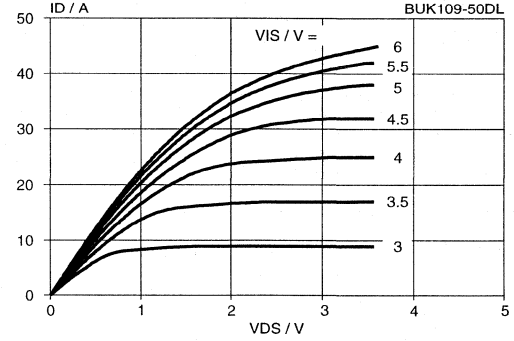


Fig.6. Typical on-state characteristics, $T_j = 25\ ^\circ C$.
$ID = f(V_{DS})$; *parameter* V_{IS}; $t_p = 2$ *ms*

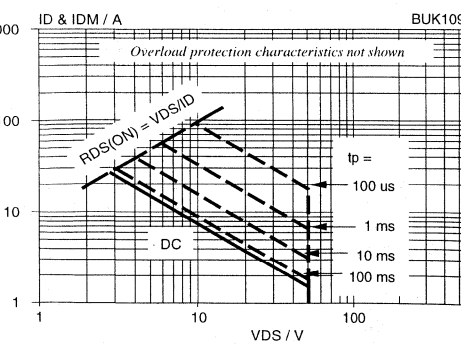


Fig.4. Safe operating area. $T_{mb} = 25\ ^\circ C$
I_D & $I_{DM} = f(V_{DS})$; I_{DM} *single pulse; parameter* t_p

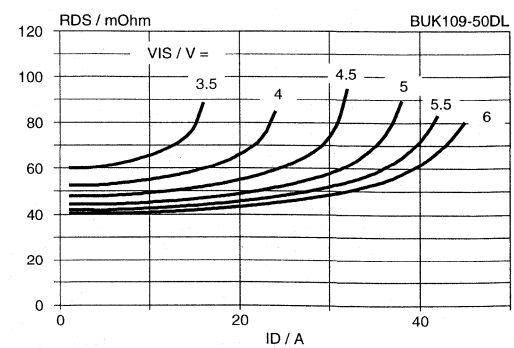


Fig.7. Typical on-state resistance, $T_j = 25\ ^\circ C$.
$R_{DS(ON)} = f(I_D)$; *parameter* V_{IS}; $t_p = 2$ *ms*

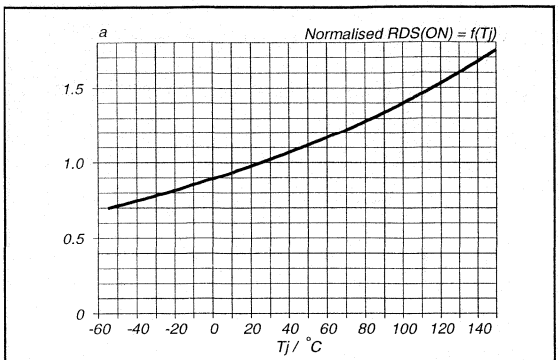


Fig.8. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25\ ^{\circ}C = f(T_j)$; I_D = 13 A; V_{IS} = 5 V

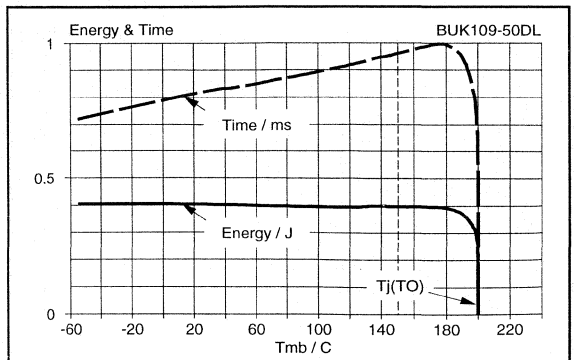


Fig.11. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; V_{IS} = 5 V; SC load = 30 mΩ

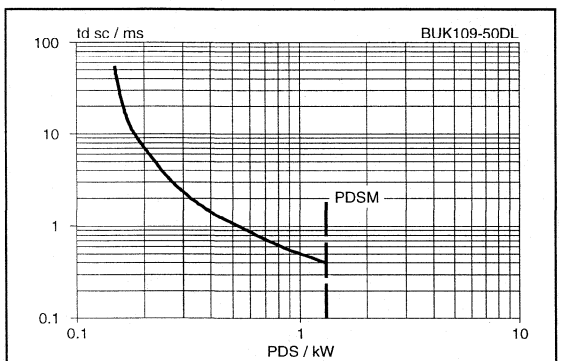


Fig.9. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{IS} \geq 4$ V; T_j = 25 °C.

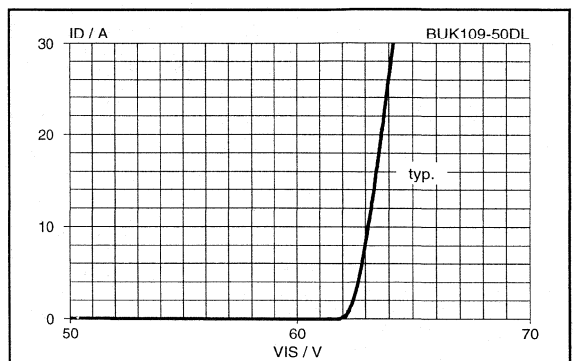


Fig.12. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: V_{IS} = 0 V; $t_p \leq 50$ µs

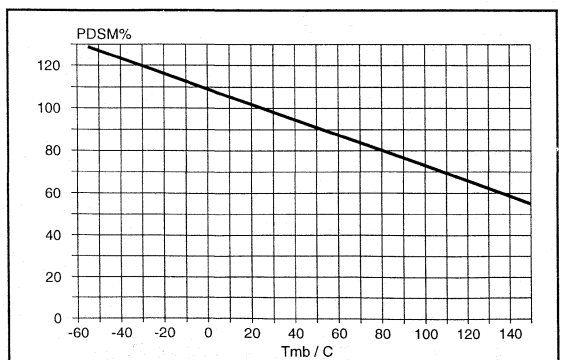


Fig.10. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ ^{\circ}C) = f(T_{mb})$

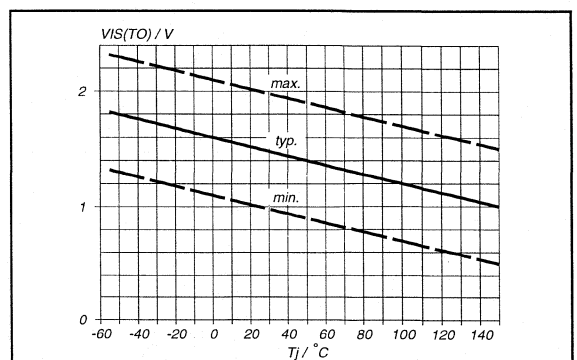


Fig.13. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

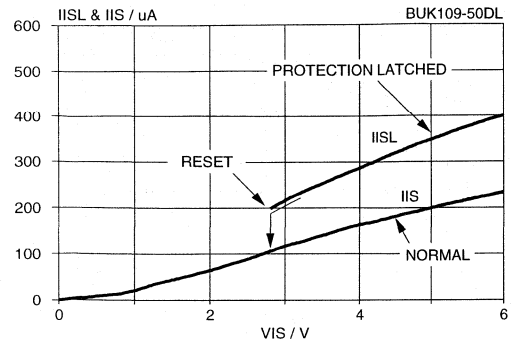


Fig.14. Typical DC input characteristics, T_j = 25 °C. I_{ISL} & I_{IS} = f(V_{IS}); protection latched & normal operation

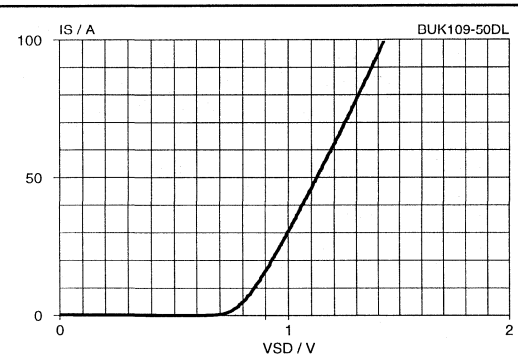


Fig.15. Typical reverse diode current, T_j = 25 °C. I_S = f(V_{SDS}); conditions: V_{IS} = 0 V

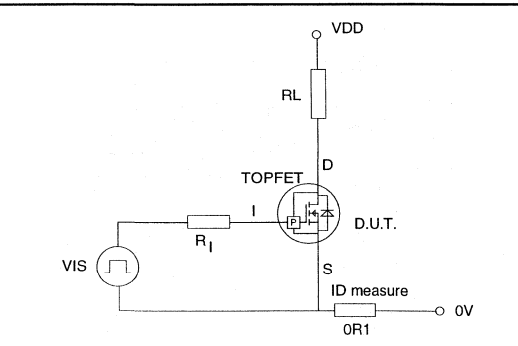


Fig.16. Test circuit for resistive load switching times.

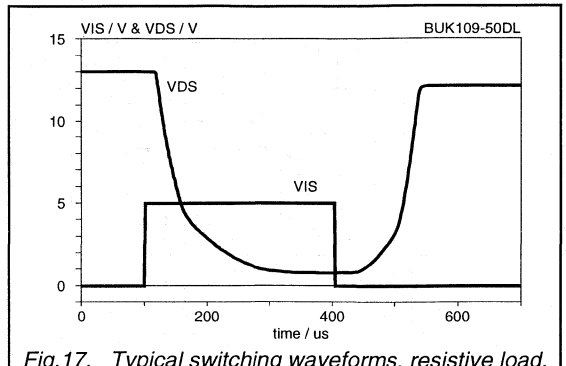


Fig.17. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 2.1 Ω; R_I = 50 Ω, T_j = 25 °C.

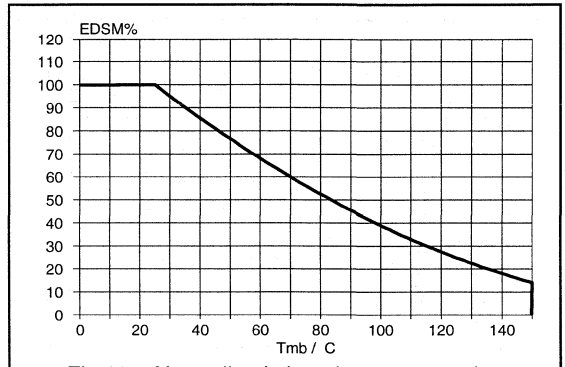


Fig.18. Normalised clamping energy rating. E_{DSM}% = f(T_{mb}); conditions: I_D = 26 A; V_{IS} = 5 V

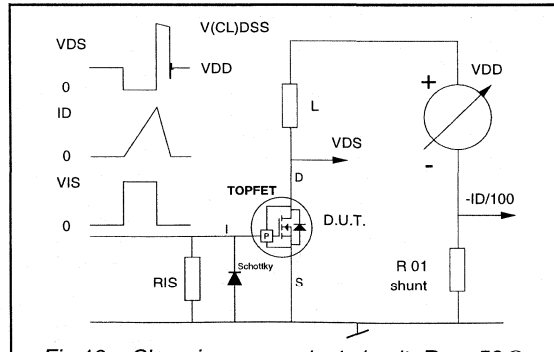


Fig.19. Clamping energy test circuit, R_{IS} = 50 Ω.

$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$$

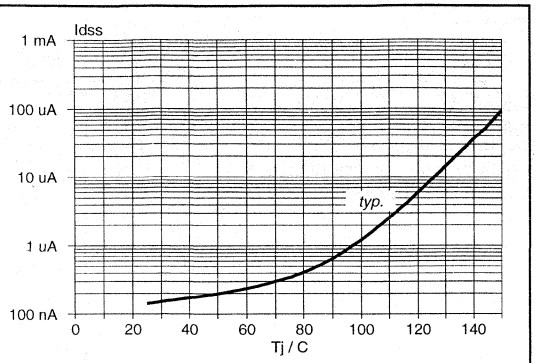


Fig.20. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

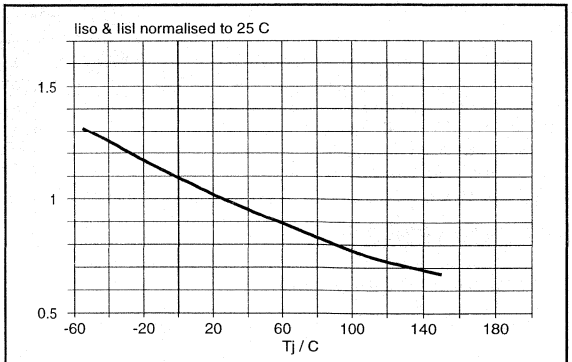


Fig.21. Normalised input currents (normal & latched). $I_{ISO}/I_{ISO}25°C$ & $I_{ISL}/I_{ISL}25°C = f(T_j)$; V_{IS} = 5 V

PowerMOS transistor Logic level TOPFET

BUK109-50GL

For maintenance only. Do not use for design-in.

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 3 pin plastic surface mount envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Low operating input current
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	26	A
P_D	Total power dissipation	75	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{IS} = 5 V	60	mΩ

FUNCTIONAL BLOCK DIAGRAM

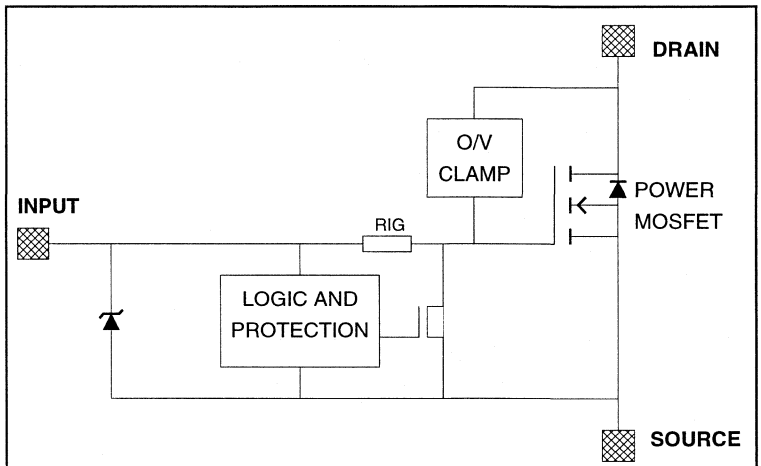
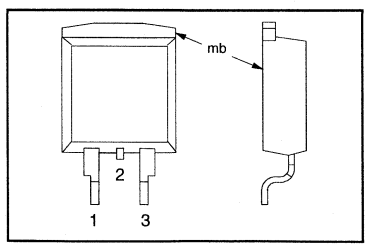


Fig.1. Elements of the TOPFET.

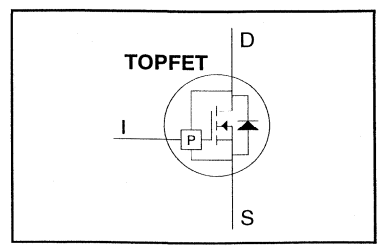
PINNING - SOT404

PIN	DESCRIPTION
1	input
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Continuous off-state drain source voltage	V_{IS} = 0 V	-	50	V
V_{IS}	Continuous input voltage	-	0	6	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; V_{IS} = 5 V	-	26	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; V_{IS} = 5 V	-	16	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; V_{IS} = 5 V	-	100	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	75	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[1]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[2]	for valid protection	4	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 5 V	-	50	V
	Short circuit load protection				
$V_{DDP(P)}$	Protected drain source supply voltage[3]	V_{IS} = 5 V	-	35	V
P_{DSM}	Instantaneous overload dissipation	T_{mb} = 25 °C	-	1.3	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	V_{IS} = 0 V	-	26	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; I_{DM} = 26 A; $V_{DD} \leq 20$ V; inductive load	-	625	mJ
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 95$ °C; I_{DM} = 8 A; $V_{DD} \leq 20$ V; f = 250 Hz	-	40	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

2 The input voltage for which the overload protection circuits are functional.

3 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	1.3	1.67	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	minimum footprint FR4 PCB (see fig. 32)	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 2 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V	-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{IS} = 5 V; I_{DM} = 13 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	45	60	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	T_{mb} = 25 °C; L ≤ 10 µH				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 5 V	-	0.4	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 5 V	-	0.8	-	ms
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 5 V; from $I_D \geq 1$ A[2]	150	-	-	°C

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA	1.0	1.5	2.0	V
I_{IS}	Input supply current	V_{IS} = 5 V; normal operation	-	0.2	0.35	mA
V_{ISR}	Protection reset voltage[3]		2.0	2.6	3.5	V
V_{ISR}	Protection reset voltage	T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	V_{IS} = 5 V; protection latched	0.5	1.2	2.0	mA
$V_{(BR)IS}$	Input clamp voltage	I_I = 10 mA	6	7	-	V
R_{IG}	Input series resistance	to gate of power MOSFET	-	4	-	kΩ

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum. Refer to OVERLOAD PROTECTION LIMITING VALUES.

2 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

3 The input voltage below which the overload protection circuits will be reset.

TRANSFER CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 13 A $t_p \leq 300$ µs; $\delta \leq 0.01$	10	16	-	S
$I_{D(SC)}$	Drain current[1]	V_{DS} = 13 V; V_{IS} = 5 V	-	40	-	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω. Refer to waveform figures and test circuits.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	2.5	-	µs
t_r	Rise time	resistive load R_L = 2.1 Ω	-	15	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	10	-	µs
t_f	Fall time	resistive load R_L = 2.1 Ω	-	7	-	µs
$t_{d\,on}$	Turn-on delay time	V_{DD} = 10 V; V_{IS} = 5 V	-	2	-	µs
t_r	Rise time	inductive load I_{DM} = 6 A	-	4	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 10 V; V_{IS} = 0 V	-	15	-	µs
t_f	Fall time	inductive load I_{DM} = 6 A	-	1	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq 25$ °C	-	26	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	I_S = 26 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from upper edge of tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

1 During overload before short circuit load protection operates.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

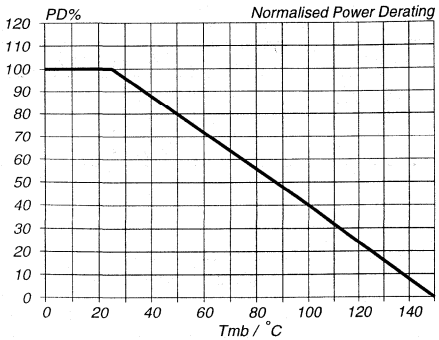


Fig.2. Normalised power dissipation.
$P_D\% = 100 \cdot P_D / P_D(25\ ^\circ C) = f(T_{mb})$

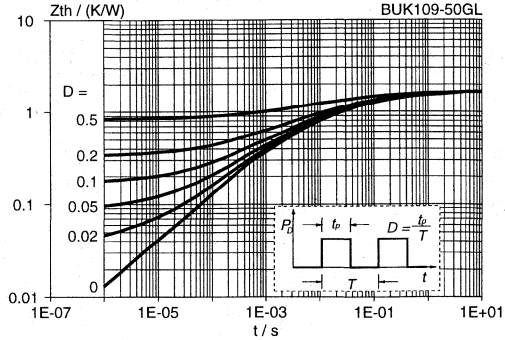


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

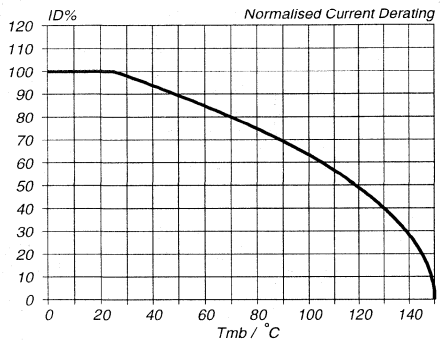


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D / I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

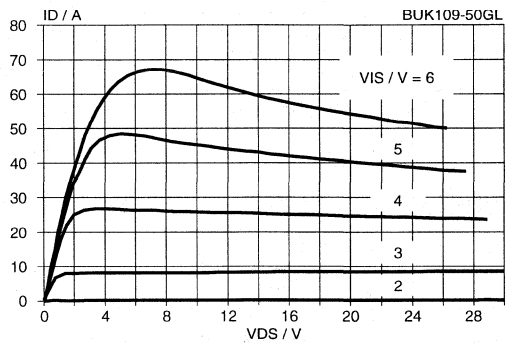


Fig.6. Typical output characteristics, $T_j = 25\ ^\circ C$.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$ & $t_p < t_{d\,sc}$

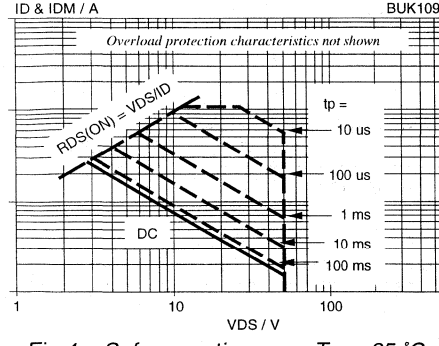


Fig.4. Safe operating area. $T_{mb} = 25\ ^\circ C$
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

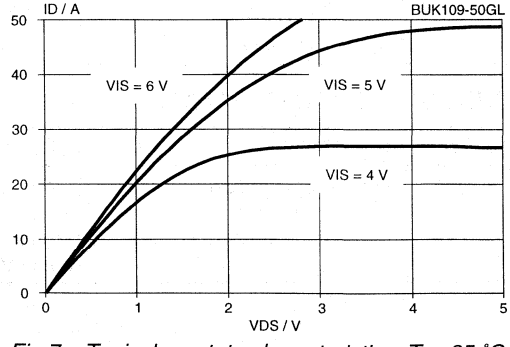


Fig.7. Typical on-state characteristics, $T_j = 25\ ^\circ C$.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$

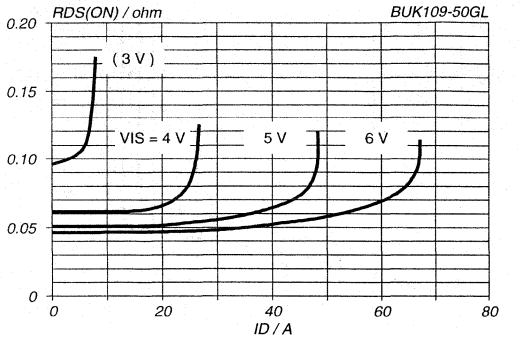


Fig.8. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

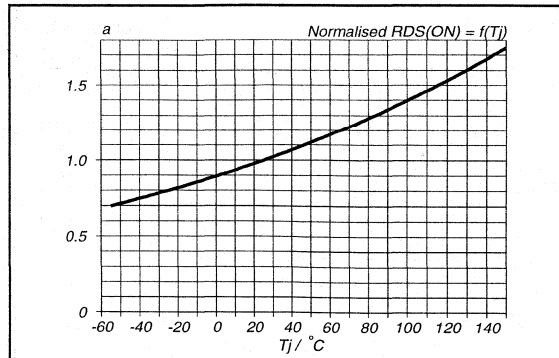


Fig.11. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25\ °C = f(T_j)$; I_D = 13 A; V_{IS} = 5 V

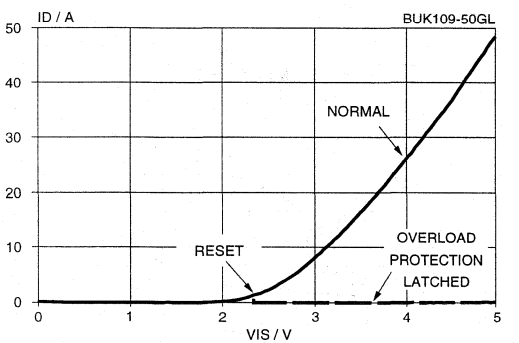


Fig.9. Typical transfer characteristics, T_j = 25 °C. $I_D = f(V_{IS})$; conditions: V_{DS} = 10 V; t_p = 250 µs

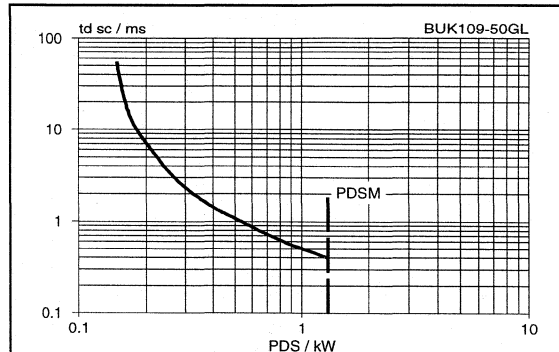


Fig.12. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{IS} \geq 4$ V; T_j = 25 °C.

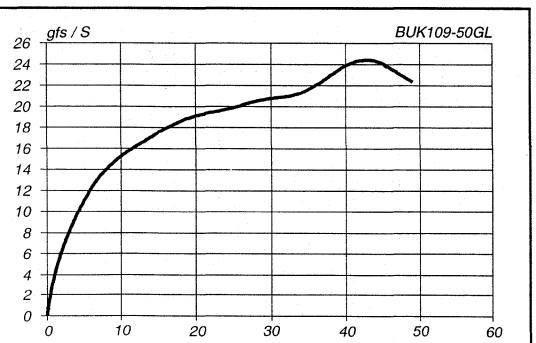


Fig.10. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V; t_p = 250 µs

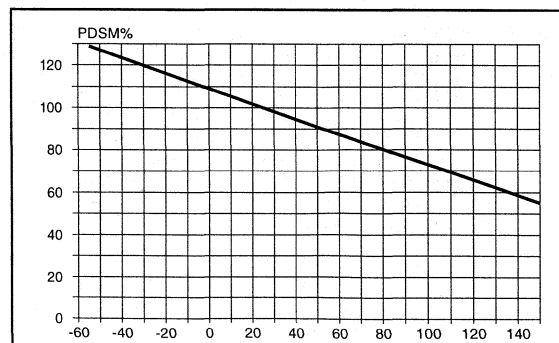


Fig.13. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ °C) = f(T_{mb})$

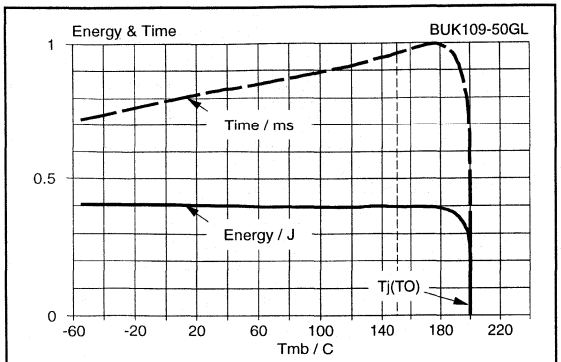


Fig.14. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; V_{IS} = 5 V; SC load = 30 mΩ

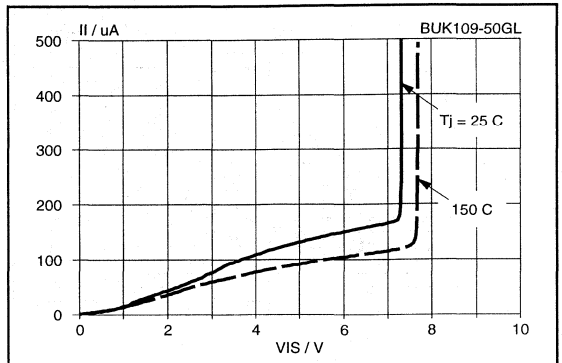


Fig.17. Typical DC input characteristics. $I_I = f(V_{IS})$; normal operation; parameter: T_j

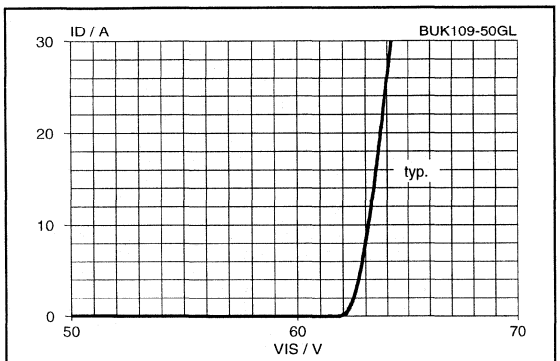


Fig.15. Typical clamping characteristics, 25 ˚C. $I_D = f(V_{DS})$; conditions: V_{IS} = 0 V; $t_p \leq 50$ µs

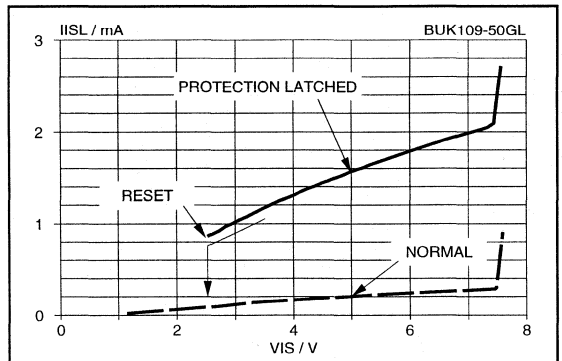


Fig.18. Typical DC input characteristics, T_j = 25 ˚C. $I_{ISL} = f(V_{IS})$; overload protection operated ⇒ I_D = 0 A

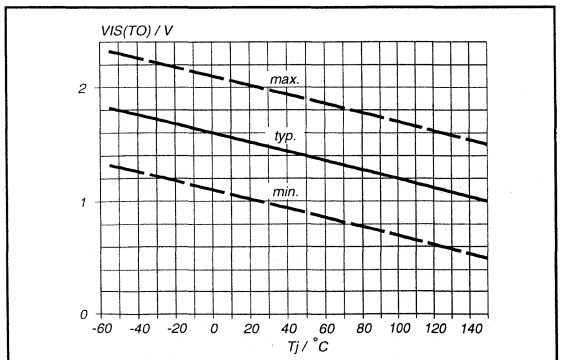


Fig.16. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

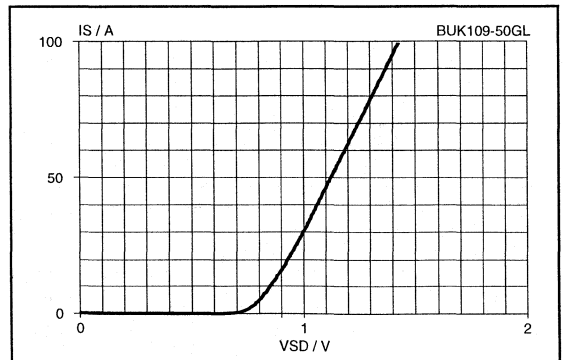


Fig.19. Typical reverse diode current, T_j = 25 ˚C. $I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V

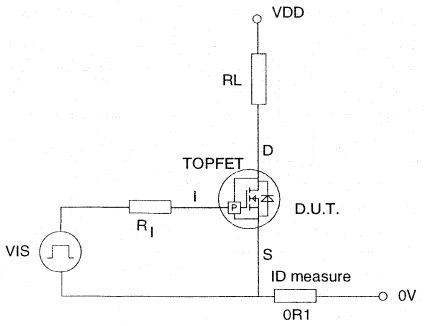


Fig.20. Test circuit for resistive load switching times.

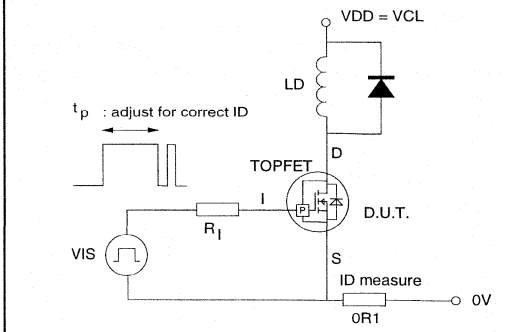


Fig.23. Test circuit for inductive load switching times.

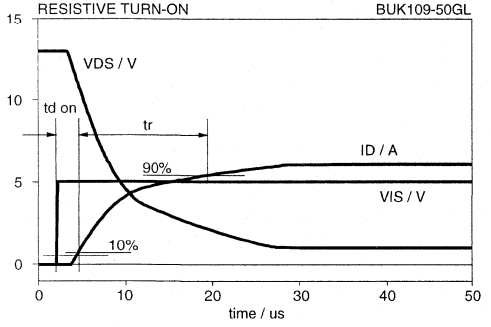


Fig.21. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 2.1 Ω; R_I = 50 Ω, T_j = 25 °C.

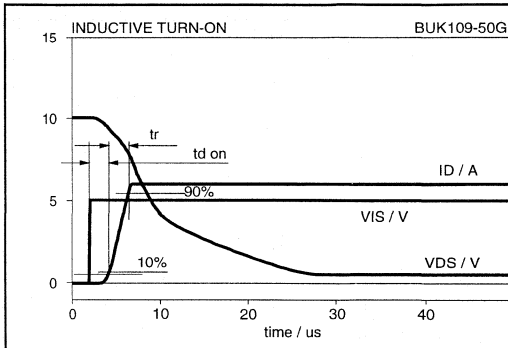


Fig.24. Typical switching waveforms, inductive load. V_{DD} = 10 V; I_D = 6 A; R_I = 50 Ω, T_j = 25 °C.

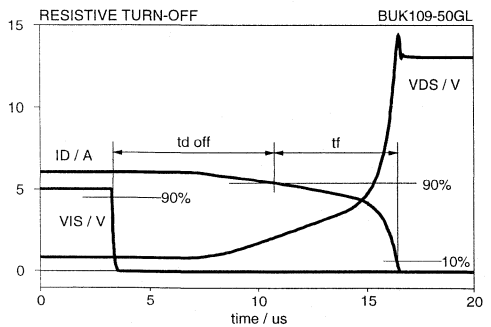


Fig.22. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 2.1 Ω; R_I = 50 Ω, T_j = 25 °C.

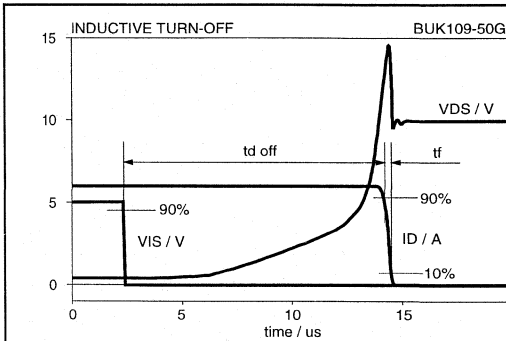


Fig.25. Typical switching waveforms, inductive load. V_{DD} = 10 V; I_D = 6 A; R_I = 50 Ω, T_j = 25 °C.

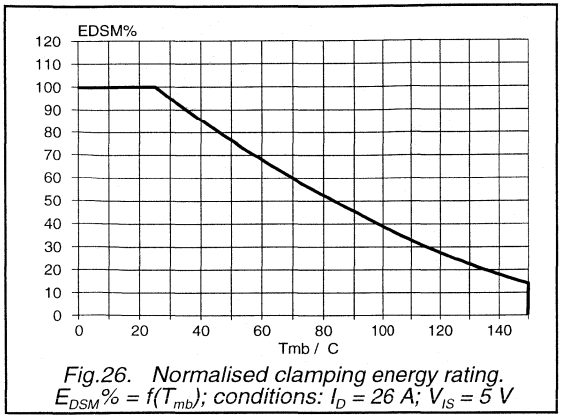


Fig.26. Normalised clamping energy rating. $E_{DSM}\% = f(T_{mb})$; conditions: I_D = 26 A; V_{IS} = 5 V

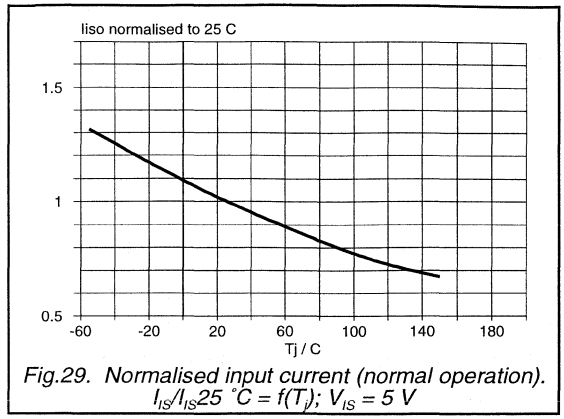


Fig.29. Normalised input current (normal operation). $I_{IS}/I_{IS}25\ ^{\circ}C = f(T_j)$; V_{IS} = 5 V

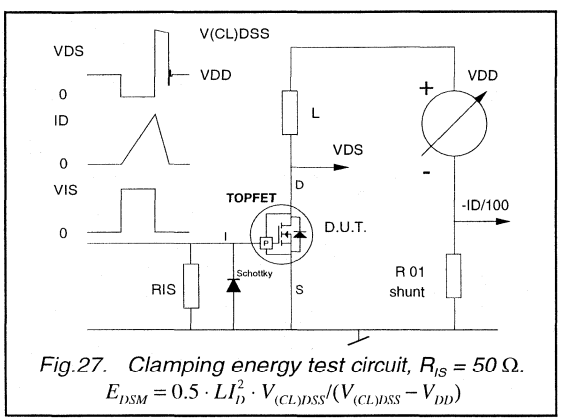


Fig.27. Clamping energy test circuit, R_{IS} = 50 Ω.

$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$$

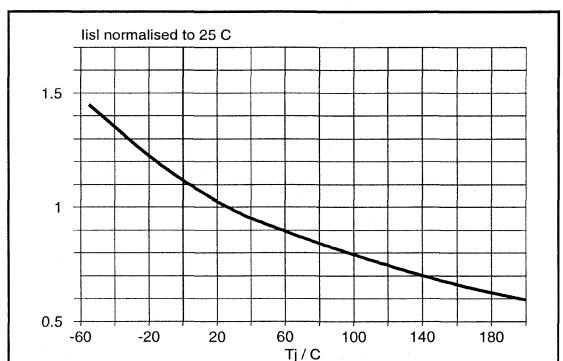


Fig.30. Normalised input current (protection latched). $I_{ISL}/I_{ISL}25\ ^{\circ}C = f(T_j)$; V_{IS} = 5 V

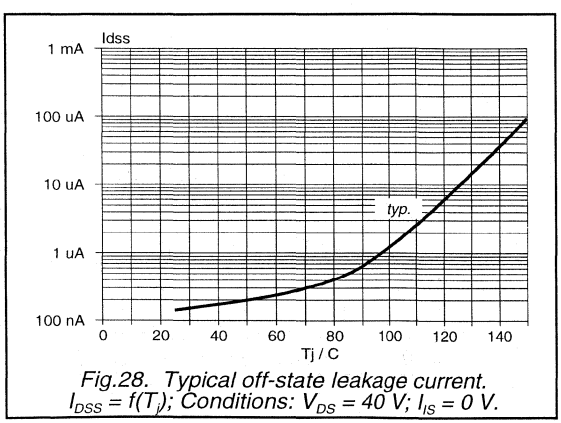


Fig.28. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

PowerMOS transistor Logic level TOPFET

BUK110-50DL

For maintenance only. Do not use for design-in.

DESCRIPTION

lonolithic temperature and verload protected logic level power IOSFET in a 3 pin plastic surface ount envelope, intended as a eneral purpose switch for utomotive systems and other pplications.

APPLICATIONS

eneral controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Lower operating input current permits direct drive by micro-controller
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER		MAX.	UNIT
V_{DS}	Continuous drain source voltage		50	V
I_D	Continuous drain current		45	A
P_D	Total power dissipation		125	W
T_j	Continuous junction temperature		150	°C
$R_{DS(ON)}$	Drain-source on-state resistance		35	mΩ
I_{ISL}	Input supply current	V_{IS} = 5 V	650	μA

FUNCTIONAL BLOCK DIAGRAM

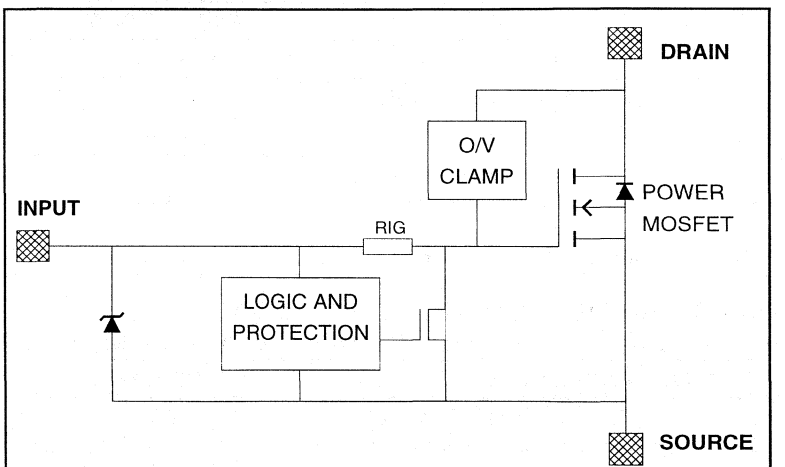
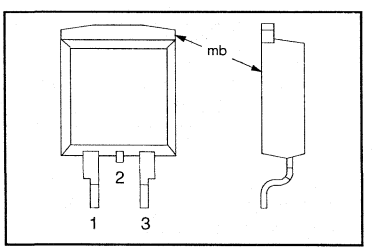


Fig.1. Elements of the TOPFET.

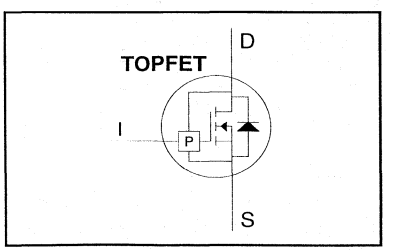
PINNING - SOT404

PIN	DESCRIPTION
1	input
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Continuous drain source voltage[1]	-	-	50	V
V_{IS}	Continuous input voltage	-	0	6	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; $V_{IS} = 5$ V	-	45	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; $V_{IS} = 5$ V	-	28	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; $V_{IS} = 5$ V	-	180	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	125	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	4	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	$V_{IS} = 5$ V	-	50	V
	Short circuit load protection[4]				
$V_{DDP(P)}$	Protected drain source supply voltage[5]	$V_{IS} = 5$ V	-	16	V
P_{DSM}	Instantaneous overload dissipation	$T_{mb} = 25$ °C	-	2.1	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	$V_{IS} = 0$ V	-	45	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; $I_{DM} = 25$ A; $V_{DD} \leq 20$ V; inductive load	-	1	J
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 85$ °C; $I_{DM} = 16$ A; $V_{DD} \leq 20$ V; f = 250 Hz	-	80	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

5 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than $V_{DDP(P)}$ maximum.

HERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	0.8	1	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	minimum footprint FR4 PCB	-	50	-	K/W

TATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 4 A; $t_p \leq 300\ \mu s$; $\delta \leq 0.01$	-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V	-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance[1]	V_{IS} = 5 V; I_{DM} = 25 A; $t_p \leq 300\ \mu s$; $\delta \leq 0.01$	-	30	35	mΩ

VERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[2]	T_{mb} = 25 °C; L ≤ 10 µH; R_L = 10 mΩ				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 5 V	-	1.1	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 5 V	-	0.8	-	ms
$I_{D(SC)}$	Drain current[3]	V_{DD} = 13 V; V_{IS} = 5 V	-	75	-	A
$I_{DM(SC)}$	Peak drain current[4]	V_{IS} = 5 V; V_{DD} = 13 V	-	200	-	A
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 5 V; from $I_D \geq 2$ A[5]	150	-	-	°C

RANSFER CHARACTERISTIC

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 25 A $t_p \leq 300\ \mu s$; $\delta \leq 0.01$	17	28	-	S

Continuous input voltage. The specified pulse width is for the drain current.

: Refer to OVERLOAD PROTECTION LIMITING VALUES.

Continuous drain-source supply voltage. Pulsed input voltage.

Continuous input voltage. Momentary short circuit load connection. (The higher peak current is due to the effect of capacitance Cgd).

The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA		1.0	1.5	2.0	V
I_{IS}	Input supply current	normal operation;	V_{IS} = 5 V	100	200	350	µA
			V_{IS} = 4 V	-	160	270	µA
V_{ISR}	Protection reset voltage[1]		T_j = 25 °C	2.0	2.6	3.5	V
			T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	protection latched;	V_{IS} = 5 V	-	330	650	µA
			V_{IS} = 3.5 V	-	240	430	µA
$V_{(BR)IS}$	Input breakdown voltage	I_I = 10 mA		6	-	-	V
R_{IG}	Input series resistance		T_j = 25 °C	-	33	-	kΩ
	to gate of power MOSFET		T_j = 150 °C	-	50	-	kΩ

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω. Refer to waveform figure and test circuit.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	30	-	µs
t_r	Rise time	resistive load R_L = 2.1 Ω	-	150	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	120	-	µs
t_f	Fall time	resistive load R_L = 2.1 Ω	-	120	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq 25$ °C; V_{IS} = 0 V	-	45	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDO}	Forward voltage	I_S = 45 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from upper edge of tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

1 The input voltage below which the overload protection circuits will be reset.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

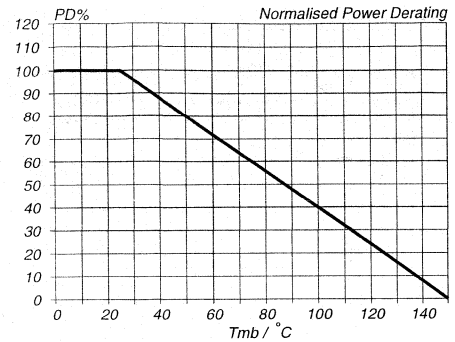


Fig.2. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D / P_D(25\ ^\circ C) = f(T_{mb})$

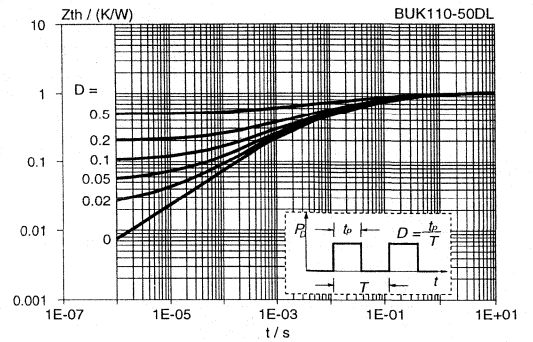


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

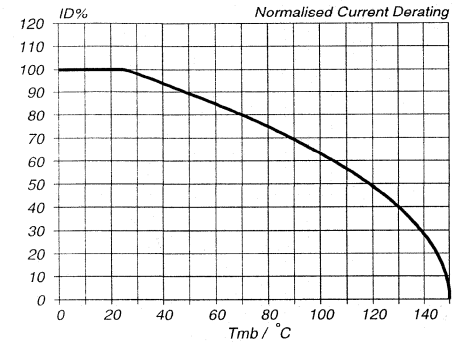


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D / I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

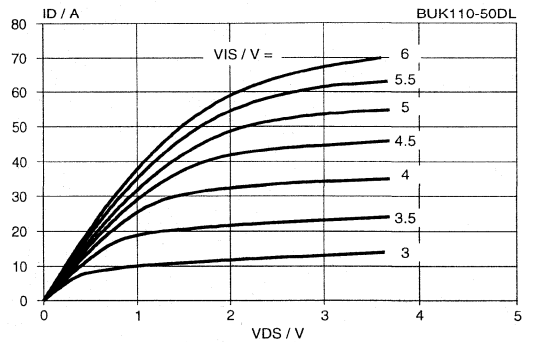


Fig.6. Typical on-state characteristics, $T_j = 25\ ^\circ C$.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 2$ ms

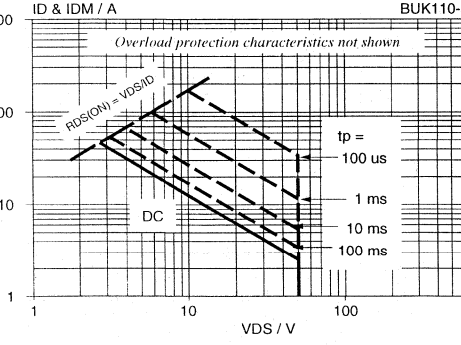


Fig.4. Safe operating area. $T_{mb} = 25\ ^\circ C$
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

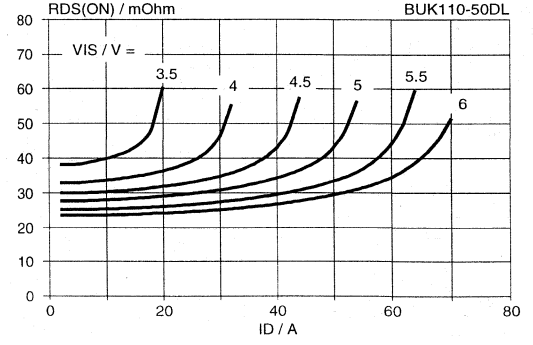


Fig.7. Typical on-state resistance, $T_j = 25\ ^\circ C$.
$R_{DS(ON)} = f(I_D)$; parameter V_{IS}; $t_p = 2$ ms

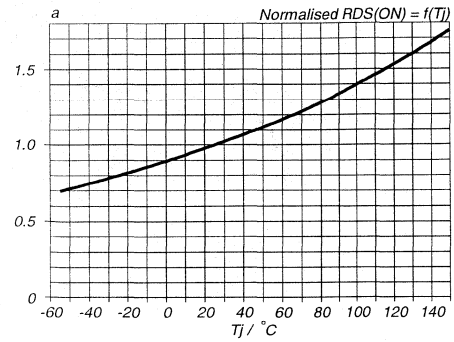


Fig.8. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25\ ^{\circ}C = f(T_j)$; $I_D = 25$ A; $V_{IS} = 5$ V

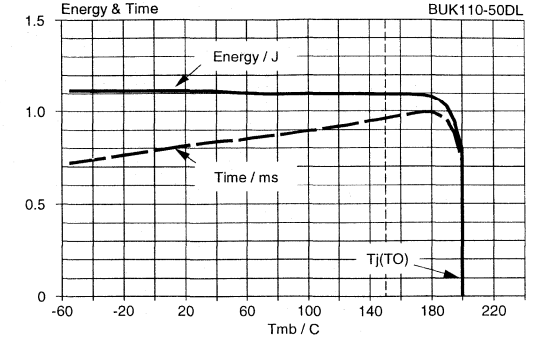


Fig.11. Typical overload protection characteristics. Conditions: $V_{DD} = 13$ V; $V_{IS} = 5$ V; SC load = 30 mΩ

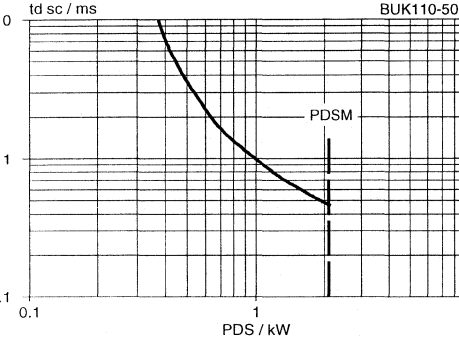


Fig.9. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{IS} \geq 4$ V; $T_j = 25\ ^{\circ}C$.

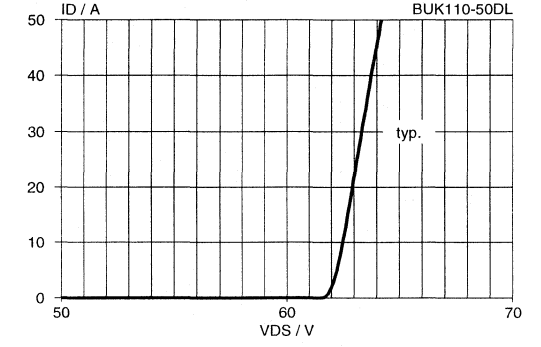


Fig.12. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: $V_{IS} = 0$ V; $t_p \leq 50$ µs

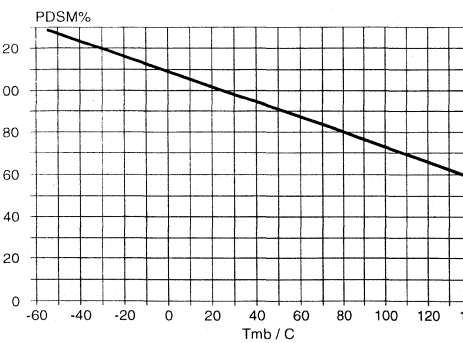


Fig.10. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ ^{\circ}C) = f(T_{mb})$

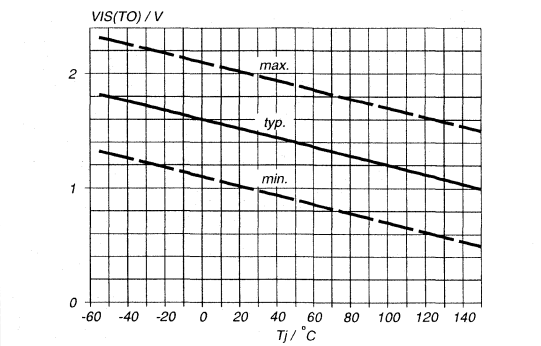


Fig.13. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = 5$ V

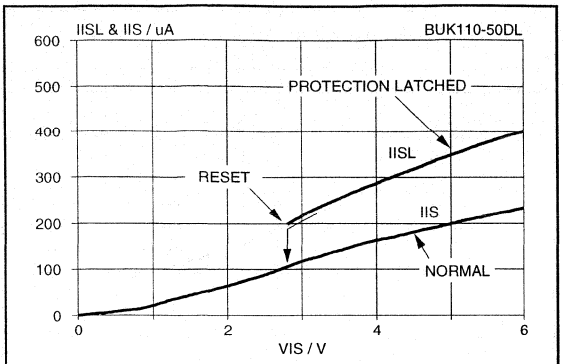


Fig.14. Typical DC input characteristics, T_j = 25 °C. I_{ISL} & I_{IS} = f(V_{IS}); protection latched & normal operation

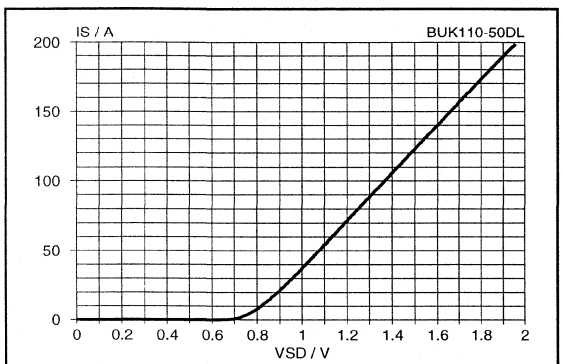


Fig.15. Typical reverse diode current, T_j = 25 °C. I_S = f(V_{SDS}); conditions: V_{IS} = 0 V; t_p = 250 µs

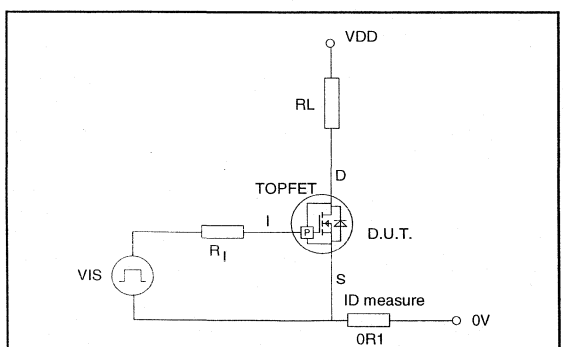


Fig.16. Test circuit for resistive load switching times.

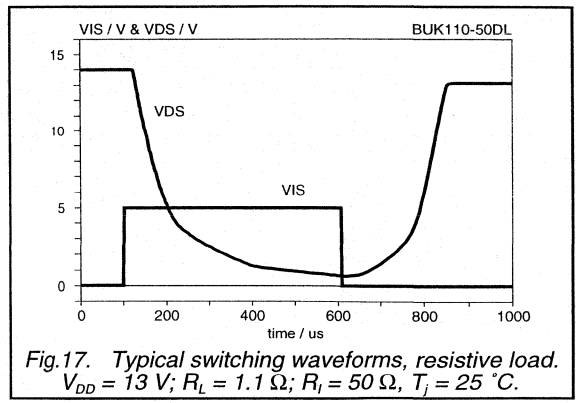


Fig.17. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 1.1 Ω; R_I = 50 Ω, T_j = 25 °C.

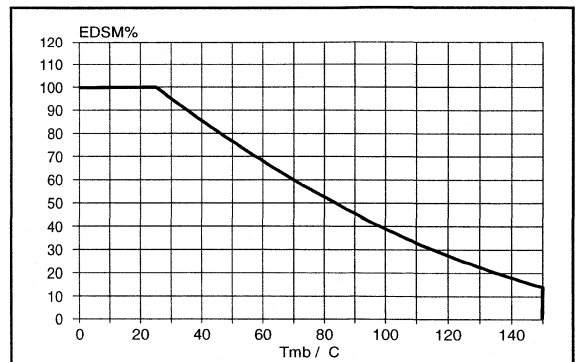


Fig.18. Normalised limiting clamping energy. E_{DSM}% = f(T_{mb}); conditions: I_D = 25 A; V_{IS} = 10 V

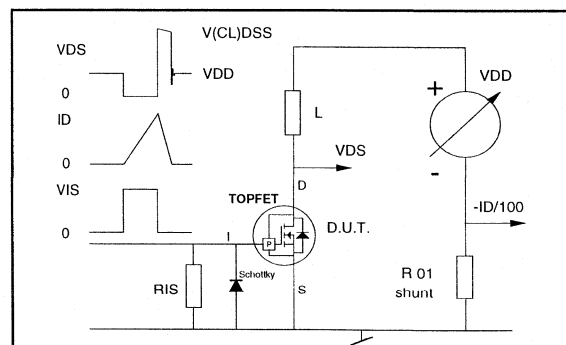


Fig.19. Clamping energy test circuit, R_{IS} = 50 Ω.

$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$$

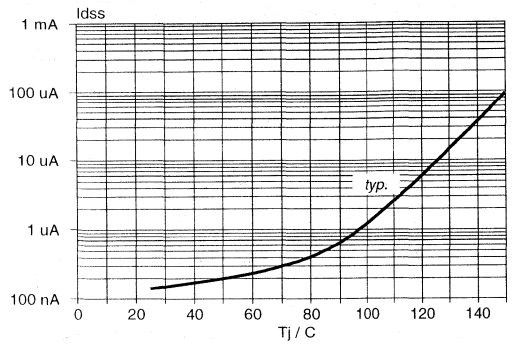


Fig.20. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_S = 0 V.

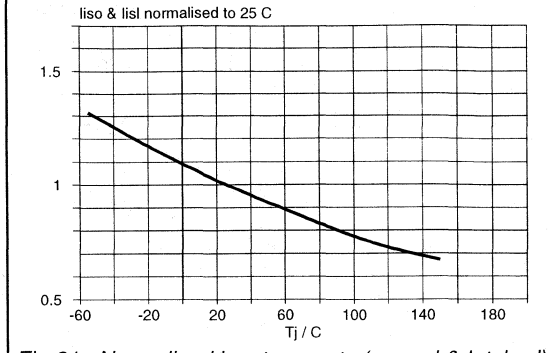


Fig.21. Normalised input currents (normal & latched). $I_{ISO}/I_{ISO}25^{\circ}C$ & $I_{ISL}/I_{ISL}25^{\circ}C = f(T_j)$; V_{IS} = 5 V

PowerMOS transistor Logic level TOPFET

BUK110-50GL

For maintenance only. Do not use for design-in.

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 3 pin plastic surface mount envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V input level
- Low threshold voltage also allows 5 V control
- Control of power MOSFET and supply of overload protection circuits derived from input
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	45	A
P_D	Total power dissipation	125	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{IS} = 5 V	35	mΩ

FUNCTIONAL BLOCK DIAGRAM

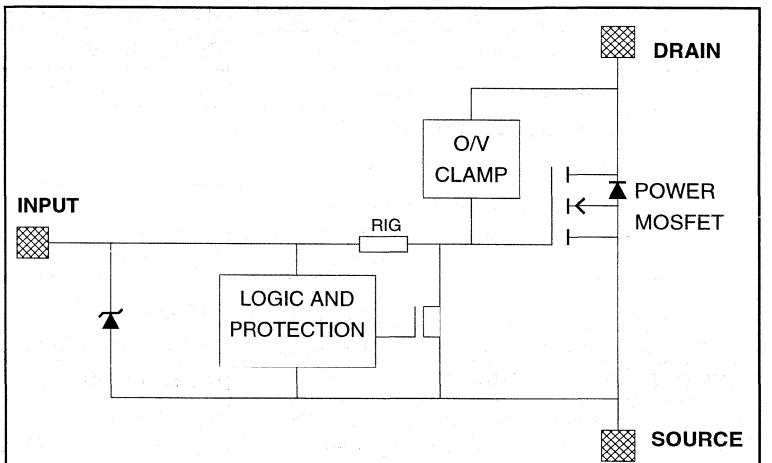
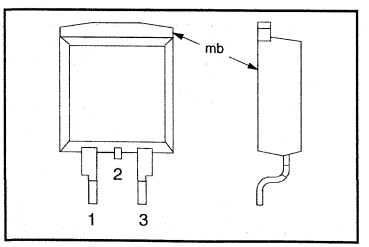


Fig.1. Elements of the TOPFET.

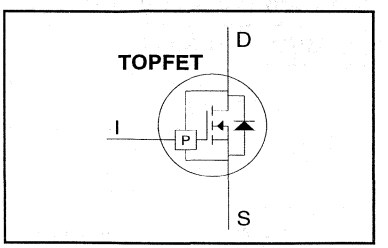
PINNING - SOT404

PIN	DESCRIPTION
1	input
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Continuous off-state drain source voltage[1]	V_{IS} = 0 V	-	50	V
V_{IS}	Continuous input voltage	-	0	6	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; V_{IS} = 5 V	-	45	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; V_{IS} = 5 V	-	28	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; V_{IS} = 5 V	-	180	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	125	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	4	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 5 V	-	50	V
	Short circuit load protection				
$V_{DDP(P)}$	Protected drain source supply voltage[4]	V_{IS} = 5 V	-	24	V
P_{DSM}	Instantaneous overload dissipation	T_{mb} = 25 °C	-	2.1	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	V_{IS} = 0 V	-	45	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; I_{DM} = 25 A; $V_{DD} \leq 25$ V; inductive load	-	1	J
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 85$ °C; I_{DM} = 16 A; $V_{DD} \leq 20$ V; f = 250 Hz	-	80	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	0.8	1.0	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	minimum footprint FR4 PCB	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 4 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V	-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	I_{DM} = 25 A; V_{IS} = 5 V; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	30	35	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	T_{mb} = 25 °C; L ≤ 10 µH				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 5 V	-	1.1	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 5 V	-	0.8	-	ms
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 5 V; from $I_D \geq 2$ A[2]	150	-	-	°C

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA	1.0	1.5	2.0	V
I_{IS}	Input supply current	V_{IS} = 5 V; normal operation	-	0.2	0.35	mA
V_{ISR}	Protection reset voltage[3]		2.0	2.6	3.5	V
V_{ISR}	Protection reset voltage	T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	V_{IS} = 5 V; protection latched	2	3.8	10	mA
$V_{(BR)IS}$	Input clamp voltage	I_I = 10 mA	6	-	-	V
R_{IG}	Input series resistance	to gate of power MOSFET	-	1.5	-	kΩ

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum. Refer to OVERLOAD PROTECTION LIMITING VALUES.

2 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

3 The input voltage below which the overload protection circuits will be reset.

TRANSFER CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 25 A $t_p \leq$ 300 µs; $\delta \leq 0.01$	17	28	-	S
$I_{D(SC)}$	Drain current[1]	V_{DS} = 13 V; V_{IS} = 5 V	-	60	-	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω. Refer to waveform figures and test circuits.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	2	-	µs
t_r	Rise time	resistive load R_L = 1.1 Ω	-	8	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	8	-	µs
t_f	Fall time	resistive load R_L = 1.1 Ω	-	8	-	µs
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	3.7	-	µs
t_r	Rise time	inductive load I_{DM} = 11 A	-	3.7	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	13	-	µs
t_f	Fall time	inductive load I_{DM} = 11 A	-	1.4	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq$ 25 °C; V_{IS} = 0 V	-	50	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	I_S = 50 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from upper edge of tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

1 During overload before short circuit load protection operates.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

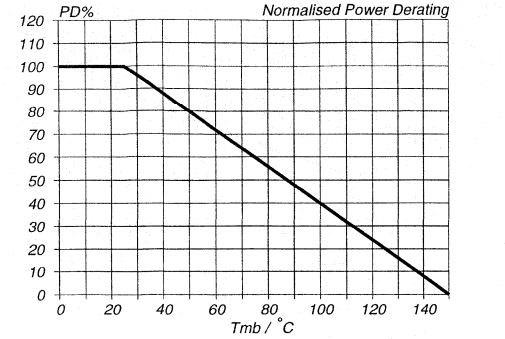


Fig.2. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

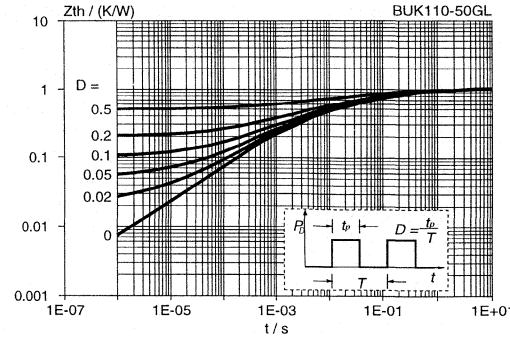


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

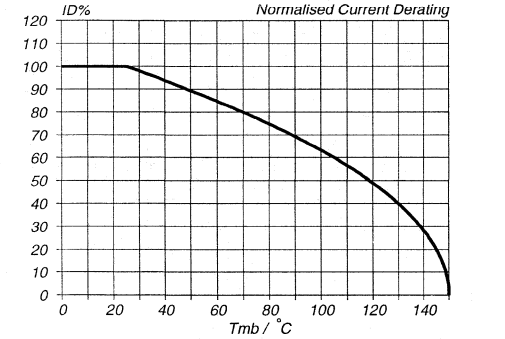


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

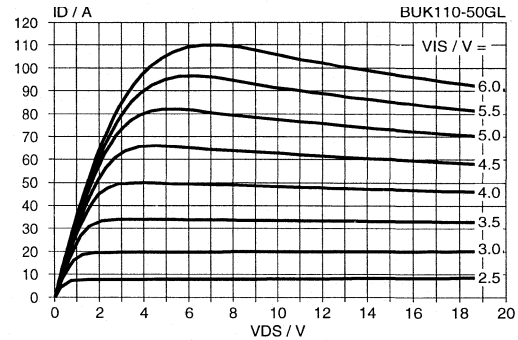


Fig.6. Typical output characteristics, $T_j = 25\ ^\circ C$.
ID = $f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$ & $t_p < t_{d\,sc}$

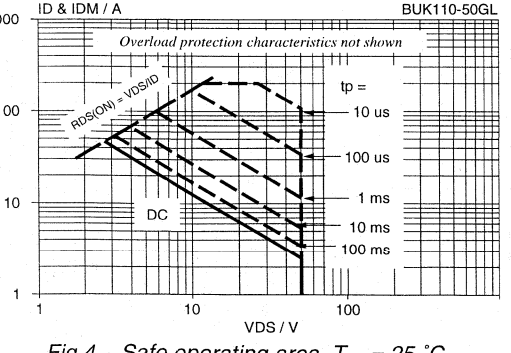


Fig.4. Safe operating area. $T_{mb} = 25\ ^\circ C$
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

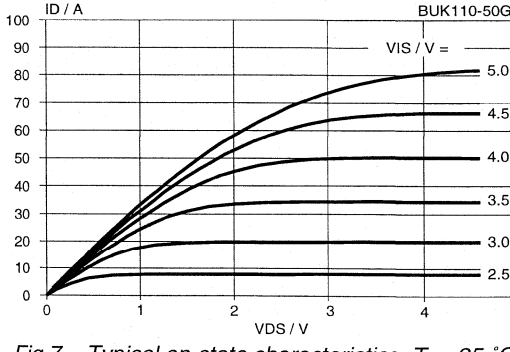


Fig.7. Typical on-state characteristics, $T_j = 25\ ^\circ C$.
ID = $f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$

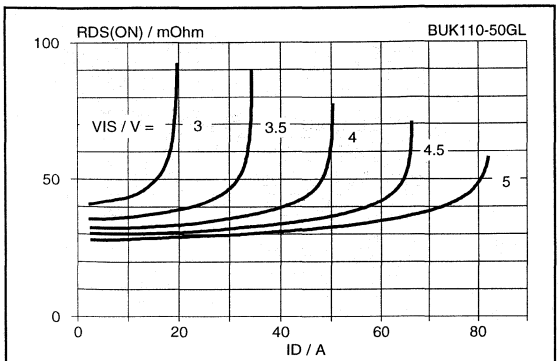


Fig.8. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

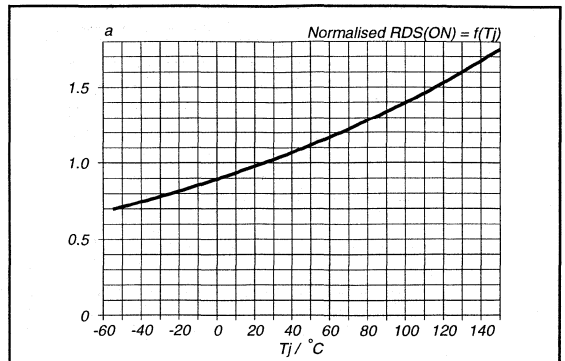


Fig.11. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25\ ^\circ C = f(T_j)$; I_D = 25 A; V_{IS} = 5 V

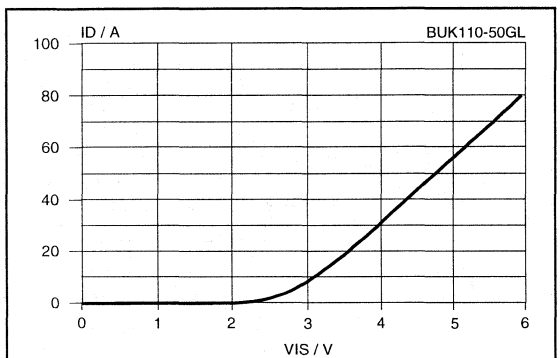


Fig.9. Typical transfer characteristics, T_j = 25 ˚C. $I_D = f(V_{IS})$; conditions: V_{DS} = 10 V; t_p = 250 µs

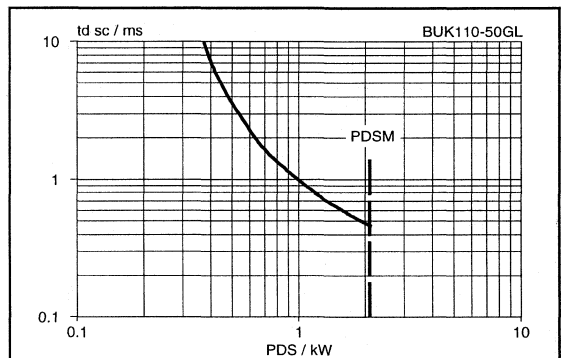


Fig.12. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{IS} \geq 4$ V; T_j = 25 ˚C.

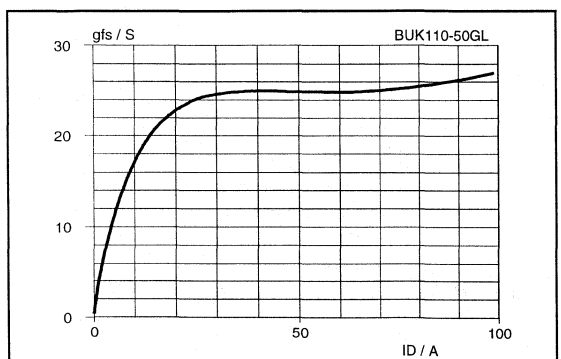


Fig.10. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V; t_p = 250 µs

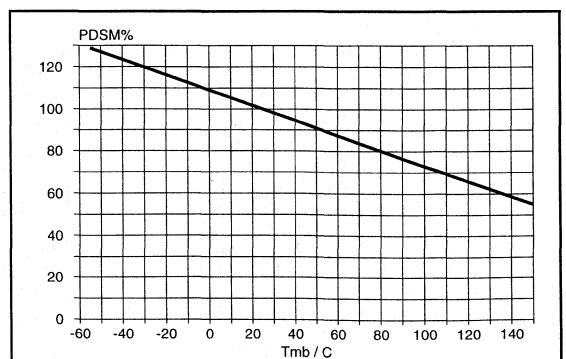


Fig.13. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ ^\circ C) = f(T_{mb})$

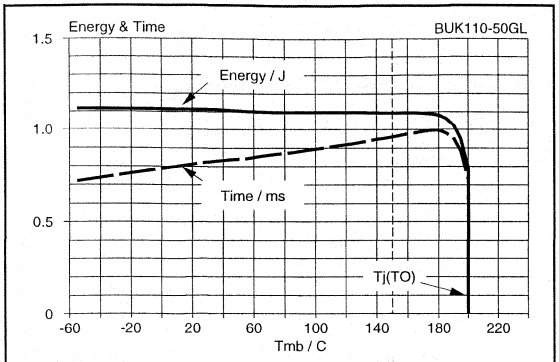


Fig.14. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; V_{IS} = 5 V; SC load = 30 mΩ

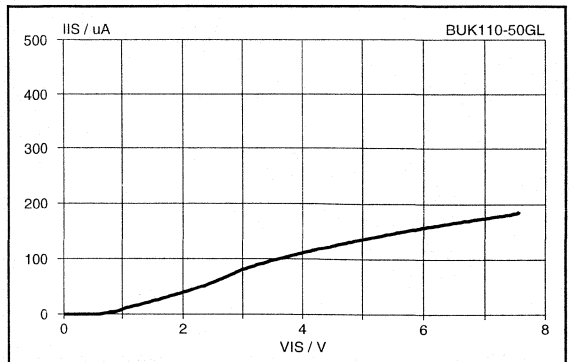


Fig.17. Typical DC input characteristics, T_j = 25 ˚C. $I_{IS} = f(V_{IS})$; normal operation

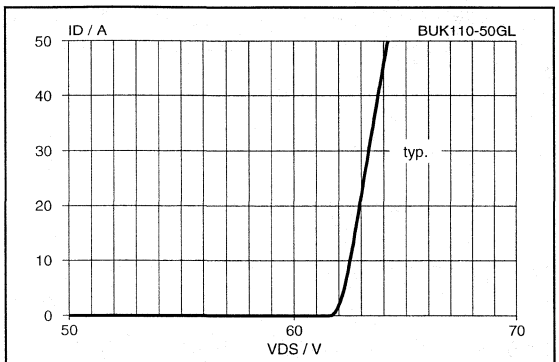


Fig.15. Typical clamping characteristics, 25 ˚C. $I_D = f(V_{DS})$; conditions: V_{IS} = 0 V; $t_p \leq 50$ µs

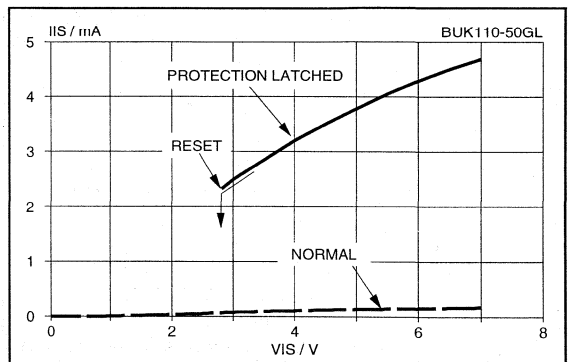


Fig.18. Typical DC input characteristics, T_j = 25 ˚C. $I_{ISL} = f(V_{IS})$; overload protection operated ⇒ I_D = 0 A

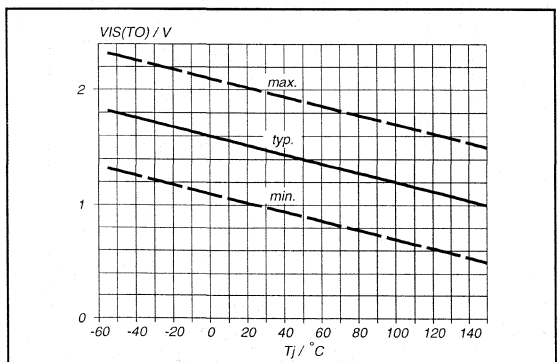


Fig.16. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

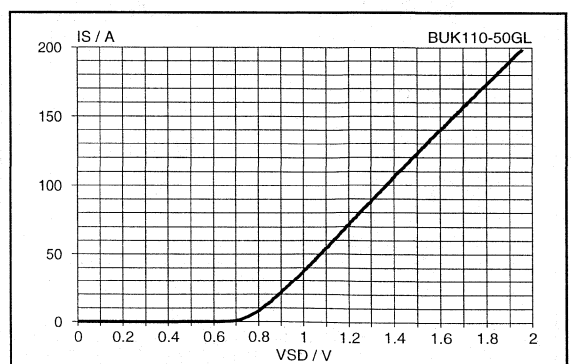


Fig.19. Typical reverse diode current, T_j = 25 ˚C. $I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V; t_p = 250 µs

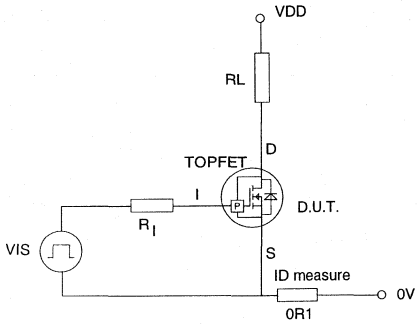


Fig.20. Test circuit for resistive load switching times.

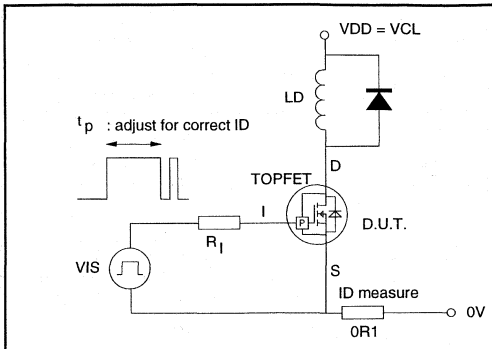


Fig.23. Test circuit for inductive load switching times.

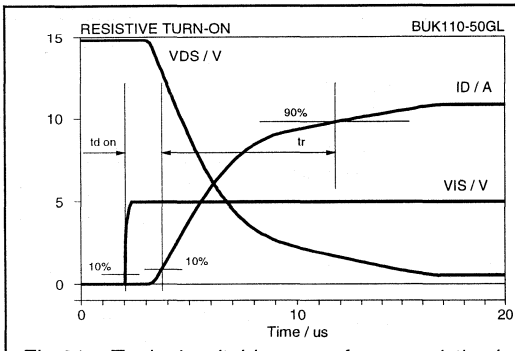


Fig.21. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 1.1 Ω; R_I = 50 Ω, T_j = 25 °C.

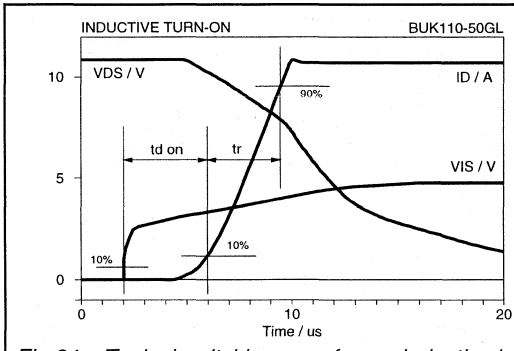


Fig.24. Typical switching waveforms, inductive load. V_{DD} = 13 V; I_D = 11 A; R_I = 50 Ω, T_j = 25 °C.

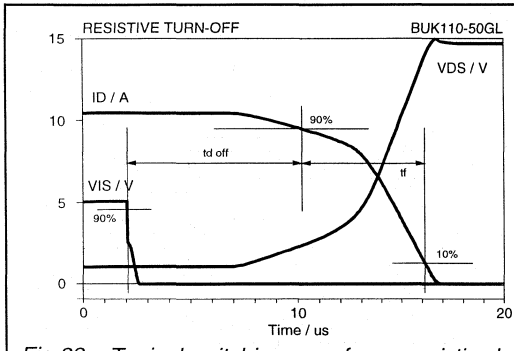


Fig.22. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 1.1 Ω; R_I = 50 Ω, T_j = 25 °C.

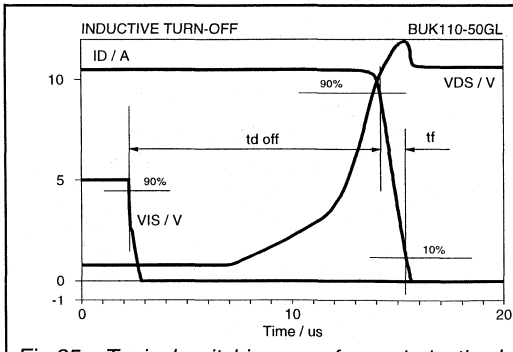


Fig.25. Typical switching waveforms, inductive load. V_{DD} = 13 V; I_D = 11 A; R_I = 50 Ω, T_j = 25 °C.

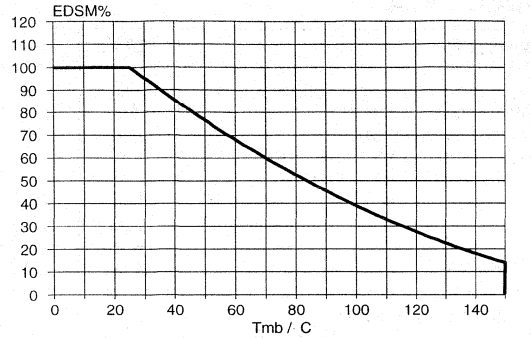


Fig.26. Normalised limiting clamping energy. E_{DSM}% = f(T_{mb}); conditions: I_D = 25 A; V_{IS} = 10 V

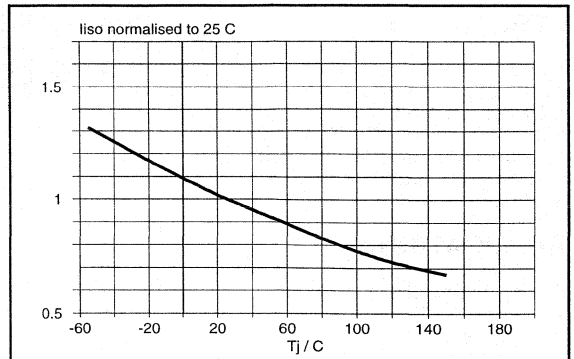


Fig.29. Normalised input current (normal operation). I_{IS}/I_{IS}25 °C = f(T_j); V_{IS} = 5 V

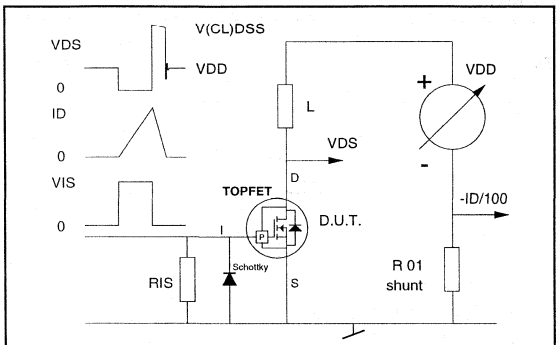


Fig.27. Clamping energy test circuit, R_{IS} = 50 Ω.
$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$$

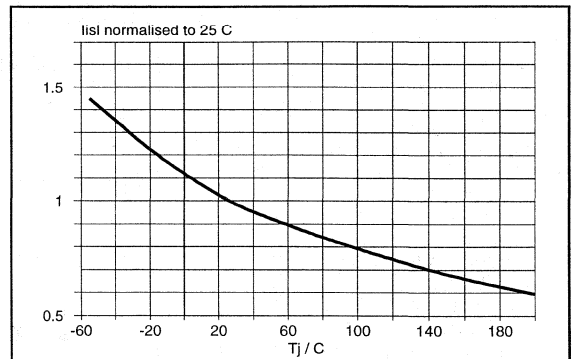


Fig.30. Normalised input current (protection latched). I_{ISL}/I_{ISL}25 °C = f(T_j); V_{IS} = 5 V

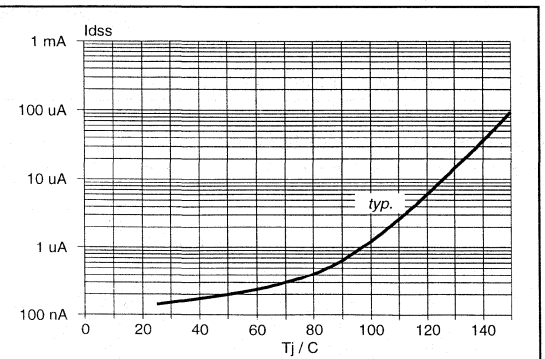


Fig.28. Typical off-state leakage current. I_{DSS} = f(T_j); Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

Logic level TOPFET
SMD version of BUK104-50L/S

BUK114-50L/S

For maintenance only. Do not use for design-in.

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 5 pin surface mounting plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Logic and protection supply from separate pin
- Low operating supply current
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by protection supply
- Protection circuit condition indicated by flag pin
- 5 V logic compatible input level
- Separate input pin for higher frequency drive
- ESD protection on input, flag and protection supply pins
- Over voltage clamping for turn off of inductive loads
- Both linear and switching operation are possible

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	15	A
P_{tot}	Total power dissipation	40	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance		
	V_{IS} = 5 V	125	mΩ
	V_{IS} = 7 V	100	mΩ
SYMBOL	**PARAMETER**	**NOM.**	**UNIT**
V_{PSN}	Protection supply voltage		
	BUK114-50L	5	V
	BUK114-50S	10	V

FUNCTIONAL BLOCK DIAGRAM

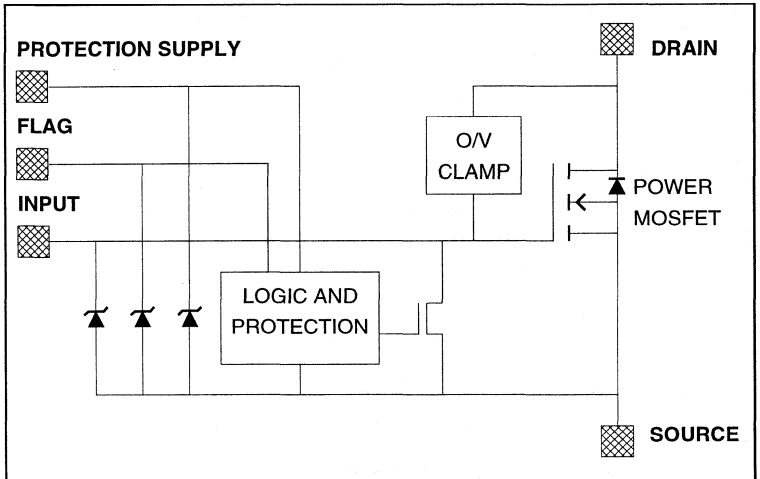


Fig.1. Elements of the TOPFET.

PINNING - SOT426

PIN	DESCRIPTION
1	input
2	flag
3	(connected to mb)
4	protection supply
5	source
mb	drain

PIN CONFIGURATION

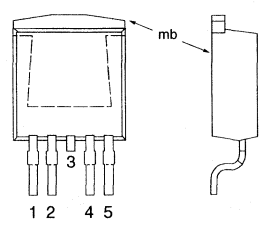


Fig. 2.

SYMBOL

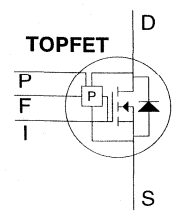


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Voltages				
V_{DSS}	Continuous off-state drain source voltage[1]	V_{IS} = 0 V	-	50	V
V_{IS}	Continuous input voltage	-	0	11	V
V_{FS}	Continuous flag voltage	-	0	11	V
V_{PS}	Continuous supply voltage	-	0	11	V
	Currents	V_{IS} =	-	7 | 5	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C	-	15 | 13	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C	-	9.5 | 8.5	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C	-	60 | 54	A
	Thermal				
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	40	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Junction temperature[2]	continuous	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply connected, TOPFET can protect itself from two types of overload - over temperature and short circuit load.

An n-MOS transistor turns on between the input and source to quickly discharge the power MOSFET gate capacitance.

For internal overload protection to remain latched while the control circuit is high, external series input resistance must be provided. Refer to INPUT CHARACTERISTICS.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
		V_{IS} =	7 | 5	-	V
V_{PSP}	Protection supply voltage[3]	for valid protection			
		BUK114-50L	4.4 | 4	-	V
		BUK114-50S	5.4 | 5	-	V
	Over temperature protection	$V_{PS} = V_{PSN}$			
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 10 V; $R_I \geq 2$ kΩ	-	50	V
		V_{IS} = 5 V; $R_I \geq 1$ kΩ	-	50	V
	Short circuit load protection	$V_{PS} = V_{PSN}$; L ≤ 10 µH			
$V_{DDP(P)}$	Protected drain source supply voltage[4]	V_{IS} = 10 V; $R_I \geq 2$ kΩ	-	25	V
		V_{IS} = 5 V; $R_I \geq 1$ kΩ	-	45	V
P_{DSM}	Instantaneous overload dissipation		-	0.8	kW

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The minimum supply voltage required for correct operation of the overload protection circuits.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DRRM}	Repetitive peak clamping drain current	$R_{IS} \geq 100\ \Omega$[1]	-	15	A
E_{DSM}	Non-repetitive inductive turn-off energy[2]	$I_{DM} = 15$ A; $R_{IS} \geq 100\ \Omega$	-	200	mJ
E_{DRM}	Repetitive inductive turn-off energy	$R_{IS} \geq 100\ \Omega$; $T_{mb} \leq 95$ °C; $I_{DM} = 4$ A; $V_{DD} \leq 20$ V; f = 250 Hz	-	20	mJ
I_{DIRM}	Repetitive peak drain to input current[3]	$R_{IS} = 0\ \Omega$; $t_p \leq 1$ ms	-	50	mA

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} = 25$ °C; $V_{IS} = V_{PS} = V_{FS} = 0$ V	-	15	A

THERMAL CHARACTERISTIC

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	2.5	3.1	K/W

STATIC CHARACTERISTICS

$T_{mb} = 25$ °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSR}$	Drain-source clamping voltage	$R_{IS} = 100\ \Omega$; $I_D = 10$ mA		50	-	65	V
$V_{(CL)DSR}$	Drain-source clamping voltage	$R_{IS} = 100\ \Omega$; $I_{DM} = 1$ A; $t_p \leq 300\ \mu$s; $\delta \leq 0.01$		50	-	70	V
I_{DSS}	Zero input voltage drain current	$V_{DS} = 12$ V; $V_{IS} = 0$ V		-	0.5	10	µA
I_{DSR}	Drain source leakage current	$V_{DS} = 50$ V; $R_{IS} = 100\ \Omega$;		-	1	20	µA
I_{DSR}	Drain source leakage current	$V_{DS} = 40$ V; $R_{IS} = 100\ \Omega$; $T_j = 125$ °C		-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	$I_{DM} = 7.5$ A; $t_p \leq 300\ \mu$s; $\delta \leq 0.01$	$V_{IS} = 7$ V	-	75	100	mΩ
			$V_{IS} = 5$ V	-	95	125	mΩ

1 The input pin must be connected to the source pin by a specified external resistance to allow the power MOSFET gate source voltage to become sufficiently positive for active clamping. Refer to INPUT CHARACTERISTICS.

2 While the protection supply voltage is connected, during overvoltage clamping it is possible that the overload protection may operate at energies close to the limiting value. Refer to OVERLOAD PROTECTION CHARACTERISTICS.

3 Shorting the input to source with low resistance inhibits the internal overvoltage protection by preventing the power MOSFET gate source voltage becoming positive.

OVERLOAD PROTECTION CHARACTERISTICS

With adequate protection supply voltage TOPFET detects when one of the overload thresholds is exceeded.

Provided there is adequate input series resistance it switches off and remains latched off until reset by the protection supply pin.

Refer also to OVERLOAD PROTECTION LIMITING VALUES and INPUT CHARACTERISTICS.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	$V_{PS} = V_{PSN}$[2]; $T_{mb} = 25$ °C; $L \leq 10$ µH; $R_I \geq 2$ kΩ				
$E_{DS(TO)}$	Overload threshold energy	$V_{DD} = 13$ V; $V_{IS} = 10$ V	-	150	-	mJ
$t_{d\,sc}$	Response time	$V_{DD} = 13$ V; $V_{IS} = 10$ V	-	375	-	µs
	Over temperature protection	$V_{PS} = V_{PSN}$; $R_I \geq 2$ kΩ				
$T_{j(TO)}$	Threshold junction temperature	from $I_D \geq 0.65$ A[3]	150	-	-	°C

TRANSFER CHARACTERISTICS

$T_{mb} = 25$ °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 10$ V; $I_{DM} = 7.5$ A $t_p \leq 300$ µs; $\delta \leq 0.01$	5	9	-	S
I_D	Drain current[4]	$V_{DS} = 13$ V; $V_{IS} = 5$ V	-	25	-	A
		$V_{IS} = 10$ V		40	-	A

PROTECTION SUPPLY CHARACTERISTICS

$T_{mb} = 25$ °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Protection supply					
I_{PS}, I_{PSL}	Protection supply current	normal operation or protection latched				
		BUK114-50L $V_{PS} = 5$ V	-	0.2	0.35	mA
		BUK114-50S $V_{PS} = 10$ V	-	0.4	1.0	mA
V_{PSR}	Protection reset voltage[5]		1.5	2.5	3.5	V
		$T_j = 150$ °C	1.0	-	-	V
$V_{(CL)PS}$	Protection clamp voltage	$I_P = 1.35$ mA	11	13	-	V

REVERSE DIODE CHARACTERISTICS

$T_{mb} = 25$ °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	$I_S = 15$ A; $V_{IS} = V_{PS} = V_{FS} = 0$ V; $t_p = 300$ µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[6]	-	-	-	-

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum.

2 At the appropriate nominal protection supply voltage for each type. Refer to QUICK REFERENCE DATA.

3 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

4 During overload condition. Refer also to OVERLOAD PROTECTION LIMITING VALUES and CHARACTERISTICS.

5 The supply voltage below which the overload protection circuits will be reset.

6 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
	Normal operation						
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA		1.0	1.5	2.0	V
			T_{mb} = 150 °C	0.5	-	-	V
I_{IS}	Input current	V_{IS} = 10 V		-	10	100	nA
$V_{(CL)IS}$	Input clamp voltage	I_I = 1 mA		11	13	-	V
	Overload protection latched						
R_{ISL}	Input resistance[1]	V_{PS} = 5 V	I_I = 5 mA;	-	55	-	Ω
			T_{mb} = 150 °C	-	95	-	Ω
		V_{PS} = 10 V	I_I = 5 mA;	-	35	-	Ω
			T_{mb} = 150 °C	-	60	-	Ω
	Application information						
	External input resistances for	(see figure 29)					
R_{IS}	internal overvoltage clamping[2]	R_I = ∞ Ω;	V_{DS} > 30 V	100	-	-	Ω
R_I	internal overload protection[3]	R_{IS} = ∞ Ω;	V_{II} = 5 V	1	-	-	kΩ
			V_{II} = 10 V	2	-	-	kΩ

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C; R_I = 50 Ω; R_{IS} = 50 Ω (see figure 29); resistive load R_L = 10 Ω. For waveforms see figure 28.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 15 V; V_{IS}: 0 V ⇒ 10 V	-	8	-	ns
t_r	Rise time		-	13	-	ns
$t_{d\,off}$	Turn-off delay time	V_{DD} = 15 V; V_{IS}: 10 V ⇒ 0 V	-	100	-	ns
t_f	Fall time		-	45	-	ns

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{iss}	Input capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	415	600	pF
C_{oss}	Output capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	275	400	pF
C_{rss}	Reverse transfer capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	55	80	pF
C_{pso}	Protection supply pin capacitance	V_{PS} = 10 V	-	30	-	pF
C_{fso}	Flag pin capacitance	V_{FS} = 10 V; V_{PS} = 0 V	-	20	-	pF

1 The resistance of the internal transistor which discharges the power MOSFET gate capacitance when overload protection operates.
The external drive circuit should be such that the input voltage does not exceed $V_{IS(TO)}$ minimum when the overload protection has operated. Refer also to figure for latched input characteristics.

2 Applications using a lower value for R_{IS} would require external overvoltage protection.

3 For applications requiring a lower value for R_I, an external overload protection strategy is possible using the flag pin to 'tell' the control circuit to switch off the input.

FLAG DESCRIPTION

The flag pin provides a means to detect the presence of the protection supply and indicate the state of the overload detectors. The flag is the open drain of an n-MOS transistor and requires an external pull-up resistor[1]. It is suitable for both 5 V and 10 V logic. Flag may be used to implement an external protection strategy[2] for applications which require low input drive impedance.

TRUTH TABLE

CONDITION	DESCRIPTION	FLAG
NORMAL	Normal operation and adequate protection supply voltage	LOGIC LOW
OVER TEMP.	Over temperature detected	LOGIC HIGH
SHORT CIRCUIT	Overload condition detected	LOGIC HIGH
SUPPLY FAULT	Inadequate protection supply voltage	LOGIC HIGH

FLAG CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Flag 'low'	normal operation				
V_{FS}	Flag voltage	I_F = 1.6 mA	-	0.15	0.4	V
I_{FSS}	Flag saturation current	V_{FS} = 10 V	-	15	-	mA
	Flag 'high'	overload or fault				
I_{FS}	Flag leakage current	V_{FS} = 10 V	-	-	10	µA
V_{PSF}	Protection supply threshold voltage	V_{FF} = 5 V; R_F = 3 kΩ;				
		BUK114-50L	2.5	3.3	4	V
		BUK114-50S	3.3	4.2	5	V
$V_{(CL)FS}$	Flag clamping voltage	I_F = 1 mA; V_{PS} = 0 V	11	13	-	V
	Application information					
R_F	Suitable external pull-up resistance	V_{FF} =5 V	1	10	50	kΩ
		V_{FF} =10 V	2	20	100	kΩ

Even if the flag pin is not used, it is recommended that it is connected to the protection supply via a pull-up resistor. It should not be left floating.

Low pass filtering of the flag signal may be advisable to prevent false tripping.

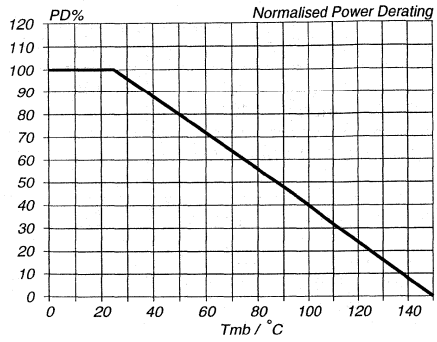


Fig.4. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

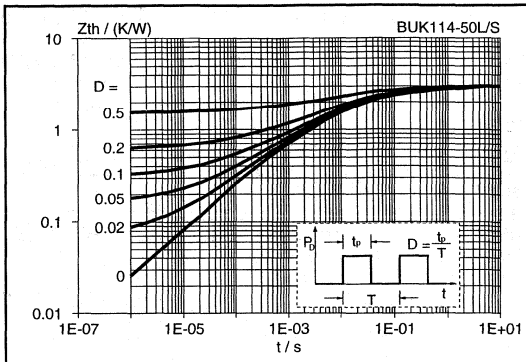


Fig.7. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

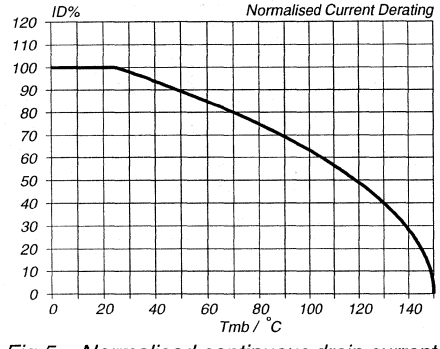


Fig.5. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

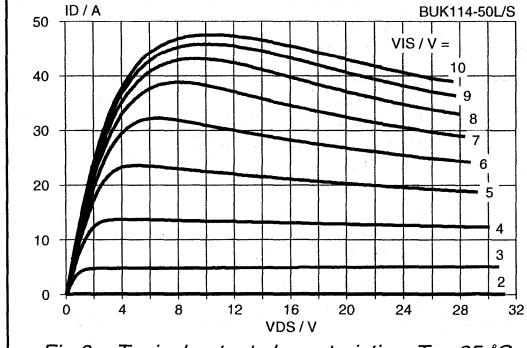


Fig.8. Typical output characteristics, $T_j = 25\ ^\circ C$.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$ & $t_p < t_{d\,sc}$

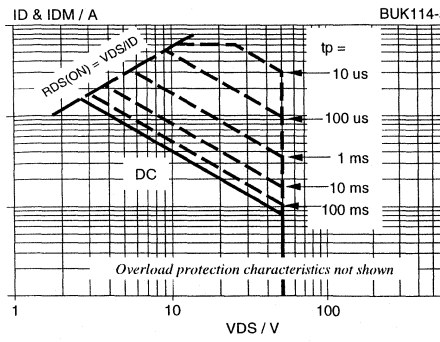


Fig.6. Safe operating area. $T_{mb} = 25\ ^\circ C$
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

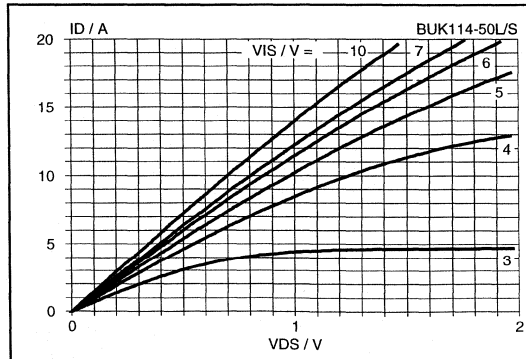


Fig.9. Typical on-state characteristics, $T_j = 25\ ^\circ C$.
$I_D = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$

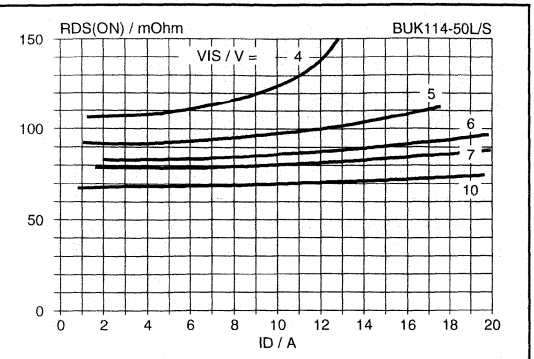


Fig.10. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

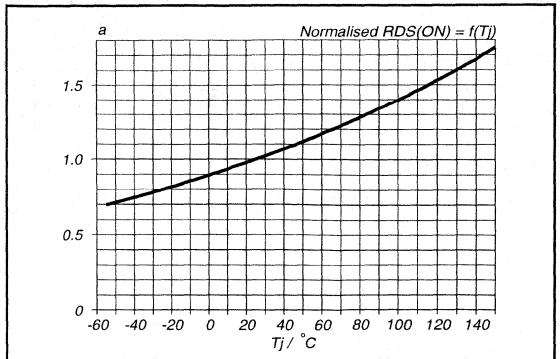


Fig.13. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25$ ˚C = $f(T_j)$; I_D = 7.5 A; $V_{IS} \geq$ 5 V

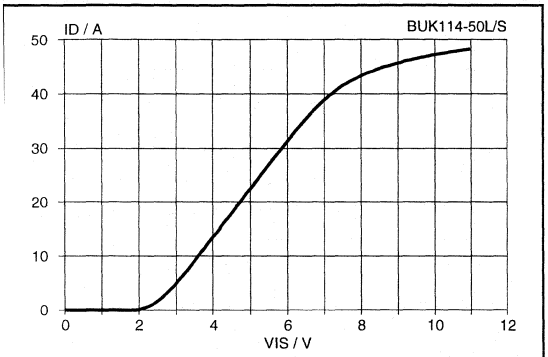


Fig.11. Typical transfer characteristics, T_j = 25 ˚C. $I_D = f(V_{IS})$; conditions: V_{DS} = 10 V; t_p = 250 µs

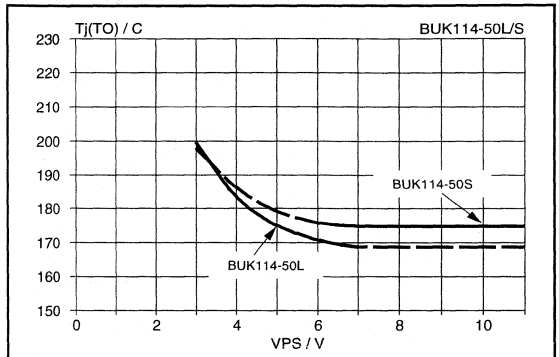


Fig.14. Typical over temperature protection threshold $T_{j(TO)} = f(V_{PS})$; conditions: V_{DS} > 0.1 V

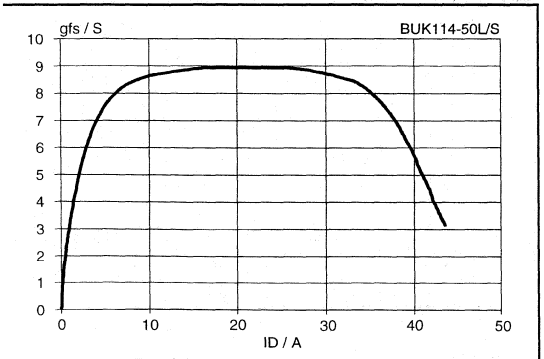


Fig.12. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V; t_p = 250 µs

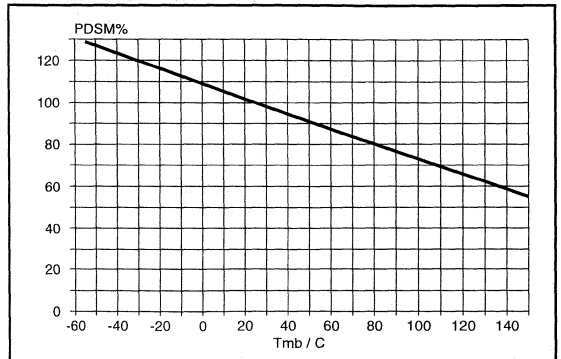


Fig.15. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ ^\circ C) = f(T_{mb})$

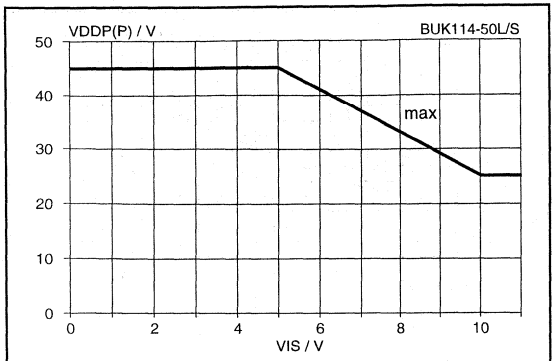


Fig.16. Maximum drain source supply voltage for SC load protection. $V_{DDP(P)} = f(V_{IS})$; $T_{mb} \leq 150$ °C

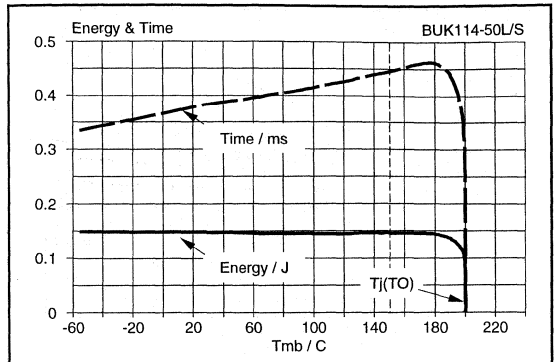


Fig.19. Typical overload protection characteristics. Conditions: $V_{DD} = 13$ V; $V_{PS} = V_{PSN}$, $V_{IS} = 7$ V; SC load

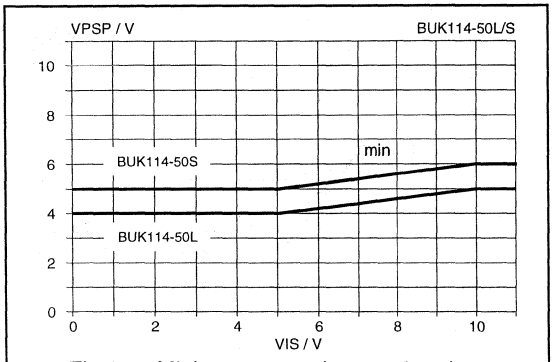


Fig.17. Minimum protection supply voltage for SC load protection. $V_{PSP} = f(V_{IS})$; $T_{mb} \geq 25$ °C

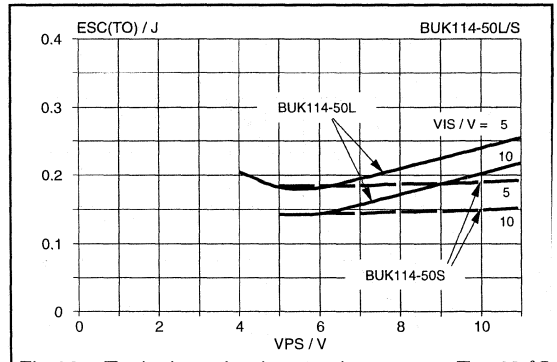


Fig.20. Typical overload protection energy, $T_j = 25$ °C $E_{SC(TO)} = f(V_{PS})$; conditions: $V_{DS} = 13$ V, parameter V_{IS}

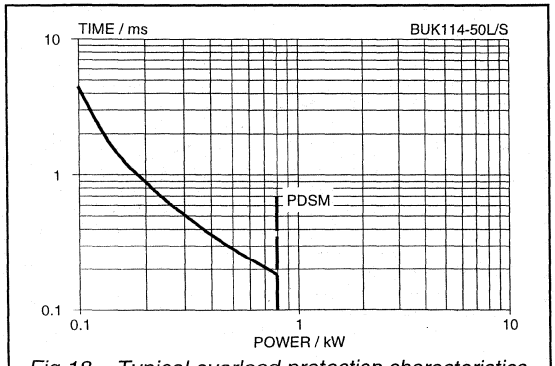


Fig.18. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{PS} \geq V_{PSP}$; $V_{IS} \geq 5$ V

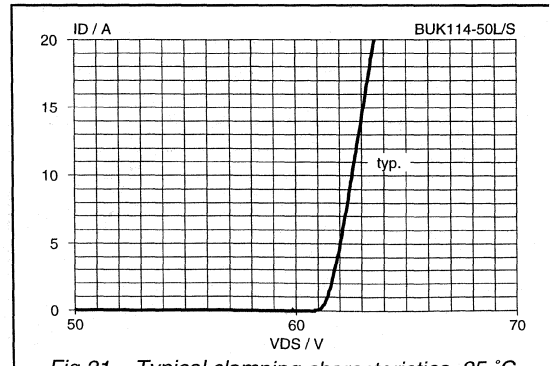


Fig.21. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: $R_{IS} = 100\ \Omega$; $t_p \leq 50\ \mu s$

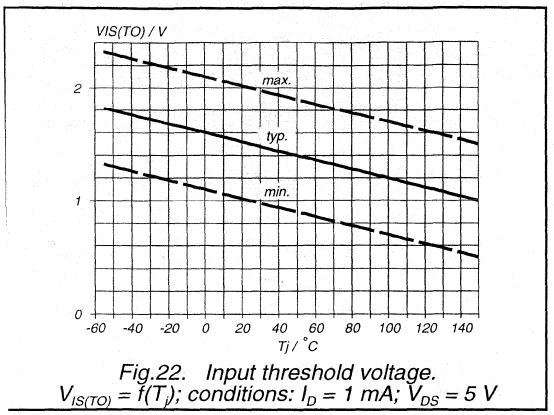


Fig.22. Input threshold voltage.
$V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

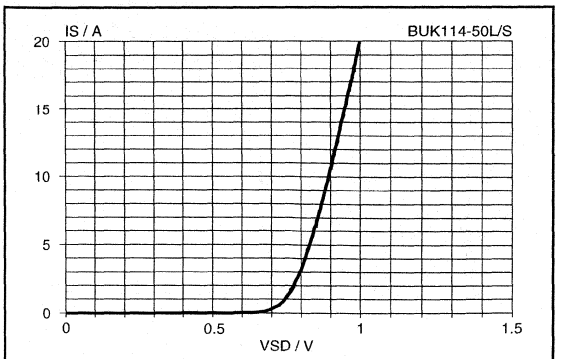


Fig.25. Typical reverse diode current, T_j = 25 °C.
$I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V; t_p = 250 µs

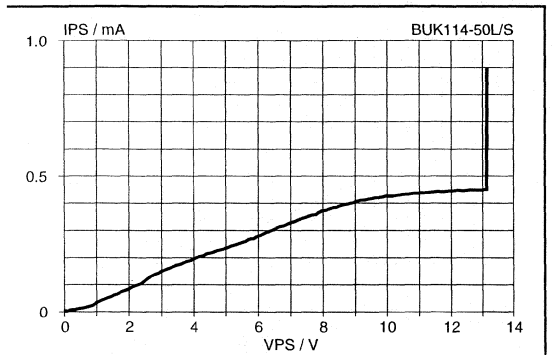


Fig.23. Typical DC protection supply characteristics.
$I_{PS} = f(V_{PS})$; normal or overload operation; T_j = 25 °C

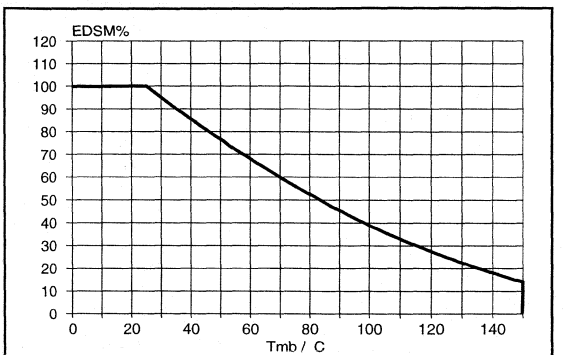


Fig.26. Normalised limiting clamping energy.
E_{DSM}% = $f(T_{mb})$; conditions: I_D = 15 A

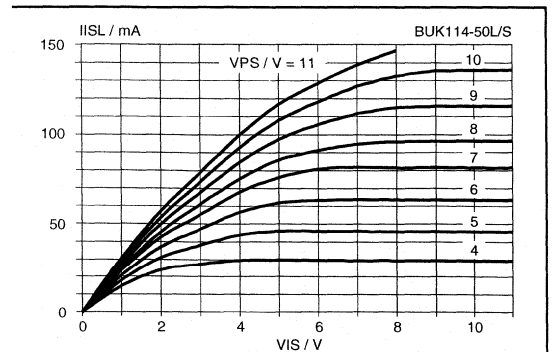


Fig.24. Typical latched input characteristics, 25 °C.
$I_{ISL} = f(V_{IS})$; after overload protection latched

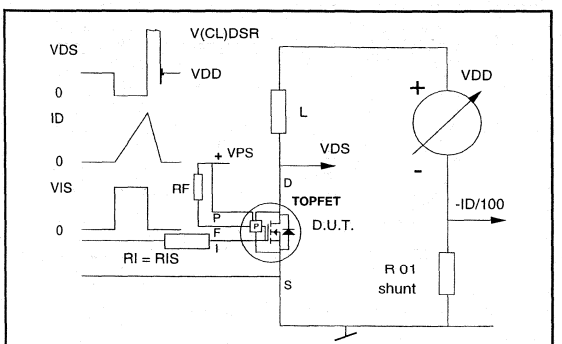


Fig.27. Clamping energy test circuit, R_{IS} = 100 Ω.
$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSR}/(V_{(CL)DSR} - V_{DD})$$

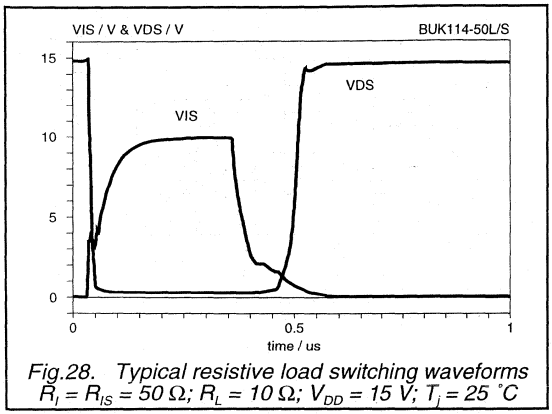


Fig.28. Typical resistive load switching waveforms $R_l = R_{IS} = 50\ \Omega$; $R_L = 10\ \Omega$; $V_{DD} = 15$ V; $T_j = 25$ ˚C

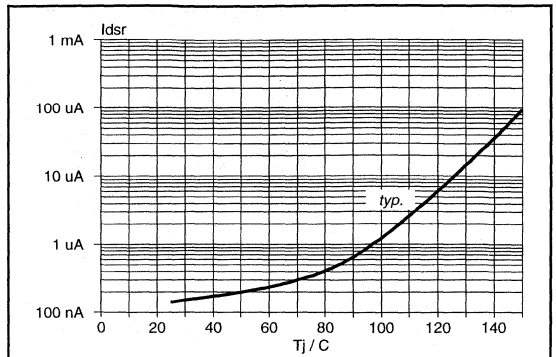


Fig.31. Typical off-state leakage current. $I_{DSR} = f(T_j)$; Conditions: $V_{DS} = 40$ V; $R_{IS} = 100\ \Omega$.

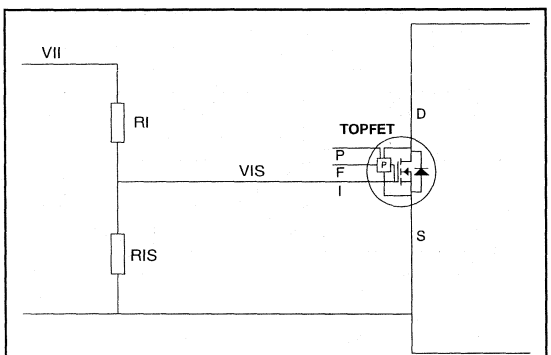


Fig.29. External input resistances R_I and R_{IS}, generator voltage V_{II} and input voltage V_{IS}.

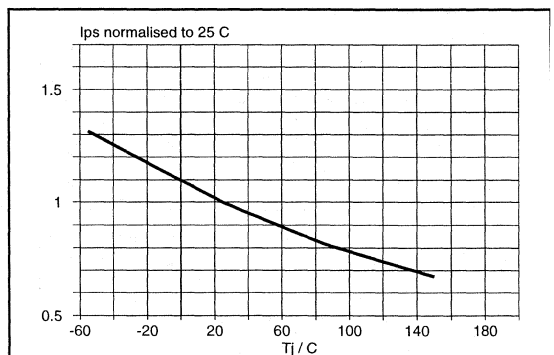


Fig.32. Normalised protection supply current. $I_{PS}/I_{PS}25$ ˚C $= f(T_j)$; $V_{PS} = V_{PSN}$

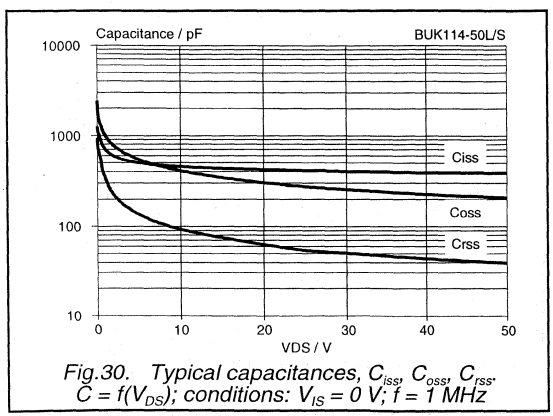


Fig.30. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: $V_{IS} = 0$ V; $f = 1$ MHz

Logic level TOPFET
SMD version of BUK106-50L/S

BUK116-50L/S

For maintenance only. Do not use for design-in.

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 5 pin surface mounting plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	50	A
P_{tot}	Total power dissipation	125	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance		
	V_{IS} = 5 V	35	mΩ
	V_{IS} = 8 V	28	mΩ
SYMBOL	**PARAMETER**	**NOM.**	**UNIT**
V_{PSN}	Protection supply voltage		
	BUK116-50L	5	V
	BUK116-50S	10	V

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Logic and protection supply from separate pin
- Low operating supply current
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by protection supply
- Protection circuit condition indicated by flag pin
- 5 V logic compatible input level
- Separate input pin for higher frequency drive
- ESD protection on input, flag and protection supply pins
- Over voltage clamping for turn off of inductive loads
- Both linear and switching operation are possible

FUNCTIONAL BLOCK DIAGRAM

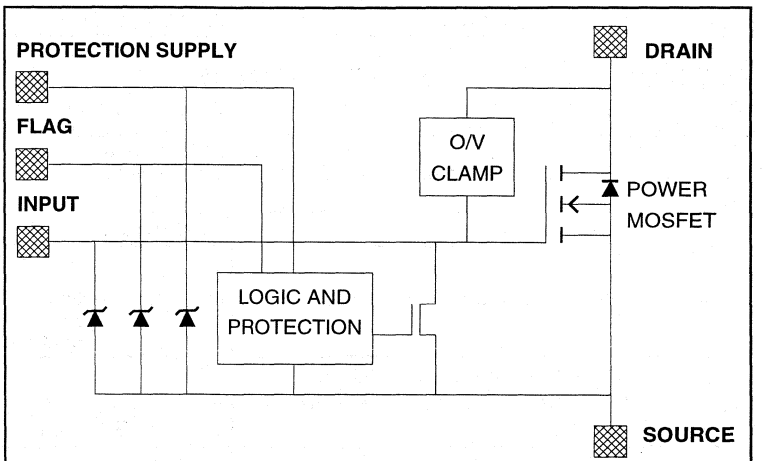


Fig.1. Elements of the TOPFET.

PINNING - SOT426

PIN	DESCRIPTION
1	input
2	flag
3	(connected to mb)
4	protection supply
5	source
mb	drain

PIN CONFIGURATION

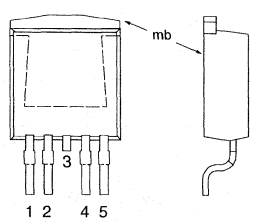


Fig. 2.

SYMBOL

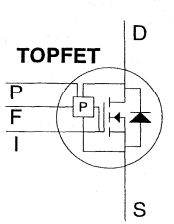


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
	Voltages					
V_{DSS}	Continuous off-state drain source voltage[1]	V_{IS} = 0 V	-	50		V
V_{IS}	Continuous input voltage	-	0	11		V
V_{FS}	Continuous flag voltage	-	0	11		V
V_{PS}	Continuous supply voltage	-	0	11		V
	Currents	V_{IS} =	-	8	5	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C	-	50	45	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C	-	31	28	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C	-	200	180	A
	Thermal					
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125		W
T_{stg}	Storage temperature	-	-55	150		°C
T_j	Junction temperature[2]	continuous	-	150		°C
T_{sold}	Lead temperature	during soldering	-	250		°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply connected, TOPFET can protect itself from two types of overload - over temperature and short circuit load.

An n-MOS transistor turns on between the input and source to quickly discharge the power MOSFET gate capacitance.

For internal overload protection to remain latched while the control circuit is high, external series input resistance must be provided. Refer to INPUT CHARACTERISTICS.

SYMBOL	PARAMETER	CONDITIONS	MIN.		MAX.	UNIT
		V_{IS} =	8	5	-	V
V_{PSP}	Protection supply voltage[3]	for valid protection				
		BUK116-50L	4.4	4	-	V
		BUK116-50S	5.4	5	-	V
	Over temperature protection	$V_{PS} = V_{PSN}$				
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 10 V; $R_l \geq 2$ kΩ	-		50	V
		V_{IS} = 5 V; $R_l \geq 1$ kΩ	-		50	V
	Short circuit load protection	$V_{PS} = V_{PSN}$; L ≤ 10 µH				
$V_{DDP(P)}$	Protected drain source supply voltage[4]	V_{IS} = 10 V; $R_l \geq 2$ kΩ	-		24	V
		V_{IS} = 5 V; $R_l \geq 1$ kΩ	-		45	V
P_{DSM}	Instantaneous overload dissipation		-		4	kW

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The minimum supply voltage required for correct operation of the overload protection circuits.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DRRM}	Repetitive peak clamping drain current	$R_{IS} \geq 100\ \Omega$[1]	-	50	A
E_{DSM}	Non-repetitive inductive turn-off energy[2]	$I_{DM} = 27$ A; $R_{IS} \geq 100\ \Omega$	-	1	J
E_{DRM}	Repetitive inductive turn-off energy	$R_{IS} \geq 100\ \Omega$; $T_{mb} \leq 85$ °C; $I_{DM} = 16$ A; $V_{DD} \leq 20$ V; f = 250 Hz	-	80	mJ
I_{DIRM}	Repetitive peak drain to input current[3]	$R_{IS} = 0\ \Omega$; $t_p \leq 1$ ms	-	50	mA

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} = 25$ °C; $V_{IS} = V_{PS} = V_{FS} = 0$ V	-	50	A

THERMAL CHARACTERISTIC

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	0.8	1.0	K/W

STATIC CHARACTERISTICS

$T_{mb} = 25$ °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSR}$	Drain-source clamping voltage	$R_{IS} = 100\ \Omega$; $I_D = 10$ mA		50	-	65	V
$V_{(CL)DSR}$	Drain-source clamping voltage	$R_{IS} = 100\ \Omega$; $I_{DM} = 1$ A; $t_p \leq 300$ µs; $\delta \leq 0.01$		50	-	70	V
I_{DSS}	Zero input voltage drain current	$V_{DS} = 12$ V; $V_{IS} = 0$ V		-	0.5	10	µA
I_{DSR}	Drain source leakage current	$V_{DS} = 50$ V; $R_{IS} = 100\ \Omega$;		-	1	20	µA
I_{DSR}	Drain source leakage current	$V_{DS} = 40$ V; $R_{IS} = 100\ \Omega$; $T_j = 125$ °C		-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	$I_{DM} = 25$ A; $t_p \leq 300$ µs; $\delta \leq 0.01$	$V_{IS} = 8$ V	-	22	28	mΩ
			$V_{IS} = 5$ V	-	28	35	mΩ

1 The input pin must be connected to the source pin by a specified external resistance to allow the power MOSFET gate source voltage to become sufficiently positive for active clamping. Refer to INPUT CHARACTERISTICS.

2 While the protection supply voltage is connected, during overvoltage clamping it is possible that the overload protection may operate at energies close to the limiting value. Refer to OVERLOAD PROTECTION CHARACTERISTICS.

3 Shorting the input to source with low resistance inhibits the internal overvoltage protection by preventing the power MOSFET gate source voltage becoming positive.

OVERLOAD PROTECTION CHARACTERISTICS

With adequate protection supply voltage TOPFET detects when one of the overload thresholds is exceeded.

Provided there is adequate input series resistance it switches off and remains latched off until reset by the protection supply pin.

Refer also to OVERLOAD PROTECTION LIMITING VALUES and INPUT CHARACTERISTICS.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	$V_{PS} = V_{PSN}$[2]; $T_{mb} = 25$ °C; $L \leq 10$ µH				
$E_{DS(TO)}$	Overload threshold energy	$V_{DD} = 13$ V; $V_{IS} = 10$ V	-	550	-	mJ
$t_{d\,sc}$	Response time	$V_{DD} = 13$ V; $V_{IS} = 10$ V	-	0.4	-	ms
	Over temperature protection	$V_{PS} = V_{PSN}$				
$T_{j(TO)}$	Threshold junction temperature	from $I_D \geq 2.5$ A[3]	150	-	-	°C

TRANSFER CHARACTERISTICS

$T_{mb} = 25$ °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 12$ V; $I_{DM} = 25$ A $t_p \leq 300$ µs; $\delta \leq 0.01$	17	28	-	S
I_D	Drain current[4]	$V_{DS} = 13$ V; $V_{IS} = 5$ V	-	80	-	A
		$V_{IS} = 10$ V		160	-	A

PROTECTION SUPPLY CHARACTERISTICS

$T_{mb} = 25$ °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Protection supply					
I_{PS}, I_{PSL}	Protection supply current	normal operation or protection latched				
		BUK116-50L $V_{PS} = 5$ V	-	0.2	0.35	mA
		BUK116-50S $V_{PS} = 10$ V	-	0.4	1.0	mA
V_{PSR}	Protection reset voltage[5]		1.5	2.5	3.5	V
		$T_j = 150$ °C	1.0	-	-	V
$V_{(CL)PS}$	Protection clamp voltage	$I_P = 1.35$ mA	11	13	-	V

REVERSE DIODE CHARACTERISTICS

$T_{mb} = 25$ °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	$I_S = 20$ A; $V_{IS} = V_{PS} = V_{FS} = 0$ V; $t_p = 300$ µs	-	0.9	1.2	V
t_{rr}	Reverse recovery time	not applicable[6]	-	-	-	-

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum.

2 At the appropriate nominal protection supply voltage for each type. Refer to QUICK REFERENCE DATA.

3 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

4 During overload condition. Refer also to OVERLOAD PROTECTION LIMITING VALUES and CHARACTERISTICS.

5 The supply voltage below which the overload protection circuits will be reset.

6 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Normal operation					
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA	1.0	1.5	2.0	V
		T_{mb} = 150 °C	0.5	-	-	V
I_{IS}	Input current	V_{IS} = 10 V	-	10	100	nA
$V_{(CL)IS}$	Input clamp voltage	I_I = 1 mA	11	13	-	V
	Overload protection latched					
R_{ISL}	Input resistance[1]	V_{PS} = 5 V; I_I = 5 mA	-	55	-	Ω
		T_{mb} = 150 °C	-	95	-	Ω
		V_{PS} = 10 V; I_I = 5 mA	-	35	-	Ω
		T_{mb} = 150 °C	-	60	-	Ω
	Application information					
	External input resistances for	(see figure 29)				
R_{IS}	internal overvoltage clamping[2]	R_I = ∞ Ω; V_{DS} > 30 V	100	-	-	Ω
R_I	internal overload protection[3]	R_{IS} = ∞ Ω; V_{II} = 5 V	1	-	-	kΩ
		V_{II} = 10 V	2	-	-	kΩ

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C; R_I = 50 Ω; R_{IS} = 50 Ω (see figure 29); resistive load R_L = 10 Ω. For waveforms see figure 28.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 15 V; V_{IS}: 0 V ⇒ 10 V	-	10	-	ns
t_r	Rise time		-	35	-	ns
$t_{d\,off}$	Turn-off delay time	V_{DD} = 15 V; V_{IS}: 10 V ⇒ 0 V	-	280	-	ns
t_f	Fall time		-	120	-	ns

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{iss}	Input capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	1250	1800	pF
C_{oss}	Output capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	650	1000	pF
C_{rss}	Reverse transfer capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	150	250	pF
C_{pso}	Protection supply pin capacitance	V_{PS} = 10 V	-	30	-	pF
C_{fso}	Flag pin capacitance	V_{FS} = 10 V; V_{PS} = 0 V	-	20	-	pF

1 The resistance of the internal transistor which discharges the power MOSFET gate capacitance when overload protection operates.
The external drive circuit should be such that the input voltage does not exceed $V_{IS(TO)}$ minimum when the overload protection has operated. Refer also to figure for latched input characteristics.

2 Applications using a lower value for R_{IS} would require external overvoltage protection.

3 For applications requiring a lower value for R_I, an external overload protection strategy is possible using the flag pin to 'tell' the control circuit to switch off the input.

FLAG DESCRIPTION

The flag pin provides a means to detect the presence of the protection supply and indicate the state of the overload detectors. The flag is the open drain of an n-MOS transistor and requires an external pull-up resistor[1]. It is suitable for both 5 V and 10 V logic. Flag may be used to implement an external protection strategy[2] for applications which require low input drive impedance.

TRUTH TABLE

CONDITION	DESCRIPTION	FLAG
NORMAL	Normal operation and adequate protection supply voltage	LOGIC LOW
OVER TEMP.	Over temperature detected	LOGIC HIGH
SHORT CIRCUIT	Overload condition detected	LOGIC HIGH
SUPPLY FAULT	Inadequate protection supply voltage	LOGIC HIGH

FLAG CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Flag 'low'	normal operation				
V_{FS}	Flag voltage	I_F = 1.6 mA	-	0.15	0.4	V
I_{FSS}	Flag saturation current	V_{FS} = 10 V	-	15	-	mA
	Flag 'high'	overload or fault				
I_{FS}	Flag leakage current	V_{FS} = 10 V	-	-	10	µA
V_{PSF}	Protection supply threshold voltage	V_{FF} = 5 V; R_F = 3 kΩ;				
		BUK116-50L	2.5	3.3	4	V
		BUK116-50S	3.3	4.2	5	V
$V_{(CL)FS}$	Flag clamping voltage	I_F = 1 mA; V_{PS} = 0 V	11	13	-	V
	Application information					
R_F	Suitable external pull-up resistance	V_{FF} =5 V	1	10	50	kΩ
		V_{FF} =10 V	2	20	100	kΩ

1 Even if the flag pin is not used, it is recommended that it is connected to the protection supply via a pull-up resistor. It should not be left floating.

2 Low pass filtering of the flag signal may be advisable to prevent false tripping.

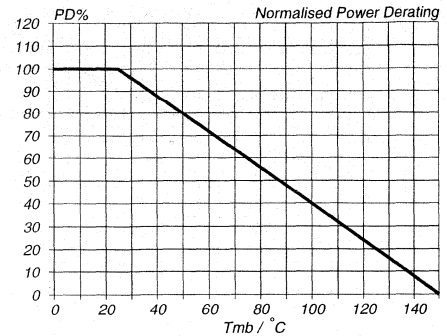


Fig.4. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

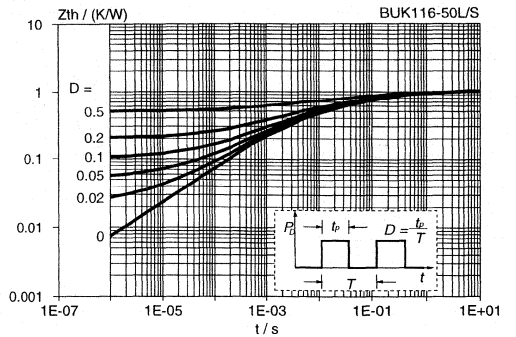


Fig.7. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

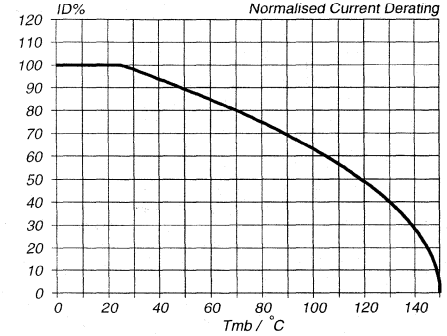


Fig.5. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

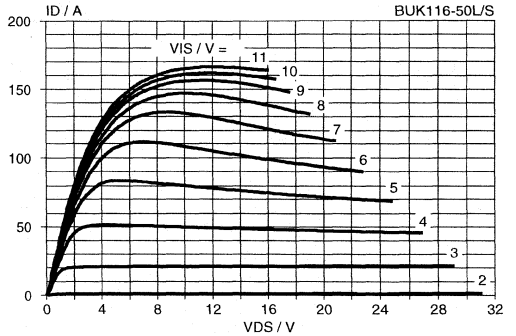


Fig.8. Typical output characteristics, $T_j = 25\ ^\circ C$.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$ & $t_p < t_{d\,sc}$

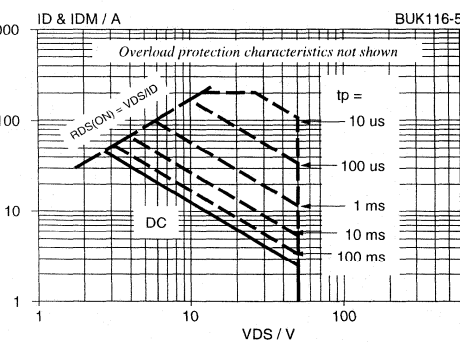


Fig.6. Safe operating area. $T_{mb} = 25\ ^\circ C$
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

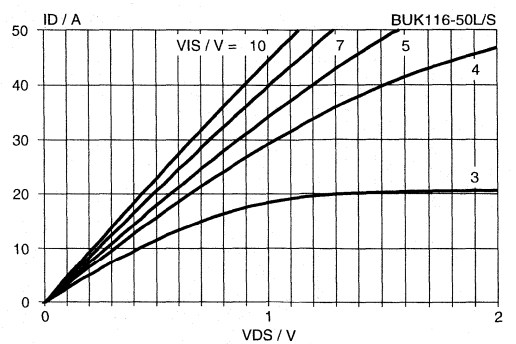


Fig.9. Typical on-state characteristics, $T_j = 25\ ^\circ C$.
$I_D = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$

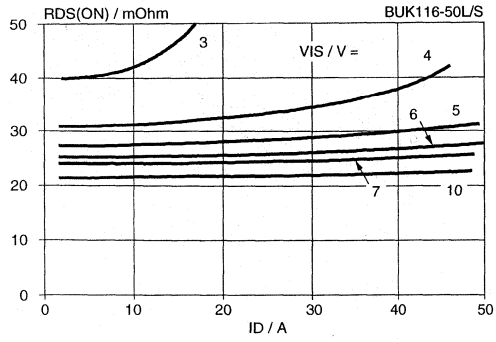


Fig.10. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

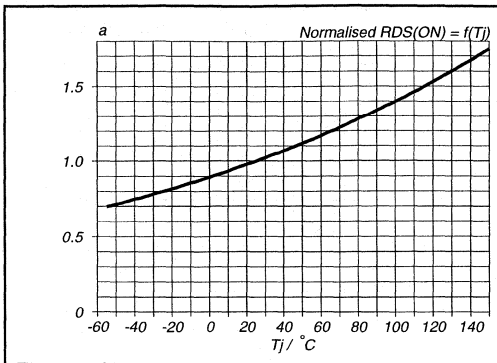


Fig.13. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25$ ˚C $= f(T_j)$; I_D = 25 A; $V_{IS} \geq$ 5 V

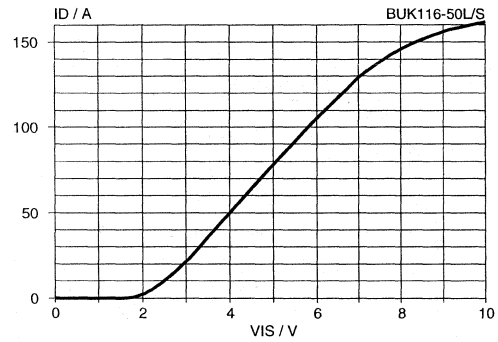


Fig.11. Typical transfer characteristics, T_j = 25 ˚C. $I_D = f(V_{IS})$; conditions: V_{DS} = 12 V; t_p = 250 µs

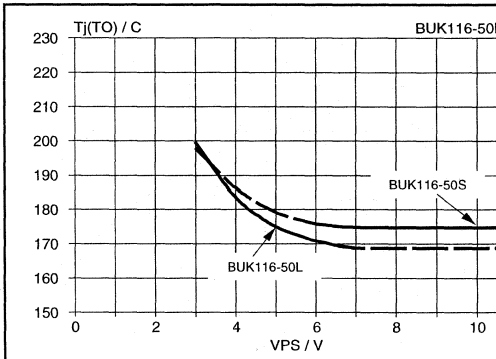


Fig.14. Typical over temperature protection threshold $T_{j(TO)} = f(V_{PS})$; conditions: V_{DS} > 0.1 V

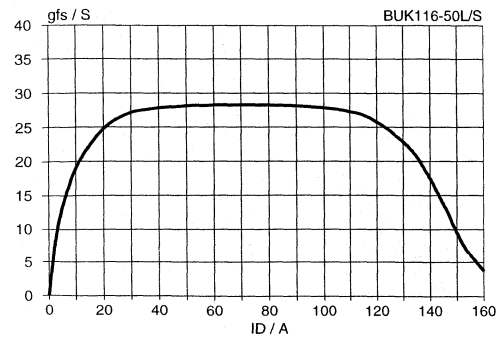


Fig.12. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 12 V; t_p = 250 µs

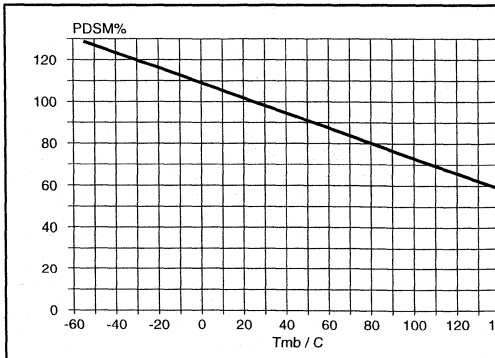


Fig.15. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ ^\circ C) = f(T_{mb})$

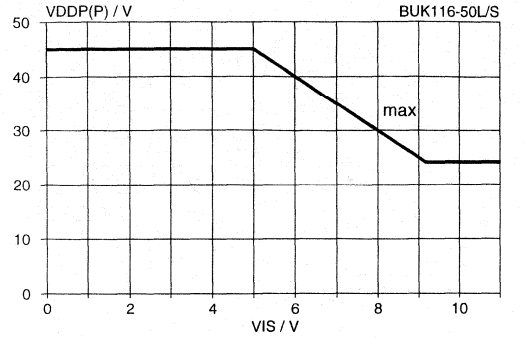


Fig.16. Maximum drain source supply voltage for SC load protection. $V_{DDP(P)} = f(V_{IS})$; $T_{mb} \leq 150$ °C

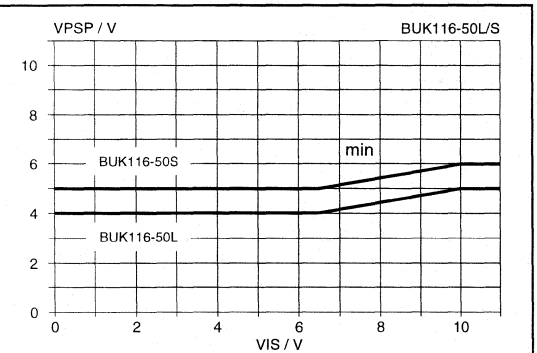


Fig.17. Minimum protection supply voltage for SC load protection. $V_{PSP} = f(V_{IS})$; $T_{mb} \geq 25$ °C

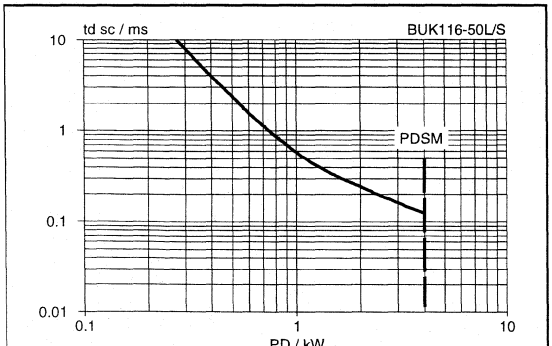


Fig.18. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{PS} \geq V_{PSP}$; $V_{IS} \geq 5$ V

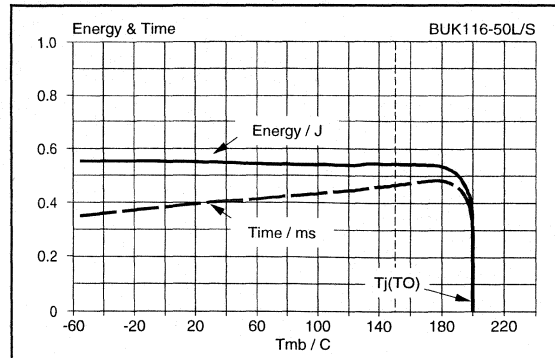


Fig.19. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; $V_{PS} = V_{PSN}$, V_{IS} = 8 V; SC load

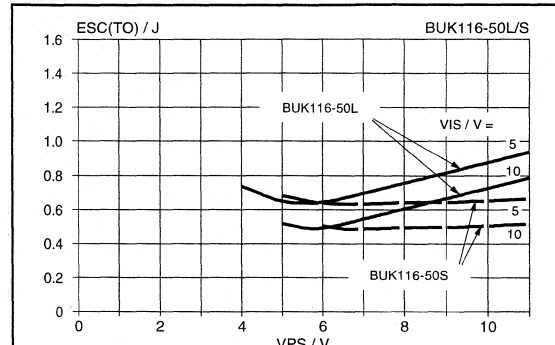


Fig.20. Typical overload protection energy, T_j = 25 °C $E_{SC(TO)} = f(V_{PS})$; conditions: V_{DS} = 13 V, parameter V_{IS}

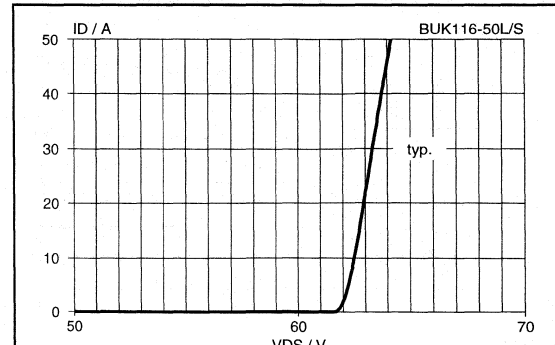


Fig.21. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: R_{IS} = 100 Ω; $t_p \leq 50$ µs

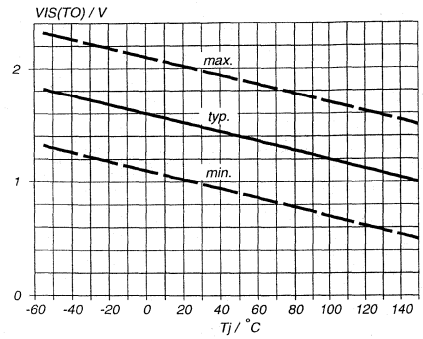


Fig.22. Input threshold voltage.
$V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

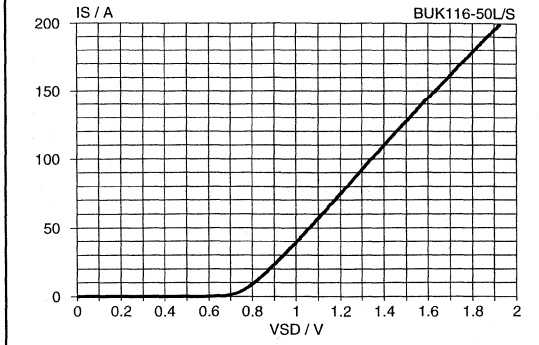


Fig.25. Typical reverse diode current, T_j = 25 °C.
$I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V; t_p = 250 µs

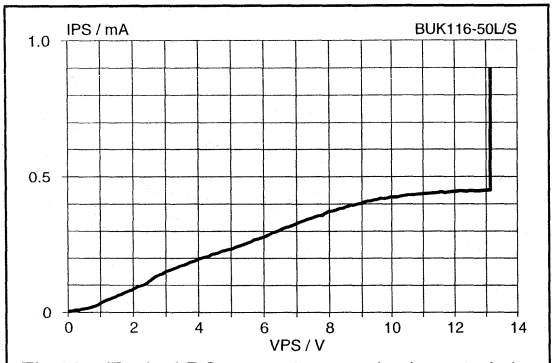


Fig.23. Typical DC protection supply characteristics.
$I_{PS} = f(V_{PS})$; normal or overload operation; T_j = 25 °C

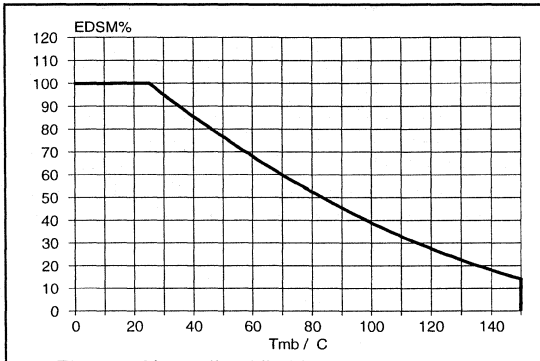


Fig.26. Normalised limiting clamping energy.
$E_{DSM}\% = f(T_{mb})$; conditions: I_D = 27 A

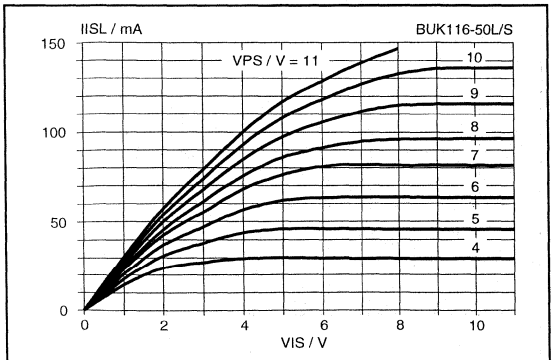


Fig.24. Typical latched input characteristics, 25 °C.
$I_{ISL} = f(V_{IS})$; after overload protection latched

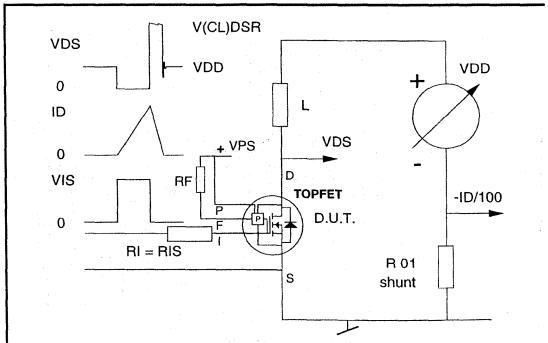


Fig.27. Clamping energy test circuit, R_{IS} = 100 Ω.
$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSR}/(V_{(CL)DSR} - V_{DD})$

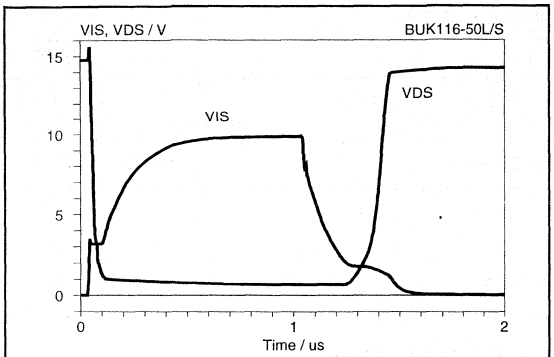


Fig.28. Typical resistive load switching waveforms $R_I = R_{IS} = 50\ \Omega$; $R_L = 10\ \Omega$; $V_{DD} = 15$ V; $T_j = 25$ °C

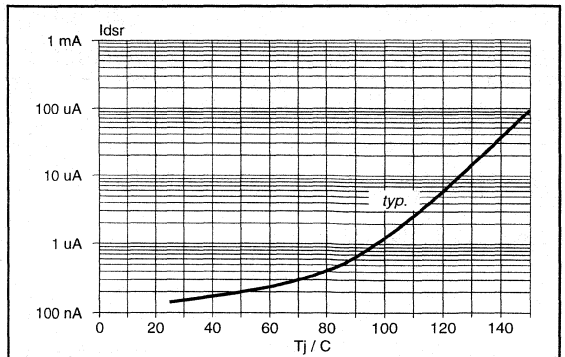


Fig.31. Typical off-state leakage current. $I_{DSR} = f(T_j)$; Conditions: $V_{DS} = 40$ V; $R_{IS} = 100\ \Omega$.

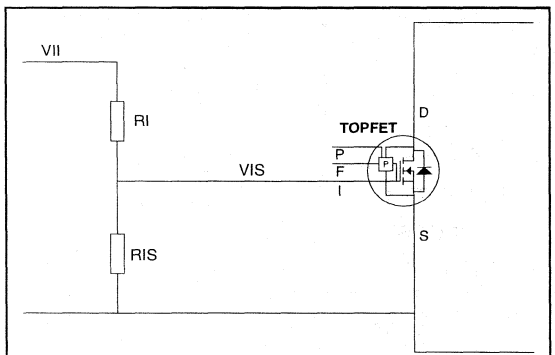


Fig.29. External input resistances R_I and R_{IS}, generator voltage V_{II} and input voltage V_{IS}.

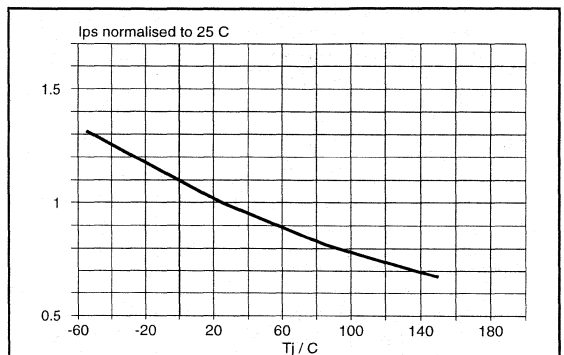


Fig.32. Normalised protection supply current. $I_{PS}/I_{PS}25\ ^\circ C = f(T_j)$; $V_{PS} = V_{PSN}$

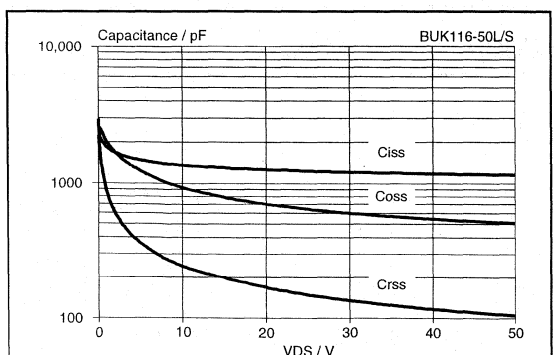


Fig.30. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: $V_{IS} = 0$ V; $f = 1$ MHz

PowerMOS transistor TOPFET high side switch

BUK200-50Y

For maintenance only. Do not use for design-in.

DESCRIPTION

Monolithic temperature and overload protected power switch based on MOSFET technology in a 5 pin plastic envelope, configured as a single high side switch.

APPLICATIONS

General controller for driving lamps, motors, solenoids, heaters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	UNIT
I_L	Nominal load current (ISO)	3.5	A
SYMBOL	**PARAMETER**	**MAX.**	**UNIT**
V_{BG}	Continuous off-state supply voltage	50	V
I_L	Continuous load current	10	A
T_j	Continuous junction temperature	150	°C
R_{ON}	On-state resistance	100	mΩ

FEATURES

- Vertical power DMOS switch
- Low on-state resistance
- 5 V logic compatible input
- Overtemperature protection - self resets with hysteresis
- Overload protection against short circuit load with output current limiting; latched - reset by input
- High supply voltage load protection
- Supply undervoltage lock out
- Status indication for overload protection activated
- Diagnostic status indication of open circuit load
- Very low quiescent current
- Voltage clamping for turn off of inductive loads
- ESD protection on all pins
- Reverse battery and overvoltage protection

FUNCTIONAL BLOCK DIAGRAM

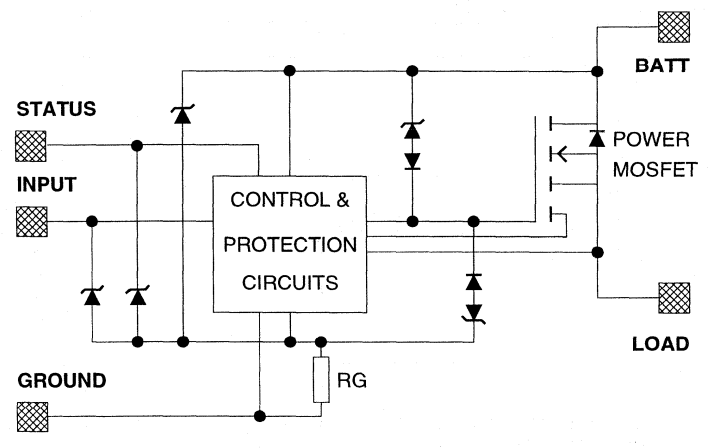


Fig.1. Elements of the TOPFET HSS with internal ground resistor.

PINNING - SOT263

PIN	DESCRIPTION
1	Ground
2	Input
3	Battery (+ve supply)
4	Status
5	Load
tab	connected to pin 3

PIN CONFIGURATION

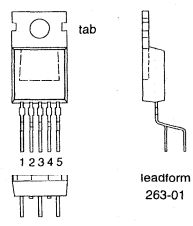


Fig. 2.

SYMBOL

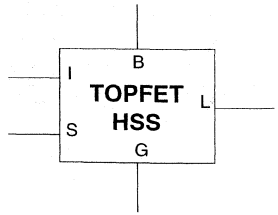


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Battery voltages				
V_{BG}	Continuous off-state supply voltage	-	0	50	V
	Reverse battery voltages[1]	External resistors:			
$-V_{BG}$	Repetitive peak supply voltage	$R_I = R_S \geq 4.7\ k\Omega$, $\delta \leq 0.1$	-	32	V
$-V_{BG}$	Continuous reverse supply voltage	$R_I = R_S \geq 4.7\ k\Omega$	-	16	V
I_L	Continuous load current	$T_{mb} \leq 115\ ^\circ C$	-	10	A
P_D	Total power dissipation	$T_{mb} \leq 25\ ^\circ C$	-	62.5	W
T_{stg}	Storage temperature	-	-55	175	°C
T_j	Continuous junction temperature[2]	-	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C
	Input and status				
I_I	Continuous input current	-	-5	5	mA
I_S	Continuous status current	-	-5	5	mA
I_I	Repetitive peak input current	$\delta \leq 0.1$	-20	20	mA
I_S	Repetitive peak status current	$\delta \leq 0.1$	-20	20	mA
	Inductive load clamping				
E_{BL}	Non-repetitive clamping energy	$T_{mb} = 150\ ^\circ C$ prior to turn-off	-	1.2	J

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance[3]					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	1.5	2	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	75	K/W

1 Reverse battery voltage is allowed only with external input and status resistors to limit the currents to a safe value.

2 For normal continuous operation. A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 Of the output Power MOS transistor.

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Clamping voltages					
V_{BG}	Battery to ground	I_G = 1 mA	50	55	65	V
V_{BL}	Battery to load	$I_L = I_G$ = 1 mA	50	55	65	V
$-V_{LG}$	Negative load to ground	I_L = 1 mA	12	17	21	V
	Supply voltage	battery to ground				
V_{BG}	Operating range[1]	-	5	-	40	V
	Currents	V_{BG} = 13 V				
I_L	Nominal load current[2]	V_{BL} = 0.5 V; T_{mb} = 85 °C	3.5	-	-	A
I_B	Quiescent current[3]	V_{IG} = 0 V; V_{LG} = 0 V	-	0.1	2	µA
I_G	Operating current[4]	V_{IG} = 5 V; I_L = 0 A	1.5	2.2	4	mA
I_L	Off-state load current[5]	V_{BL} = 13 V; V_{IG} = 0 V	-	0.1	1	µA
	Resistances					
R_{ON}	On-state resistance[6]	V_{BG} = 13 V; I_L = 5 A; t_p = 300 µs	-	77	100	mΩ
R_{ON}	On-state resistance	V_{BG} = 5 V; I_L = 1 A; t_p = 300 µs	-	116	150	mΩ
R_G	Internal ground resistance	I_G = 10 mA	-	150	-	Ω

INPUT CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_I	Input current	V_{IG} = 5 V	35	60	100	µA
V_{IG}	Input clamping voltage	I_I = 200 µA	6	7.5	8.5	V
$V_{IG(ON)}$	Input turn-on threshold voltage		-	2.1	2.7	V
$V_{IG(OFF)}$	Input turn-off threshold voltage		1.5	2	-	V

1 On-state resistance is increased if the supply voltage is less than 9 V. Refer to figure 8.

2 Defined as in ISO 10483-1.

3 This is the continuous current drawn from the battery when the input is low and includes leakage current to the load.

4 This is the continuous current drawn from the battery with no load connected, but with the input high.

5 The measured current is in the load pin only.

6 The supply and input voltage for the R_{ON} tests are continuous. The specified pulse duration t_p refers only to the applied load current.

PROTECTION FUNCTIONS AND STATUS INDICATIONS

Truth table for normal, open-circuit load and overload conditions and abnormal supply voltages.

FUNCTIONS		TRUTH TABLE			THRESHOLD			
SYMBOL	CONDITION	INPUT	STATUS	OUTPUT	MIN.	TYP.	MAX.	UNIT
	Normal on-state	1	1	1				
	Normal off-state	0	1	0				
$I_{L(OC)}$	Open circuit load[1]	1	0	1	50	200	350	mA
	Open circuit load	0	1	0				
$T_{j(TO)}$	Over temperature[2]	1	0	0	150	175	-	°C
	Over temperature[3]	0	0	0				
$V_{BL(TO)}$	Short circuit load[4]	1	0	0	8.5	10.3	12	V
	Short circuit load	0	1	0				
$V_{BG(TO)}$	Low supply voltage[5]	X	1	0	3	4	5	V
$V_{BG(LP)}$	High supply voltage[6]	X	1	0	40	45	50	V

For input '0' equals low, '1' equals high, 'X' equals don't care.
For status '0' equals low, '1' equals open or high.
For output switch '0' equals off, '1' equals on.

STATUS CHARACTERISTICS

T_{mb} = 25 °C.
The status output is an open drain transistor, and requires an external pull-up circuit to indicate a logic high.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SG}	Status clamping voltage	I_S = 100 µA; V_{IG} = 0 V	6	7	8	V
V_{SG}	Status low voltage	I_S = 50 µA; V_{BG} = 13 V; V_{IG} = 5 V	-	0.7	0.8	V
I_S	Status leakage current	V_{SG} = 5 V	-	0.1	1	µA
I_S	Status saturation current[7]	V_{SS} = 5 V; R_S = 0 Ω; V_{BG} = 13 V	-	5	-	mA
	Application information					
R_S	External pull-up resistor[8]	V_{SS} = 5 V	-	100	-	kΩ

1 In the on-state, the switch detects whether the load current is less than the quoted open load threshold current. This is for status indication only. Typical hysteresis equals 80 mA. The thresholds are specified for supply voltage within the normal working range.

2 After cooling below the reset temperature the switch will resume normal operation. The reset temperature is lower than the trip temperature by typically 10 °C.

3 If the overtemperature protection has operated, status remains low to indicate the overtemperature condition even if the input is taken low, providing the device has not cooled below the reset temperature.

4 After short circuit protection has operated, the input voltage must be toggled low for the switch to resume normal operation.

5 Undervoltage sensor causes the device to switch off. Typical hysteresis equals 0.7 V.

6 Overvoltage sensor causes the device to switch off to protect the load. Typical hysteresis equals 1.3 V.

7 In a fault condition with the pull-up resistor short circuited while the status transistor is conducting.

8 The pull-up resistor also protects the status pin during reverse battery conditions.

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Inductive load turn-off					
$-V_{LG}$	Negative load voltage[1]	V_{IG} = 0 V; I_L = 5 A; t_p = 300 µs	15	20	25	V
	Short circuit load protection[2]	V_{IG} = 5 V; $R_L \leq 10$ mΩ				
$t_{d\,sc}$	Response time		-	90	-	µs
I_L	Load current prior to turn-off	$t < t_{d\,sc}$	-	35	-	A
	Overload protection[3]					
$I_{L(lim)}$	Load current limiting	V_{BL} = 8.5 V; t_p = 300 µs	23	33	43	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C, V_{BG} = 13 V, for resistive load R_L = 13 Ω.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	During turn-on	to V_{IG} = 5 V				
$t_{d\,on}$	Delay time	to 10% V_L	-	16	-	µs
dV/dt_{on}	Rate of rise of load voltage		-	1	2.5	V/µs
t_{on}	Total switching time	to 90% V_L	-	40	-	µs
	During turn-off	to V_{IG} = 0 V				
$t_{d\,off}$	Delay time	to 90% V_L	-	30	-	µs
dV/dt_{off}	Rate of fall of load voltage		-	1.2	2.5	V/µs
t_{off}	Total switching time	to 10% V_L	-	50	-	µs

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz; V_{IG} = 0 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{ig}	Input capacitance	V_{BG} = 13 V	-	15	20	pF
C_{bl}	Output capacitance	$V_{BL} = V_{BG}$ = 13 V	-	330	460	pF
C_{sg}	Status capacitance	V_{SG} = 5 V	-	11	15	pF

1 For a high side switch, the load pin voltage goes negative with respect to ground during the turn-off of an inductive load. This negative voltage is clamped by the device.

2 The load current is self-limited during the response time for short circuit load protection. Response time is measured from when input goes high.

3 If the load resistance is low, but not a complete short circuit, such that the on-state voltage remains less than $V_{BL(TO)}$, the device remains in current limiting until the overtemperature protection operates.

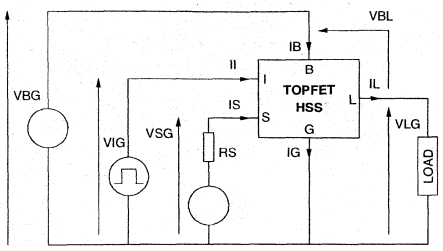


Fig.4. High side switch measurements schematic. (current and voltage conventions)

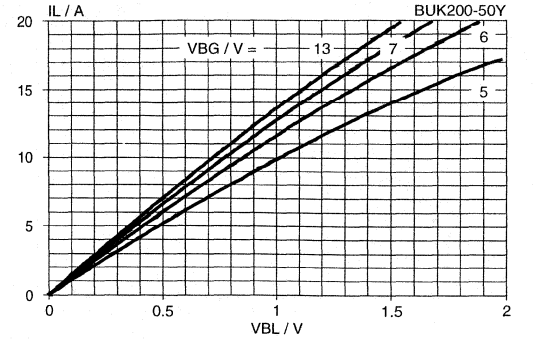


Fig.7. Typical on-state characteristics, T_j = 25 ˚C. $I_L = f(V_{BL})$; parameter V_{BG}; t_p = 250 µs

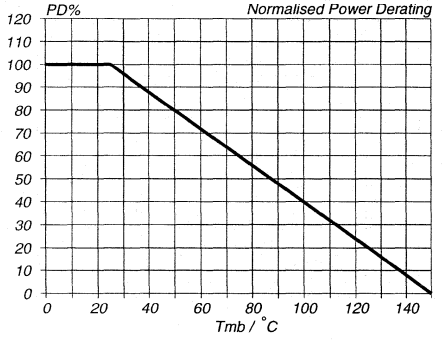


Fig.5. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

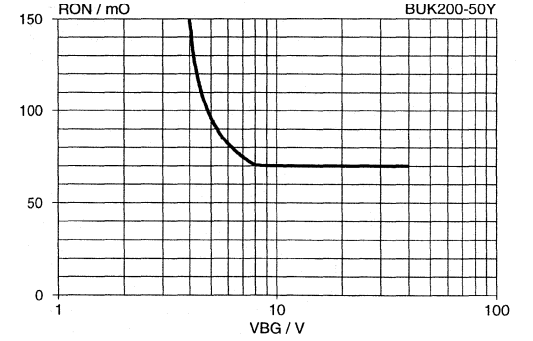


Fig.8. Typical on-state resistance, T_j = 25 ˚C. $R_{ON} = f(V_{BG})$; conditions: I_L = 5 A; t_p = 300 µs

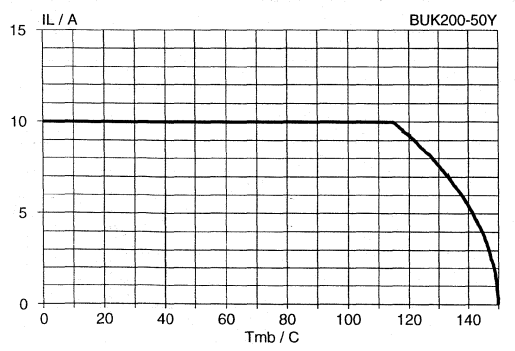


Fig.6. Limiting continuous on-state load current. $I_L = f(T_{mb})$; conditions: V_{IG} = 5 V, V_{BG} = 13 V

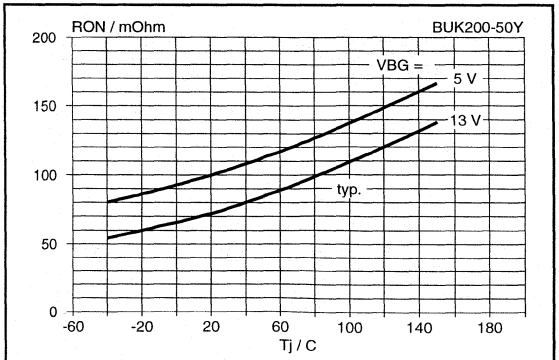


Fig.9. Typical on-state resistance, t_p = 300 µs. $R_{ON} = f(T_j)$; parameter V_{BG}; condition I_L = 1 A

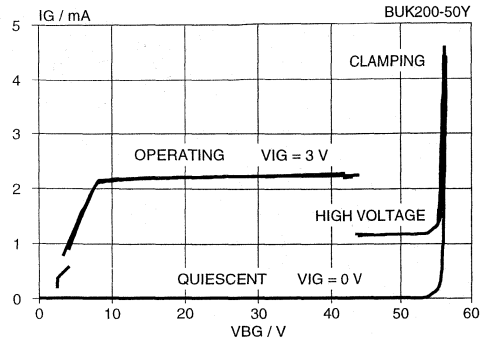


Fig.10. Typical supply characteristics, 25 ˚C. $I_G = f(V_{BG})$; parameter V_{IG}

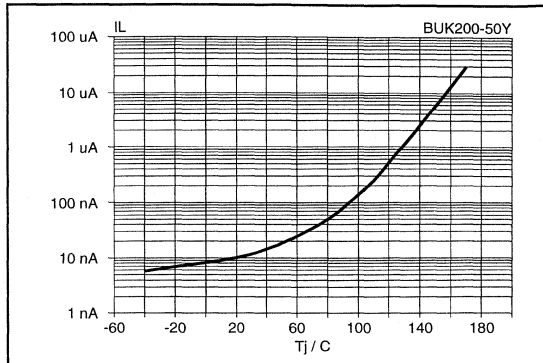


Fig.13. Typical off-state leakage current. $I_L = f(T_j)$; conditions: V_{BL} = 13 V = V_{BG}; V_{IG} = 0 V.

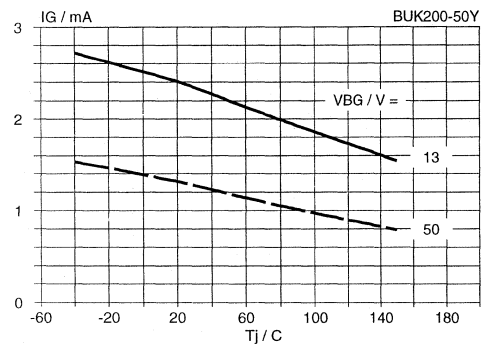


Fig.11. Typical operating supply current. $I_G = f(T_j)$; parameter V_{BG}; condition V_{IG} = 5 V

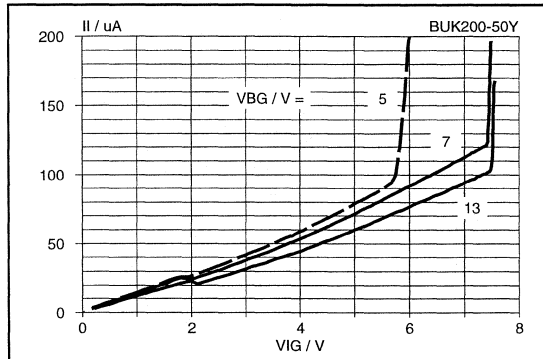


Fig.14. Typical input characteristics, T_j = 25 ˚C. $I_I = f(V_{IG})$; parameter V_{BG}

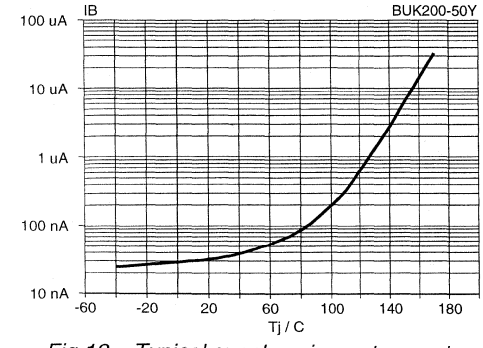


Fig.12. Typical supply quiescent current. $I_B = f(T_j)$; condition V_{BG} = 13 V, V_{IG} = 0 V, V_{LG} = 0 V

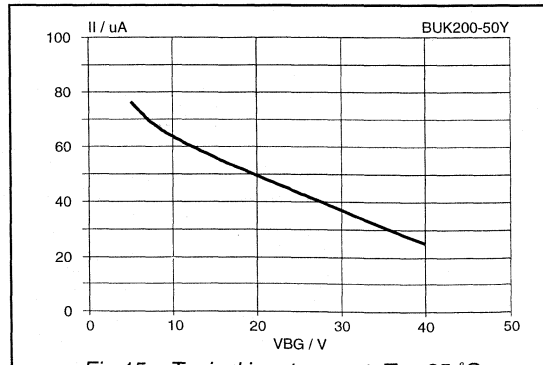


Fig.15. Typical input current, T_j = 25 ˚C. $I_I = f(V_{BG})$; condition V_{IG} = 5 V

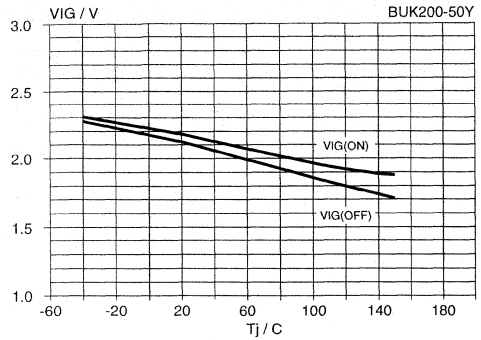


Fig.16. Typical input threshold voltages.
$V_{IG} = f(T_j)$; conditions V_{BG} = 13 V, I_L = 50 mA

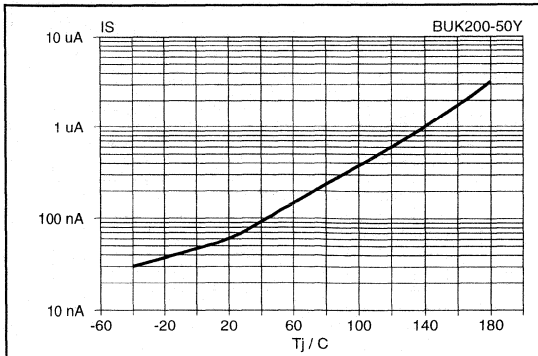


Fig.19. Typical status leakage current.
$I_S = f(T_j)$; conditions V_{SG} = 5 V, $V_{IG} = V_{BG}$ = 0 V

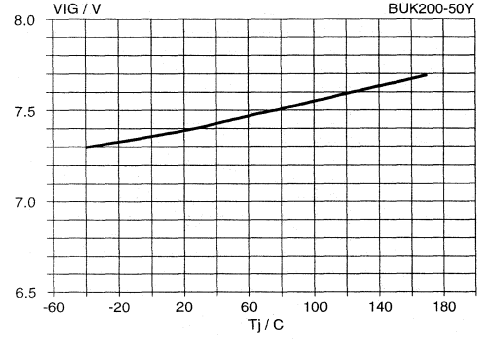


Fig.17. Typical input clamping voltage.
$V_{IG} = f(T_j)$; conditions I_I = 200 µA, V_{BG} = 13 V

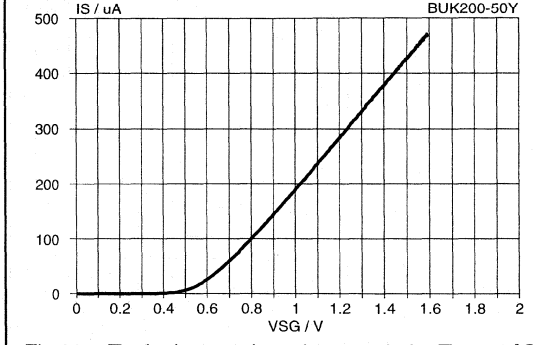


Fig.20. Typical status low characteristic, T_j = 25 °C.
$I_S = f(V_{SG})$; conditions V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

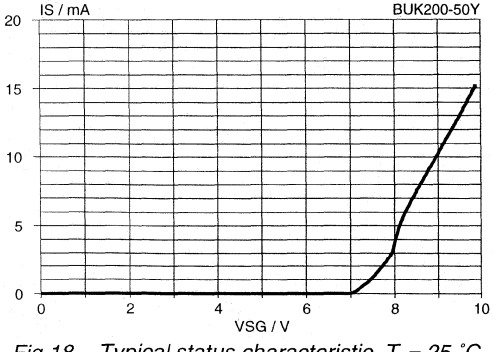


Fig.18. Typical status characteristic, T_j = 25 °C.
$I_S = f(V_{SG})$; conditions $V_{IG} = V_{BG}$ = 0 V

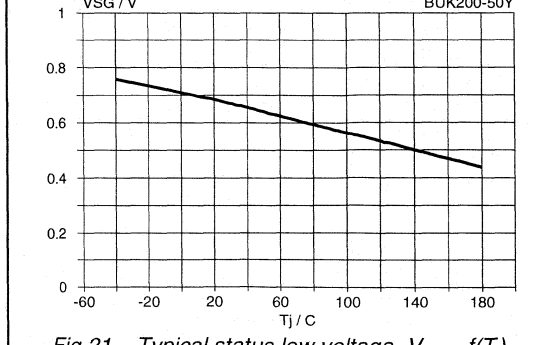


Fig.21. Typical status low voltage, $V_{SG} = f(T_j)$.
conditions I_S = 50 µA, V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

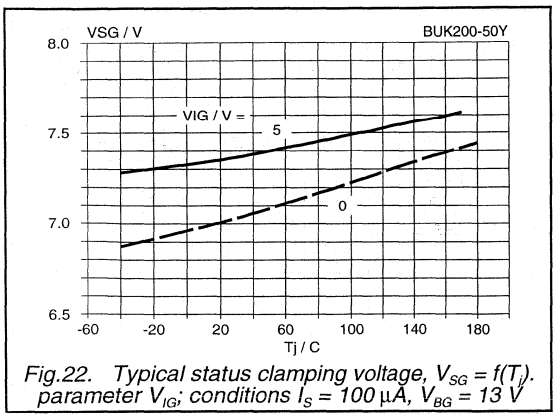


Fig.22. Typical status clamping voltage, $V_{SG} = f(T_j)$. parameter V_{IG}; conditions $I_S = 100\ \mu A$, $V_{BG} = 13\ V$

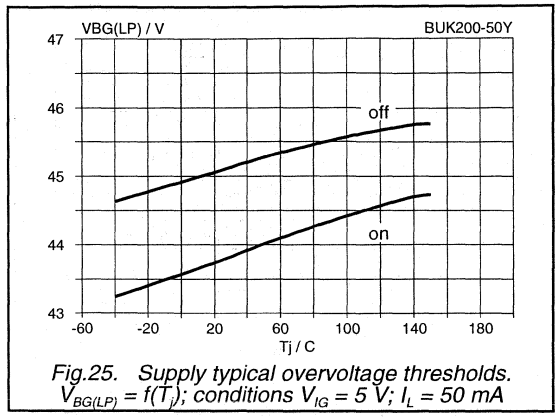


Fig.25. Supply typical overvoltage thresholds. $V_{BG(LP)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $I_L = 50\ mA$

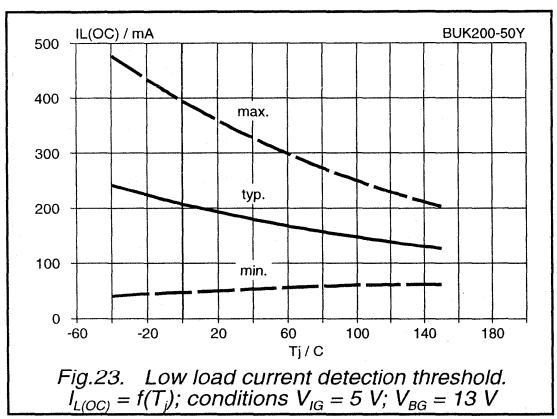


Fig.23. Low load current detection threshold. $I_{L(OC)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $V_{BG} = 13\ V$

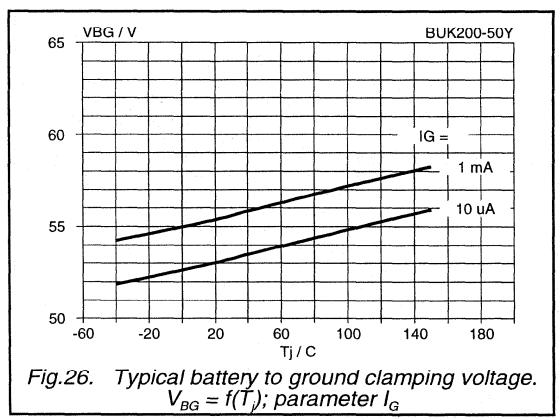


Fig.26. Typical battery to ground clamping voltage. $V_{BG} = f(T_j)$; parameter I_G

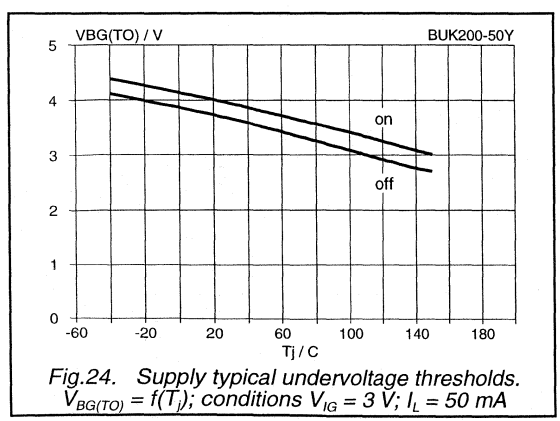


Fig.24. Supply typical undervoltage thresholds. $V_{BG(TO)} = f(T_j)$; conditions $V_{IG} = 3\ V$; $I_L = 50\ mA$

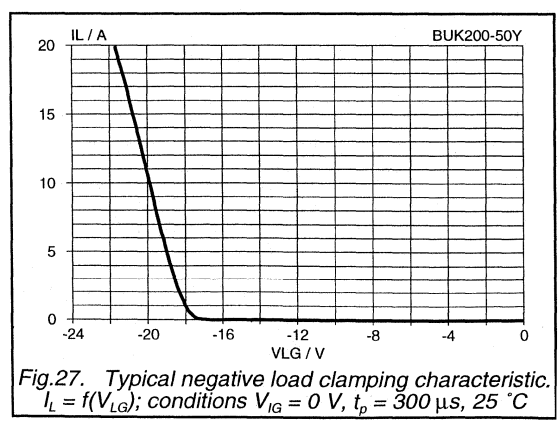


Fig.27. Typical negative load clamping characteristic. $I_L = f(V_{LG})$; conditions $V_{IG} = 0\ V$, $t_p = 300\ \mu s$, 25 °C

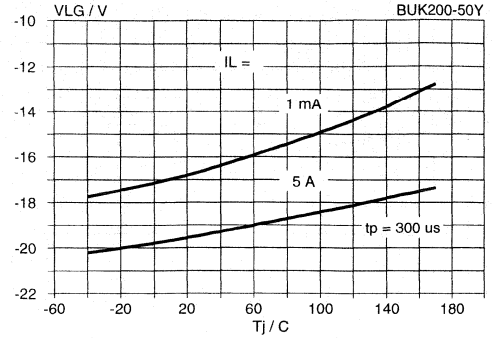


Fig.28. Typical negative load clamping voltage. $V_{LG} = f(T_j)$; parameter I_L; condition $V_{IG} = 0$ V.

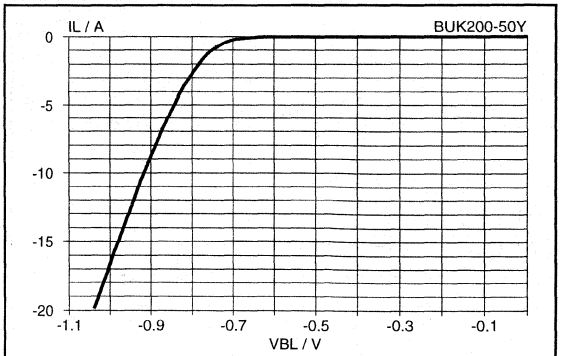


Fig.31. Typical reverse diode characteristic. $I_L = f(V_{BL})$; conditions $V_{IG} = 0$ V, $T_j = 25$ °C

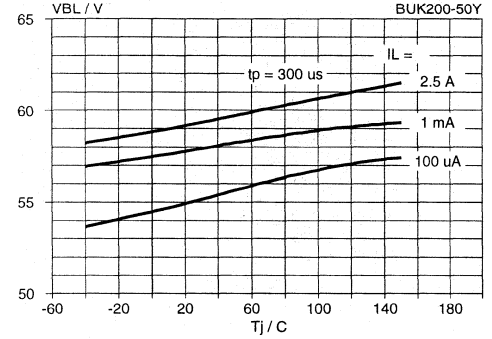


Fig.29. Typical battery to load clamping voltage. $V_{BL} = f(T_j)$; parameter I_L; condition $I_G = 5$ mA.

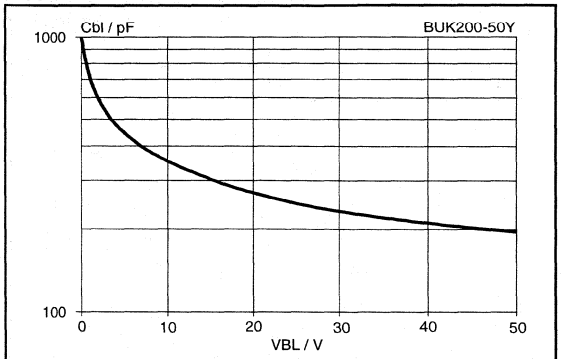


Fig.32. Typical output capacitance. $T_{mb} = 25$ °C $C_{bl} = f(V_{BL})$; conditions $f = 1$ MHz, $V_{IG} = 0$ V

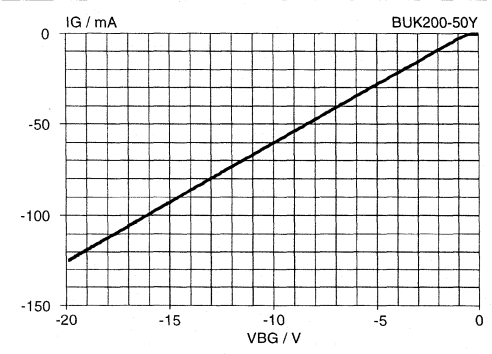


Fig.30. Typical reverse battery characteristic. $I_G = f(V_{BG})$; conditions $I_L = 0$ A, $T_j = 25$ °C

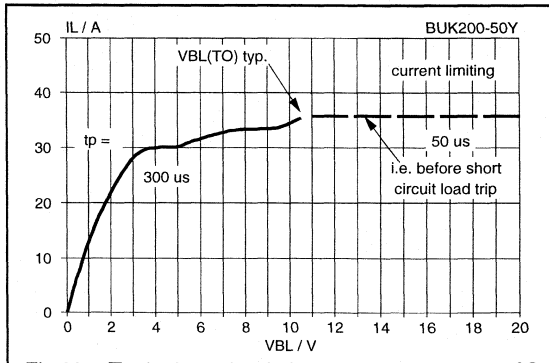


Fig.33. Typical overload characteristic, $T_{mb} = 25$ °C. $I_L = f(V_{BL})$; condition $V_{BG} = 13$ V; parameter t_p

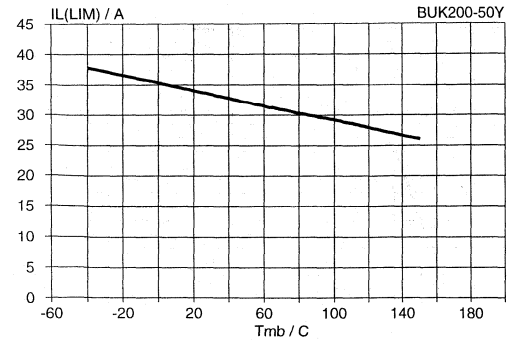


Fig.34. Typical overload current, V_{BL} = 8.5 V. $I_L = f(T_{mb})$; conditions V_{BG} = 13 V; t_p = 300 µs

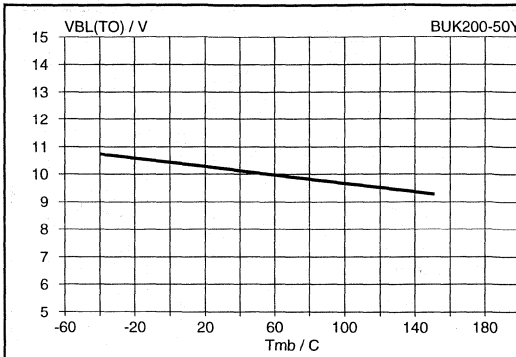


Fig.36. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(T_{mb})$; condition V_{BG} = 13 V

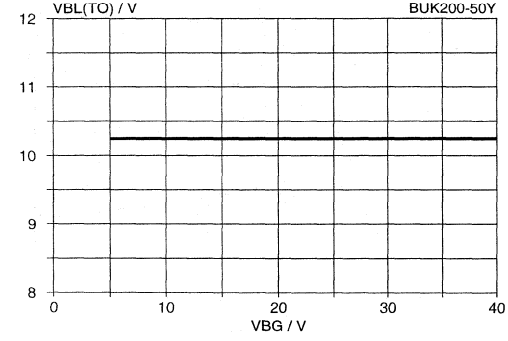


Fig.35. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(V_{BG})$; condition T_{mb} = 25 °C

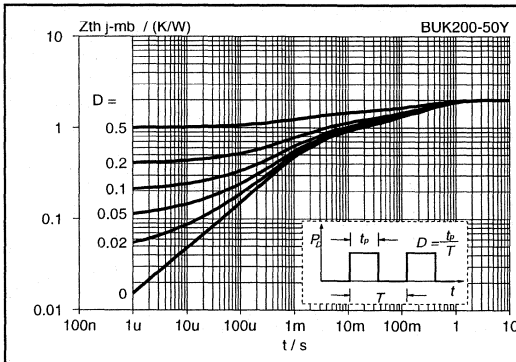


Fig.37. Transient thermal impedance. $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

PowerMOS transistor TOPFET high side switch

BUK201-50Y

For maintenance only. Do not use for design-in.

DESCRIPTION

Monolithic temperature and overload protected power switch based on MOSFET technology in a 5 pin plastic envelope, configured as a single high side switch.

APPLICATIONS

General controller for driving lamps, motors, solenoids, heaters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	UNIT
I_L	Nominal load current (ISO)	6	A
SYMBOL	**PARAMETER**	**MAX.**	**UNIT**
V_{BG}	Continuous off-state supply voltage	50	V
I_L	Continuous load current	15	A
T_j	Continuous junction temperature	150	°C
R_{ON}	On-state resistance	60	mΩ

FEATURES

- Vertical power DMOS switch
- Low on-state resistance
- 5 V logic compatible input
- Overtemperature protection - self resets with hysteresis
- Overload protection against short circuit load with output current limiting; latched - reset by input
- High supply voltage load protection
- Supply undervoltage lock out
- Status indication for overload protection activated
- Diagnostic status indication of open circuit load
- Very low quiescent current
- Voltage clamping for turn off of inductive loads
- ESD protection on all pins
- Reverse battery and overvoltage protection

FUNCTIONAL BLOCK DIAGRAM

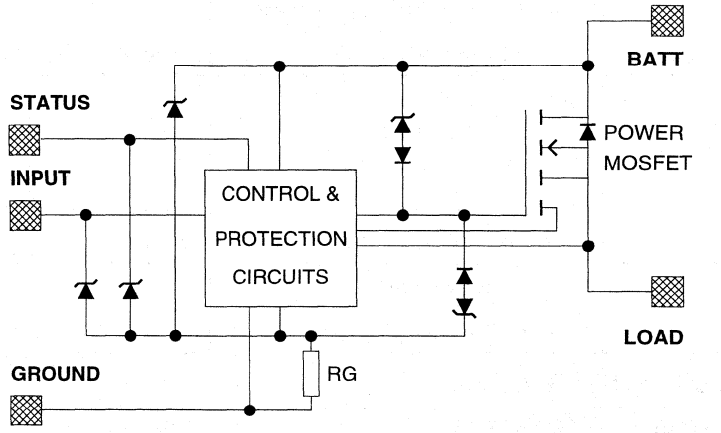


Fig.1. Elements of the TOPFET HSS with internal ground resistor.

PINNING - SOT263

PIN	DESCRIPTION
1	Ground
2	Input
3	Battery (+ve supply)
4	Status
5	Load
tab	connected to pin 3

PIN CONFIGURATION

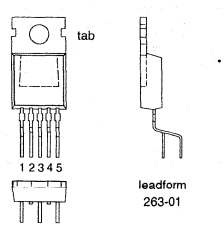


Fig. 2.

SYMBOL

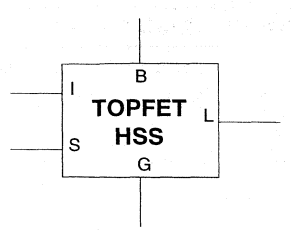


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Battery voltages				
V_{BG}	Continuous off-state supply voltage	-	0	50	V
	Reverse battery voltages[1]	External resistors:			
$-V_{BG}$	Repetitive peak supply voltage	$R_I = R_S \geq 4.7$ kΩ, $\delta \leq 0.1$	-	32	V
$-V_{BG}$	Continuous reverse supply voltage	$R_I = R_S \geq 4.7$ kΩ	-	16	V
I_L	Continuous load current	$T_{mb} \leq 115$ °C	-	15	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	83.3	W
T_{stg}	Storage temperature	-	-55	175	°C
T_j	Continuous junction temperature[2]	-	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C
	Input and status				
I_I	Continuous input current	-	-5	5	mA
I_S	Continuous status current	-	-5	5	mA
I_I	Repetitive peak input current	$\delta \leq 0.1$	-20	20	mA
I_S	Repetitive peak status current	$\delta \leq 0.1$	-20	20	mA
	Inductive load clamping				
E_{BL}	Non-repetitive clamping energy	$T_{mb} = 150$ °C prior to turn-off	-	1.2	J

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance[3]					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	1.2	1.5	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	75	K/W

1 Reverse battery voltage is allowed only with external input and status resistors to limit the currents to a safe value.

2 For normal continuous operation. A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 Of the output Power MOS transistor.

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Clamping voltages					
V_{BG}	Battery to ground	I_G = 1 mA	50	55	65	V
V_{BL}	Battery to load	$I_L = I_G$ = 1 mA	50	55	65	V
$-V_{LG}$	Negative load to ground	I_L = 1 mA	12	17	21	V
	Supply voltage	battery to ground				
V_{BG}	Operating range[1]	-	5	-	40	V
	Currents	V_{BG} = 13 V				
I_L	Nominal load current[2]	V_{BL} = 0.5 V; T_{mb} = 85 °C	6	-	-	A
I_B	Quiescent current[3]	V_{IG} = 0 V; V_{LG} = 0 V	-	0.1	2	µA
I_G	Operating current[4]	V_{IG} = 5 V; I_L = 0 A	1.5	2.2	4	mA
I_L	Off-state load current[5]	V_{BL} = 13 V; V_{IG} = 0 V	-	0.1	1	µA
	Resistances					
R_{ON}	On-state resistance[6]	V_{BG} = 13 V; I_L = 7.5 A; t_p = 300 µs	-	45	60	mΩ
R_{ON}	On-state resistance	V_{BG} = 5 V; I_L = 1.5 A; t_p = 300 µs	-	70	90	mΩ
R_G	Internal ground resistance	I_G = 10 mA	-	150	-	Ω

INPUT CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_I	Input current	V_{IG} = 5 V	35	60	100	µA
V_{IG}	Input clamping voltage	I_I = 200 µA	6	7.5	8.5	V
$V_{IG(ON)}$	Input turn-on threshold voltage		-	2.1	2.7	V
$V_{IG(OFF)}$	Input turn-off threshold voltage		1.5	2	-	V

1 On-state resistance is increased if the supply voltage is less than 9 V. Refer to figure 8.

2 Defined as in ISO 10483-1.

3 This is the continuous current drawn from the battery when the input is low and includes leakage current to the load.

4 This is the continuous current drawn from the battery with no load connected, but with the input high.

5 The measured current is in the load pin only.

6 The supply and input voltage for the R_{ON} tests are continuous. The specified pulse duration t_p refers only to the applied load current.

PROTECTION FUNCTIONS AND STATUS INDICATIONS

Truth table for normal, open-circuit load and overload conditions and abnormal supply voltages.

FUNCTIONS		TRUTH TABLE			THRESHOLD			
SYMBOL	CONDITION	INPUT	STATUS	OUTPUT	MIN.	TYP.	MAX.	UNIT
	Normal on-state	1	1	1				
	Normal off-state	0	1	0				
$I_{L(OC)}$	Open circuit load[1]	1	0	1	100	350	600	mA
	Open circuit load	0	1	0				
$T_{j(TO)}$	Over temperature[2]	1	0	0	150	175	-	°C
	Over temperature[3]	0	0	0				
$V_{BL(TO)}$	Short circuit load[4]	1	0	0	9	10.5	12	V
	Short circuit load	0	1	0				
$V_{BG(TO)}$	Low supply voltage[5]	X	1	0	3	4	5	V
$V_{BG(LP)}$	High supply voltage[6]	X	1	0	40	45	50	V

For input '0' equals low, '1' equals high, 'X' equals don't care.
For status '0' equals low, '1' equals open or high.
For output switch '0' equals off, '1' equals on.

STATUS CHARACTERISTICS

T_{mb} = 25 °C.
The status output is an open drain transistor, and requires an external pull-up circuit to indicate a logic high.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SG}	Status clamping voltage	I_S = 100 µA; V_{IG} = 0 V	6	7	8	V
V_{SG}	Status low voltage	I_S = 50 µA; V_{BG} = 13 V; V_{IG} = 5 V	-	0.7	0.8	V
I_S	Status leakage current	V_{SG} = 5 V	-	0.1	1	µA
I_S	Status saturation current[7]	V_{SS} = 5 V; R_S = 0 Ω; V_{BG} = 13 V	-	5	-	mA
	Application information					
R_S	External pull-up resistor[8]	V_{SS} = 5 V	-	100	-	kΩ

1 In the on-state, the switch detects whether the load current is less than the quoted open load threshold current. This is for status indication only. Typical hysteresis equals 140 mA. The thresholds are specified for supply voltage within the normal working range.

2 After cooling below the reset temperature the switch will resume normal operation. The reset temperature is lower than the trip temperature by typically 10 °C.

3 If the overtemperature protection has operated, status remains low to indicate the overtemperature condition even if the input is taken low, providing the device has not cooled below the reset temperature.

4 After short circuit protection has operated, the input voltage must be toggled low for the switch to resume normal operation.

5 Undervoltage sensor causes the device to switch off. Typical hysteresis equals 0.7 V.

6 Overvoltage sensor causes the device to switch off to protect the load. Typical hysteresis equals 1.3 V.

7 In a fault condition with the pull-up resistor short circuited while the status transistor is conducting.

8 The pull-up resistor also protects the status pin during reverse battery conditions.

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Inductive load turn-off					
$-V_{LG}$	Negative load voltage[1]	V_{IG} = 0 V; I_L = 7.5 A; t_p = 300 µs	15	20	25	V
	Short circuit load protection[2]	V_{IG} = 5 V; $R_L \leq 10$ mΩ				
$t_{d\,sc}$	Response time		-	90	-	µs
I_L	Load current prior to turn-off	$t < t_{d\,sc}$	-	42	-	A
	Overload protection[3]					
$I_{L(lim)}$	Load current limiting	V_{BL} = 9 V; t_p = 300 µs	28	40	52	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C, V_{BG} = 13 V, for resistive load R_L = 13 Ω.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	During turn-on	to V_{IG} = 5 V				
$t_{d\,on}$	Delay time	to 10% V_L	-	16	-	µs
dV/dt_{on}	Rate of rise of load voltage		-	1	2.5	V/µs
t_{on}	Total switching time	to 90% V_L	-	40	-	µs
	During turn-off	to V_{IG} = 0 V				
$t_{d\,off}$	Delay time	to 90% V_L	-	30	-	µs
dV/dt_{off}	Rate of fall of load voltage		-	1.2	2.5	V/µs
t_{off}	Total switching time	to 10% V_L	-	50	-	µs

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz; V_{IG} = 0 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{ig}	Input capacitance	V_{BG} = 13 V	-	15	20	pF
C_{bl}	Output capacitance	$V_{BL} = V_{BG}$ = 13 V	-	415	580	pF
C_{sg}	Status capacitance	V_{SG} = 5 V	-	11	15	pF

1 For a high side switch, the load pin voltage goes negative with respect to ground during the turn-off of an inductive load. This negative voltage is clamped by the device.

2 The load current is self-limited during the response time for short circuit load protection. Response time is measured from when input goes high.

3 If the load resistance is low, but not a complete short circuit, such that the on-state voltage remains less than $V_{BL(TO)}$, the device remains in current limiting until the overtemperature protection operates.

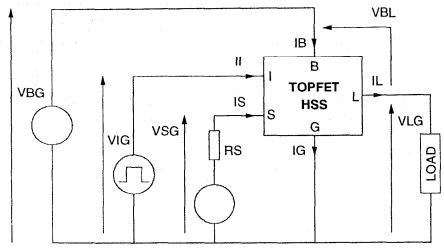


Fig.4. High side switch measurements schematic. (current and voltage conventions)

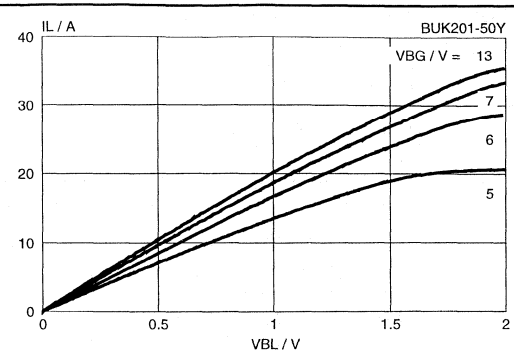


Fig.7. Typical on-state characteristics, T_j = 25 ˚C. $I_L = f(V_{BL})$; parameter V_{BG}; t_p = 250 µs

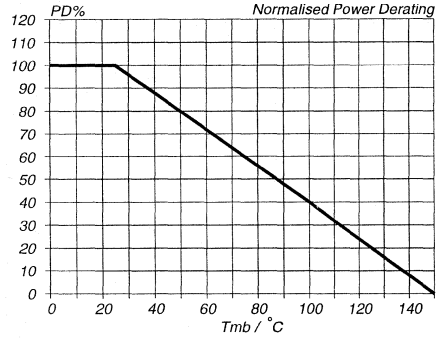


Fig.5. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

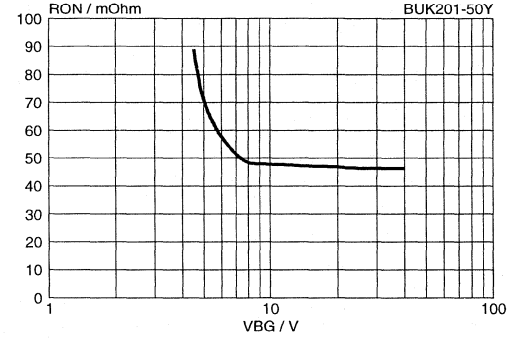


Fig.8. Typical on-state resistance, T_j = 25 ˚C. $R_{ON} = f(V_{BG})$; conditions: I_L = 7.5 A; t_p = 300 µs

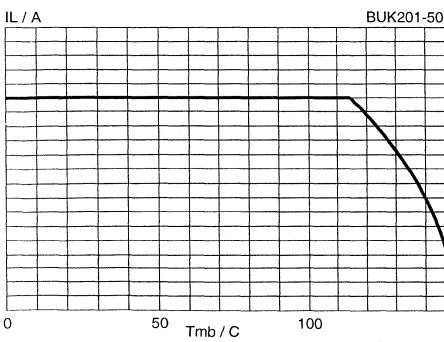


Fig.6. Limiting continuous on-state load current. $I_L = f(T_{mb})$; conditions: V_{IG} = 5 V, V_{BG} = 13 V

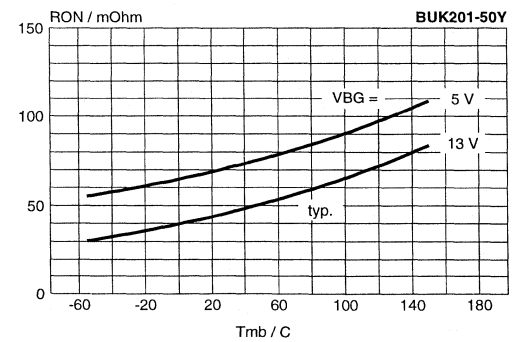


Fig.9. Typical on-state resistance, t_p = 300 µs. $R_{ON} = f(T_j)$; parameter V_{BG}; condition I_L = 1.5 A

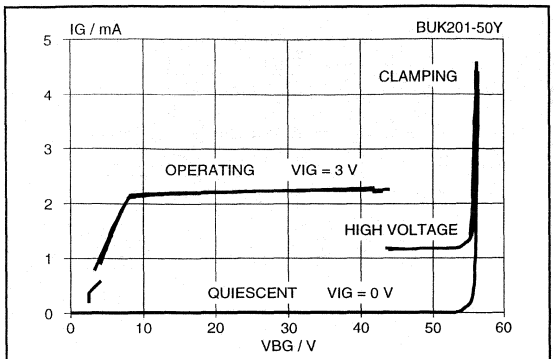


Fig.10. Typical supply characteristics, 25 ˚C.
$I_G = f(V_{BG})$; parameter V_{IG}

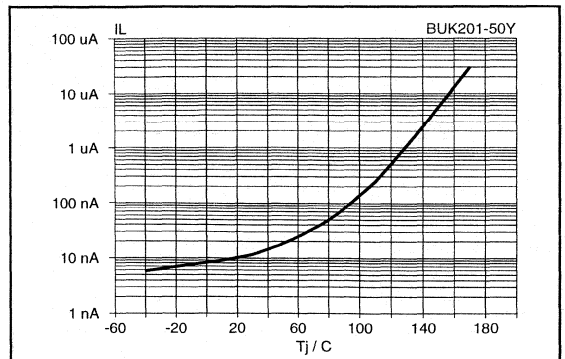


Fig.13. Typical off-state leakage current.
$I_L = f(T_j)$; conditions: V_{BL} = 13 V = V_{BG}; V_{IG} = 0 V.

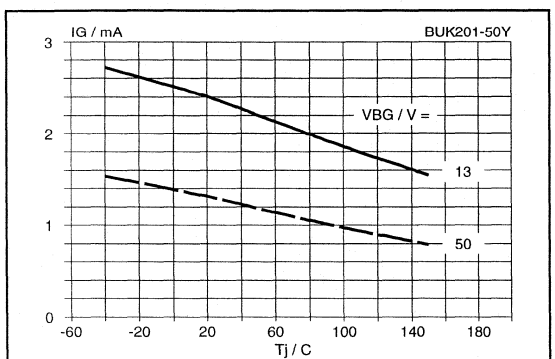


Fig.11. Typical operating supply current.
$I_G = f(T_j)$; parameter V_{BG}; condition V_{IG} = 5 V

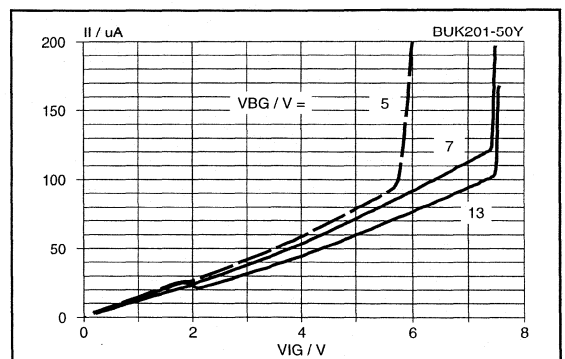


Fig.14. Typical input characteristics, T_j = 25 ˚C.
$I_I = f(V_{IG})$; parameter V_{BG}

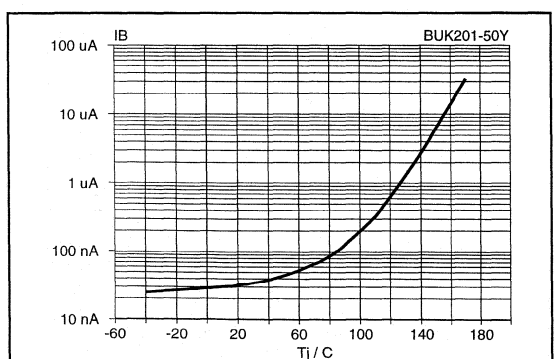


Fig.12. Typical supply quiescent current.
$I_B = f(T_j)$; condition V_{BG} = 13 V, V_{IG} = 0 V, V_{LG} = 0 V

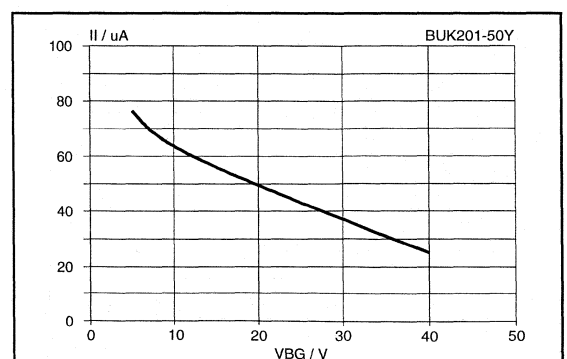


Fig.15. Typical input current, T_j = 25 ˚C.
$I_I = f(V_{BG})$; condition V_{IG} = 5 V

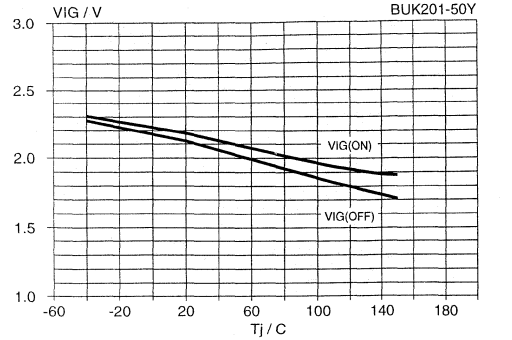


Fig.16. Typical input threshold voltages. $V_{IG} = f(T_j)$; conditions $V_{BG} = 13$ V, $I_L = 80$ mA

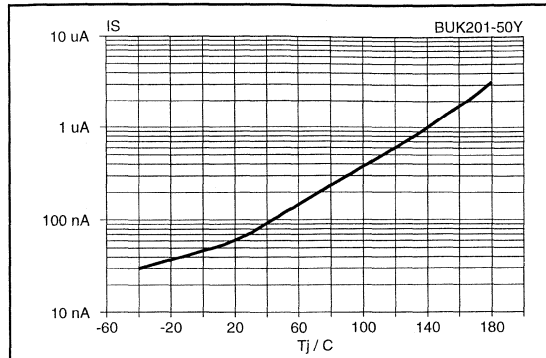


Fig.19. Typical status leakage current. $I_S = f(T_j)$; conditions $V_{SG} = 5$ V, $V_{IG} = V_{BG} = 0$ V

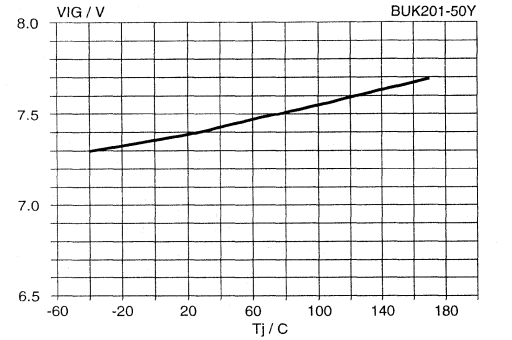


Fig.17. Typical input clamping voltage. $V_{IG} = f(T_j)$; conditions $I_I = 200$ µA, $V_{BG} = 13$ V

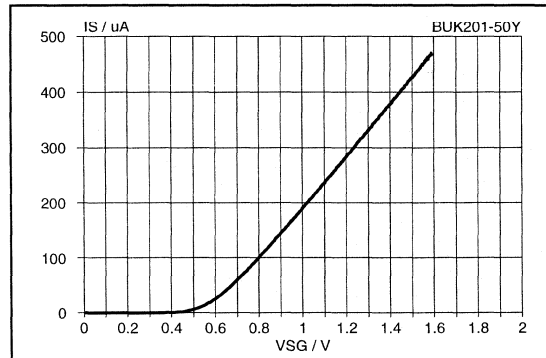


Fig.20. Typical status low characteristic, $T_j = 25$ °C. $I_S = f(V_{SG})$; conditions $V_{IG} = 5$ V, $V_{BG} = 13$ V, $I_L = 0$ A

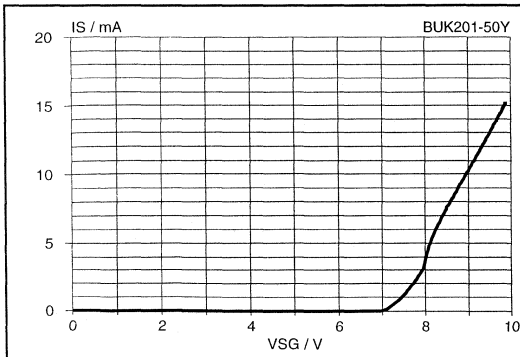


Fig.18. Typical status characteristic, $T_j = 25$ °C. $I_S = f(V_{SG})$; conditions $V_{IG} = V_{BG} = 0$ V

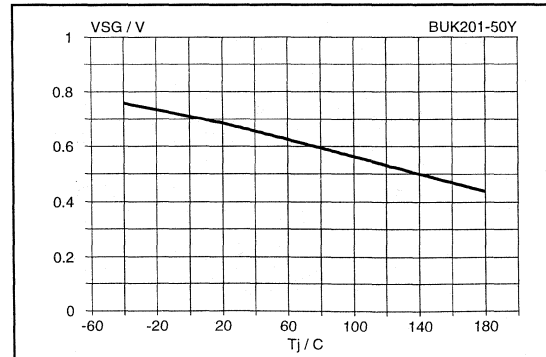


Fig.21. Typical status low voltage, $V_{SG} = f(T_j)$. conditions $I_S = 50$ µA, $V_{IG} = 5$ V, $V_{BG} = 13$ V, $I_L = 0$ A

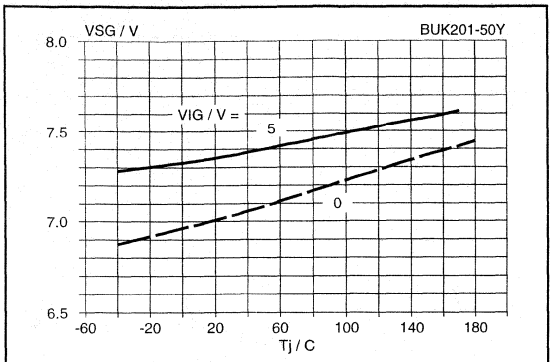


Fig.22. Typical status clamping voltage, $V_{SG} = f(T_j)$. parameter V_{IG}; conditions $I_S = 100\ \mu A$, $V_{BG} = 13\ V$

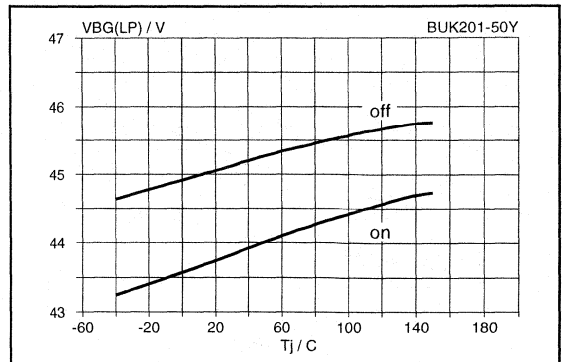


Fig.25. Supply typical overvoltage thresholds. $V_{BG(LP)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $I_L = 80\ mA$

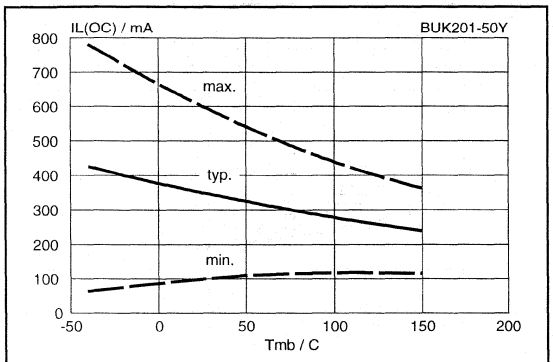


Fig.23. Low load current detection threshold. $I_{L(OC)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $V_{BG} = 13\ V$

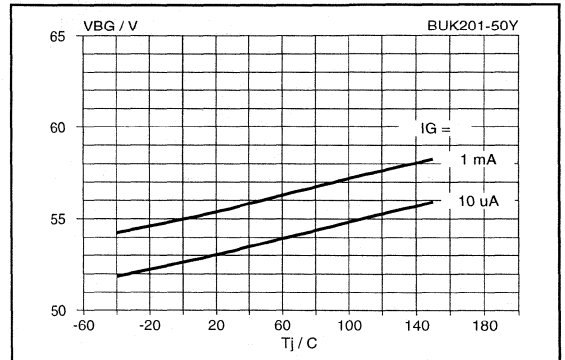


Fig.26. Typical battery to ground clamping voltage. $V_{BG} = f(T_j)$; parameter I_G

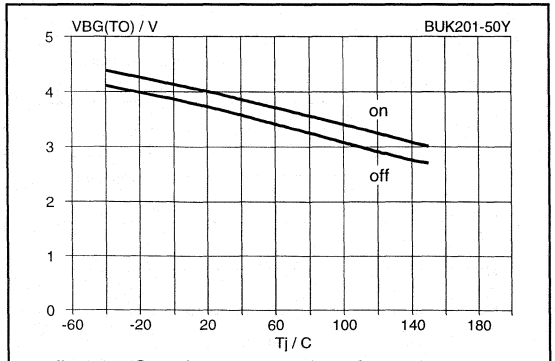


Fig.24. Supply typical undervoltage thresholds. $V_{BG(TO)} = f(T_j)$; conditions $V_{IG} = 3\ V$; $I_L = 80\ mA$

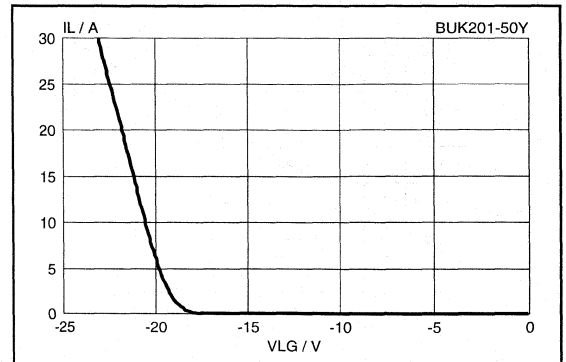


Fig.27. Typical negative load clamping characteristic. $I_L = f(V_{LG})$; conditions $V_{IG} = 0\ V$, $t_p = 300\ \mu s$, 25 ˚C

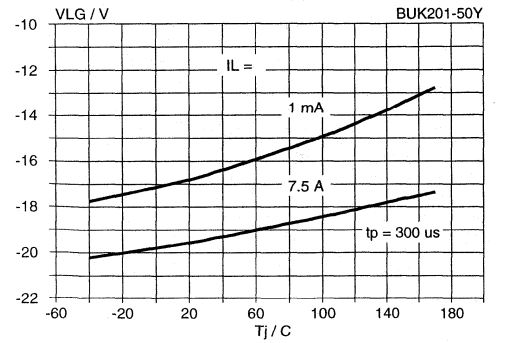


Fig.28. Typical negative load clamping voltage. $V_{LG} = f(T_j)$; parameter I_L; condition $V_{IG} = 0$ V.

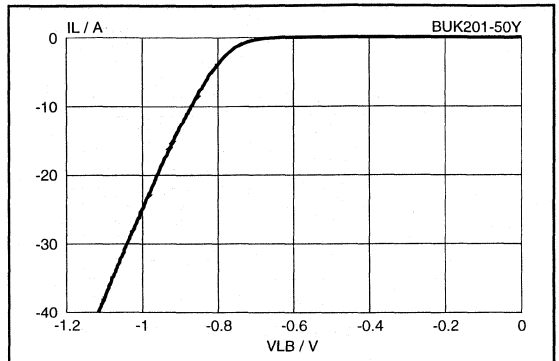


Fig.31. Typical reverse diode characteristic. $I_L = f(V_{BL})$; conditions $V_{IG} = 0$ V, $T_j = 25$ °C

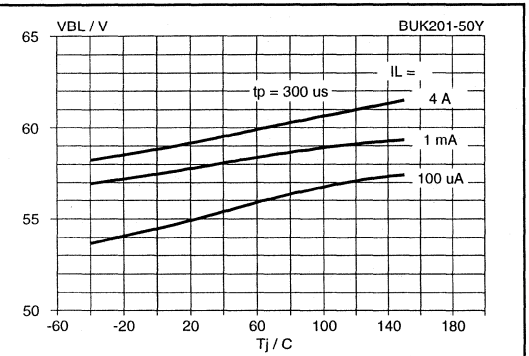


Fig.29. Typical battery to load clamping voltage. $V_{BL} = f(T_j)$; parameter I_L; condition $I_G = 5$ mA.

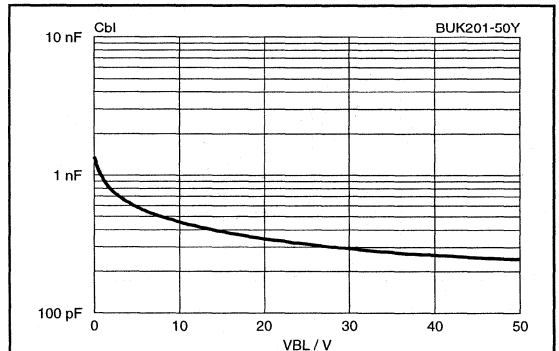


Fig.32. Typical output capacitance. $T_{mb} = 25$ °C $C_{bl} = f(V_{BL})$; conditions f = 1 MHz, $V_{IG} = 0$ V

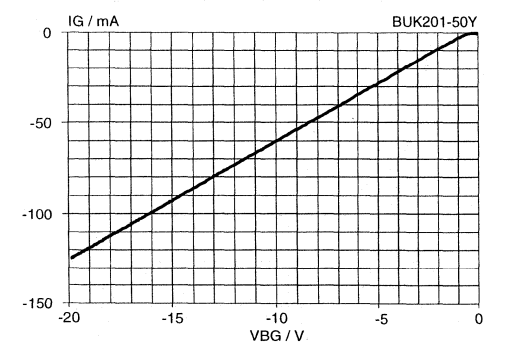


Fig.30. Typical reverse battery characteristic. $I_G = f(V_{BG})$; conditions $I_L = 0$ A, $T_j = 25$ °C

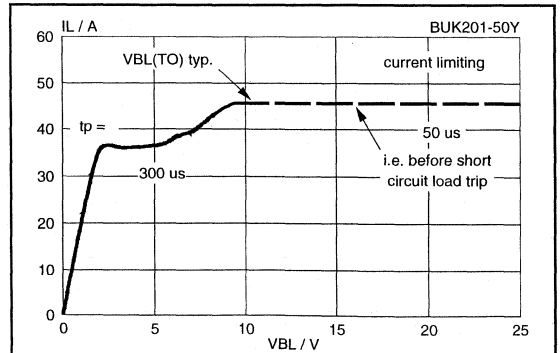


Fig.33. Typical overload characteristic, $T_{mb} = 25$ °C. $I_L = f(V_{BL})$; condition $V_{BG} = 13$ V; parameter t_p

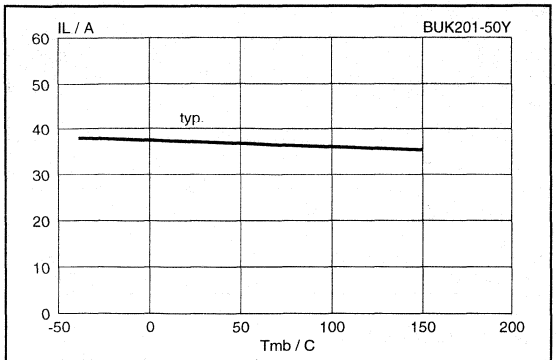


Fig.34. Typical overload current, V_{BL} = 9 V. $I_L = f(T_{mb})$; conditions V_{BG} = 13 V; t_p = 300 µs

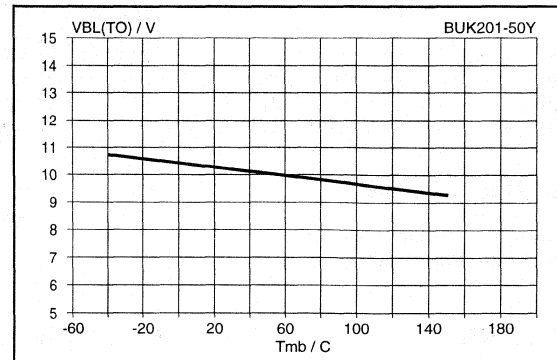


Fig.36. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(T_{mb})$; condition V_{BG} = 13 V

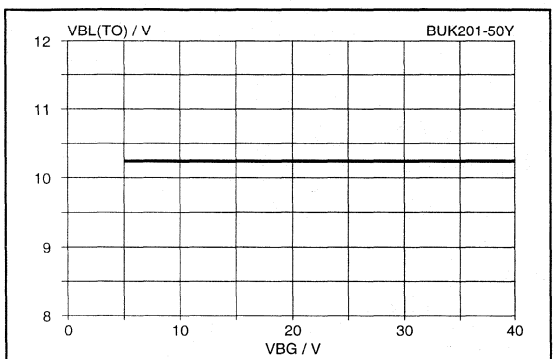


Fig.35. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(V_{BG})$; condition T_{mb} = 25 °C

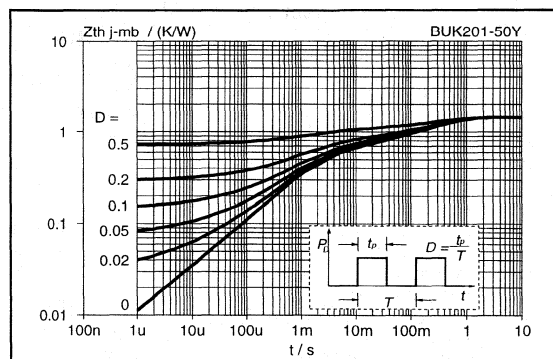


Fig.37. Transient thermal impedance. $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

PowerMOS transistor TOPFET high side switch

BUK202-50Y

For maintenance only. Do not use for design-in.

DESCRIPTION

Monolithic temperature and overload protected power switch based on MOSFET technology in a 5 pin plastic envelope, configured as a single high side switch.

APPLICATIONS

General controller for driving lamps, motors, solenoids, heaters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	UNIT
I_L	Nominal load current (ISO)	9	A
SYMBOL	**PARAMETER**	**MAX.**	**UNIT**
V_{BG}	Continuous off-state supply voltage	50	V
I_L	Continuous load current	20	A
T_j	Continuous junction temperature	150	°C
R_{ON}	On-state resistance	38	mΩ

FEATURES

- Vertical power DMOS switch
- Low on-state resistance
- 5 V logic compatible input
- Overtemperature protection - self resets with hysteresis
- Overload protection against short circuit load with output current limiting; latched - reset by input
- High supply voltage load protection
- Supply undervoltage lock out
- Status indication for overload protection activated
- Diagnostic status indication of open circuit load
- Very low quiescent current
- Voltage clamping for turn off of inductive loads
- ESD protection on all pins
- Reverse battery and overvoltage protection

FUNCTIONAL BLOCK DIAGRAM

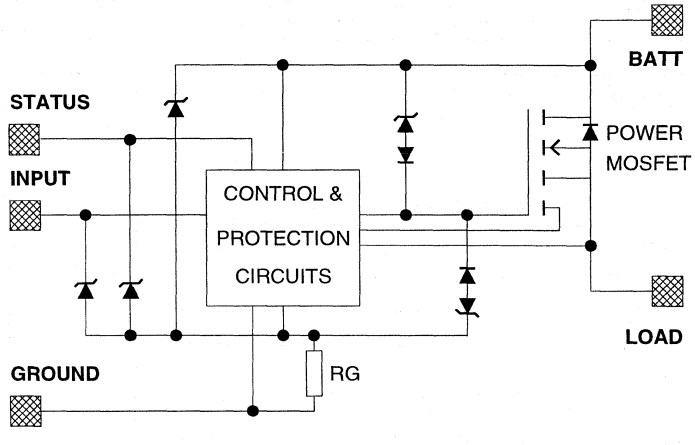


Fig.1. Elements of the TOPFET HSS with internal ground resistor.

PINNING - SOT263

PIN	DESCRIPTION
1	Ground
2	Input
3	Battery (+ve supply)
4	Status
5	Load
tab	connected to pin 3

PIN CONFIGURATION

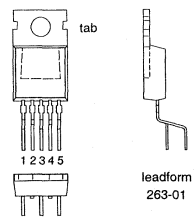


Fig. 2.

SYMBOL

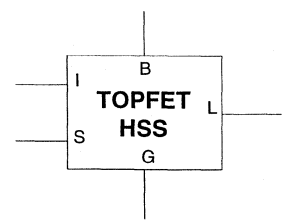


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Battery voltages				
V_{BG}	Continuous off-state supply voltage	-	0	50	V
	Reverse battery voltages[1]	External resistors:			
$-V_{BG}$	Repetitive peak supply voltage	$R_I = R_S \geq 4.7\ k\Omega$, $\delta \leq 0.1$	-	32	V
$-V_{BG}$	Continuous reverse supply voltage	$R_I = R_S \geq 4.7\ k\Omega$	-	16	V
I_L	Continuous load current	$T_{mb} \leq 110$ °C	-	20	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	125	W
T_{stg}	Storage temperature	-	-55	175	°C
T_j	Continuous junction temperature[2]	-	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C
	Input and status				
I_I	Continuous input current	-	-5	5	mA
I_S	Continuous status current	-	-5	5	mA
I_I	Repetitive peak input current	$\delta \leq 0.1$	-20	20	mA
I_S	Repetitive peak status current	$\delta \leq 0.1$	-20	20	mA
	Inductive load clamping				
E_{BL}	Non-repetitive clamping energy	$T_{mb} = 150$ °C prior to turn-off	-	1.7	J

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance[3]					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	0.8	1	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	75	K/W

1 Reverse battery voltage is allowed only with external input and status resistors to limit the currents to a safe value.

2 For normal continuous operation. A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 Of the output Power MOS transistor.

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Clamping voltages					
V_{BG}	Battery to ground	I_G = 1 mA	50	55	65	V
V_{BL}	Battery to load	$I_L = I_G$ = 1 mA	50	55	65	V
$-V_{LG}$	Negative load to ground	I_L = 1 mA	12	17	21	V
	Supply voltage	battery to ground				
V_{BG}	Operating range[1]	-	5	-	40	V
	Currents	V_{BG} = 13 V				
I_L	Nominal load current[2]	V_{BL} = 0.5 V; T_{mb} = 85 °C	9	-	-	A
I_B	Quiescent current[3]	V_{IG} = 0 V; V_{LG} = 0 V	-	0.1	2	µA
I_G	Operating current[4]	V_{IG} = 5 V; I_L = 0 A	1.5	2.2	4	mA
I_L	Off-state load current[5]	V_{BL} = 13 V; V_{IG} = 0 V	-	0.1	1	µA
	Resistances					
R_{ON}	On-state resistance[6]	V_{BG} = 13 V; I_L = 10 A; t_p = 300 µs	-	28	38	mΩ
R_{ON}	On-state resistance	V_{BG} = 5 V; I_L = 2 A; t_p = 300 µs	-	36	48	mΩ
R_G	Internal ground resistance	I_G = 10 mA	-	150	-	Ω

INPUT CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_I	Input current	V_{IG} = 5 V	35	60	100	µA
V_{IG}	Input clamping voltage	I_I = 200 µA	6	7.5	8.5	V
$V_{IG(ON)}$	Input turn-on threshold voltage		-	2.1	2.7	V
$V_{IG(OFF)}$	Input turn-off threshold voltage		1.5	2	-	V

1 On-state resistance is increased if the supply voltage is less than 9 V. Refer to figure 8.

2 Defined as in ISO 10483-1.

3 This is the continuous current drawn from the supply when the input is low and includes leakage current to the load.

4 This is the continuous current drawn from the supply with no load connected, but with the input high.

5 The measured current is in the load pin only.

6 The supply and input voltage for the R_{ON} tests are continuous. The specified pulse duration t_p refers only to the applied load current.

PROTECTION FUNCTIONS AND STATUS INDICATIONS

Truth table for normal, open-circuit load and overload conditions and abnormal supply voltages.

FUNCTIONS		TRUTH TABLE			THRESHOLD			
SYMBOL	CONDITION	INPUT	STATUS	OUTPUT	MIN.	TYP.	MAX.	UNIT
	Normal on-state	1	1	1				
	Normal off-state	0	1	0				
$I_{L(OC)}$	Open circuit load[1]	1	0	1	150	450	750	mA
	Open circuit load	0	1	0				
$T_{j(TO)}$	Over temperature[2]	1	0	0	150	175	-	°C
	Over temperature[3]	0	0	0				
$V_{BL(TO)}$	Short circuit load[4]	1	0	0	9	10.5	12	V
	Short circuit load	0	1	0				
$V_{BG(TO)}$	Low supply voltage[5]	X	1	0	3	4	5	V
$V_{BG(LP)}$	High supply voltage[6]	X	1	0	40	45	50	V

For input '0' equals low, '1' equals high, 'X' equals don't care.
For status '0' equals low, '1' equals open or high.
For output switch '0' equals off, '1' equals on.

STATUS CHARACTERISTICS

T_{mb} = 25 °C.
The status output is an open drain transistor, and requires an external pull-up circuit to indicate a logic high.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SG}	Status clamping voltage	I_S = 100 µA; V_{IG} = 0 V	6	7	8	V
V_{SG}	Status low voltage	I_S = 50 µA; V_{BG} = 13 V; V_{IG} = 5 V	-	0.7	0.8	V
I_S	Status leakage current	V_{SG} = 5 V	-	0.1	1	µA
I_S	Status saturation current[7]	V_{SS} = 5 V; R_S = 0 Ω; V_{BG} = 13 V	-	5	-	mA
	Application information					
R_S	External pull-up resistor[8]	V_{SS} = 5 V	-	100	-	kΩ

1 In the on-state, the switch detects whether the load current is less than the quoted open load threshold current. This is for status indication only. Typical hysteresis equals 230 mA. The thresholds are specified for supply voltage within the normal working range.

2 After cooling below the reset temperature the switch will resume normal operation. The reset temperature is lower than the trip temperature by typically 10 °C.

3 If the overtemperature protection has operated, status remains low to indicate the overtemperature condition even if the input is taken low, providing the device has not cooled below the reset temperature.

4 After short circuit protection has operated, the input voltage must be toggled low for the switch to resume normal operation.

5 Undervoltage sensor causes the device to switch off. Typical hysteresis equals 0.5 V.

6 Overvoltage sensor causes the device to switch off. Typical hysteresis equals 1.3 V.

7 In a fault condition with the pull-up resistor short circuited while the status transistor is conducting.

8 The pull-up resistor also protects the status pin during reverse battery conditions.

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Inductive load turn-off					
$-V_{LG}$	Negative load voltage[1]	V_{IG} = 0 V; I_L = 10 A; t_p = 300 µs	15	20	25	V
	Short circuit load protection[2]	V_{IG} = 5 V; $R_L \leq$ 10 mΩ				
$t_{d\,sc}$	Response time		-	75	-	µs
I_L	Load current prior to turn-off	$t < t_{d\,sc}$	-	50	-	A
	Overload protection[3]					
$I_{L(lim)}$	Load current limiting	V_{BL} = 9 V; t_p = 300 µs	34	45	64	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C, V_{BG} = 13 V, for resistive load R_L = 13 Ω.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	During turn-on	to V_{IG} = 5 V				
$t_{d\,on}$	Delay time	to 10% V_L	-	16	-	µs
dV/dt_{on}	Rate of rise of load voltage		-	0.7	2	V/µs
t_{on}	Total switching time	to 90% V_L	-	140	-	µs
	During turn-off	to V_{IG} = 0 V				
$t_{d\,off}$	Delay time	to 90% V_L	-	40	-	µs
dV/dt_{off}	Rate of fall of load voltage		-	0.7	2	V/µs
t_{off}	Total switching time	to 10% V_L	-	70	-	µs

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz; V_{IG} = 0 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{ig}	Input capacitance	V_{BG} = 13 V	-	15	20	pF
C_{bl}	Output capacitance	V_{BL} = V_{BG} = 13 V	-	500	700	pF
C_{sg}	Status capacitance	V_{SG} = 5 V	-	11	15	pF

1 For a high side switch, the load pin voltage goes negative with respect to ground during the turn-off of an inductive load. This negative voltage is clamped by the device.

2 The load current is self-limited during the response time for short circuit load protection. Response time is measured from when input goes high.

3 If the load resistance is low, but not a complete short circuit, such that the on-state voltage remains less than $V_{BL(TO)}$, the device remains in current limiting until the overtemperature protection operates.

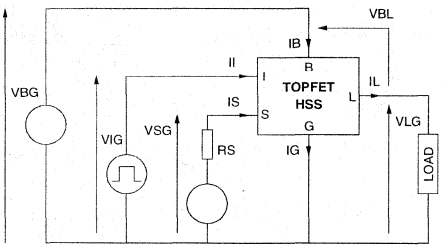


Fig.4. High side switch measurements schematic. (current and voltage conventions)

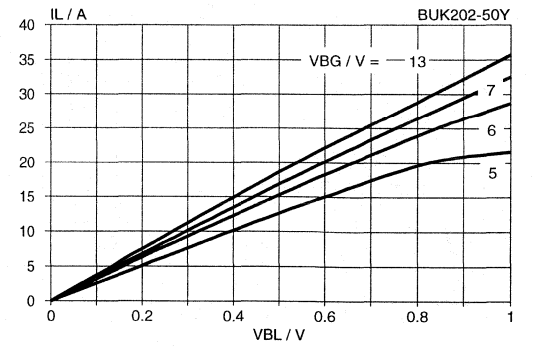


Fig.7. Typical on-state characteristics, T_j = 25 °C. $I_L = f(V_{BL})$; parameter V_{BG}; t_p = 250 µs

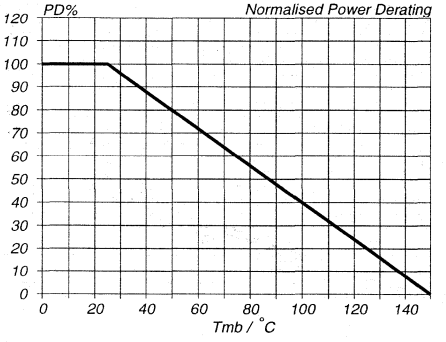


Fig.5. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\ °C) = f(T_{mb})$

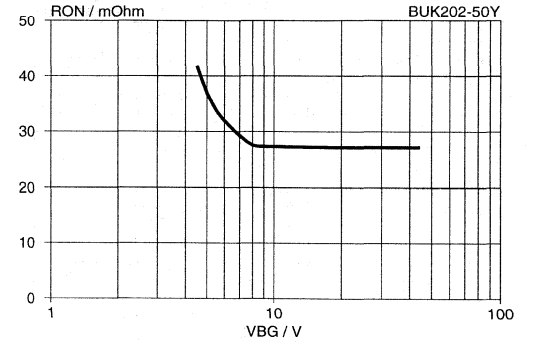


Fig.8. Typical on-state resistance, T_j = 25 °C. $R_{ON} = f(V_{BG})$; conditions: I_L = 10 A; t_p = 300 µs

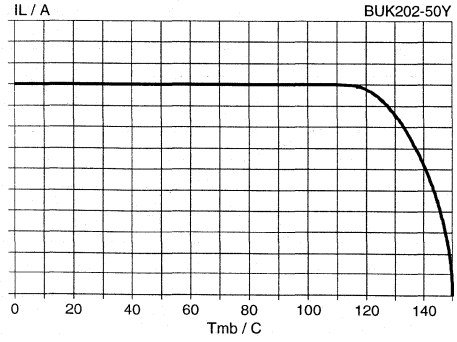


Fig.6. Limiting continuous on-state load current. $I_L = f(T_{mb})$; conditions: V_{IG} = 5 V, V_{BG} = 13 V

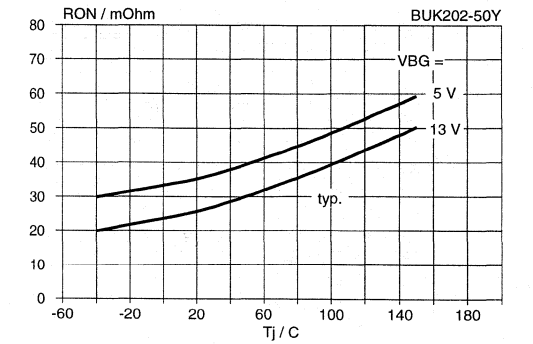


Fig.9. Typical on-state resistance, t_p = 300 µs. $R_{ON} = f(T_j)$; parameter V_{BG}; condition I_L = 2 A

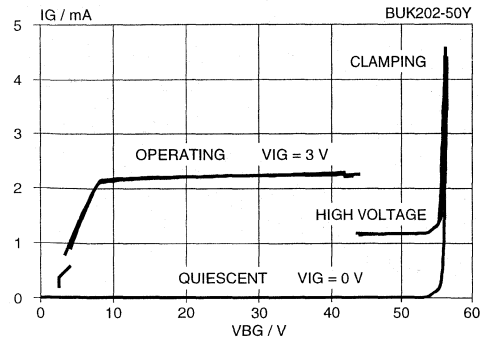


Fig.10. Typical supply characteristics, 25 ˚C. $I_G = f(V_{BG})$; parameter V_{IG}

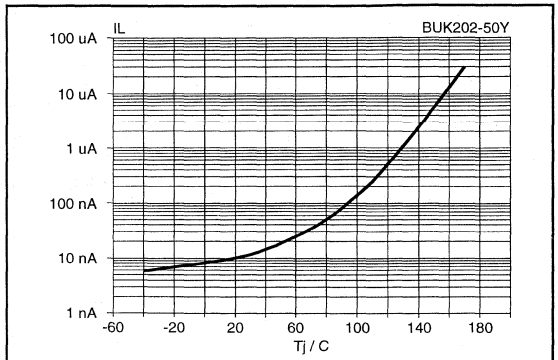


Fig.13. Typical off-state leakage current. $I_L = f(T_j)$; conditions: V_{BL} = 13 V = V_{BG}; V_{IG} = 0 V.

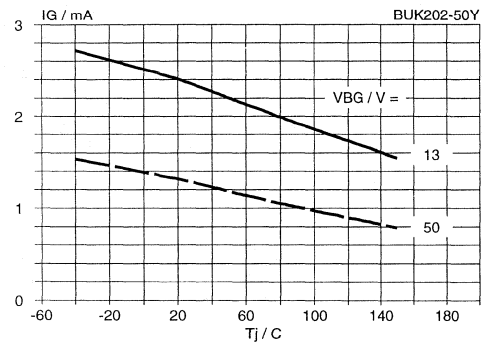


Fig.11. Typical operating supply current. $I_G = f(T_j)$; parameter V_{BG}; condition V_{IG} = 5 V

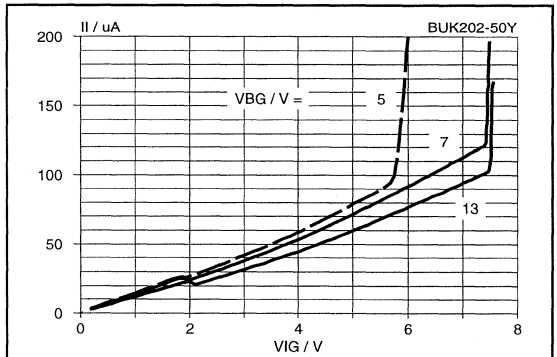


Fig.14. Typical input characteristics, T_j = 25 ˚C. $I_I = f(V_{IG})$; parameter V_{BG}

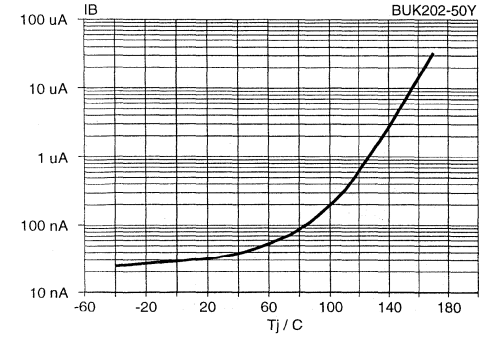


Fig.12. Typical supply quiescent current. $I_B = f(T_j)$; condition V_{BG} = 13 V, V_{IG} = 0 V, V_{LG} = 0 V

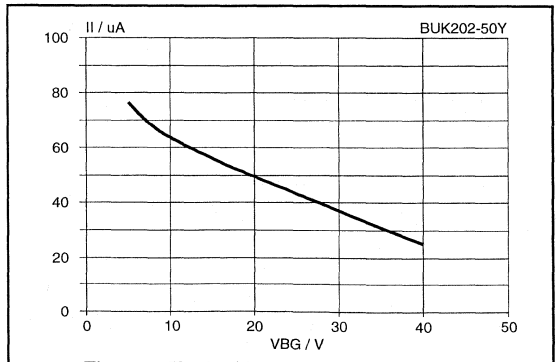


Fig.15. Typical input current, T_j = 25 ˚C. $I_I = f(V_{BG})$; condition V_{IG} = 5 V

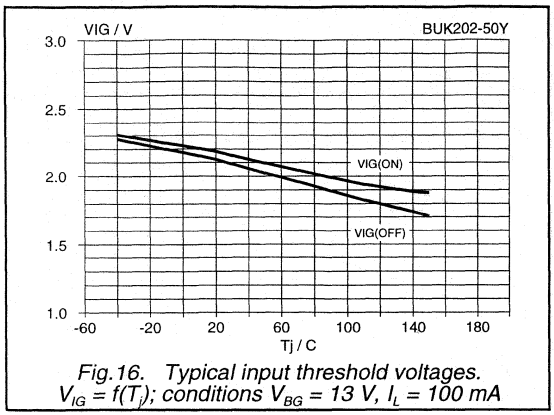


Fig.16. Typical input threshold voltages. $V_{IG} = f(T_j)$; conditions V_{BG} = 13 V, I_L = 100 mA

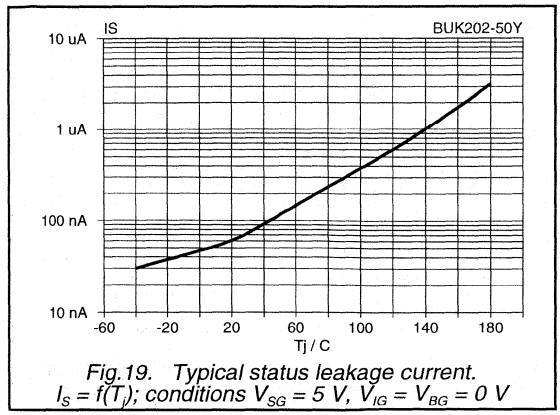


Fig.19. Typical status leakage current. $I_S = f(T_j)$; conditions V_{SG} = 5 V, $V_{IG} = V_{BG}$ = 0 V

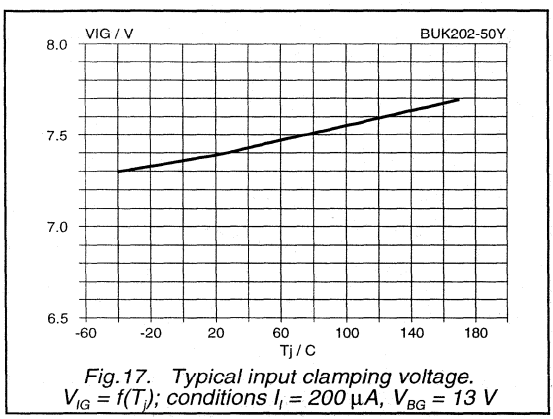


Fig.17. Typical input clamping voltage. $V_{IG} = f(T_j)$; conditions I_I = 200 µA, V_{BG} = 13 V

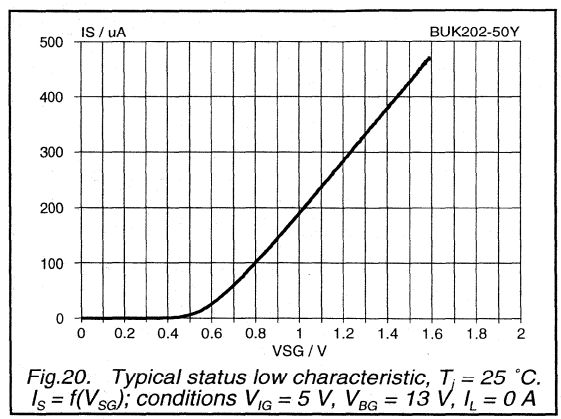


Fig.20. Typical status low characteristic, T_j = 25 °C. $I_S = f(V_{SG})$; conditions V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

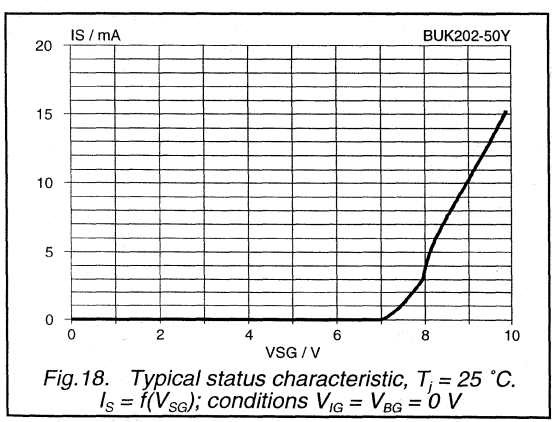


Fig.18. Typical status characteristic, T_j = 25 °C. $I_S = f(V_{SG})$; conditions $V_{IG} = V_{BG}$ = 0 V

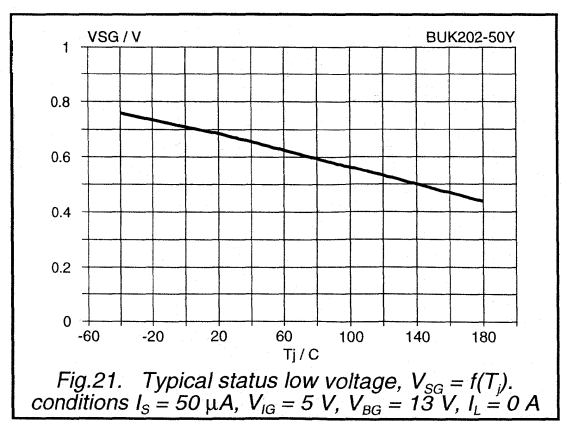


Fig.21. Typical status low voltage, $V_{SG} = f(T_j)$. conditions I_S = 50 µA, V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

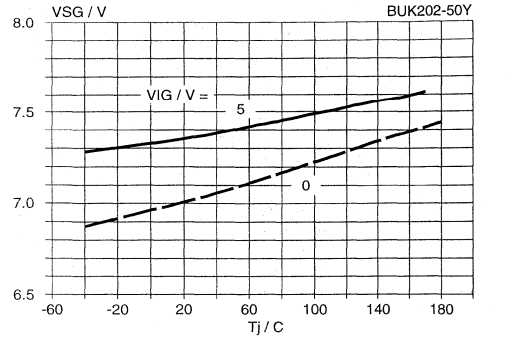


Fig.22. Typical status clamping voltage, $V_{SG} = f(T_j)$. parameter V_{IG}; conditions $I_S = 100\ \mu A$, $V_{BG} = 13\ V$

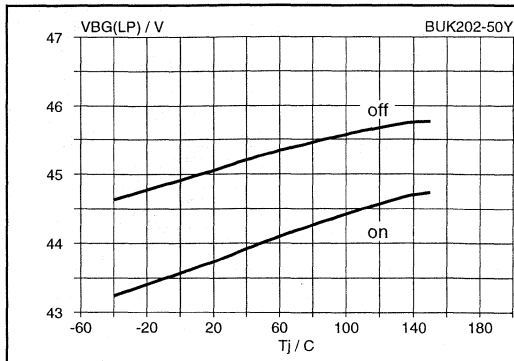


Fig.25. Supply typical overvoltage thresholds. $V_{BG(LP)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $I_L = 100\ mA$

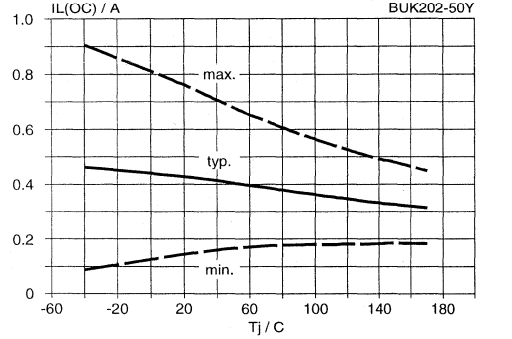


Fig.23. Low load current detection threshold. $I_{L(OC)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $V_{BG} = 13\ V$

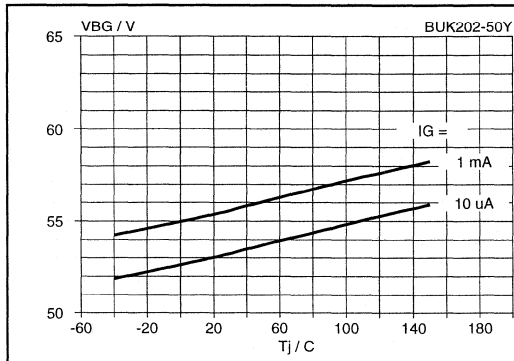


Fig.26. Typical battery to ground clamping voltage. $V_{BG} = f(T_j)$; parameter I_G

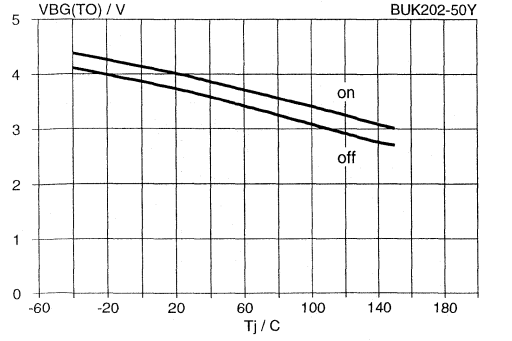


Fig.24. Supply typical undervoltage thresholds. $V_{BG(TO)} = f(T_j)$; conditions $V_{IG} = 3\ V$; $I_L = 100\ mA$

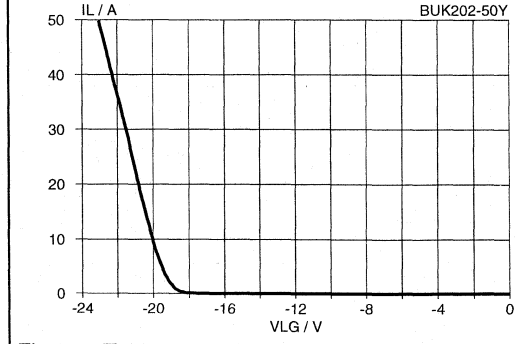


Fig.27. Typical negative load clamping characteristic. $I_L = f(V_{LG})$; conditions $V_{IG} = 0\ V$, $t_p = 300\ \mu s$, 25 ˚C

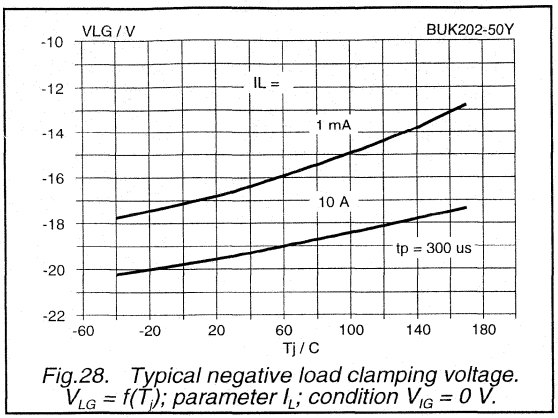


Fig.28. Typical negative load clamping voltage. $V_{LG} = f(T_j)$; parameter I_L; condition $V_{IG} = 0$ V.

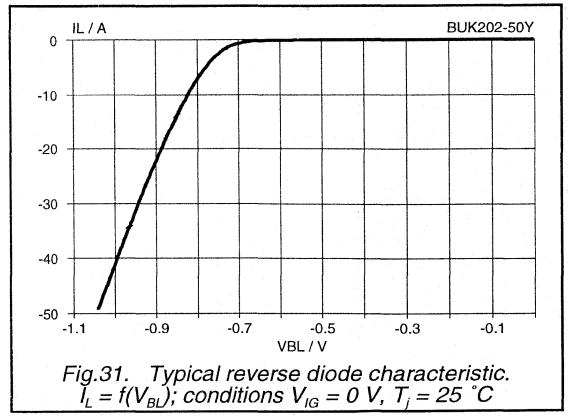


Fig.31. Typical reverse diode characteristic. $I_L = f(V_{BL})$; conditions $V_{IG} = 0$ V, $T_j = 25$ ˚C

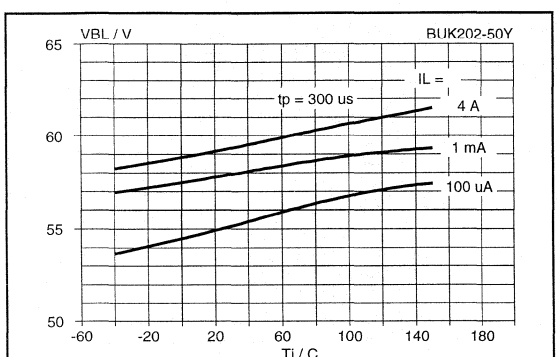


Fig.29. Typical battery to load clamping voltage. $V_{BL} = f(T_j)$; parameter I_L; condition $I_G = 5$ mA.

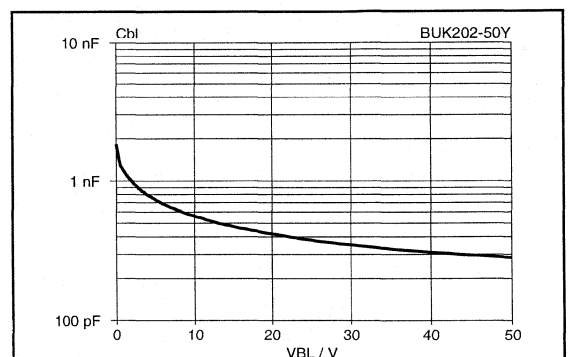


Fig.32. Typical output capacitance. $T_{mb} = 25$ ˚C $C_{bl} = f(V_{BL})$; conditions $f = 1$ MHz, $V_{IG} = 0$ V

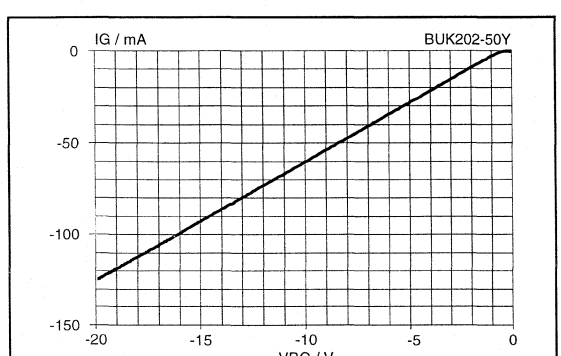


Fig.30. Typical reverse battery characteristic. $I_G = f(V_{BG})$; conditions $I_L = 0$ A, $T_j = 25$ ˚C

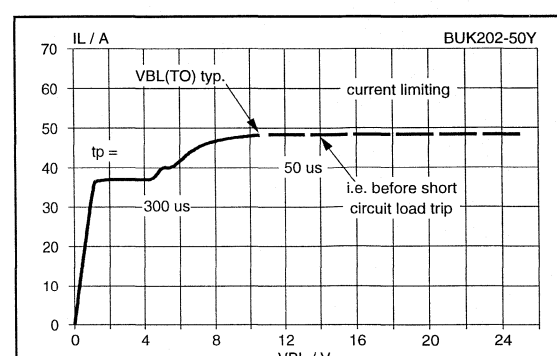


Fig.33. Typical overload characteristic, $T_{mb} = 25$ ˚C. $I_L = f(V_{BL})$; condition $V_{BG} = 13$ V; parameter t_p

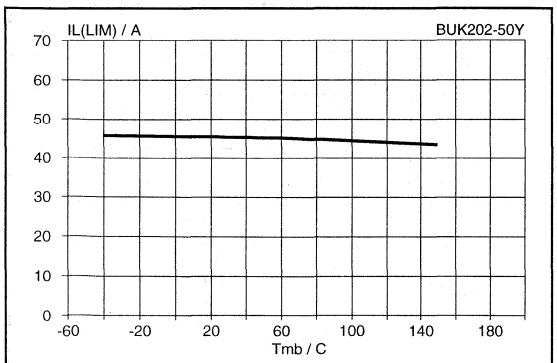


Fig.34. Typical overload current, V_{BL} = 9 V. $I_L = f(T_{mb})$; conditions V_{BG} = 13 V; t_p = 100 µs

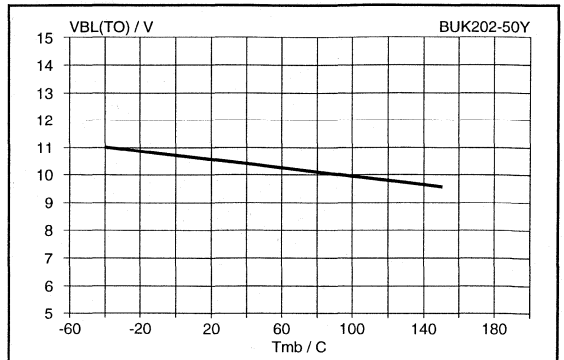


Fig.36. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(T_{mb})$; condition V_{BG} = 13 V

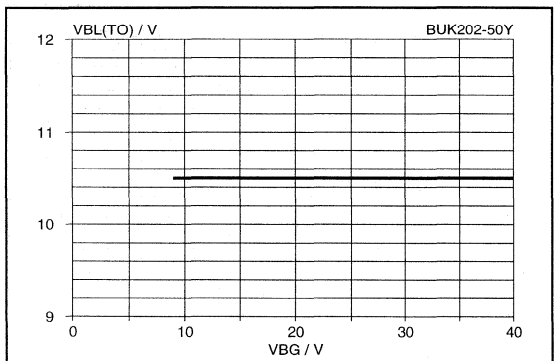


Fig.35. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(V_{BG})$; condition T_{mb} = 25 °C

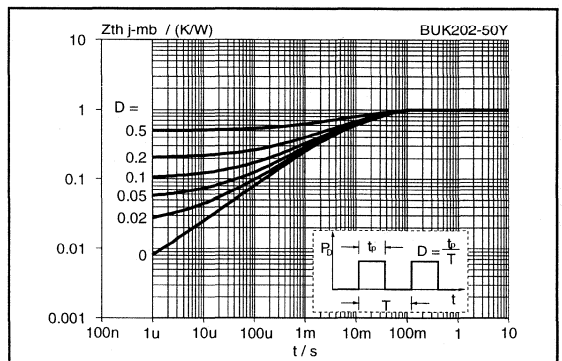


Fig.37. Transient thermal impedance. $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

PowerMOS transistor TOPFET high side switch

BUK203-50Y

For maintenance only. Do not use for design-in.

DESCRIPTION

Monolithic temperature and overload protected power switch based on MOSFET technology in a 5 pin plastic envelope, configured as a single high side switch.

APPLICATIONS

General controller for driving lamps, motors, solenoids, heaters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	UNIT
I_L	Nominal load current (ISO)	1.6	A
SYMBOL	**PARAMETER**	**MAX.**	**UNIT**
V_{BG}	Continuous off-state supply voltage	50	V
I_L	Continuous load current	4	A
T_j	Continuous junction temperature	150	°C
R_{ON}	On-state resistance	220	mΩ

FEATURES

- Vertical power DMOS switch
- Low on-state resistance
- 5 V logic compatible input
- Overtemperature protection - self resets with hysteresis
- Overload protection against short circuit load with output current limiting; latched - reset by input
- High supply voltage load protection
- Supply undervoltage lock out
- Status indication for overload protection activated
- Diagnostic status indication of open circuit load
- Very low quiescent current
- Voltage clamping for turn off of inductive loads
- ESD protection on all pins
- Reverse battery and overvoltage protection

FUNCTIONAL BLOCK DIAGRAM

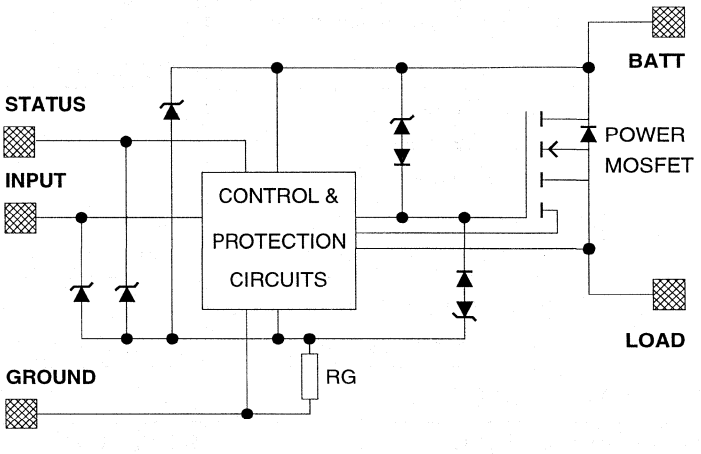


Fig.1. Elements of the TOPFET HSS with internal ground resistor.

PINNING - SOT263

PIN	DESCRIPTION
1	Ground
2	Input
3	Battery (+ve supply)
4	Status
5	Load
tab	connected to pin 3

PIN CONFIGURATION

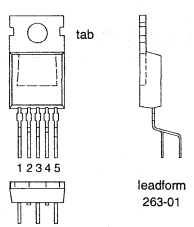


Fig. 2.

SYMBOL

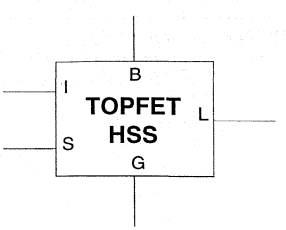


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Battery voltages				
V_{BG}	Continuous off-state supply voltage	-	0	50	V
	Reverse battery voltages[1]	External resistors:			
$-V_{BG}$	Repetitive peak supply voltage	$R_I = R_S \geq 4.7\ k\Omega$, $\delta \leq 0.1$	-	32	V
$-V_{BG}$	Continuous reverse supply voltage	$R_I = R_S \geq 4.7\ k\Omega$	-	16	V
I_L	Continuous load current	$T_{mb} \leq 110\ ^\circ C$	-	4	A
P_D	Total power dissipation	$T_{mb} \leq 25\ ^\circ C$	-	50	W
T_{stg}	Storage temperature	-	-55	175	°C
T_j	Continuous junction temperature[2]	-	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C
	Input and status				
I_I	Continuous input current	-	-5	5	mA
I_S	Continuous status current	-	-5	5	mA
I_I	Repetitive peak input current	$\delta \leq 0.1$	-20	20	mA
I_S	Repetitive peak status current	$\delta \leq 0.1$	-20	20	mA
	Inductive load clamping				
E_{BL}	Non-repetitive clamping energy	$T_{mb} = 150\ ^\circ C$ prior to turn-off	-	1.4	J

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance[3]					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	2	2.5	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	75	K/W

1 Reverse battery voltage is allowed only with external input and status resistors to limit the currents to a safe value.

2 For normal continuous operation. A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 Of the output Power MOS transistor.

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Clamping voltages					
V_{BG}	Battery to ground	I_G = 1 mA	50	55	65	V
V_{BL}	Battery to load	$I_L = I_G$ = 1 mA	50	55	65	V
$-V_{LG}$	Negative load to ground	I_L = 1 mA	12	17	21	V
	Supply voltage	battery to ground				
V_{BG}	Operating range[1]	-	5	-	40	V
	Currents	V_{BG} = 13 V				
I_L	Nominal load current[2]	V_{BL} = 0.5 V; T_{mb} = 85 °C	1.6	-	-	A
I_B	Quiescent current[3]	V_{IG} = 0 V; V_{LG} = 0 V	-	0.1	2	µA
I_G	Operating current[4]	V_{IG} = 5 V; I_L = 0 A	1.5	2.2	4	mA
I_L	Off-state load current[5]	V_{BL} = 13 V; V_{IG} = 0 V	-	0.1	1	µA
	Resistances					
R_{ON}	On-state resistance[6]	V_{BG} = 13 V; I_L = 2 A; t_p = 300 µs	-	160	220	mΩ
R_{ON}	On-state resistance	V_{BG} = 5 V; I_L = 0.5 A; t_p = 300 µs	-	225	320	mΩ
R_G	Internal ground resistance	I_G = 10 mA	-	150	-	Ω

INPUT CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_I	Input current	V_{IG} = 5 V	35	60	100	µA
V_{IG}	Input clamping voltage	I_I = 200 µA	6	7.5	8.5	V
$V_{IG(ON)}$	Input turn-on threshold voltage		-	2.1	2.7	V
$V_{IG(OFF)}$	Input turn-off threshold voltage		1.5	2	-	V

1 On-state resistance is increased if the supply voltage is less than 9 V. Refer to figure 8.

2 Defined as in ISO 10483-1.

3 This is the continuous current drawn from the battery when the input is low and includes leakage current to the load.

4 This is the continuous current drawn from the battery with no load connected, but with the input high.

5 The measured current is in the load pin only.

6 The supply and input voltage for the R_{ON} tests are continuous. The specified pulse duration t_p refers only to the applied load current.

PROTECTION FUNCTIONS AND STATUS INDICATIONS

Truth table for normal, open-circuit load and overload conditions and abnormal supply voltages.

FUNCTIONS		TRUTH TABLE			THRESHOLD			
SYMBOL	CONDITION	INPUT	STATUS	OUTPUT	MIN.	TYP.	MAX.	UNIT
	Normal on-state	1	1	1				
	Normal off-state	0	1	0				
$I_{L(OC)}$	Open circuit load[1]	1	0	1	30	90	150	mA
	Open circuit load	0	1	0				
$T_{j(TO)}$	Over temperature[2]	1	0	0	150	175	-	°C
	Over temperature[3]	0	0	0				
$V_{BL(TO)}$	Short circuit load[4]	1	0	0	9	10.5	12	V
	Short circuit load	0	1	0				
$V_{BG(TO)}$	Low supply voltage[5]	X	1	0	3	4	5	V
$V_{BG(LP)}$	High supply voltage[6]	X	1	0	40	45	50	V

For input '0' equals low, '1' equals high, 'X' equals don't care.
For status '0' equals low, '1' equals open or high.
For output switch '0' equals off, '1' equals on.

STATUS CHARACTERISTICS

T_{mb} = 25 °C.
The status output is an open drain transistor, and requires an external pull-up circuit to indicate a logic high.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SG}	Status clamping voltage	I_S = 100 µA; V_{IG} = 0 V	6	7	8	V
V_{SG}	Status low voltage	I_S = 50 µA; V_{BG} = 13 V; V_{IG} = 5 V	-	0.7	0.8	V
I_S	Status leakage current	V_{SG} = 5 V	-	0.1	1	µA
I_S	Status saturation current[7]	V_{SS} = 5 V; R_S = 0 Ω; V_{BG} = 13 V	-	5	-	mA
	Application information					
R_S	External pull-up resistor[8]	V_{SS} = 5 V	-	100	-	kΩ

1 In the on-state, the switch detects whether the load current is less than the quoted open load threshold current. This is for status indication only. Typical hysteresis equals 25 mA. The thresholds are specified for supply voltage within the normal working range.

2 After cooling below the reset temperature the switch will resume normal operation. The reset temperature is lower than the trip temperature by typically 10 °C.

3 If the overtemperature protection has operated, status remains low to indicate the overtemperature condition even if the input is taken low, providing the device has not cooled below the reset temperature.

4 After short circuit protection has operated, the input voltage must be toggled low for the switch to resume normal operation.

5 Undervoltage sensor causes the device to switch off. Typical hysteresis equals 0.7 V.

6 Overvoltage sensor causes the device to switch off to protect the load. Typical hysteresis equals 1.3 V.

7 In a fault condition with the pull-up resistor short circuited while the status transistor is conducting.

8 The pull-up resistor also protects the status pin during reverse battery conditions.

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Inductive load turn-off					
$-V_{LG}$	Negative load voltage[1]	V_{IG} = 0 V; I_L = 2 A; t_p = 300 µs	15	20	25	V
	Short circuit load protection[2]	V_{IG} = 5 V; $R_L \leq 10$ mΩ				
$t_{d\,sc}$	Response time		-	75	-	µs
I_L	Load current prior to turn-off	$t < t_{d\,sc}$	-	17	-	A
	Overload protection[3]					
$I_{L(lim)}$	Load current limiting	V_{BL} = 9 V; t_p = 300 µs	12	15	22	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C, V_{BG} = 13 V, for resistive load R_L = 13 Ω.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	During turn-on	to V_{IG} = 5 V				
$t_{d\,on}$	Delay time	to 10% V_L	-	16	-	µs
dV/dt_{on}	Rate of rise of load voltage		-	1.3	3	V/µs
t_{on}	Total switching time	to 90% V_L	-	40	-	µs
	During turn-off	to V_{IG} = 0 V				
$t_{d\,off}$	Delay time	to 90% V_L	-	20	-	µs
dV/dt_{off}	Rate of fall of load voltage		-	1.6	3	V/µs
t_{off}	Total switching time	to 10% V_L	-	35	-	µs

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz; V_{IG} = 0 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{ig}	Input capacitance	V_{BG} = 13 V	-	15	20	pF
C_{bl}	Output capacitance	$V_{BL} = V_{BG}$ = 13 V	-	120	170	pF
C_{sg}	Status capacitance	V_{SG} = 5 V	-	11	15	pF

1 For a high side switch, the load pin voltage goes negative with respect to ground during the turn-off of an inductive load. This negative voltage is clamped by the device.

2 The load current is self-limited during the response time for short circuit load protection. Response time is measured from when input goes high.

3 If the load resistance is low, but not a complete short circuit, such that the on-state voltage remains less than $V_{BL(TO)}$, the device remains in current limiting until the overtemperature protection operates.

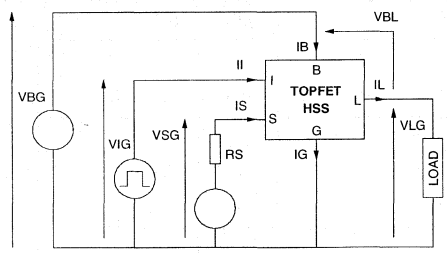


Fig.4. High side switch measurements schematic. (current and voltage conventions)

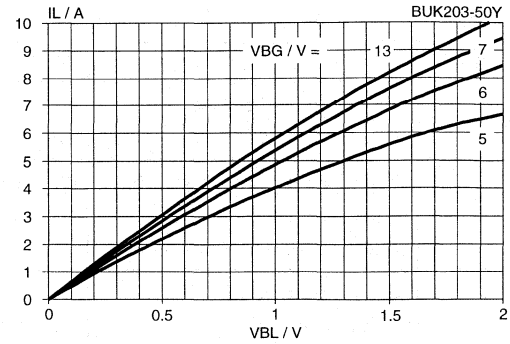


Fig.7. Typical on-state characteristics, T_j = 25 ˚C. $I_L = f(V_{BL})$; parameter V_{BG}; t_p = 250 µs

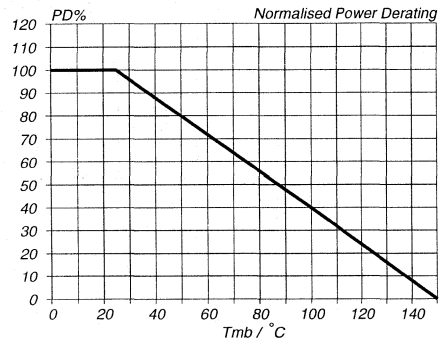


Fig.5. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

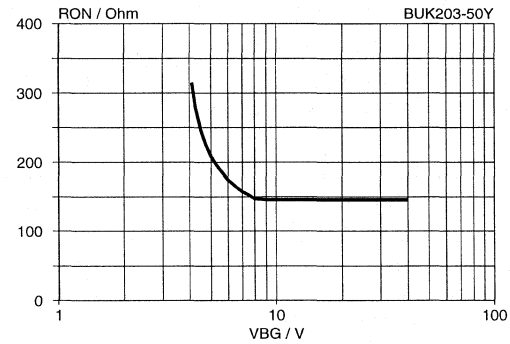


Fig.8. Typical on-state resistance, T_j = 25 ˚C. $R_{ON} = f(V_{BG})$; conditions: I_L = 2 A; t_p = 300 µs

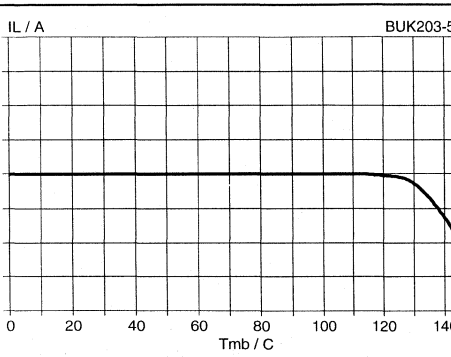


Fig.6. Limiting continuous on-state load current. $I_L = f(T_{mb})$; conditions: V_{IG} = 5 V, V_{BG} = 13 V

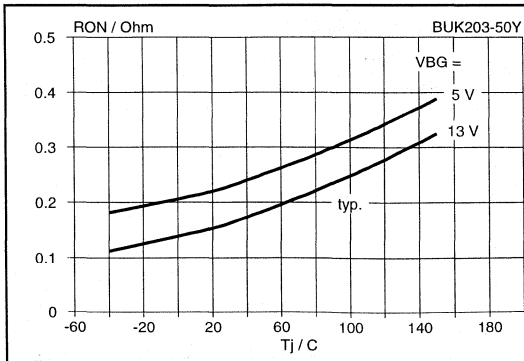


Fig.9. Typical on-state resistance, t_p = 300 µs. $R_{ON} = f(T_j)$; parameter V_{BG}; condition I_L = 0.5 A

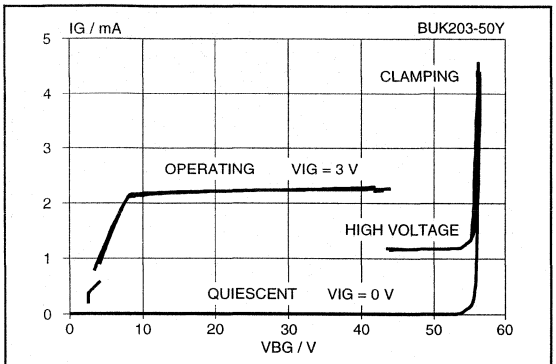


Fig.10. Typical supply characteristics, 25 °C.
$I_G = f(V_{BG})$; parameter V_{IG}

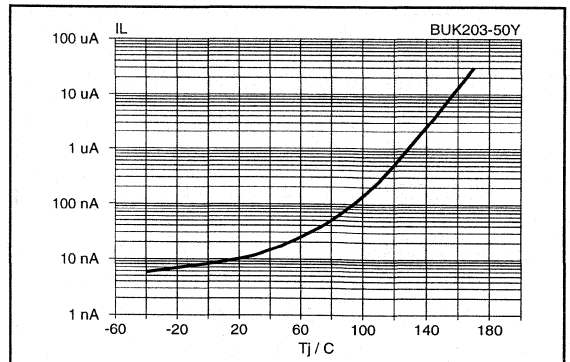


Fig.13. Typical off-state leakage current.
$I_L = f(T_j)$; conditions: V_{BL} = 13 V = V_{BG}; V_{IG} = 0 V.

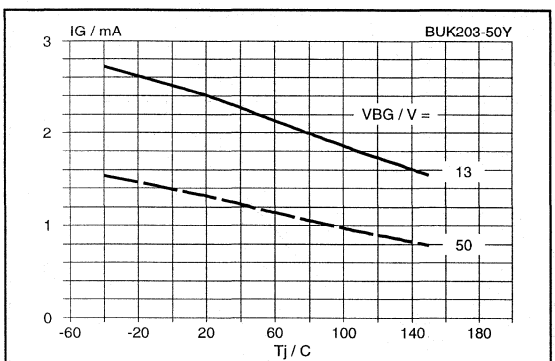


Fig.11. Typical operating supply current.
$I_G = f(T_j)$; parameter V_{BG}; condition V_{IG} = 5 V

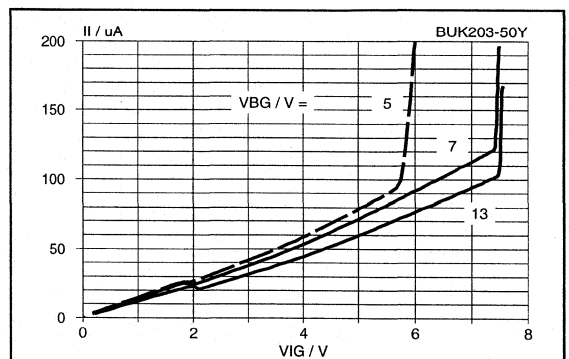


Fig.14. Typical input characteristics, T_j = 25 °C.
$I_I = f(V_{IG})$; parameter V_{BG}

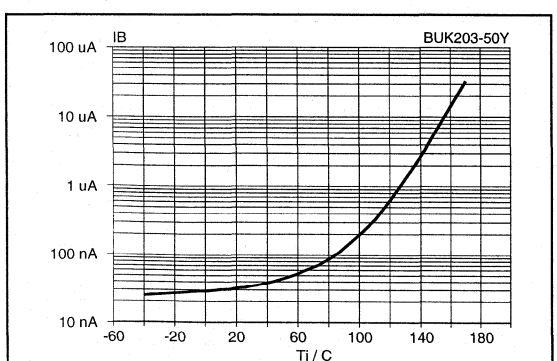


Fig.12. Typical supply quiescent current.
$I_B = f(T_j)$; condition V_{BG} = 13 V, V_{IG} = 0 V, V_{LG} = 0 V

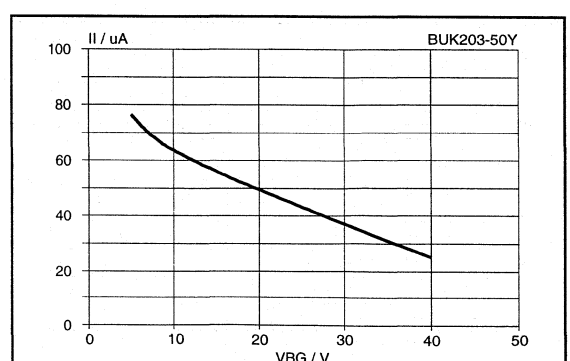


Fig.15. Typical input current, T_j = 25 °C.
$I_I = f(V_{BG})$; condition V_{IG} = 5 V

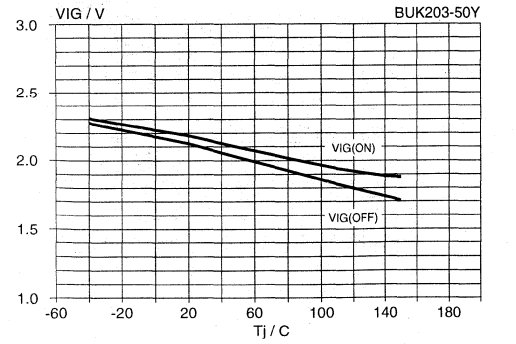


Fig.16. Typical input threshold voltages.
V_{IG} = f(T_j); conditions V_{BG} = 13 V, I_L = 100 mA

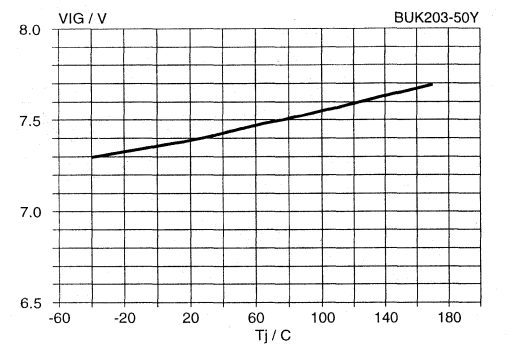


Fig.17. Typical input clamping voltage.
V_{IG} = f(T_j); conditions I_I = 200 μA, V_{BG} = 13 V

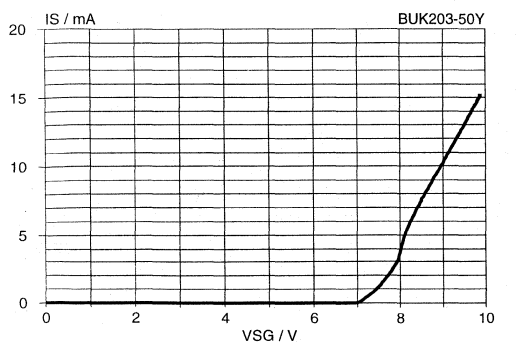


Fig.18. Typical status characteristic, T_j = 25 °C.
I_S = f(V_{SG}); conditions V_{IG} = V_{BG} = 0 V

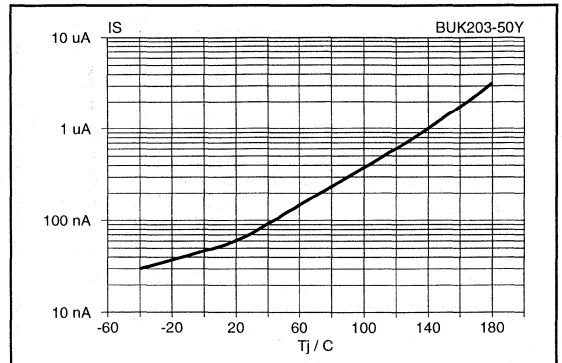


Fig.19. Typical status leakage current.
I_S = f(T_j); conditions V_{SG} = 5 V, V_{IG} = V_{BG} = 0 V

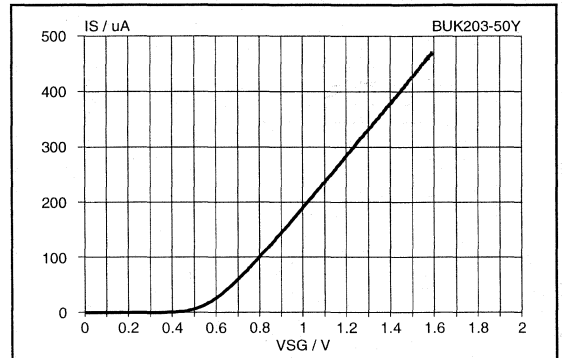


Fig.20. Typical status low characteristic, T_j = 25 °C.
I_S = f(V_{SG}); conditions V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

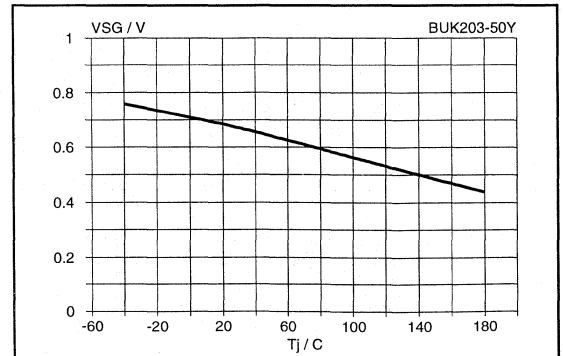


Fig.21. Typical status low voltage, V_{SG} = f(T_j).
conditions I_S = 50 μA, V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

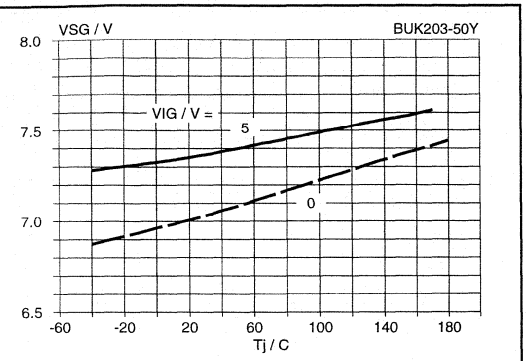


Fig.22. Typical status clamping voltage, $V_{SG} = f(T_j)$. parameter V_{IG}; conditions $I_S = 100\ \mu A$, $V_{BG} = 13\ V$

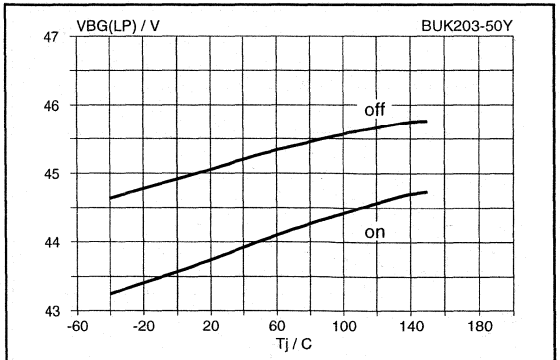


Fig.25. Supply typical overvoltage thresholds. $V_{BG(LP)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $I_L = 100\ mA$

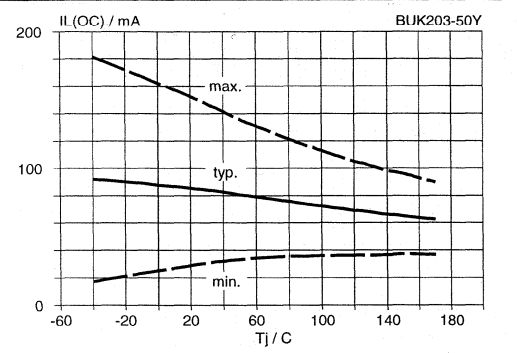


Fig.23. Low load current detection threshold. $I_{L(OC)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $V_{BG} = 13\ V$

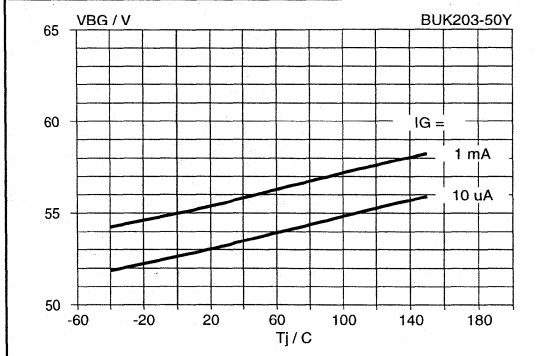


Fig.26. Typical battery to ground clamping voltage. $V_{BG} = f(T_j)$; parameter I_G

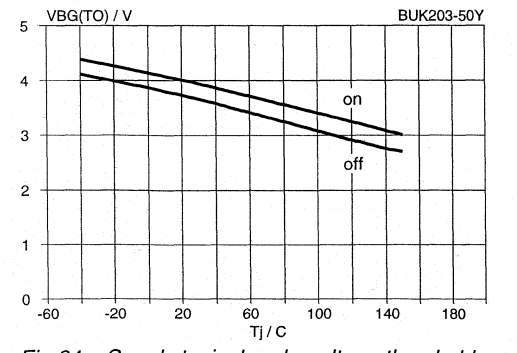


Fig.24. Supply typical undervoltage thresholds. $V_{BG(TO)} = f(T_j)$; conditions $V_{IG} = 3\ V$; $I_L = 100\ mA$

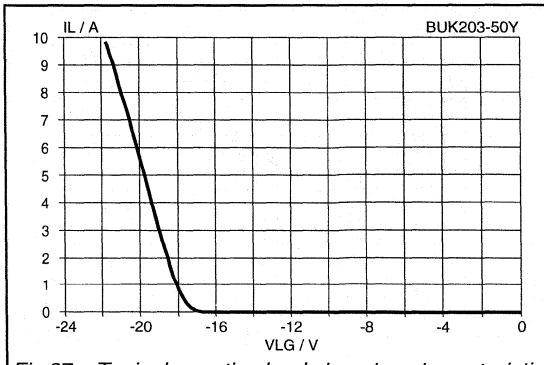


Fig.27. Typical negative load clamping characteristic. $I_L = f(V_{LG})$; conditions $V_{IG} = 0\ V$, $t_p = 300\ \mu s$, 25 °C

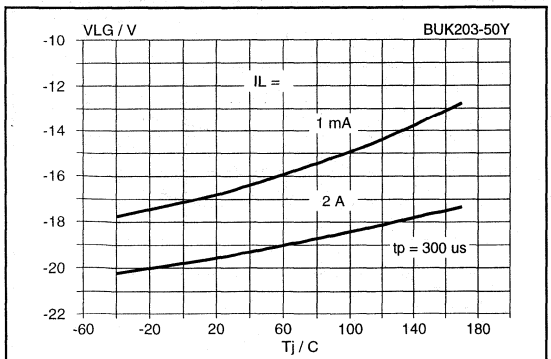


Fig.28. Typical negative load clamping voltage. $V_{LG} = f(T_j)$; parameter I_L; condition $V_{IG} = 0$ V.

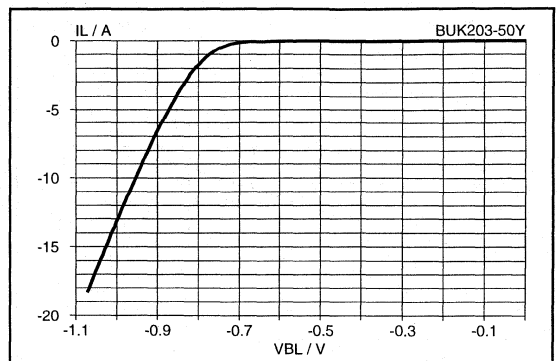


Fig.31. Typical reverse diode characteristic. $I_L = f(V_{BL})$; conditions $V_{IG} = 0$ V, $T_j = 25$ °C

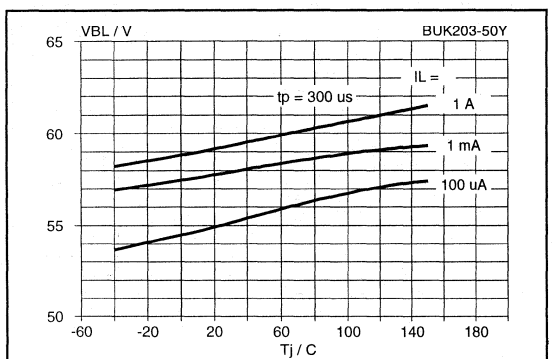


Fig.29. Typical battery to load clamping voltage. $V_{BL} = f(T_j)$; parameter I_L; condition $I_G = 5$ mA.

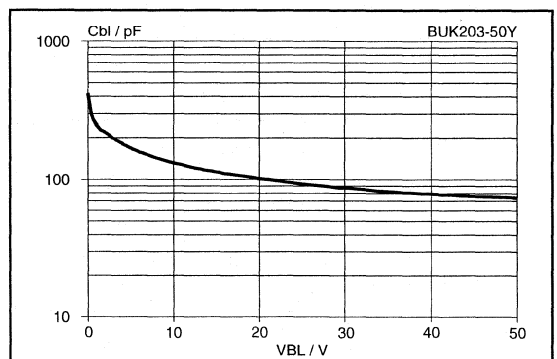


Fig.32. Typical output capacitance. $T_{mb} = 25$ °C $C_{bl} = f(V_{BL})$; conditions f = 1 MHz, $V_{IG} = 0$ V

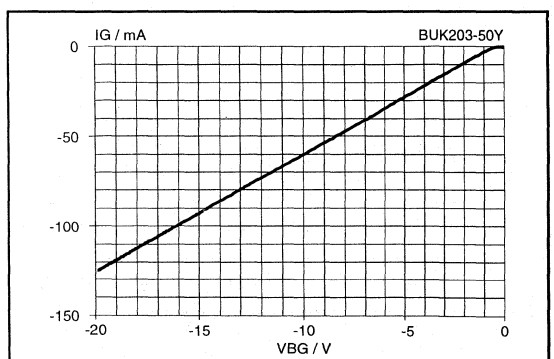


Fig.30. Typical reverse battery characteristic. $I_G = f(V_{BG})$; conditions $I_L = 0$ A, $T_j = 25$ °C

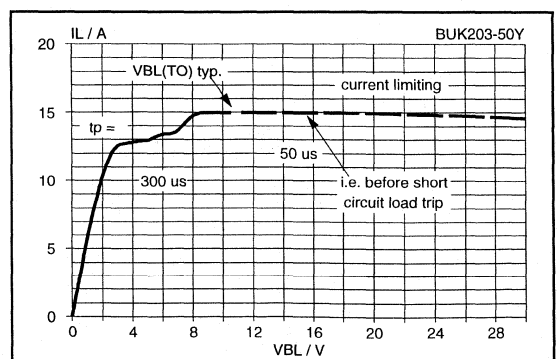


Fig.33. Typical overload characteristic, $T_{mb} = 25$ °C. $I_L = f(V_{BL})$; condition $V_{BG} = 13$ V; parameter t_p

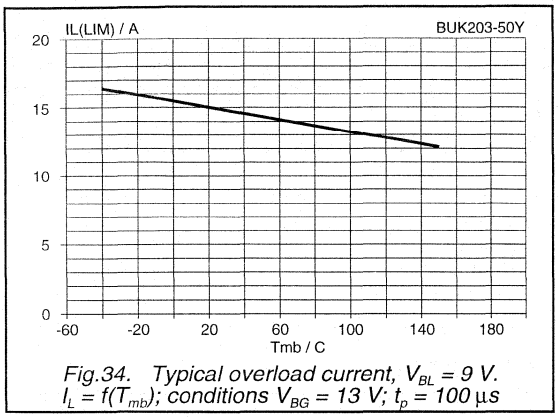


Fig.34. Typical overload current, V_{BL} = 9 V. $I_L = f(T_{mb})$; conditions V_{BG} = 13 V; t_p = 100 µs

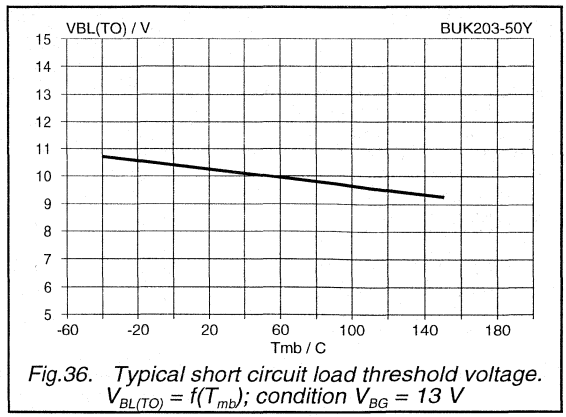


Fig.36. Typical short circuit threshold voltage. $V_{BL(TO)} = f(T_{mb})$; condition V_{BG} = 13 V

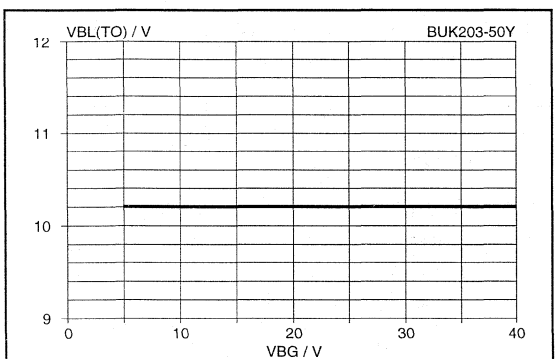


Fig.35. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(V_{BG})$; condition T_{mb} = 25 °C

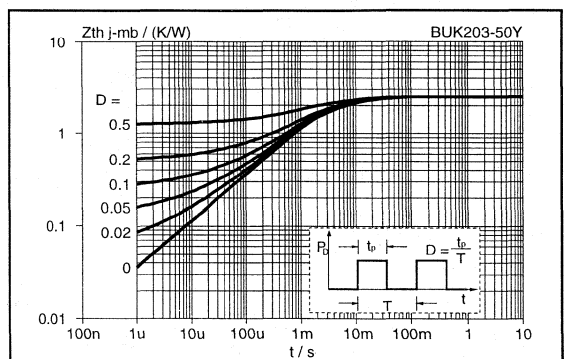


Fig.37. Transient thermal impedance. $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

TOPFET high side switch SMD version of BUK200-50Y

BUK204-50Y

For maintenance only. Do not use for design-in.

DESCRIPTION

Monolithic temperature and overload protected power switch based on MOSFET technology in a 5 pin plastic surface mount envelope, configured as a single high side switch.

APPLICATIONS

General controller for driving lamps, motors, solenoids, heaters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	UNIT
I_L	Nominal load current (ISO)	3.5	A
SYMBOL	**PARAMETER**	**MAX.**	**UNIT**
V_{BG}	Continuous off-state supply voltage	50	V
I_L	Continuous load current	10	A
T_j	Continuous junction temperature	150	°C
R_{ON}	On-state resistance	100	mΩ

FEATURES

- Vertical power DMOS switch
- Low on-state resistance
- 5 V logic compatible input
- Overtemperature protection - self resets with hysteresis
- Overload protection against short circuit load with output current limiting; latched - reset by input
- High supply voltage load protection
- Supply undervoltage lock out
- Status indication for overload protection activated
- Diagnostic status indication of open circuit load
- Very low quiescent current
- Voltage clamping for turn off of inductive loads
- ESD protection on all pins
- Reverse battery and overvoltage protection

FUNCTIONAL BLOCK DIAGRAM

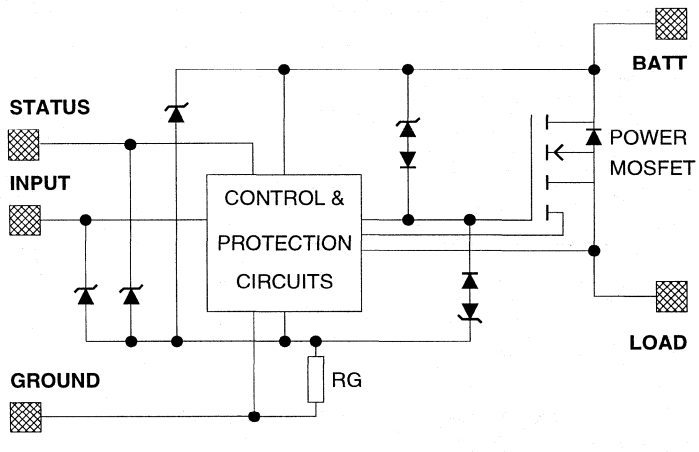


Fig.1. Elements of the TOPFET HSS with internal ground resistor.

PINNING - SOT426

PIN	DESCRIPTION
1	Ground
2	Input
3	(connected to mb)
4	Status
5	Load
mb	Battery

PIN CONFIGURATION

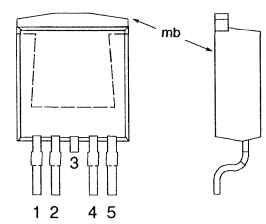


Fig. 2.

SYMBOL

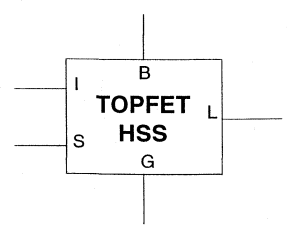


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Battery voltages				
V_{BG}	Continuous off-state supply voltage	-	0	50	V
	Reverse battery voltages[1]	External resistors:			
$-V_{BG}$	Repetitive peak supply voltage	$R_I = R_S \geq 4.7\ k\Omega$, $\delta \leq 0.1$	-	32	V
$-V_{BG}$	Continuous reverse supply voltage	$R_I = R_S \geq 4.7\ k\Omega$	-	16	V
I_L	Continuous load current	$T_{mb} \leq 115$ °C	-	10	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	62.5	W
T_{stg}	Storage temperature	-	-55	175	°C
T_j	Continuous junction temperature[2]	-	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C
	Input and status				
I_I	Continuous input current	-	-5	5	mA
I_S	Continuous status current	-	-5	5	mA
I_I	Repetitive peak input current	$\delta \leq 0.1$	-20	20	mA
I_S	Repetitive peak status current	$\delta \leq 0.1$	-20	20	mA
	Inductive load clamping				
E_{BL}	Non-repetitive clamping energy	$T_{mb} = 150$ °C prior to turn-off	-	1.2	J

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

THERMAL CHARACTERISTIC

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance[3]					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	1.5	2	K/W

1 Reverse battery voltage is allowed only with external input and status resistors to limit the currents to a safe value.

2 For normal continuous operation. A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 Of the output Power MOS transistor.

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Clamping voltages					
V_{BG}	Battery to ground	I_G = 1 mA	50	55	65	V
V_{BL}	Battery to load	$I_L = I_G$ = 1 mA	50	55	65	V
$-V_{LG}$	Negative load to ground	I_L = 1 mA	12	17	21	V
	Supply voltage	battery to ground				
V_{BG}	Operating range[1]	-	5	-	40	V
	Currents	V_{BG} = 13 V				
I_L	Nominal load current[2]	V_{BL} = 0.5 V; T_{mb} = 85 °C	3.5	-	-	A
I_B	Quiescent current[3]	V_{IG} = 0 V; V_{LG} = 0 V	-	0.1	2	µA
I_G	Operating current[4]	V_{IG} = 5 V; I_L = 0 A	1.5	2.2	4	mA
I_L	Off-state load current[5]	V_{BL} = 13 V; V_{IG} = 0 V	-	0.1	1	µA
	Resistances					
R_{ON}	On-state resistance[6]	V_{BG} = 13 V; I_L = 5 A; t_p = 300 µs	-	77	100	mΩ
R_{ON}	On-state resistance	V_{BG} = 5 V; I_L = 1 A; t_p = 300 µs	-	116	150	mΩ
R_G	Internal ground resistance	I_G = 10 mA	-	150	-	Ω

INPUT CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_I	Input current	V_{IG} = 5 V	35	60	100	µA
V_{IG}	Input clamping voltage	I_I = 200 µA	6	7.5	8.5	V
$V_{IG(ON)}$	Input turn-on threshold voltage		-	2.1	2.7	V
$V_{IG(OFF)}$	Input turn-off threshold voltage		1.5	2	-	V

1 On-state resistance is increased if the supply voltage is less than 9 V. Refer to figure 8.

2 Defined as in ISO 10483-1.

3 This is the continuous current drawn from the battery when the input is low and includes leakage current to the load.

4 This is the continuous current drawn from the battery with no load connected, but with the input high.

5 The measured current is in the load pin only.

6 The supply and input voltage for the R_{ON} tests are continuous. The specified pulse duration t_p refers only to the applied load current.

PROTECTION FUNCTIONS AND STATUS INDICATIONS

Truth table for normal, open-circuit load and overload conditions and abnormal supply voltages.

FUNCTIONS		TRUTH TABLE			THRESHOLD			
SYMBOL	CONDITION	INPUT	STATUS	OUTPUT	MIN.	TYP.	MAX.	UNIT
	Normal on-state	1	1	1				
	Normal off-state	0	1	0				
$I_{L(OC)}$	Open circuit load[1]	1	0	1	50	200	350	mA
	Open circuit load	0	1	0				
$T_{j(TO)}$	Over temperature[2]	1	0	0	150	175	-	°C
	Over temperature[3]	0	0	0				
$V_{BL(TO)}$	Short circuit load[4]	1	0	0	8.5	10.3	12	V
	Short circuit load	0	1	0				
$V_{BG(TO)}$	Low supply voltage[5]	X	1	0	3	4	5	V
$V_{BG(LP)}$	High supply voltage[6]	X	1	0	40	45	50	V

For input '0' equals low, '1' equals high, 'X' equals don't care.
For status '0' equals low, '1' equals open or high.
For output switch '0' equals off, '1' equals on.

STATUS CHARACTERISTICS

T_{mb} = 25 °C.
The status output is an open drain transistor, and requires an external pull-up circuit to indicate a logic high.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SG}	Status clamping voltage	I_S = 100 µA; V_{IG} = 0 V	6	7	8	V
V_{SG}	Status low voltage	I_S = 50 µA; V_{BG} = 13 V; V_{IG} = 5 V	-	0.7	0.8	V
I_S	Status leakage current	V_{SG} = 5 V	-	0.1	1	µA
I_S	Status saturation current[7]	V_{SS} = 5 V; R_S = 0 Ω; V_{BG} = 13 V	-	5	-	mA
	Application information					
R_S	External pull-up resistor[8]	V_{SS} = 5 V	-	100	-	kΩ

1 In the on-state, the switch detects whether the load current is less than the quoted open load threshold current. This is for status indication only. Typical hysteresis equals 80 mA. The thresholds are specified for supply voltage within the normal working range.

2 After cooling below the reset temperature the switch will resume normal operation. The reset temperature is lower than the trip temperature by typically 10 °C.

3 If the overtemperature protection has operated, status remains low to indicate the overtemperature condition even if the input is taken low, providing the device has not cooled below the reset temperature.

4 After short circuit protection has operated, the input voltage must be toggled low for the switch to resume normal operation.

5 Undervoltage sensor causes the device to switch off. Typical hysteresis equals 0.7 V.

6 Overvoltage sensor causes the device to switch off to protect the load. Typical hysteresis equals 1.3 V.

7 In a fault condition with the pull-up resistor short circuited while the status transistor is conducting.

8 The pull-up resistor also protects the status pin during reverse battery conditions.

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Inductive load turn-off					
$-V_{LG}$	Negative load voltage[1]	V_{IG} = 0 V; I_L = 5 A; t_p = 300 µs	15	20	25	V
	Short circuit load protection[2]	V_{IG} = 5 V; $R_L \leq$ 10 mΩ				
$t_{d\,sc}$	Response time		-	90	-	µs
I_L	Load current prior to turn-off	$t < t_{d\,sc}$	-	35	-	A
	Overload protection[3]					
$I_{L(lim)}$	Load current limiting	V_{BL} = 8.5 V; t_p = 300 µs	23	33	43	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C, V_{BG} = 13 V, for resistive load R_L = 13 Ω.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	During turn-on	to V_{IG} = 5 V				
$t_{d\,on}$	Delay time	to 10% V_L	-	16	-	µs
dV/dt_{on}	Rate of rise of load voltage		-	1	2.5	V/µs
t_{on}	Total switching time	to 90% V_L	-	40	-	µs
	During turn-off	to V_{IG} = 0 V				
$t_{d\,off}$	Delay time	to 90% V_L	-	30	-	µs
dV/dt_{off}	Rate of fall of load voltage		-	1.2	2.5	V/µs
t_{off}	Total switching time	to 10% V_L	-	50	-	µs

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz; V_{IG} = 0 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{ig}	Input capacitance	V_{BG} = 13 V	-	15	20	pF
C_{bl}	Output capacitance	V_{BL} = V_{BG} = 13 V	-	330	460	pF
C_{sg}	Status capacitance	V_{SG} = 5 V	-	11	15	pF

1 For a high side switch, the load pin voltage goes negative with respect to ground during the turn-off of an inductive load. This negative voltage is clamped by the device.

2 The load current is self-limited during the response time for short circuit load protection. Response time is measured from when input goes high.

3 If the load resistance is low, but not a complete short circuit, such that the on-state voltage remains less than $V_{BL(TO)}$, the device remains in current limiting until the overtemperature protection operates.

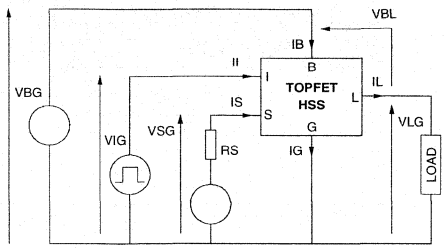


Fig.4. High side switch measurements schematic. (current and voltage conventions)

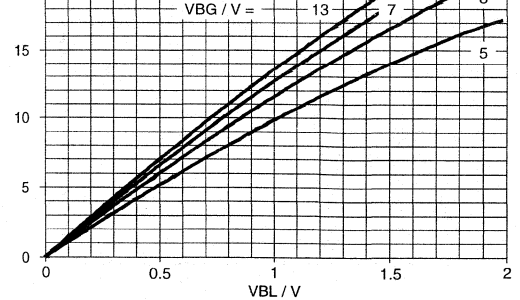


Fig.7. Typical on-state characteristics, T_j = 25 ˚C. $I_L = f(V_{BL})$; parameter V_{BG}; t_p = 250 µs

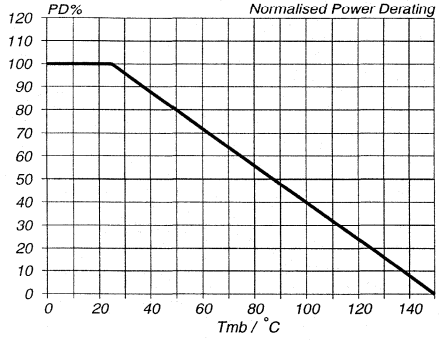


Fig.5. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

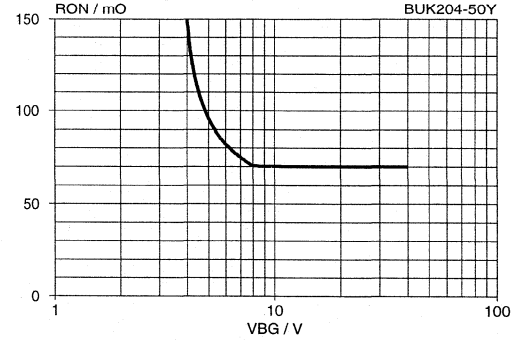


Fig.8. Typical on-state resistance, T_j = 25 ˚C. $R_{ON} = f(V_{BG})$; conditions: I_L = 5 A; t_p = 300 µs

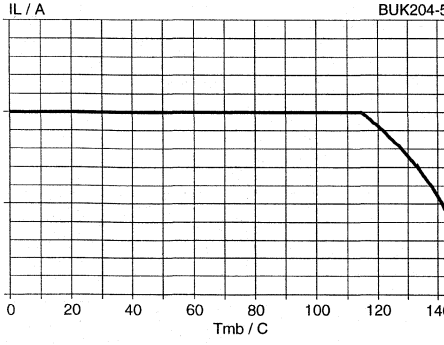


Fig.6. Limiting continuous on-state load current. $I_L = f(T_{mb})$; conditions: V_{IG} = 5 V, V_{BG} = 13 V

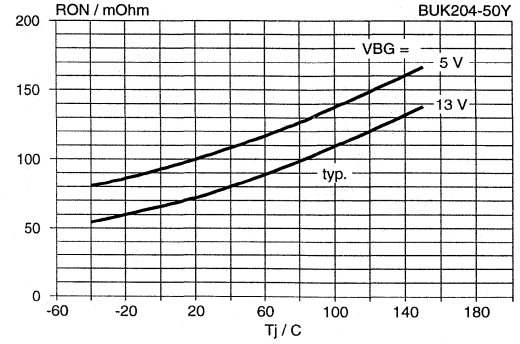


Fig.9. Typical on-state resistance, t_p = 300 µs. $R_{ON} = f(T_j)$; parameter V_{BG}; condition I_L = 1 A

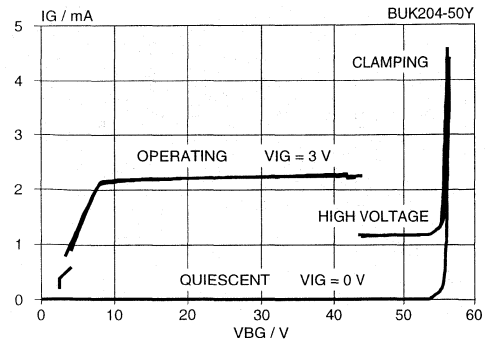


Fig.10. Typical supply characteristics, 25 ˚C.
$I_G = f(V_{BG})$; parameter V_{IG}

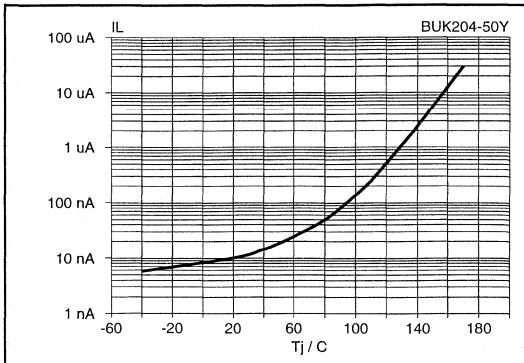


Fig.13. Typical off-state leakage current.
$I_L = f(T_j)$; conditions: V_{BL} = 13 V = V_{BG}; V_{IG} = 0 V.

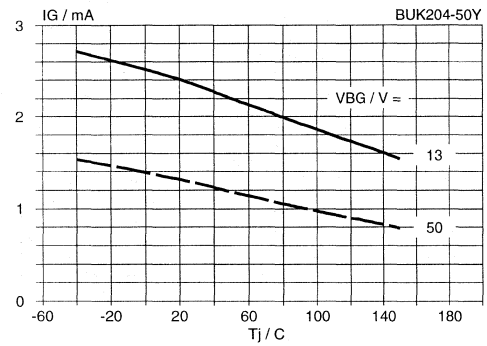


Fig.11. Typical operating supply current.
$I_G = f(T_j)$; parameter V_{BG}; condition V_{IG} = 5 V

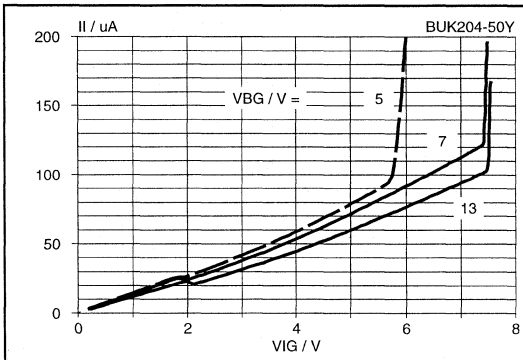


Fig.14. Typical input characteristics, T_j = 25 ˚C.
$I_I = f(V_{IG})$; parameter V_{BG}

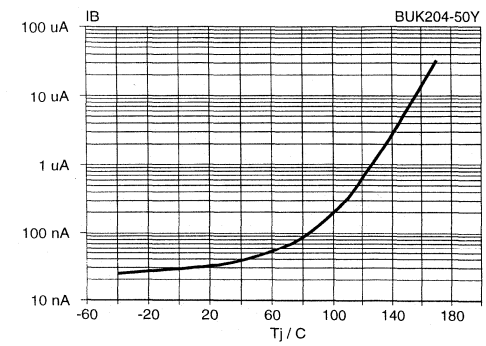


Fig.12. Typical supply quiescent current.
$I_B = f(T_j)$; condition V_{BG} = 13 V, V_{IG} = 0 V, V_{LG} = 0 V

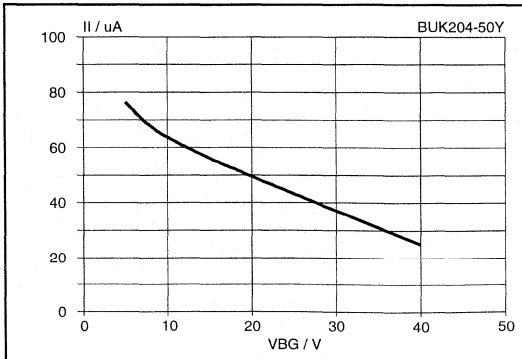


Fig.15. Typical input current, T_j = 25 ˚C.
$I_I = f(V_{BG})$; condition V_{IG} = 5 V

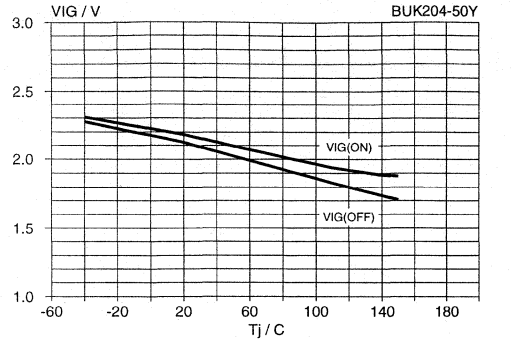


Fig.16. Typical input threshold voltages.
$V_{IG} = f(T_j)$; conditions V_{BG} = 13 V, I_L = 50 mA

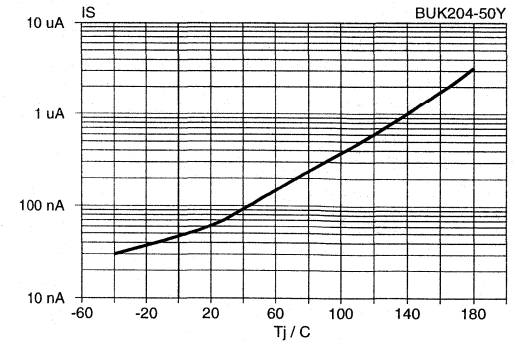


Fig.19. Typical status leakage current.
$I_S = f(T_j)$; conditions V_{SG} = 5 V, $V_{IG} = V_{BG}$ = 0 V

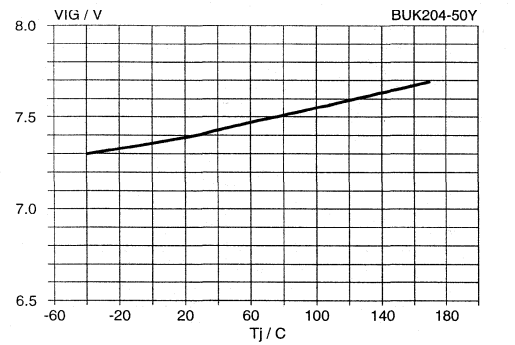


Fig.17. Typical input clamping voltage.
$V_{IG} = f(T_j)$; conditions I_I = 200 µA, V_{BG} = 13 V

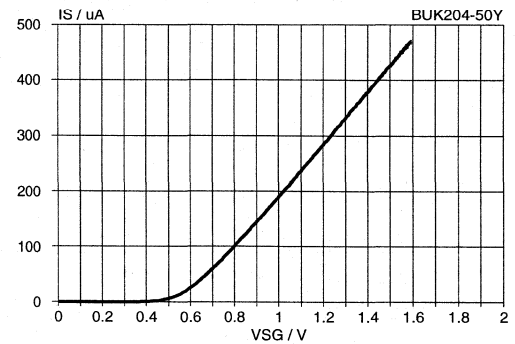


Fig.20. Typical status low characteristic, T_j = 25 ˚C.
$I_S = f(V_{SG})$; conditions V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

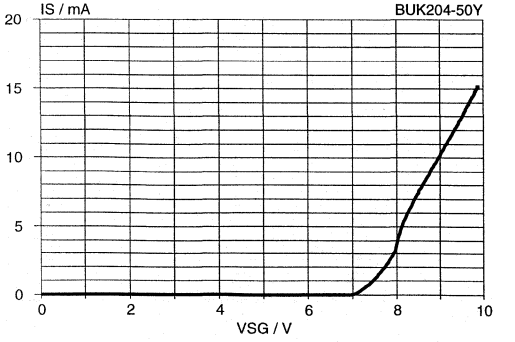


Fig.18. Typical status characteristic, T_j = 25 ˚C.
$I_S = f(V_{SG})$; conditions $V_{IG} = V_{BG}$ = 0 V

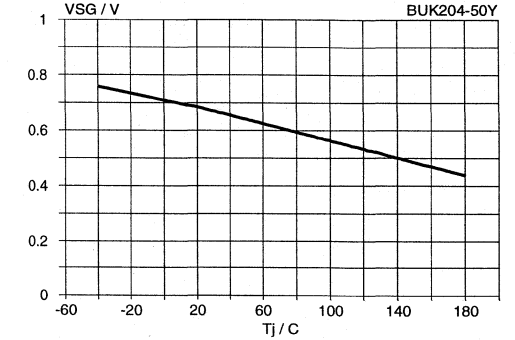


Fig.21. Typical status low voltage, $V_{SG} = f(T_j)$.
conditions I_S = 50 µA, V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

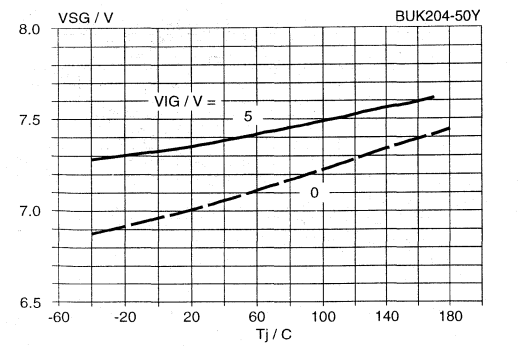


Fig.22. Typical status clamping voltage, $V_{SG} = f(T_j)$. parameter V_{IG}; conditions $I_S = 100\ \mu A$, $V_{BG} = 13\ V$

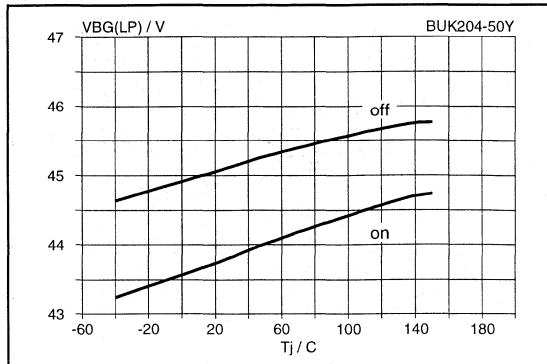


Fig.25. Supply typical overvoltage thresholds. $V_{BG(LP)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $I_L = 50\ mA$

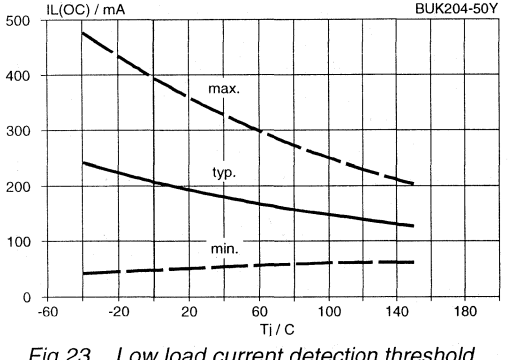


Fig.23. Low load current detection threshold. $I_{L(OC)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $V_{BG} = 13\ V$

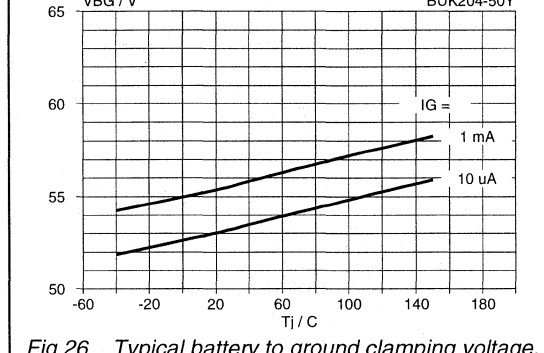


Fig.26. Typical battery to ground clamping voltage. $V_{BG} = f(T_j)$; parameter I_G

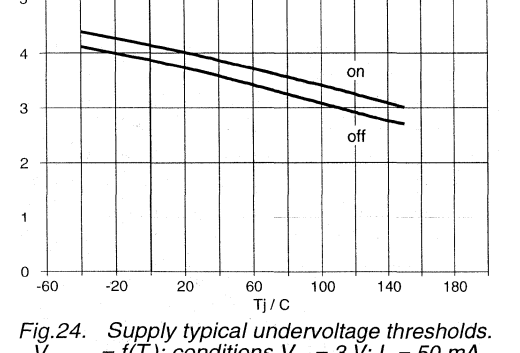


Fig.24. Supply typical undervoltage thresholds. $V_{BG(TO)} = f(T_j)$; conditions $V_{IG} = 3\ V$; $I_L = 50\ mA$

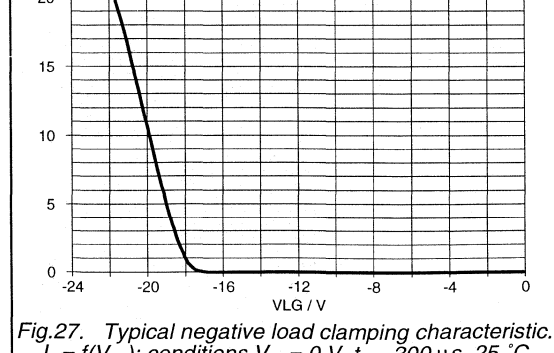


Fig.27. Typical negative load clamping characteristic. $I_L = f(V_{LG})$; conditions $V_{IG} = 0\ V$, $t_p = 300\ \mu s$, 25 °C

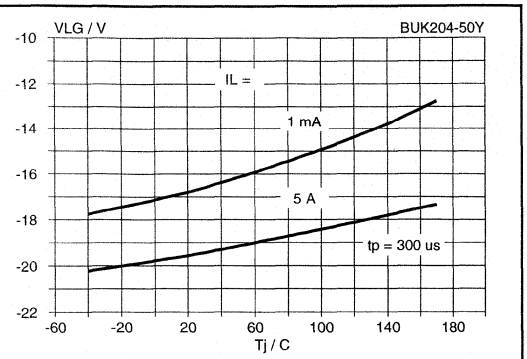


Fig.28. Typical negative load clamping voltage. $V_{LG} = f(T_j)$; parameter I_L; condition $V_{IG} = 0$ V.

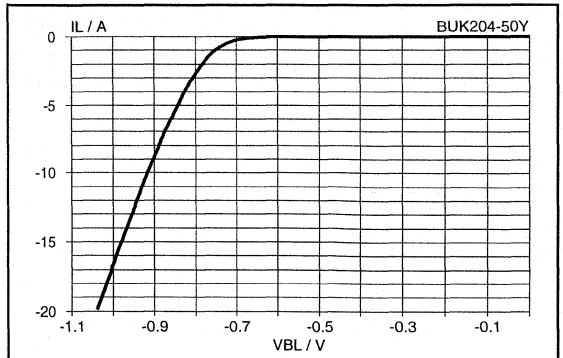


Fig.31. Typical reverse diode characteristic. $I_L = f(V_{BL})$; conditions $V_{IG} = 0$ V, $T_j = 25$ °C

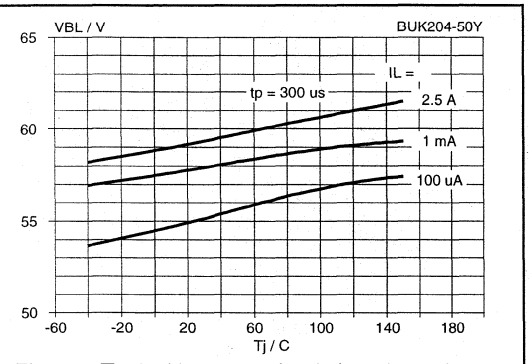


Fig.29. Typical battery to load clamping voltage. $V_{BL} = f(T_j)$; parameter I_L; condition $I_G = 5$ mA.

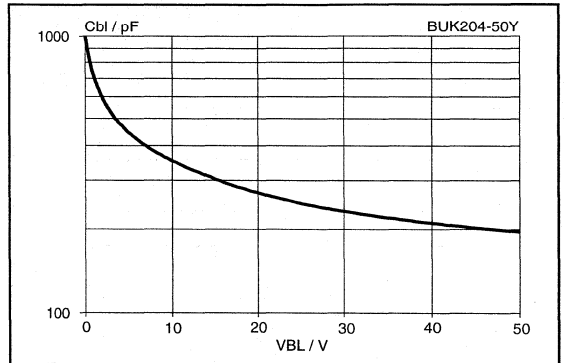


Fig.32. Typical output capacitance. $T_{mb} = 25$ °C $C_{bl} = f(V_{BL})$; conditions f = 1 MHz, $V_{IG} = 0$ V

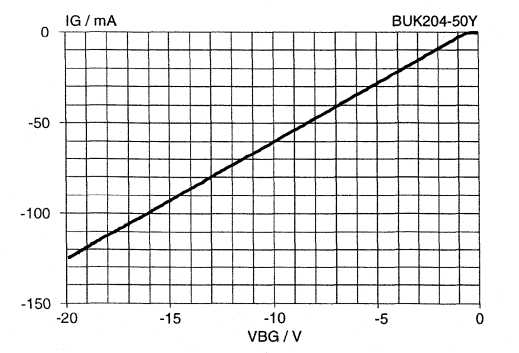


Fig.30. Typical reverse battery characteristic. $I_G = f(V_{BG})$; conditions $I_L = 0$ A, $T_j = 25$ °C

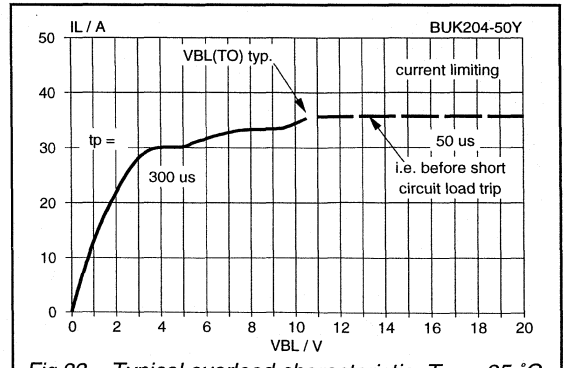


Fig.33. Typical overload characteristic, $T_{mb} = 25$ °C. $I_L = f(V_{BL})$; condition $V_{BG} = 13$ V; parameter t_p

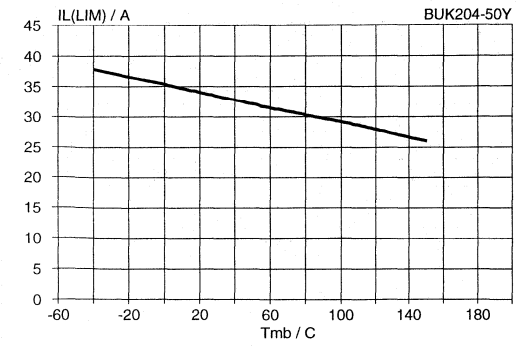


Fig.34. Typical overload current, V_{BL} = 8.5 V. $I_L = f(T_{mb})$; conditions V_{BG} = 13 V; t_p = 300 µs

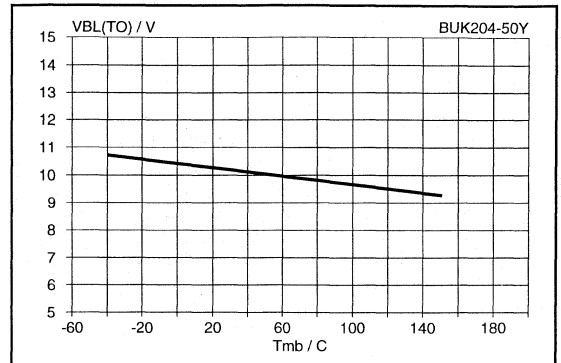


Fig.36. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(T_{mb})$; condition V_{BG} = 13 V

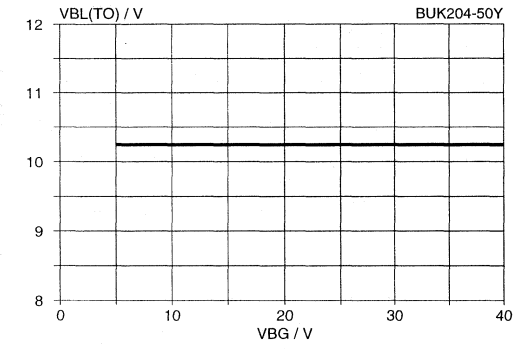


Fig.35. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(V_{BG})$; condition T_{mb} = 25 °C

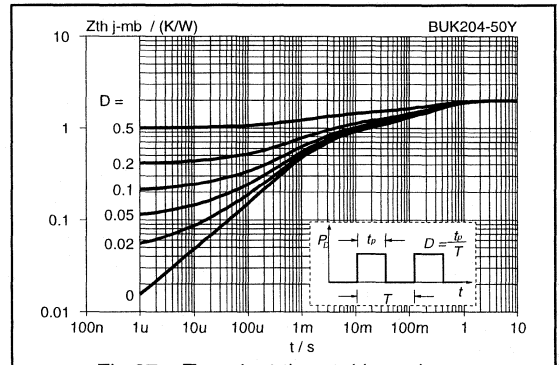


Fig.37. Transient thermal impedance. $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

TOPFET high side switch SMD version of BUK201-50Y

BUK205-50Y

For maintenance only. Do not use for design-in.

DESCRIPTION

Monolithic temperature and overload protected power switch based on MOSFET technology in a 5 pin plastic surface mount envelope, configured as a single high side switch.

APPLICATIONS

General controller for driving lamps, motors, solenoids, heaters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	UNIT
I_L	Nominal load current (ISO)	6	A
SYMBOL	**PARAMETER**	**MAX.**	**UNIT**
V_{BG}	Continuous off-state supply voltage	50	V
I_L	Continuous load current	15	A
T_j	Continuous junction temperature	150	°C
R_{ON}	On-state resistance	60	mΩ

FEATURES

- Vertical power DMOS switch
- Low on-state resistance
- 5 V logic compatible input
- Overtemperature protection - self resets with hysteresis
- Overload protection against short circuit load with output current limiting; latched - reset by input
- High supply voltage load protection
- Supply undervoltage lock out
- Status indication for overload protection activated
- Diagnostic status indication of open circuit load
- Very low quiescent current
- Voltage clamping for turn off of inductive loads
- ESD protection on all pins
- Reverse battery and overvoltage protection

FUNCTIONAL BLOCK DIAGRAM

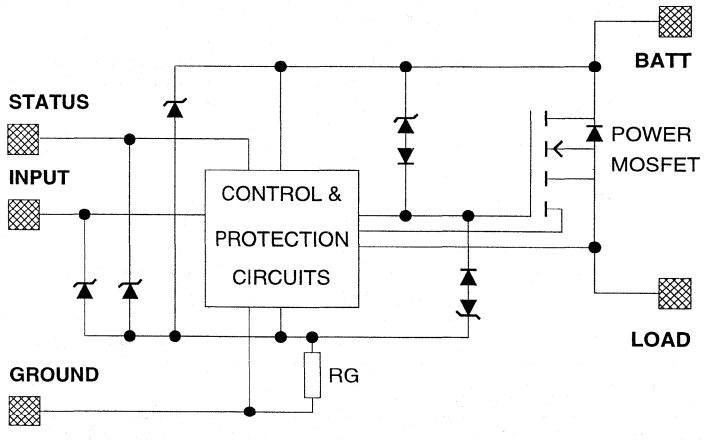


Fig.1. Elements of the TOPFET HSS with internal ground resistor.

PINNING - SOT426

PIN	DESCRIPTION
1	Ground
2	Input
3	(connected to mb)
4	Status
5	Load
mb	Battery

PIN CONFIGURATION

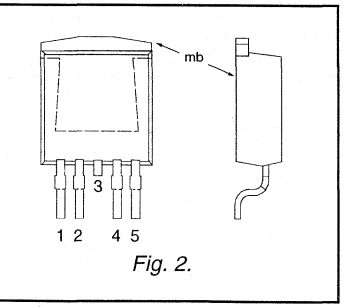


Fig. 2.

SYMBOL

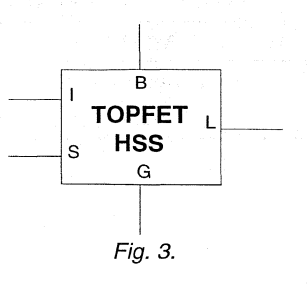


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Battery voltages				
V_{BG}	Continuous off-state supply voltage	-	0	50	V
	Reverse battery voltages[1]	External resistors:			
$-V_{BG}$	Repetitive peak supply voltage	$R_I = R_S \geq 4.7\ k\Omega$, $\delta \leq 0.1$	-	32	V
$-V_{BG}$	Continuous reverse supply voltage	$R_I = R_S \geq 4.7\ k\Omega$	-	16	V
I_L	Continuous load current	$T_{mb} \leq 115\ ^\circ C$	-	15	A
P_D	Total power dissipation	$T_{mb} \leq 25\ ^\circ C$	-	83.3	W
T_{stg}	Storage temperature	-	-55	175	°C
T_j	Continuous junction temperature[2]	-	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C
	Input and status				
I_I	Continuous input current	-	-5	5	mA
I_S	Continuous status current	-	-5	5	mA
I_I	Repetitive peak input current	$\delta \leq 0.1$	-20	20	mA
I_S	Repetitive peak status current	$\delta \leq 0.1$	-20	20	mA
	Inductive load clamping				
E_{BL}	Non-repetitive clamping energy	$T_{mb} = 150\ ^\circ C$ prior to turn-off	-	1.2	J

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

THERMAL CHARACTERISTIC

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance[3]					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	1.2	1.5	K/W

1 Reverse battery voltage is allowed only with external input and status resistors to limit the currents to a safe value.

2 For normal continuous operation. A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 Of the output Power MOS transistor.

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Clamping voltages					
V_{BG}	Battery to ground	I_G = 1 mA	50	55	65	V
V_{BL}	Battery to load	$I_L = I_G$ = 1 mA	50	55	65	V
$-V_{LG}$	Negative load to ground	I_L = 1 mA	12	17	21	V
	Supply voltage	battery to ground				
V_{BG}	Operating range[1]	-	5	-	40	V
	Currents	V_{BG} = 13 V				
I_L	Nominal load current[2]	V_{BL} = 0.5 V; T_{mb} = 85 °C	6	-	-	A
I_B	Quiescent current[3]	V_{IG} = 0 V; V_{LG} = 0 V	-	0.1	2	µA
I_G	Operating current[4]	V_{IG} = 5 V; I_L = 0 A	1.5	2.2	4	mA
I_L	Off-state load current[5]	V_{BL} = 13 V; V_{IG} = 0 V	-	0.1	1	µA
	Resistances					
R_{ON}	On-state resistance[6]	V_{BG} = 13 V; I_L = 7.5 A; t_p = 300 µs	-	45	60	mΩ
R_{ON}	On-state resistance	V_{BG} = 5 V; I_L = 1.5 A; t_p = 300 µs	-	70	90	mΩ
R_G	Internal ground resistance	I_G = 10 mA	-	150	-	Ω

INPUT CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_I	Input current	V_{IG} = 5 V	35	60	100	µA
V_{IG}	Input clamping voltage	I_I = 200 µA	6	7.5	8.5	V
$V_{IG(ON)}$	Input turn-on threshold voltage		-	2.1	2.7	V
$V_{IG(OFF)}$	Input turn-off threshold voltage		1.5	2	-	V

1 On-state resistance is increased if the supply voltage is less than 9 V. Refer to figure 8.
2 Defined as in ISO 10483-1.
3 This is the continuous current drawn from the battery when the input is low and includes leakage current to the load.
4 This is the continuous current drawn from the battery with no load connected, but with the input high.
5 The measured current is in the load pin only.
6 The supply and input voltage for the R_{ON} tests are continuous. The specified pulse duration t_p refers only to the applied load current.

PROTECTION FUNCTIONS AND STATUS INDICATIONS

Truth table for normal, open-circuit load and overload conditions and abnormal supply voltages.

FUNCTIONS		TRUTH TABLE			THRESHOLD			
SYMBOL	CONDITION	INPUT	STATUS	OUTPUT	MIN.	TYP.	MAX.	UNIT
	Normal on-state	1	1	1				
	Normal off-state	0	1	0				
$I_{L(OC)}$	Open circuit load[1]	1	0	1	100	350	600	mA
	Open circuit load	0	1	0				
$T_{j(TO)}$	Over temperature[2]	1	0	0	150	175	-	°C
	Over temperature[3]	0	0	0				
$V_{BL(TO)}$	Short circuit load[4]	1	0	0	9	10.5	12	V
	Short circuit load	0	1	0				
$V_{BG(TO)}$	Low supply voltage[5]	X	1	0	3	4	5	V
$V_{BG(LP)}$	High supply voltage[6]	X	1	0	40	45	50	V

For input '0' equals low, '1' equals high, 'X' equals don't care.
For status '0' equals low, '1' equals open or high.
For output switch '0' equals off, '1' equals on.

STATUS CHARACTERISTICS

T_{mb} = 25 °C.
The status output is an open drain transistor, and requires an external pull-up circuit to indicate a logic high.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SG}	Status clamping voltage	I_S = 100 µA; V_{IG} = 0 V	6	7	8	V
V_{SG}	Status low voltage	I_S = 50 µA; V_{BG} = 13 V; V_{IG} = 5 V	-	0.7	0.8	V
I_S	Status leakage current	V_{SG} = 5 V	-	0.1	1	µA
I_S	Status saturation current[7]	V_{SS} = 5 V; R_S = 0 Ω; V_{BG} = 13 V	-	5	-	mA
	Application information					
R_S	External pull-up resistor[8]	V_{SS} = 5 V	-	100	-	kΩ

1 In the on-state, the switch detects whether the load current is less than the quoted open load threshold current. This is for status indication only. Typical hysteresis equals 140 mA. The thresholds are specified for supply voltage within the normal working range.

2 After cooling below the reset temperature the switch will resume normal operation. The reset temperature is lower than the trip temperature by typically 10 °C.

3 If the overtemperature protection has operated, status remains low to indicate the overtemperature condition even if the input is taken low, providing the device has not cooled below the reset temperature.

4 After short circuit protection has operated, the input voltage must be toggled low for the switch to resume normal operation.

5 Undervoltage sensor causes the device to switch off. Typical hysteresis equals 0.7 V.

6 Overvoltage sensor causes the device to switch off to protect the load. Typical hysteresis equals 1.3 V.

7 In a fault condition with the pull-up resistor short circuited while the status transistor is conducting.

8 The pull-up resistor also protects the status pin during reverse battery conditions.

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Inductive load turn-off					
$-V_{LG}$	Negative load voltage[1]	V_{IG} = 0 V; I_L = 7.5 A; t_p = 300 µs	15	20	25	V
	Short circuit load protection[2]	V_{IG} = 5 V; $R_L \leq$ 10 mΩ				
$t_{d\,sc}$	Response time		-	90	-	µs
I_L	Load current prior to turn-off	$t < t_{d\,sc}$	-	42	-	A
	Overload protection[3]					
$I_{L(lim)}$	Load current limiting	V_{BL} = 9 V; t_p = 300 µs	28	40	52	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C, V_{BG} = 13 V, for resistive load R_L = 13 Ω.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	During turn-on	to V_{IG} = 5 V				
$t_{d\,on}$	Delay time	to 10% V_L	-	16	-	µs
dV/dt_{on}	Rate of rise of load voltage		-	1	2.5	V/µs
t_{on}	Total switching time	to 90% V_L	-	40	-	µs
	During turn-off	to V_{IG} = 0 V				
$t_{d\,off}$	Delay time	to 90% V_L	-	30	-	µs
dV/dt_{off}	Rate of fall of load voltage		-	1.2	2.5	V/µs
t_{off}	Total switching time	to 10% V_L	-	50	-	µs

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz; V_{IG} = 0 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{ig}	Input capacitance	V_{BG} = 13 V	-	15	20	pF
C_{bl}	Output capacitance	$V_{BL} = V_{BG}$ = 13 V	-	415	580	pF
C_{sg}	Status capacitance	V_{SG} = 5 V	-	11	15	pF

1 For a high side switch, the load pin voltage goes negative with respect to ground during the turn-off of an inductive load. This negative voltage is clamped by the device.

2 The load current is self-limited during the response time for short circuit load protection. Response time is measured from when input goes high.

3 If the load resistance is low, but not a complete short circuit, such that the on-state voltage remains less than $V_{BL(TO)}$, the device remains in current limiting until the overtemperature protection operates.

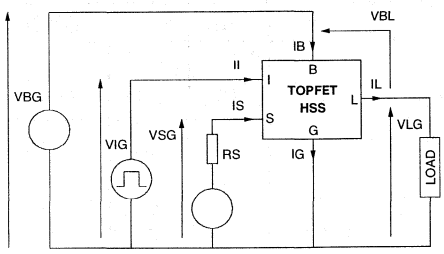


Fig.4. High side switch measurements schematic. (current and voltage conventions)

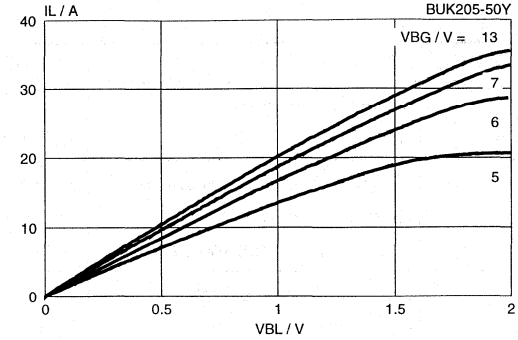


Fig.7. Typical on-state characteristics, T_j = 25 ˚C. $I_L = f(V_{BL})$; parameter V_{BG}; t_p = 250 µs

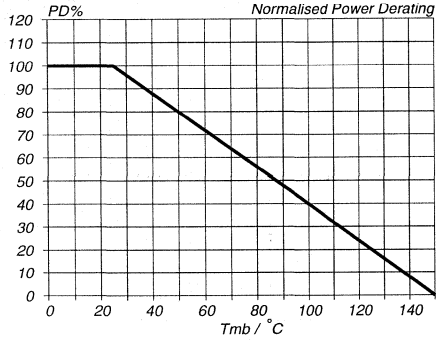


Fig.5. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

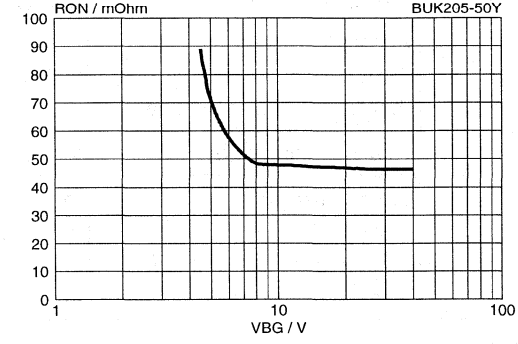


Fig.8. Typical on-state resistance, T_j = 25 ˚C. $R_{ON} = f(V_{BG})$; conditions: I_L = 7.5 A; t_p = 300 µs

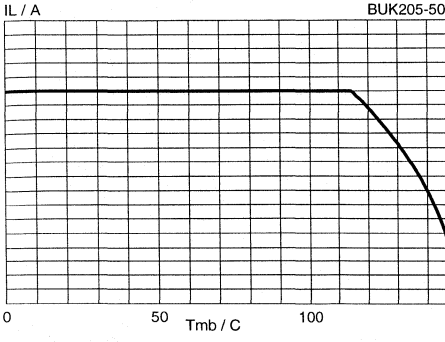


Fig.6. Limiting continuous on-state load current. $I_L = f(T_{mb})$; conditions: V_{IG} = 5 V, V_{BG} = 13 V

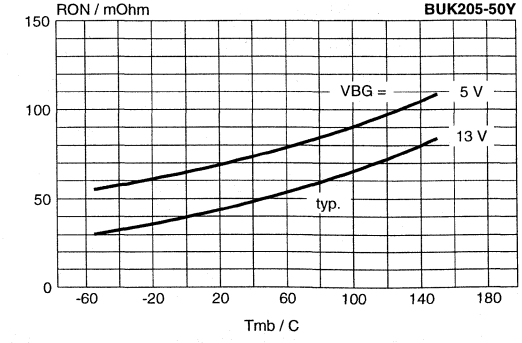


Fig.9. Typical on-state resistance, t_p = 300 µs. $R_{ON} = f(T_j)$; parameter V_{BG}; condition I_L = 1.5 A

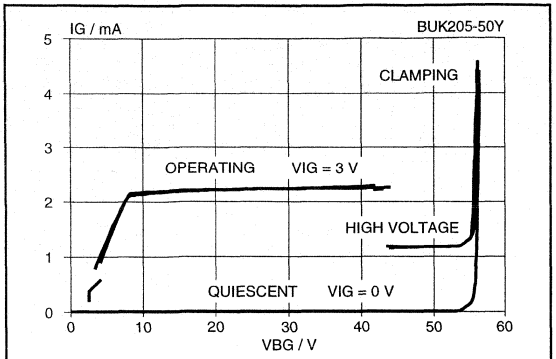


Fig.10. Typical supply characteristics, 25 ˚C.
$I_G = f(V_{BG})$; parameter V_{IG}

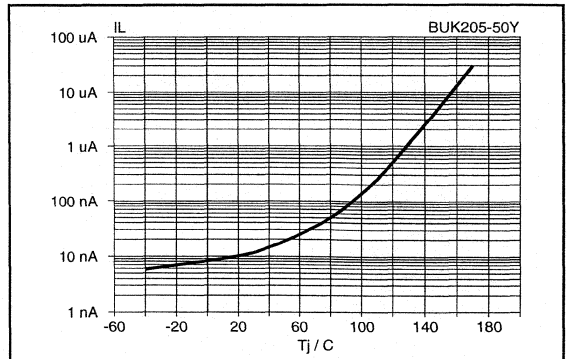


Fig.13. Typical off-state leakage current.
$I_L = f(T_j)$; conditions: V_{BL} = 13 V = V_{BG}; V_{IG} = 0 V.

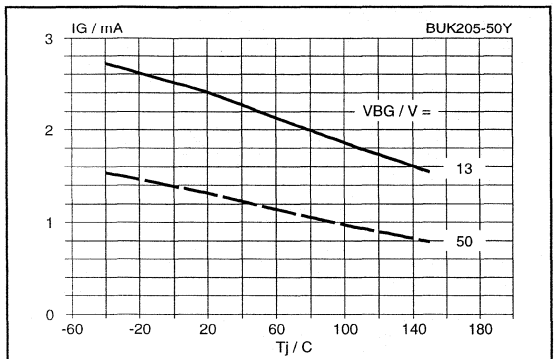


Fig.11. Typical operating supply current.
$I_G = f(T_j)$; parameter V_{BG}; condition V_{IG} = 5 V

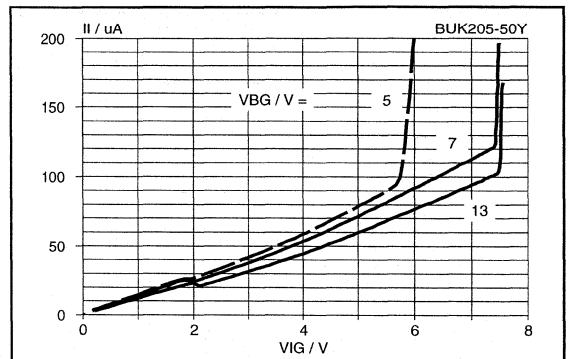


Fig.14. Typical input characteristics, T_j = 25 ˚C.
$I_I = f(V_{IG})$; parameter V_{BG}

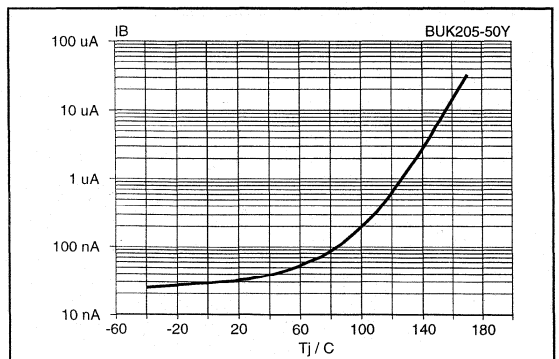


Fig.12. Typical supply quiescent current.
$I_B = f(T_j)$; condition V_{BG} = 13 V, V_{IG} = 0 V, V_{LG} = 0 V

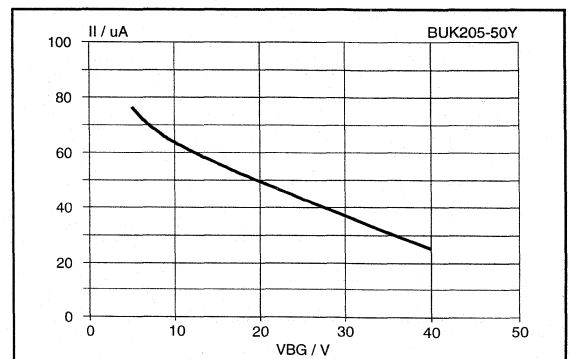


Fig.15. Typical input current, T_j = 25 ˚C.
$I_I = f(V_{BG})$; condition V_{IG} = 5 V

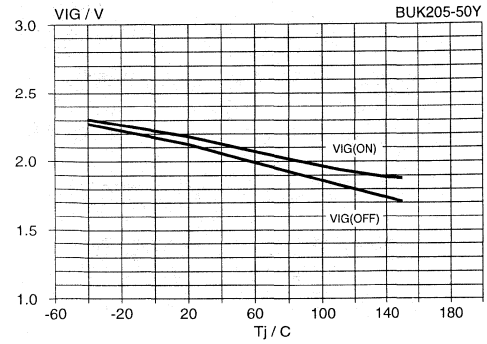


Fig.16. Typical input threshold voltages. $V_{IG} = f(T_j)$; conditions V_{BG} = 13 V, I_L = 80 mA

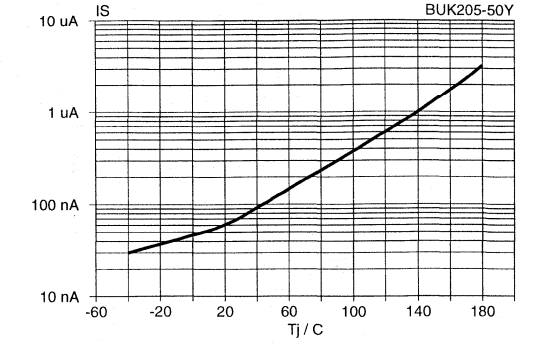


Fig.19. Typical status leakage current. $I_S = f(T_j)$; conditions V_{SG} = 5 V, $V_{IG} = V_{BG}$ = 0 V

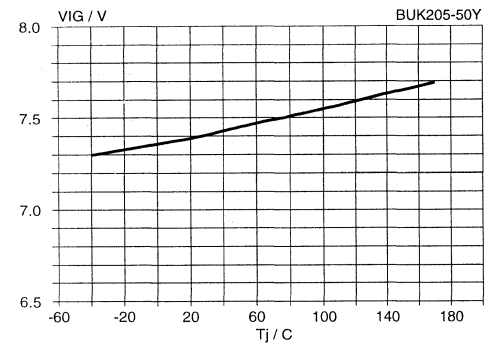


Fig.17. Typical input clamping voltage. $V_{IG} = f(T_j)$; conditions I_I = 200 µA, V_{BG} = 13 V

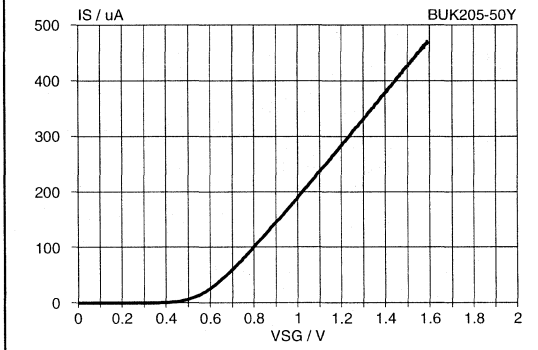


Fig.20. Typical status low characteristic, T_j = 25 °C. $I_S = f(V_{SG})$; conditions V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

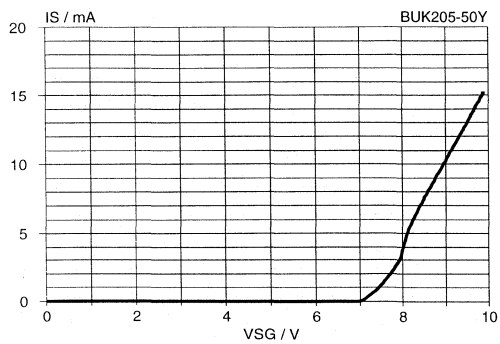


Fig.18. Typical status characteristic, T_j = 25 °C. $I_S = f(V_{SG})$; conditions $V_{IG} = V_{BG}$ = 0 V

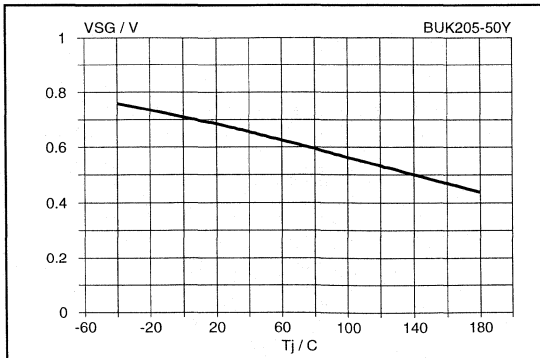


Fig.21. Typical status low voltage, $V_{SG} = f(T_j)$. conditions I_S = 50 µA, V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

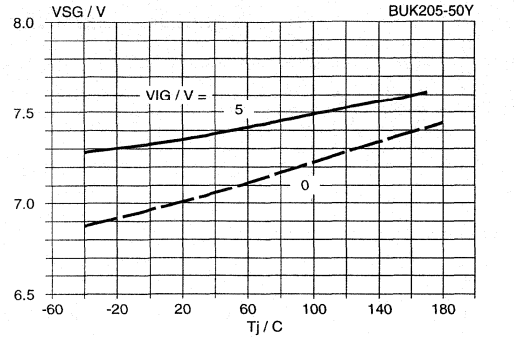


Fig.22. Typical status clamping voltage, $V_{SG} = f(T_j)$. parameter V_{IG}; conditions $I_S = 100\ \mu A$, $V_{BG} = 13\ V$

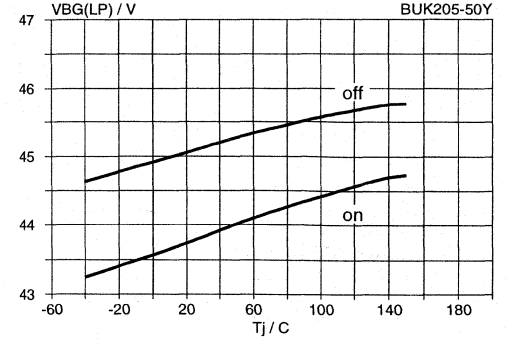


Fig.25. Supply typical overvoltage thresholds. $V_{BG(LP)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $I_L = 80\ mA$

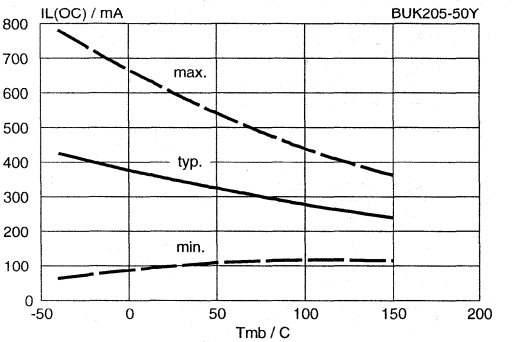


Fig.23. Low load current detection threshold. $I_{L(OC)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $V_{BG} = 13\ V$

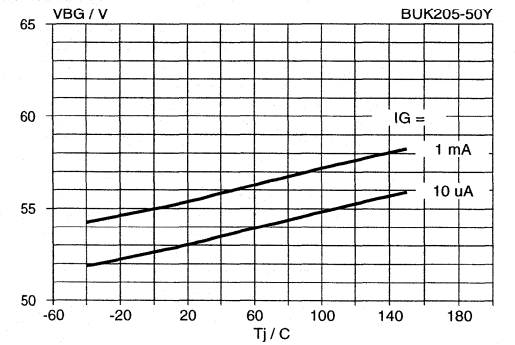


Fig.26. Typical battery to ground clamping voltage. $V_{BG} = f(T_j)$; parameter I_G

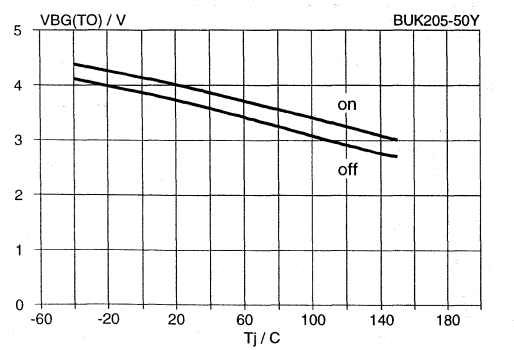


Fig.24. Supply typical undervoltage thresholds. $V_{BG(TO)} = f(T_j)$; conditions $V_{IG} = 3\ V$; $I_L = 80\ mA$

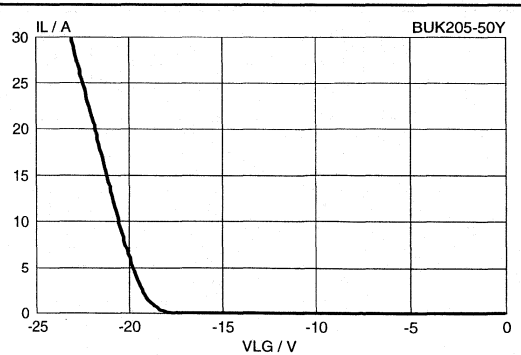


Fig.27. Typical negative load clamping characteristic. $I_L = f(V_{LG})$; conditions $V_{IG} = 0\ V$, $t_p = 300\ \mu s$, 25 °C

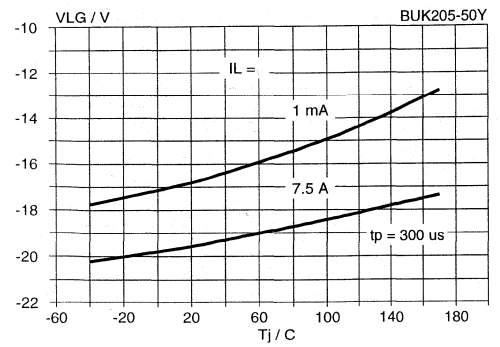


Fig.28. Typical negative load clamping voltage. $V_{LG} = f(T_j)$; parameter I_L; condition $V_{IG} = 0$ V.

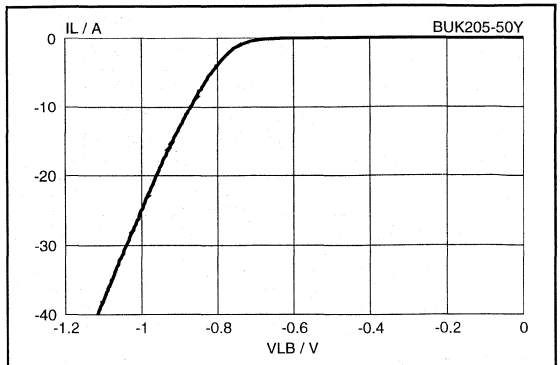


Fig.31. Typical reverse diode characteristic. $I_L = f(V_{BL})$; conditions $V_{IG} = 0$ V, $T_j = 25$ °C

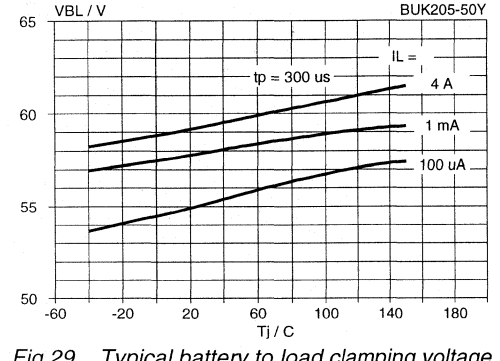


Fig.29. Typical battery to load clamping voltage. $V_{BL} = f(T_j)$; parameter I_L; condition $I_G = 5$ mA.

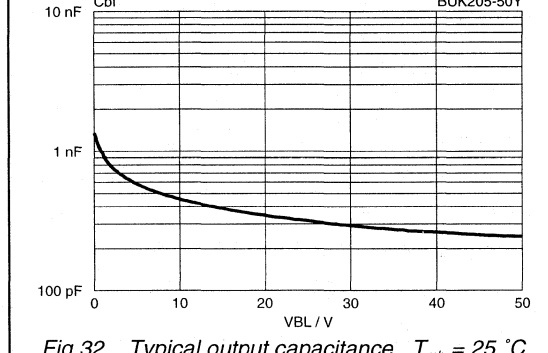


Fig.32. Typical output capacitance. $T_{mb} = 25$ °C $C_{bl} = f(V_{BL})$; conditions f = 1 MHz, $V_{IG} = 0$ V

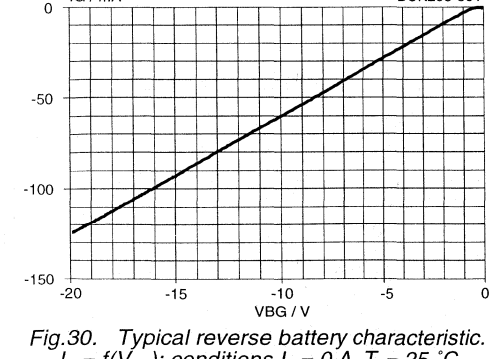


Fig.30. Typical reverse battery characteristic. $I_G = f(V_{BG})$; conditions $I_L = 0$ A, $T_j = 25$ °C

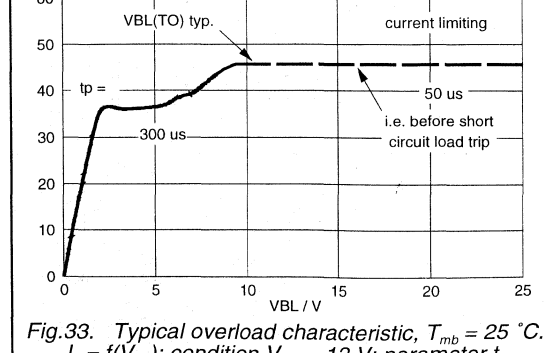


Fig.33. Typical overload characteristic, $T_{mb} = 25$ °C. $I_L = f(V_{BL})$; condition $V_{BG} = 13$ V; parameter t_p

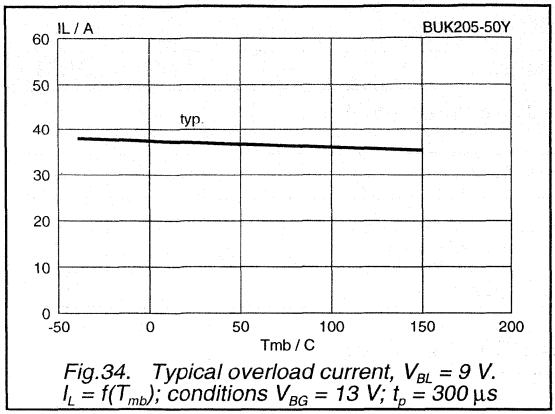


Fig.34. Typical overload current, V_{BL} = 9 V. $I_L = f(T_{mb})$; conditions V_{BG} = 13 V; t_p = 300 µs

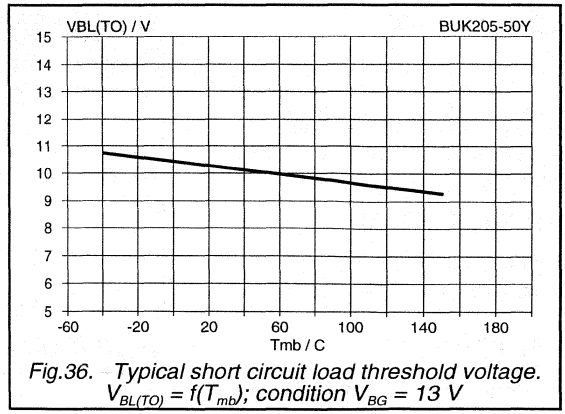


Fig.36. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(T_{mb})$; condition V_{BG} = 13 V

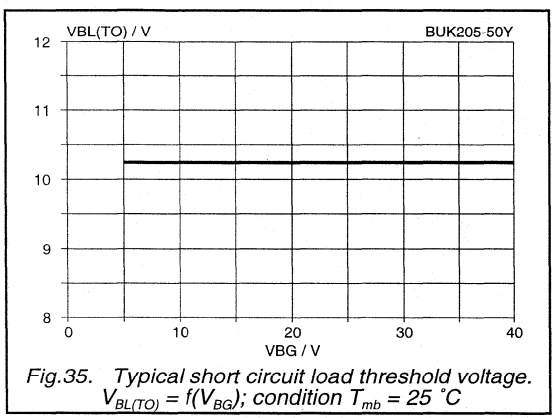


Fig.35. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(V_{BG})$; condition T_{mb} = 25 °C

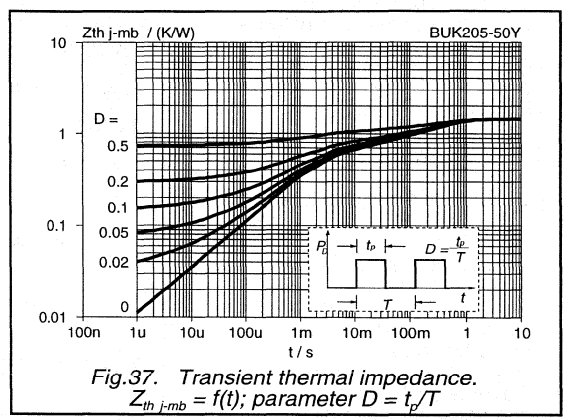


Fig.37. Transient thermal impedance. $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

TOPFET high side switch SMD version of BUK202-50Y

BUK206-50Y

For maintenance only. Do not use for design-in.

DESCRIPTION

Monolithic temperature and overload protected power switch based on MOSFET technology in a 5 pin plastic surface mount envelope, configured as a single high side switch.

APPLICATIONS

General controller for driving lamps, motors, solenoids, heaters.

FEATURES

- Vertical power DMOS switch
- Low on-state resistance
- 5 V logic compatible input
- Overtemperature protection - self resets with hysteresis
- Overload protection against short circuit load with output current limiting; latched - reset by input
- High supply voltage load protection
- Supply undervoltage lock out
- Status indication for overload protection activated
- Diagnostic status indication of open circuit load
- Very low quiescent current
- Voltage clamping for turn off of inductive loads
- ESD protection on all pins
- Reverse battery and overvoltage protection

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	UNIT
I_L	Nominal load current (ISO)	9	A
SYMBOL	**PARAMETER**	**MAX.**	**UNIT**
V_{BG}	Continuous off-state supply voltage	50	V
I_L	Continuous load current	20	A
T_j	Continuous junction temperature	150	°C
R_{ON}	On-state resistance	38	mΩ

FUNCTIONAL BLOCK DIAGRAM

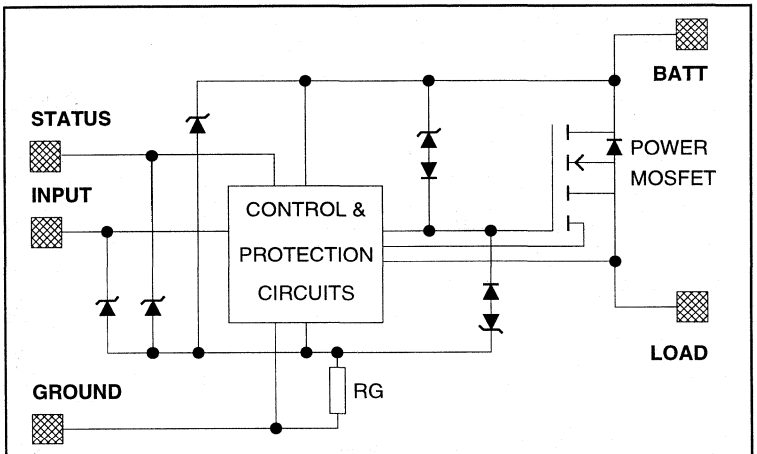


Fig.1. Elements of the TOPFET HSS with internal ground resistor.

PINNING - SOT426

PIN	DESCRIPTION
1	Ground
2	Input
3	(connected to mb)
4	Status
5	Load
mb	Battery

PIN CONFIGURATION

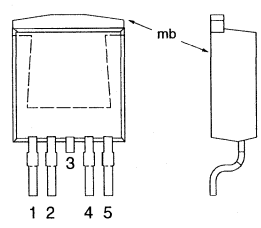


Fig. 2.

SYMBOL

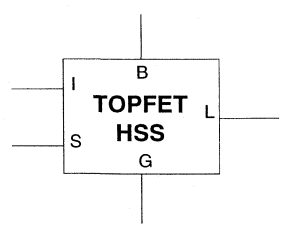


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Battery voltages				
V_{BG}	Continuous off-state supply voltage	-	0	50	V
	Reverse battery voltages[1]	External resistors:			
$-V_{BG}$	Repetitive peak supply voltage	$R_I = R_S \geq 4.7\ k\Omega$, $\delta \leq 0.1$	-	32	V
$-V_{BG}$	Continuous reverse supply voltage	$R_I = R_S \geq 4.7\ k\Omega$	-	16	V
I_L	Continuous load current	$T_{mb} \leq 110\ ^\circ C$	-	20	A
P_D	Total power dissipation	$T_{mb} \leq 25\ ^\circ C$	-	125	W
T_{stg}	Storage temperature	-	-55	175	°C
T_j	Continuous junction temperature[2]	-	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C
	Input and status				
I_I	Continuous input current	-	-5	5	mA
I_S	Continuous status current	-	-5	5	mA
I_I	Repetitive peak input current	$\delta \leq 0.1$	-20	20	mA
I_S	Repetitive peak status current	$\delta \leq 0.1$	-20	20	mA
	Inductive load clamping				
E_{BL}	Non-repetitive clamping energy	$T_{mb} = 150\ ^\circ C$ prior to turn-off	-	1.7	J

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

THERMAL CHARACTERISTIC

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance[3]					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	0.8	1	K/W

1 Reverse battery voltage is allowed only with external input and status resistors to limit the currents to a safe value.

2 For normal continuous operation. A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 Of the output Power MOS transistor.

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Clamping voltages					
V_{BG}	Battery to ground	I_G = 1 mA	50	55	65	V
V_{BL}	Battery to load	$I_L = I_G$ = 1 mA	50	55	65	V
$-V_{LG}$	Negative load to ground	I_L = 1 mA	12	17	21	V
	Supply voltage	battery to ground				
V_{BG}	Operating range[1]	-	5	-	40	V
	Currents	V_{BG} = 13 V				
I_L	Nominal load current[2]	V_{BL} = 0.5 V; T_{mb} = 85 °C	9	-	-	A
I_B	Quiescent current[3]	V_{IG} = 0 V; V_{LG} = 0 V	-	0.1	2	µA
I_G	Operating current[4]	V_{IG} = 5 V; I_L = 0 A	1.5	2.2	4	mA
I_L	Off-state load current[5]	V_{BL} = 13 V; V_{IG} = 0 V	-	0.1	1	µA
	Resistances					
R_{ON}	On-state resistance[6]	V_{BG} = 13 V; I_L = 10 A; t_p = 300 µs	-	28	38	mΩ
R_{ON}	On-state resistance	V_{BG} = 5 V; I_L = 2 A; t_p = 300 µs	-	36	48	mΩ
R_G	Internal ground resistance	I_G = 10 mA	-	150	-	Ω

INPUT CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_I	Input current	V_{IG} = 5 V	35	60	100	µA
V_{IG}	Input clamping voltage	I_I = 200 µA	6	7.5	8.5	V
$V_{IG(ON)}$	Input turn-on threshold voltage		-	2.1	2.7	V
$V_{IG(OFF)}$	Input turn-off threshold voltage		1.5	2	-	V

1 On-state resistance is increased if the supply voltage is less than 9 V. Refer to figure 8.

2 Defined as in ISO 10483-1.

3 This is the continuous current drawn from the supply when the input is low and includes leakage current to the load.

4 This is the continuous current drawn from the supply with no load connected, but with the input high.

5 The measured current is in the load pin only.

6 The supply and input voltage for the R_{ON} tests are continuous. The specified pulse duration t_p refers only to the applied load current.

PROTECTION FUNCTIONS AND STATUS INDICATIONS

Truth table for normal, open-circuit load and overload conditions and abnormal supply voltages.

FUNCTIONS		TRUTH TABLE			THRESHOLD			
SYMBOL	CONDITION	INPUT	STATUS	OUTPUT	MIN.	TYP.	MAX.	UNIT
	Normal on-state	1	1	1				
	Normal off-state	0	1	0				
$I_{L(OC)}$	Open circuit load[1]	1	0	1	150	450	750	mA
	Open circuit load	0	1	0				
$T_{j(TO)}$	Over temperature[2]	1	0	0	150	175	-	°C
	Over temperature[3]	0	0	0				
$V_{BL(TO)}$	Short circuit load[4]	1	0	0	9	10.5	12	V
	Short circuit load	0	1	0				
$V_{BG(TO)}$	Low supply voltage[5]	X	1	0	3	4	5	V
$V_{BG(LP)}$	High supply voltage[6]	X	1	0	40	45	50	V

For input '0' equals low, '1' equals high, 'X' equals don't care.
For status '0' equals low, '1' equals open or high.
For output switch '0' equals off, '1' equals on.

STATUS CHARACTERISTICS

T_{mb} = 25 °C.
The status output is an open drain transistor, and requires an external pull-up circuit to indicate a logic high.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SG}	Status clamping voltage	I_S = 100 µA; V_{IG} = 0 V	6	7	8	V
V_{SG}	Status low voltage	I_S = 50 µA; V_{BG} = 13 V; V_{IG} = 5 V	-	0.7	0.8	V
I_S	Status leakage current	V_{SG} = 5 V	-	0.1	1	µA
I_S	Status saturation current[7]	V_{SS} = 5 V; R_S = 0 Ω; V_{BG} = 13 V	-	5	-	mA
	Application information					
R_S	External pull-up resistor[8]	V_{SS} = 5 V	-	100	-	kΩ

[1] In the on-state, the switch detects whether the load current is less than the quoted open load threshold current. This is for status indication only. Typical hysteresis equals 230 mA. The thresholds are specified for supply voltage within the normal working range.
[2] After cooling below the reset temperature the switch will resume normal operation. The reset temperature is lower than the trip temperature by typically 10 °C.
[3] If the overtemperature protection has operated, status remains low to indicate the overtemperature condition even if the input is taken low, providing the device has not cooled below the reset temperature.
[4] After short circuit protection has operated, the input voltage must be toggled low for the switch to resume normal operation.
[5] Undervoltage sensor causes the device to switch off. Typical hysteresis equals 0.5 V.
[6] Overvoltage sensor causes the device to switch off. Typical hysteresis equals 1.3 V.
[7] In a fault condition with the pull-up resistor short circuited while the status transistor is conducting.
[8] The pull-up resistor also protects the status pin during reverse battery conditions.

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Inductive load turn-off					
$-V_{LG}$	Negative load voltage[1]	V_{IG} = 0 V; I_L = 10 A; t_p = 300 µs	15	20	25	V
	Short circuit load protection[2]	V_{IG} = 5 V; $R_L \leq$ 10 mΩ				
$t_{d\,sc}$	Response time		-	75	-	µs
I_L	Load current prior to turn-off	$t < t_{d\,sc}$	-	50	-	A
	Overload protection[3]					
$I_{L(lim)}$	Load current limiting	V_{BL} = 9 V; t_p = 300 µs	34	45	64	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C, V_{BG} = 13 V, for resistive load R_L = 13 Ω.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	During turn-on	to V_{IG} = 5 V				
$t_{d\,on}$	Delay time	to 10% V_L	-	16	-	µs
dV/dt_{on}	Rate of rise of load voltage		-	0.7	2	V/µs
t_{on}	Total switching time	to 90% V_L	-	140	-	µs
	During turn-off	to V_{IG} = 0 V				
$t_{d\,off}$	Delay time	to 90% V_L	-	40	-	µs
dV/dt_{off}	Rate of fall of load voltage		-	0.7	2	V/µs
t_{off}	Total switching time	to 10% V_L	-	70	-	µs

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz; V_{IG} = 0 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{ig}	Input capacitance	V_{BG} = 13 V	-	15	20	pF
C_{bl}	Output capacitance	V_{BL} = V_{BG} = 13 V	-	500	700	pF
C_{sg}	Status capacitance	V_{SG} = 5 V	-	11	15	pF

1 For a high side switch, the load pin voltage goes negative with respect to ground during the turn-off of an inductive load. This negative voltage is clamped by the device.

2 The load current is self-limited during the response time for short circuit load protection. Response time is measured from when input goes high.

3 If the load resistance is low, but not a complete short circuit, such that the on-state voltage remains less than $V_{BL(TO)}$, the device remains in current limiting until the overtemperature protection operates.

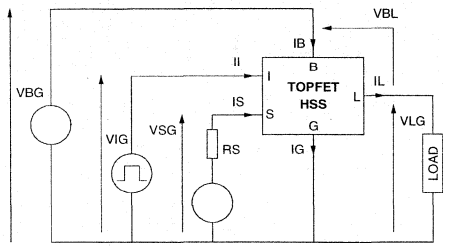


Fig.4. High side switch measurements schematic. (current and voltage conventions)

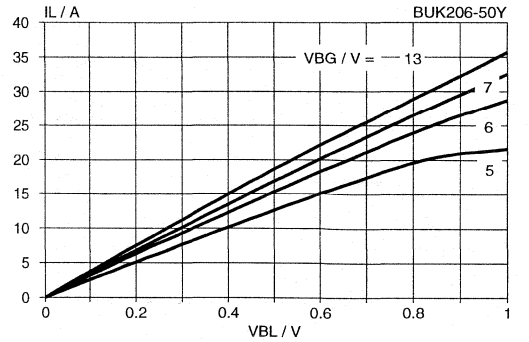


Fig.7. Typical on-state characteristics, T_j = 25 °C. $I_L = f(V_{BL})$; parameter V_{BG}; t_p = 250 µs

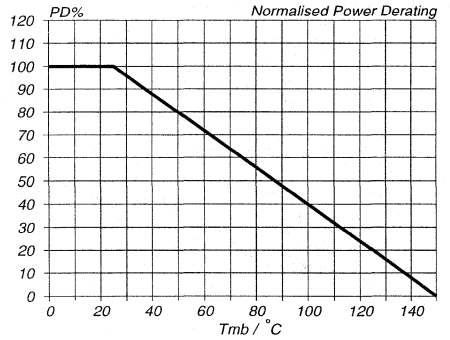


Fig.5. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\ °C) = f(T_{mb})$

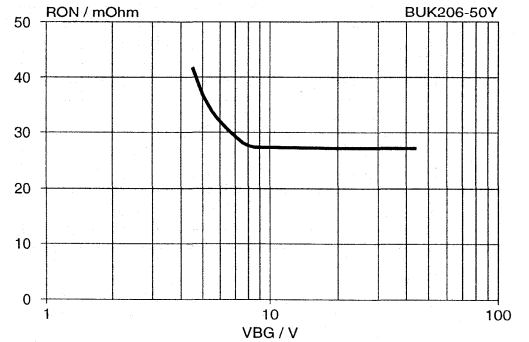


Fig.8. Typical on-state resistance, T_j = 25 °C. $R_{ON} = f(V_{BG})$; conditions: I_L = 10 A; t_p = 300 µs

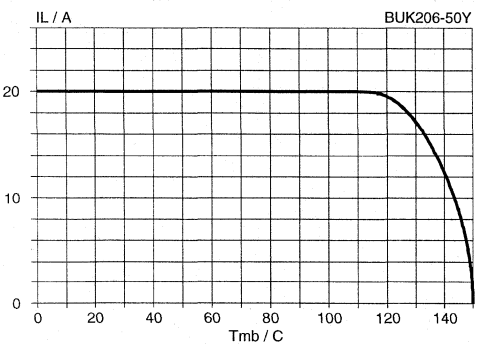


Fig.6. Limiting continuous on-state load current. $I_L = f(T_{mb})$; conditions: V_{IG} = 5 V, V_{BG} = 13 V

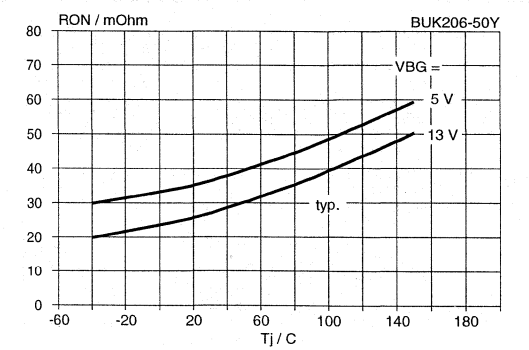


Fig.9. Typical on-state resistance, t_p = 300 µs. $R_{ON} = f(T_j)$; parameter V_{BG}; condition I_L = 2 A

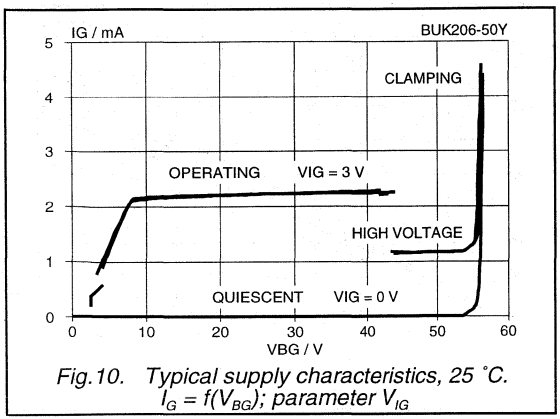


Fig.10. Typical supply characteristics, 25 ˚C. $I_G = f(V_{BG})$; parameter V_{IG}

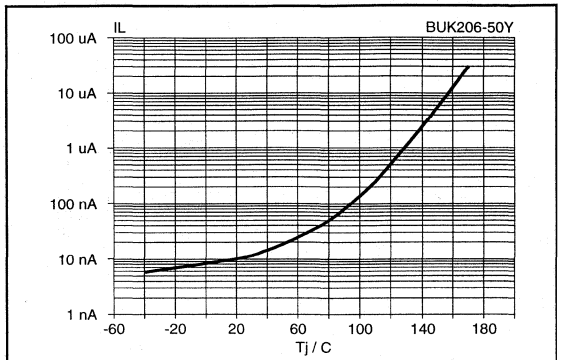


Fig.13. Typical off-state leakage current. $I_L = f(T_j)$; conditions: V_{BL} = 13 V = V_{BG}; V_{IG} = 0 V.

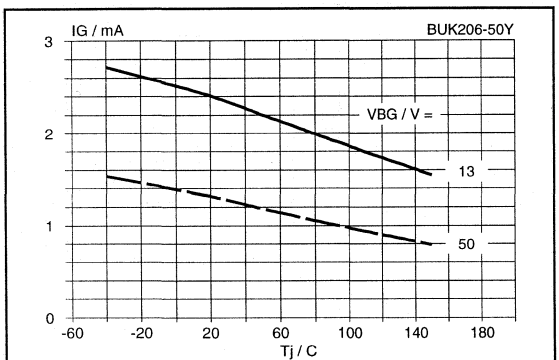


Fig.11. Typical operating supply current. $I_G = f(T_j)$; parameter V_{BG}; condition V_{IG} = 5 V

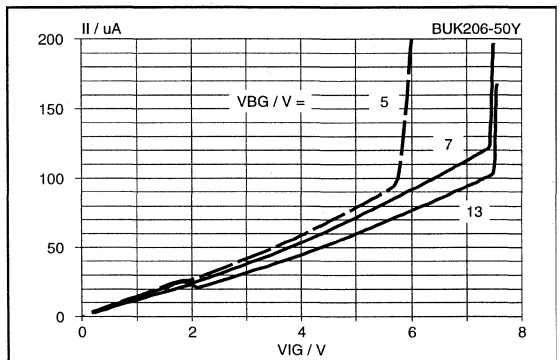


Fig.14. Typical input characteristics, T_j = 25 ˚C. $I_I = f(V_{IG})$; parameter V_{BG}

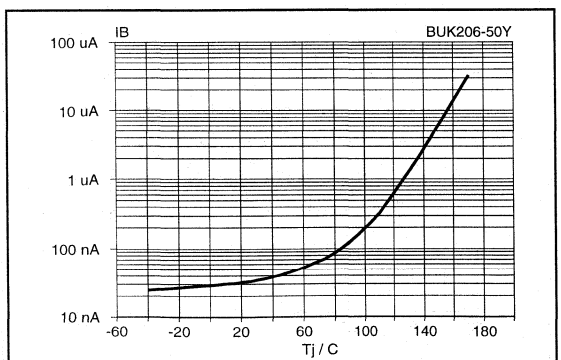


Fig.12. Typical supply quiescent current. $I_B = f(T_j)$; condition V_{BG} = 13 V, V_{IG} = 0 V, V_{LG} = 0 V

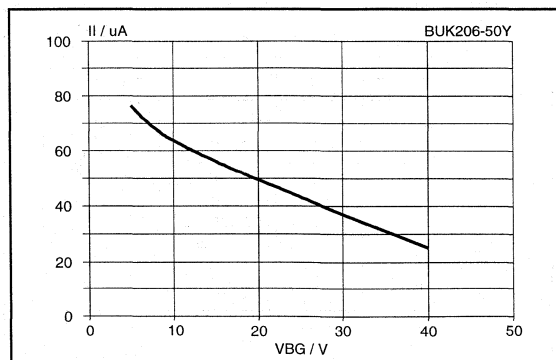


Fig.15. Typical input current, T_j = 25 ˚C. $I_I = f(V_{BG})$; condition V_{IG} = 5 V

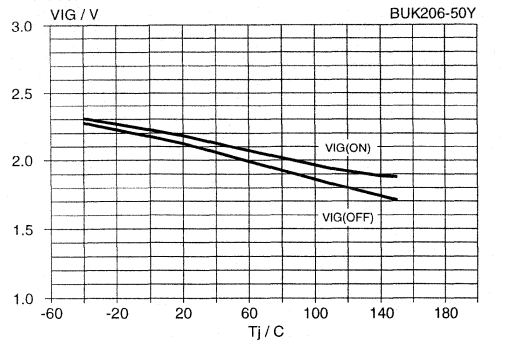


Fig.16. Typical input threshold voltages. $V_{IG} = f(T_j)$; conditions V_{BG} = 13 V, I_L = 100 mA

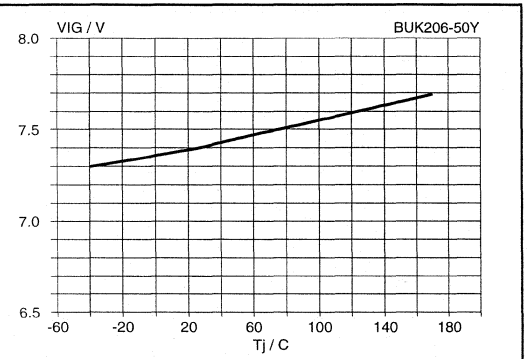


Fig.17. Typical input clamping voltage. $V_{IG} = f(T_j)$; conditions I_I = 200 µA, V_{BG} = 13 V

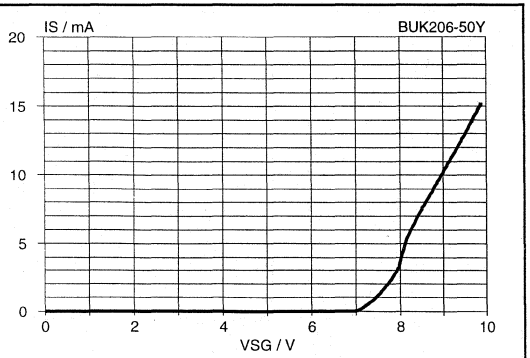


Fig.18. Typical status characteristic, T_j = 25 ˚C. $I_S = f(V_{SG})$; conditions $V_{IG} = V_{BG}$ = 0 V

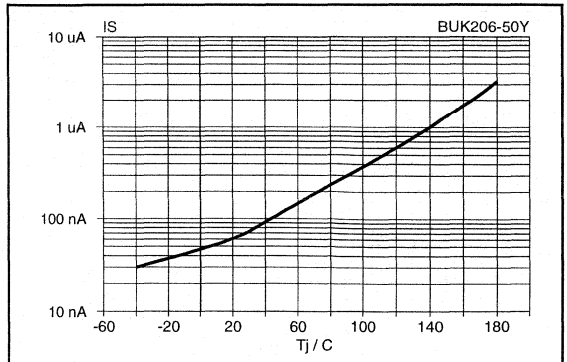


Fig.19. Typical status leakage current. $I_S = f(T_j)$; conditions V_{SG} = 5 V, $V_{IG} = V_{BG}$ = 0 V

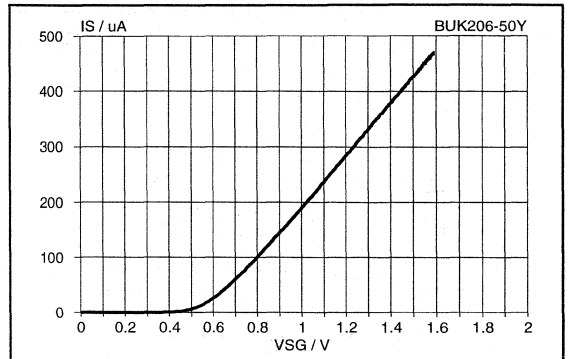


Fig.20. Typical status low characteristic, T_j = 25 ˚C. $I_S = f(V_{SG})$; conditions V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

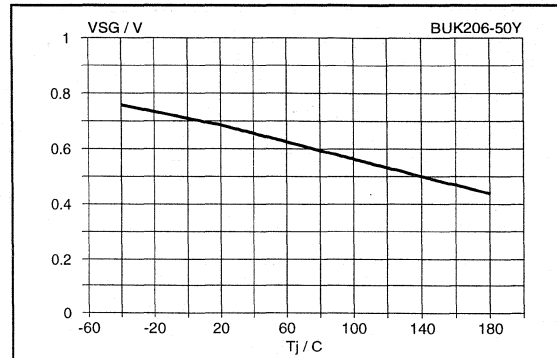


Fig.21. Typical status low voltage, $V_{SG} = f(T_j)$. conditions I_S = 50 µA, V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

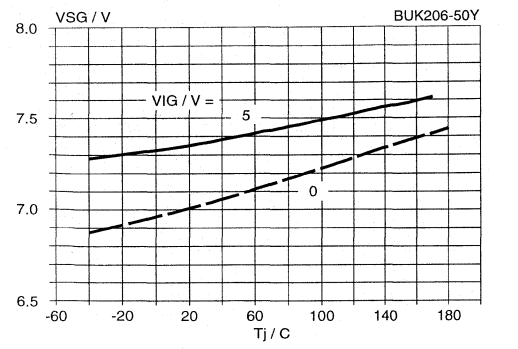


Fig.22. Typical status clamping voltage, $V_{SG} = f(T_j)$. parameter V_{IG}; conditions I_S = 100 µA, V_{BG} = 13 V

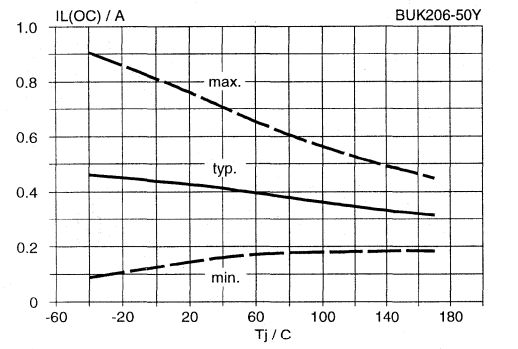


Fig.23. Low load current detection threshold. $I_{L(OC)} = f(T_j)$; conditions V_{IG} = 5 V; V_{BG} = 13 V

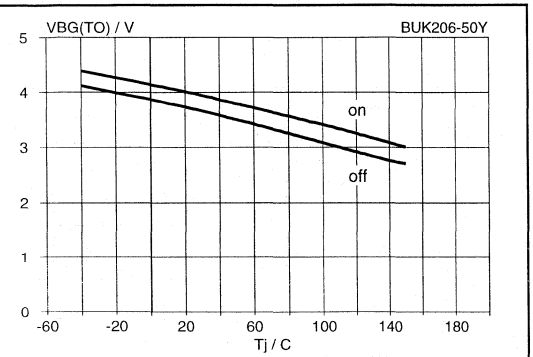


Fig.24. Supply typical undervoltage thresholds. $V_{BG(TO)} = f(T_j)$; conditions V_{IG} = 3 V; I_L = 100 mA

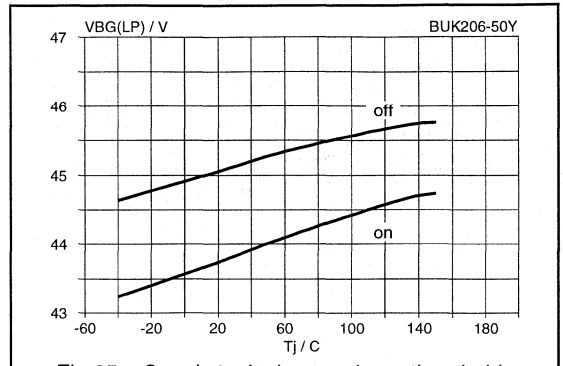


Fig.25. Supply typical overvoltage thresholds. $V_{BG(LP)} = f(T_j)$; conditions V_{IG} = 5 V; I_L = 100 mA

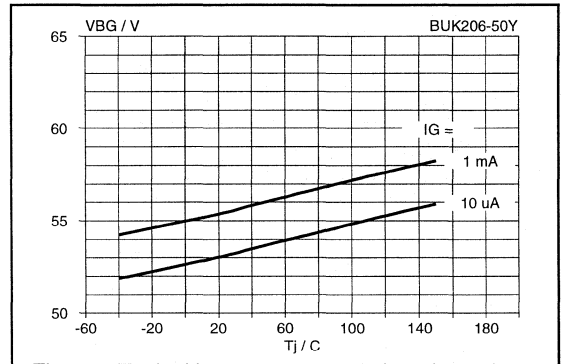


Fig.26. Typical battery to ground clamping voltage. $V_{BG} = f(T_j)$; parameter I_G

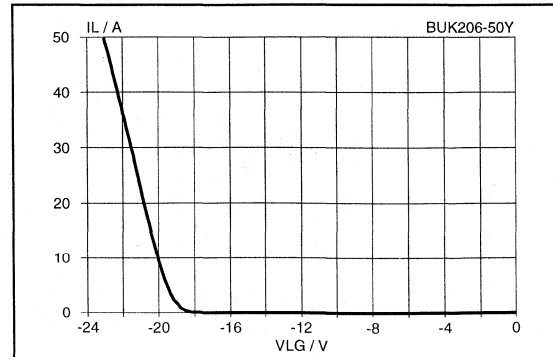


Fig.27. Typical negative load clamping characteristic. $I_L = f(V_{LG})$; conditions V_{IG} = 0 V, t_p = 300 µs, 25 ˚C

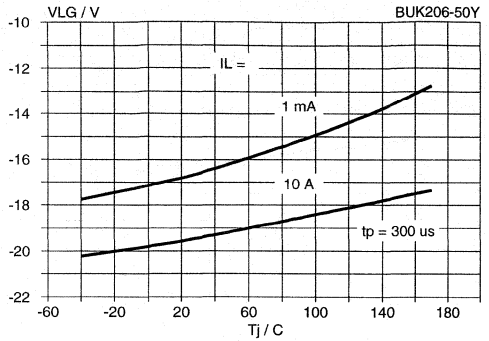


Fig.28. Typical negative load clamping voltage. $V_{LG} = f(T_j)$; parameter I_L; condition $V_{IG} = 0$ V.

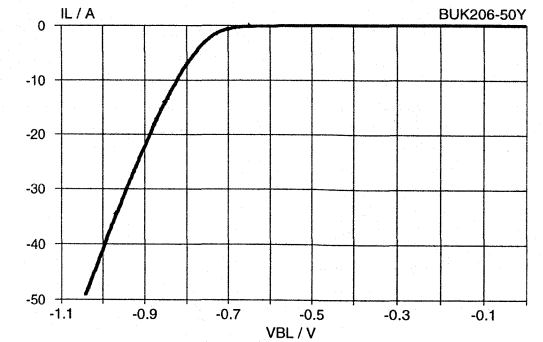


Fig.31. Typical reverse diode characteristic. $I_L = f(V_{BL})$; conditions $V_{IG} = 0$ V, $T_j = 25$ °C

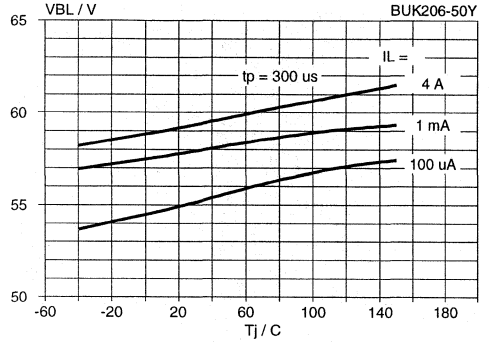


Fig.29. Typical battery to load clamping voltage. $V_{BL} = f(T_j)$; parameter I_L; condition $I_G = 5$ mA.

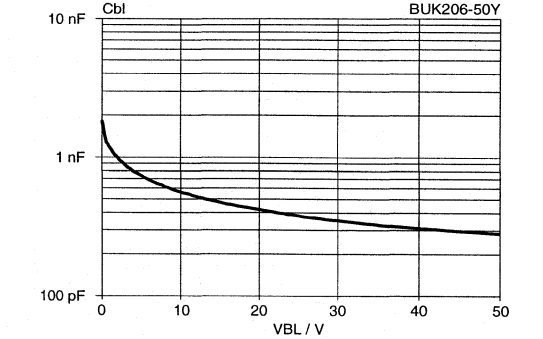


Fig.32. Typical output capacitance. $T_{mb} = 25$ °C $C_{bl} = f(V_{BL})$; conditions f = 1 MHz, $V_{IG} = 0$ V

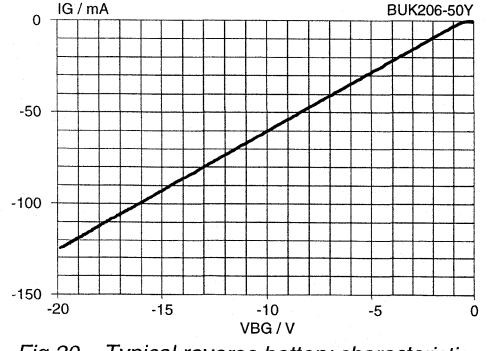


Fig.30. Typical reverse battery characteristic. $I_G = f(V_{BG})$; conditions $I_L = 0$ A, $T_j = 25$ °C

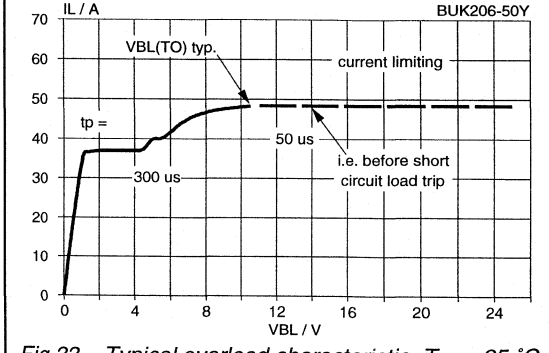


Fig.33. Typical overload characteristic, $T_{mb} = 25$ °C. $I_L = f(V_{BL})$; condition $V_{BG} = 13$ V; parameter t_p

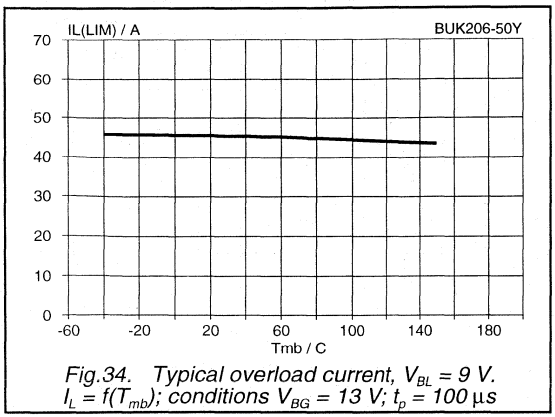


Fig.34. Typical overload current, V_{BL} = 9 V. $I_L = f(T_{mb})$; conditions V_{BG} = 13 V; t_p = 100 µs

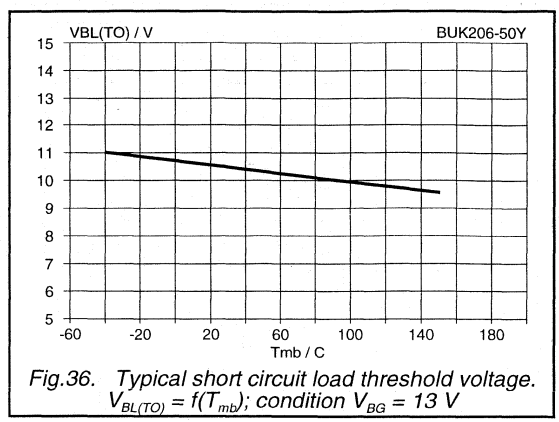


Fig.36. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(T_{mb})$; condition V_{BG} = 13 V

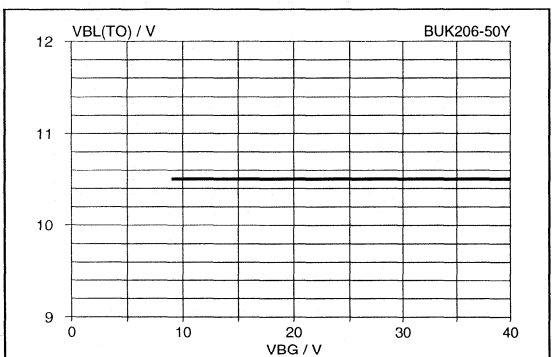


Fig.35. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(V_{BG})$; condition T_{mb} = 25 °C

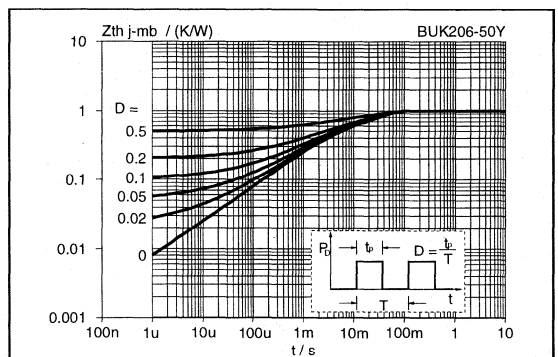


Fig.37. Transient thermal impedance. $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

TOPFET high side switch SMD version of BUK203-50Y

BUK207-50Y

For maintenance only. Do not use for design-in.

DESCRIPTION

Monolithic temperature and overload protected power switch based on MOSFET technology in a 5 pin plastic surface mount envelope, configured as a single high side switch.

APPLICATIONS

General controller for driving lamps, motors, solenoids, heaters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	UNIT
I_L	Nominal load current (ISO)	1.6	A
SYMBOL	**PARAMETER**	**MAX.**	**UNIT**
V_{BG}	Continuous off-state supply voltage	50	V
I_L	Continuous load current	4	A
T_j	Continuous junction temperature	150	°C
R_{ON}	On-state resistance	220	mΩ

FEATURES

- Vertical power DMOS switch
- Low on-state resistance
- 5 V logic compatible input
- Overtemperature protection - self resets with hysteresis
- Overload protection against short circuit load with output current limiting; latched - reset by input
- High supply voltage load protection
- Supply undervoltage lock out
- Status indication for overload protection activated
- Diagnostic status indication of open circuit load
- Very low quiescent current
- Voltage clamping for turn off of inductive loads
- ESD protection on all pins
- Reverse battery and overvoltage protection

FUNCTIONAL BLOCK DIAGRAM

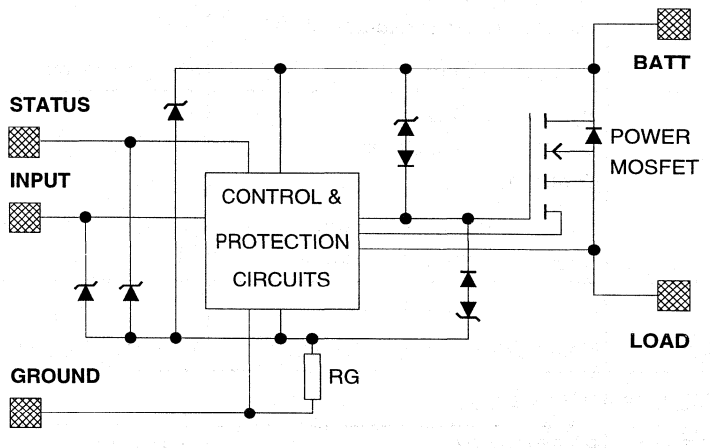


Fig.1. Elements of the TOPFET HSS with internal ground resistor.

PINNING - SOT426

PIN	DESCRIPTION
1	Ground
2	Input
3	(connected to mb)
4	Status
5	Load
mb	Battery

PIN CONFIGURATION

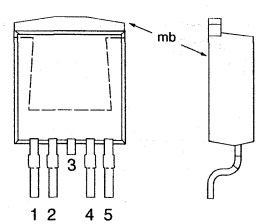


Fig. 2.

SYMBOL

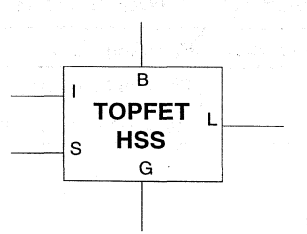


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Battery voltages				
V_{BG}	Continuous off-state supply voltage	-	0	50	V
	Reverse battery voltages[1]	External resistors:			
$-V_{BG}$	Repetitive peak supply voltage	$R_I = R_S \geq 4.7\ k\Omega$, $\delta \leq 0.1$	-	32	V
$-V_{BG}$	Continuous reverse supply voltage	$R_I = R_S \geq 4.7\ k\Omega$	-	16	V
I_L	Continuous load current	$T_{mb} \leq 110$ °C	-	4	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	50	W
T_{stg}	Storage temperature	-	-55	175	°C
T_j	Continuous junction temperature[2]	-	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C
	Input and status				
I_I	Continuous input current	-	-5	5	mA
I_S	Continuous status current	-	-5	5	mA
I_I	Repetitive peak input current	$\delta \leq 0.1$	-20	20	mA
I_S	Repetitive peak status current	$\delta \leq 0.1$	-20	20	mA
	Inductive load clamping				
E_{BL}	Non-repetitive clamping energy	$T_{mb} = 150$ °C prior to turn-off	-	1.4	J

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

THERMAL CHARACTERISTIC

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance[3]					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	2	2.5	K/W

1 Reverse battery voltage is allowed only with external input and status resistors to limit the currents to a safe value.

2 For normal continuous operation. A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 Of the output Power MOS transistor.

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Clamping voltages					
V_{BG}	Battery to ground	I_G = 1 mA	50	55	65	V
V_{BL}	Battery to load	$I_L = I_G$ = 1 mA	50	55	65	V
$-V_{LG}$	Negative load to ground	I_L = 1 mA	12	17	21	V
	Supply voltage	battery to ground				
V_{BG}	Operating range[1]	-	5	-	40	V
	Currents	V_{BG} = 13 V				
I_L	Nominal load current[2]	V_{BL} = 0.5 V; T_{mb} = 85 °C	1.6	-	-	A
I_B	Quiescent current[3]	V_{IG} = 0 V; V_{LG} = 0 V	-	0.1	2	µA
I_G	Operating current[4]	V_{IG} = 5 V; I_L = 0 A	1.5	2.2	4	mA
I_L	Off-state load current[5]	V_{BL} = 13 V; V_{IG} = 0 V	-	0.1	1	µA
	Resistances					
R_{ON}	On-state resistance[6]	V_{BG} = 13 V; I_L = 2 A; t_p = 300 µs	-	160	220	mΩ
R_{ON}	On-state resistance	V_{BG} = 5 V; I_L = 0.5 A; t_p = 300 µs	-	225	320	mΩ
R_G	Internal ground resistance	I_G = 10 mA	-	150	-	Ω

INPUT CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_I	Input current	V_{IG} = 5 V	35	60	100	µA
V_{IG}	Input clamping voltage	I_I = 200 µA	6	7.5	8.5	V
$V_{IG(ON)}$	Input turn-on threshold voltage		-	2.1	2.7	V
$V_{IG(OFF)}$	Input turn-off threshold voltage		1.5	2	-	V

1 On-state resistance is increased if the supply voltage is less than 9 V. Refer to figure 8.

2 Defined as in ISO 10483-1.

3 This is the continuous current drawn from the battery when the input is low and includes leakage current to the load.

4 This is the continuous current drawn from the battery with no load connected, but with the input high.

5 The measured current is in the load pin only.

6 The supply and input voltage for the R_{ON} tests are continuous. The specified pulse duration t_p refers only to the applied load current.

PROTECTION FUNCTIONS AND STATUS INDICATIONS

Truth table for normal, open-circuit load and overload conditions and abnormal supply voltages.

FUNCTIONS		TRUTH TABLE			THRESHOLD			
SYMBOL	CONDITION	INPUT	STATUS	OUTPUT	MIN.	TYP.	MAX.	UNIT
	Normal on-state	1	1	1				
	Normal off-state	0	1	0				
$I_{L(OC)}$	Open circuit load[1]	1	0	1	30	90	150	mA
	Open circuit load	0	1	0				
$T_{j(TO)}$	Over temperature[2]	1	0	0	150	175	-	°C
	Over temperature[3]	0	0	0				
$V_{BL(TO)}$	Short circuit load[4]	1	0	0	9	10.5	12	V
	Short circuit load	0	1	0				
$V_{BG(TO)}$	Low supply voltage[5]	X	1	0	3	4	5	V
$V_{BG(LP)}$	High supply voltage[6]	X	1	0	40	45	50	V

For input '0' equals low, '1' equals high, 'X' equals don't care.
For status '0' equals low, '1' equals open or high.
For output switch '0' equals off, '1' equals on.

STATUS CHARACTERISTICS

T_{mb} = 25 °C.
The status output is an open drain transistor, and requires an external pull-up circuit to indicate a logic high.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SG}	Status clamping voltage	I_S = 100 µA; V_{IG} = 0 V	6	7	8	V
V_{SG}	Status low voltage	I_S = 50 µA; V_{BG} = 13 V; V_{IG} = 5 V	-	0.7	0.8	V
I_S	Status leakage current	V_{SG} = 5 V	-	0.1	1	µA
I_S	Status saturation current[7]	V_{SS} = 5 V; R_S = 0 Ω; V_{BG} = 13 V	-	5	-	mA
	Application information					
R_S	External pull-up resistor[8]	V_{SS} = 5 V	-	100	-	kΩ

1 In the on-state, the switch detects whether the load current is less than the quoted open load threshold current. This is for status indication only. Typical hysteresis equals 25 mA. The thresholds are specified for supply voltage within the normal working range.

2 After cooling below the reset temperature the switch will resume normal operation. The reset temperature is lower than the trip temperature by typically 10 °C.

3 If the overtemperature protection has operated, status remains low to indicate the overtemperature condition even if the input is taken low, providing the device has not cooled below the reset temperature.

4 After short circuit protection has operated, the input voltage must be toggled low for the switch to resume normal operation.

5 Undervoltage sensor causes the device to switch off. Typical hysteresis equals 0.7 V.

6 Overvoltage sensor causes the device to switch off to protect the load. Typical hysteresis equals 1.3 V.

7 In a fault condition with the pull-up resistor short circuited while the status transistor is conducting.

8 The pull-up resistor also protects the status pin during reverse battery conditions.

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Inductive load turn-off					
$-V_{LG}$	Negative load voltage[1]	V_{IG} = 0 V; I_L = 2 A; t_p = 300 µs	15	20	25	V
	Short circuit load protection[2]	V_{IG} = 5 V; $R_L \leq$ 10 mΩ				
$t_{d\,sc}$	Response time		-	75	-	µs
I_L	Load current prior to turn-off	$t < t_{d\,sc}$	-	17	-	A
	Overload protection[3]					
$I_{L(lim)}$	Load current limiting	V_{BL} = 9 V; t_p = 300 µs	12	15	22	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C, V_{BG} = 13 V, for resistive load R_L = 13 Ω.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	During turn-on	to V_{IG} = 5 V				
$t_{d\,on}$	Delay time	to 10% V_L	-	16	-	µs
dV/dt_{on}	Rate of rise of load voltage		-	1.3	3	V/µs
t_{on}	Total switching time	to 90% V_L	-	40	-	µs
	During turn-off	to V_{IG} = 0 V				
$t_{d\,off}$	Delay time	to 90% V_L	-	20	-	µs
dV/dt_{off}	Rate of fall of load voltage		-	1.6	3	V/µs
t_{off}	Total switching time	to 10% V_L	-	35	-	µs

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz; V_{IG} = 0 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{ig}	Input capacitance	V_{BG} = 13 V	-	15	20	pF
C_{bl}	Output capacitance	V_{BL} = V_{BG} = 13 V	-	120	170	pF
C_{sg}	Status capacitance	V_{SG} = 5 V	-	11	15	pF

[1] For a high side switch, the load pin voltage goes negative with respect to ground during the turn-off of an inductive load. This negative voltage is clamped by the device.

[2] The load current is self-limited during the response time for short circuit load protection. Response time is measured from when input goes high.

[3] If the load resistance is low, but not a complete short circuit, such that the on-state voltage remains less than $V_{BL(TO)}$, the device remains in current limiting until the overtemperature protection operates.

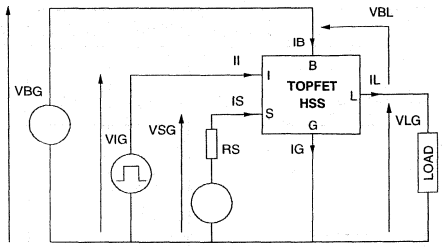


Fig.4. High side switch measurements schematic. (current and voltage conventions)

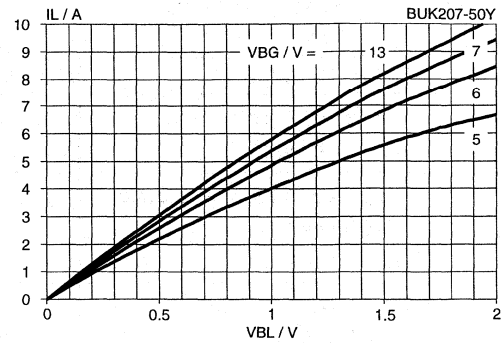


Fig.7. Typical on-state characteristics, T_j = 25 ˚C. $I_L = f(V_{BL})$; parameter V_{BG}; t_p = 250 µs

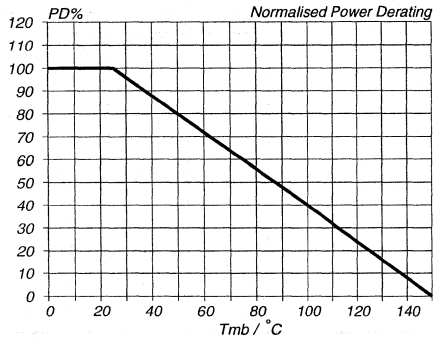


Fig.5. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

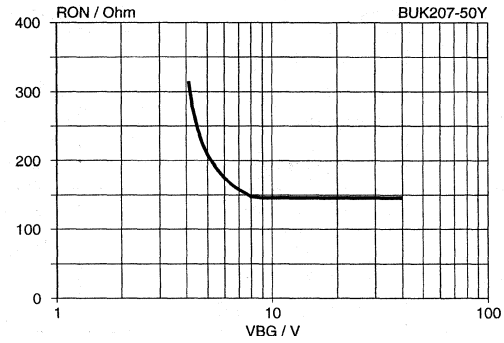


Fig.8. Typical on-state resistance, T_j = 25 ˚C. $R_{ON} = f(V_{BG})$; conditions: I_L = 2 A; t_p = 300 µs

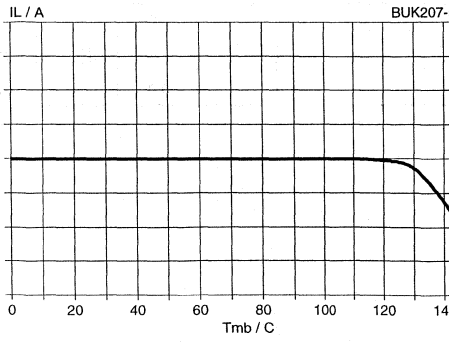


Fig.6. Limiting continuous on-state load current. $I_L = f(T_{mb})$; conditions: V_{IG} = 5 V, V_{BG} = 13 V

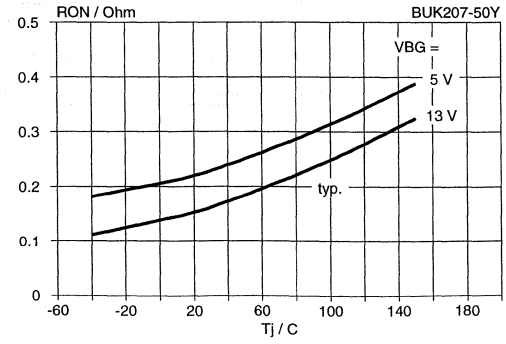


Fig.9. Typical on-state resistance, t_p = 300 µs. $R_{ON} = f(T_j)$; parameter V_{BG}; condition I_L = 0.5 A

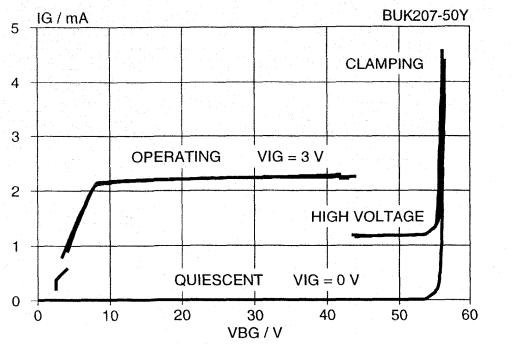


Fig.10. Typical supply characteristics, 25 ˚C. $I_G = f(V_{BG})$; parameter V_{IG}

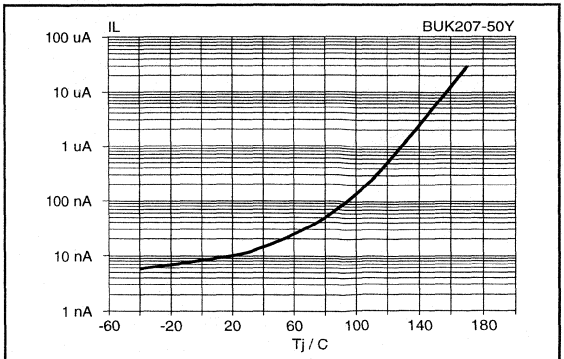


Fig.13. Typical off-state leakage current. $I_L = f(T_j)$; conditions: V_{BL} = 13 V = V_{BG}; V_{IG} = 0 V.

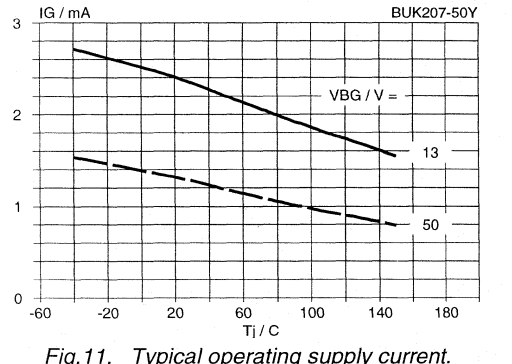


Fig.11. Typical operating supply current. $I_G = f(T_j)$; parameter V_{BG}; condition V_{IG} = 5 V

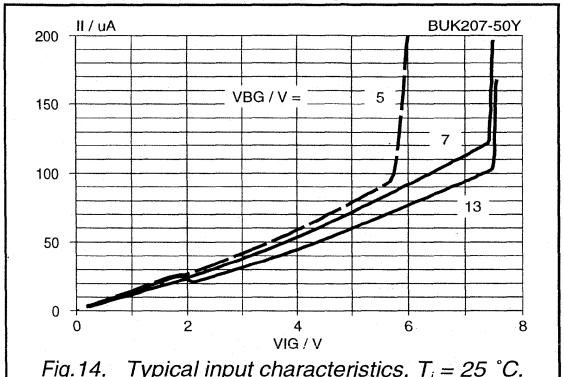


Fig.14. Typical input characteristics, T_j = 25 ˚C. $I_I = f(V_{IG})$; parameter V_{BG}

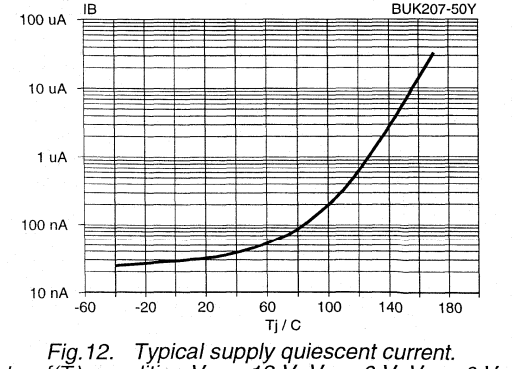


Fig.12. Typical supply quiescent current. $I_B = f(T_j)$; condition V_{BG} = 13 V, V_{IG} = 0 V, V_{LG} = 0 V

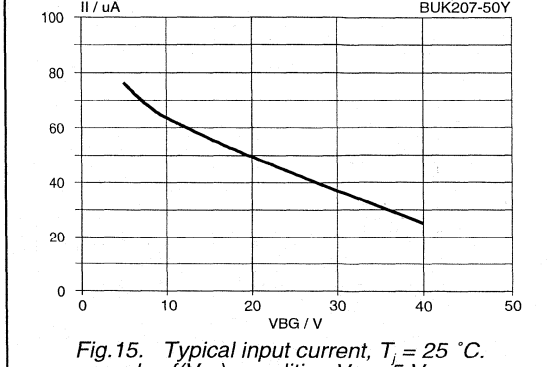


Fig.15. Typical input current, T_j = 25 ˚C. $I_I = f(V_{BG})$; condition V_{IG} = 5 V

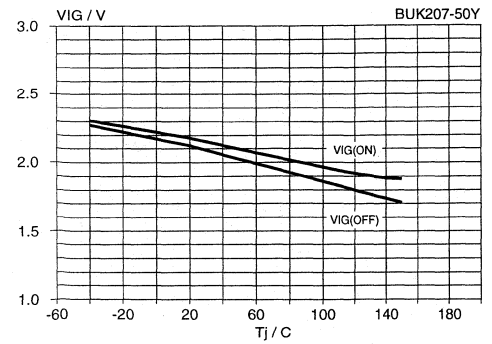


Fig.16. Typical input threshold voltages. $V_{IG} = f(T_j)$; conditions V_{BG} = 13 V, I_L = 100 mA

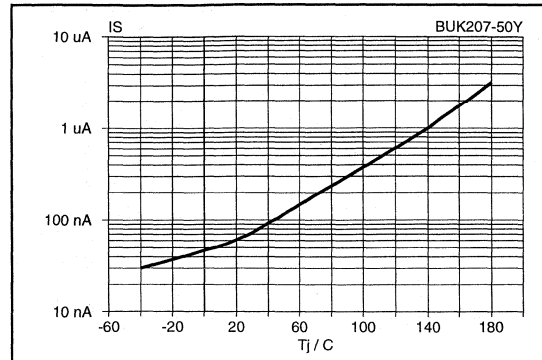


Fig.19. Typical status leakage current. $I_S = f(T_j)$; conditions V_{SG} = 5 V, $V_{IG} = V_{BG}$ = 0 V

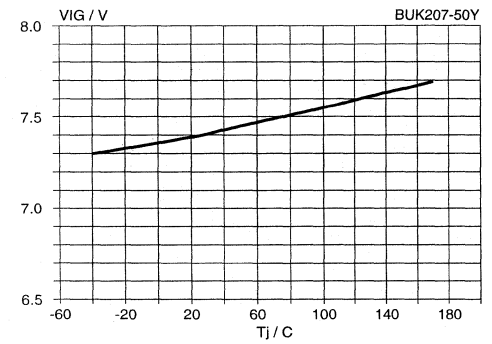


Fig.17. Typical input clamping voltage. $V_{IG} = f(T_j)$; conditions I_I = 200 µA, V_{BG} = 13 V

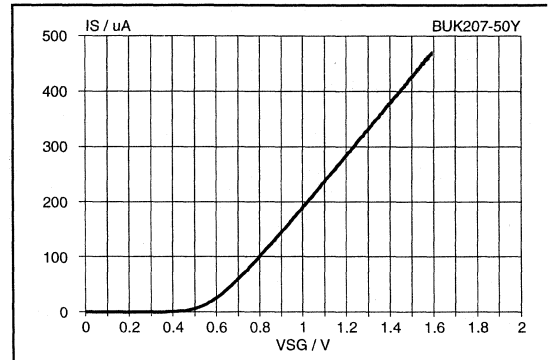


Fig.20. Typical status low characteristic, T_j = 25 ˚C. $I_S = f(V_{SG})$; conditions V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

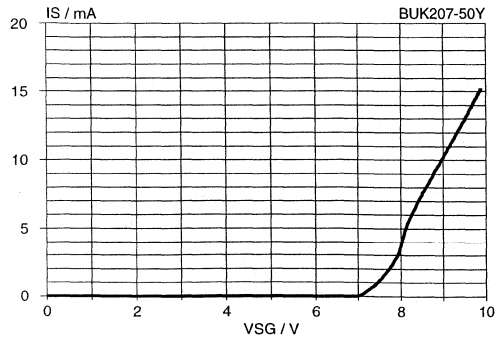


Fig.18. Typical status characteristic, T_j = 25 ˚C. $I_S = f(V_{SG})$; conditions $V_{IG} = V_{BG}$ = 0 V

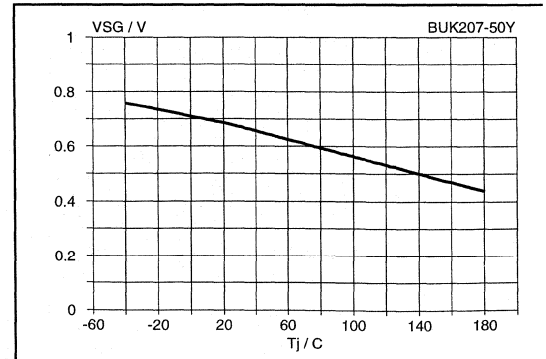


Fig.21. Typical status low voltage, $V_{SG} = f(T_j)$. conditions I_S = 50 µA, V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

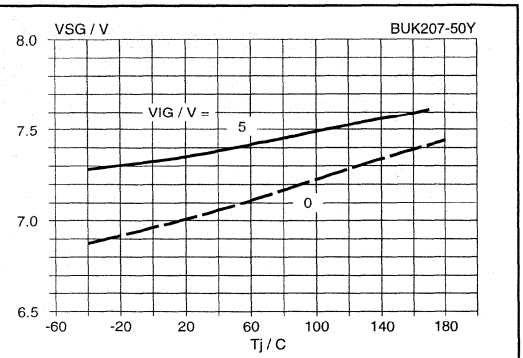


Fig.22. Typical status clamping voltage, $V_{SG} = f(T_j)$. parameter V_{IG}; conditions I_S = 100 µA, V_{BG} = 13 V

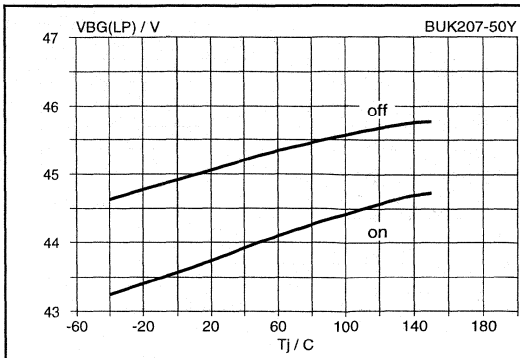


Fig.25. Supply typical overvoltage thresholds. $V_{BG(LP)} = f(T_j)$; conditions V_{IG} = 5 V; I_L = 100 mA

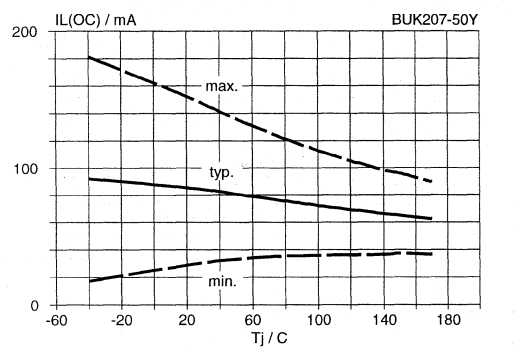


Fig.23. Low load current detection threshold. $I_{L(OC)} = f(T_j)$; conditions V_{IG} = 5 V; V_{BG} = 13 V

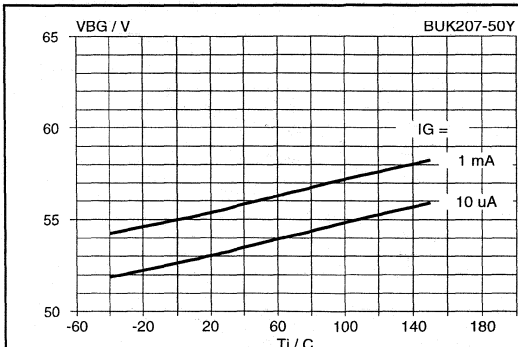


Fig.26. Typical battery to ground clamping voltage. $V_{BG} = f(T_j)$; parameter I_G

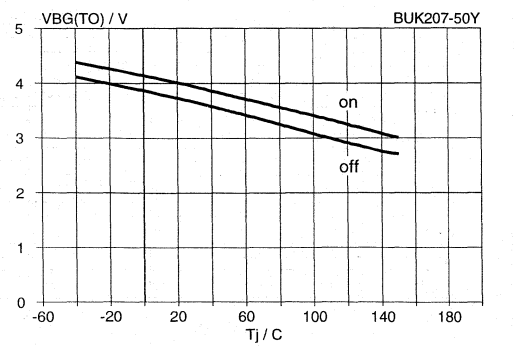


Fig.24. Supply typical undervoltage thresholds. $V_{BG(TO)} = f(T_j)$; conditions V_{IG} = 3 V; I_L = 100 mA

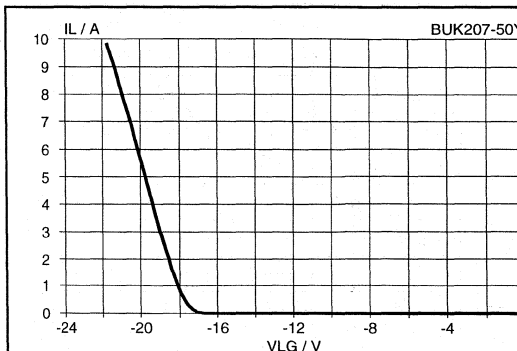


Fig.27. Typical negative load clamping characteristic. $I_L = f(V_{LG})$; conditions V_{IG} = 0 V, t_p = 300 µs, 25 °C

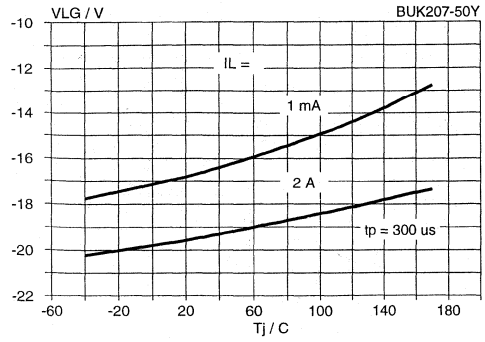


Fig.28. Typical negative load clamping voltage. $V_{LG} = f(T_j)$; parameter I_L; condition $V_{IG} = 0$ V.

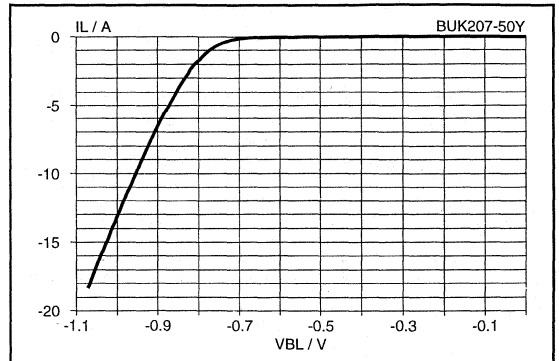


Fig.31. Typical reverse diode characteristic. $I_L = f(V_{BL})$; conditions $V_{IG} = 0$ V, $T_j = 25$ °C

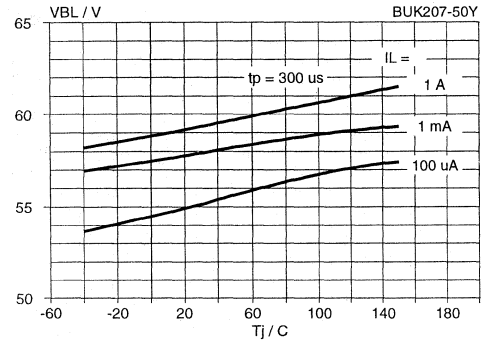


Fig.29. Typical battery to load clamping voltage. $V_{BL} = f(T_j)$; parameter I_L; condition $I_G = 5$ mA.

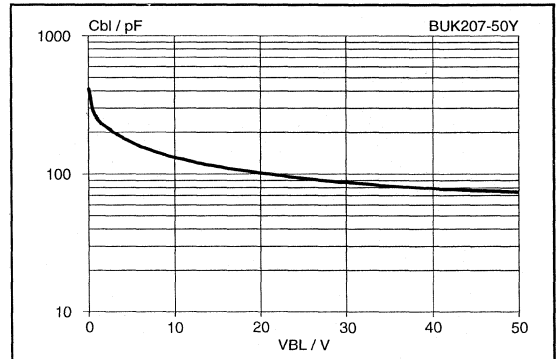


Fig.32. Typical output capacitance. $T_{mb} = 25$ °C $C_{bl} = f(V_{BL})$; conditions $f = 1$ MHz, $V_{IG} = 0$ V

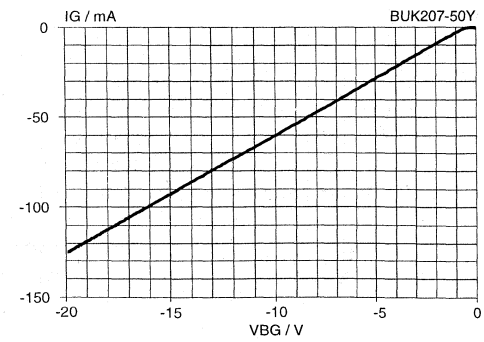


Fig.30. Typical reverse battery characteristic. $I_G = f(V_{BG})$; conditions $I_L = 0$ A, $T_j = 25$ °C

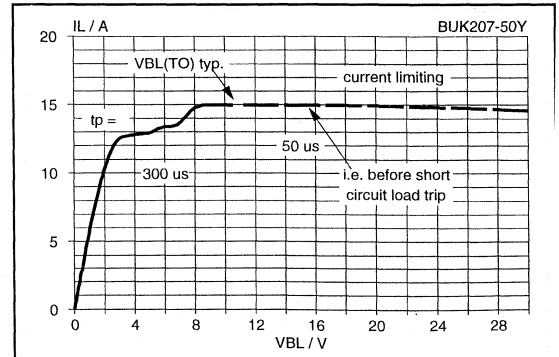


Fig.33. Typical overload characteristic, $T_{mb} = 25$ °C. $I_L = f(V_{BL})$; condition $V_{BG} = 13$ V; parameter t_p

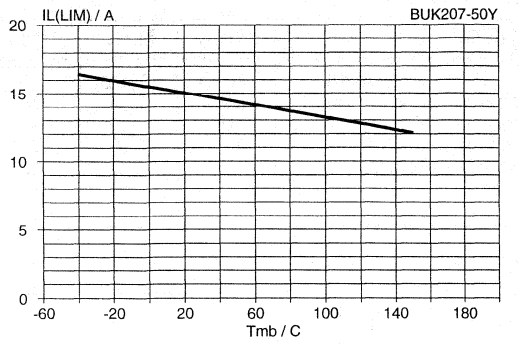


Fig.34. Typical overload current, V_{BL} = 9 V. $I_L = f(T_{mb})$; conditions V_{BG} = 13 V; t_p = 100 µs

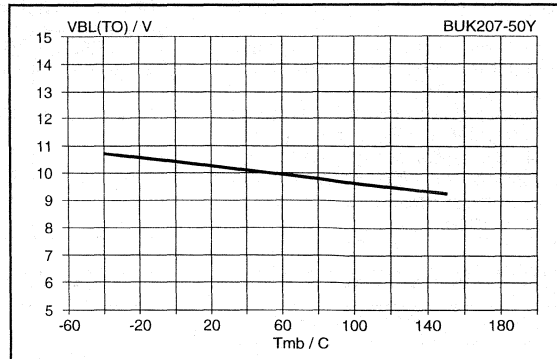


Fig.36. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(T_{mb})$; condition V_{BG} = 13 V

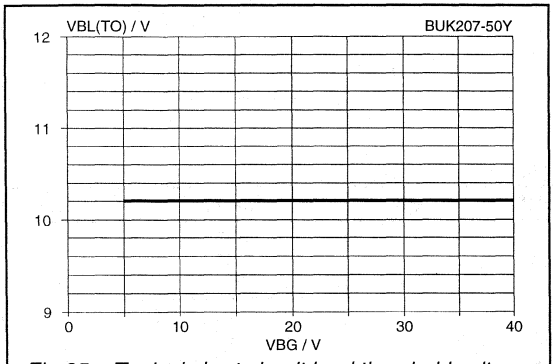


Fig.35. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(V_{BG})$; condition T_{mb} = 25 °C

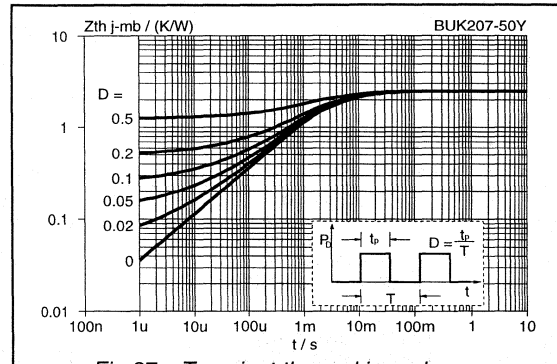


Fig.37. Transient thermal impedance. $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

PowerMOS transistor — BUK436W-200A/B

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

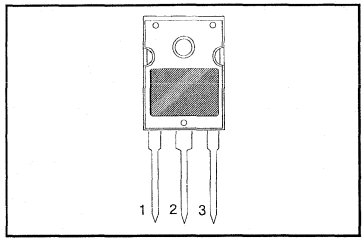
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK436	-200A	-200B	
V_{DS}	Drain-source voltage	200	200	V
I_D	Drain current (DC)	19	17	A
P_{tot}	Total power dissipation	125	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.16	0.2	Ω

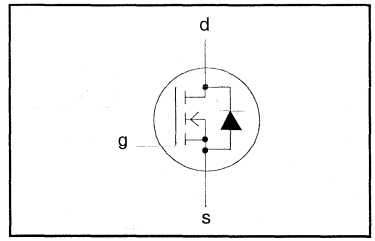
PINNING - SOT429 (TO247)

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	200		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-200A	-200B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	19	17	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	12	11	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	76	68	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction Temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	45	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK436-200A**	-	0.15	0.16	Ω
		I_D = 10 A **BUK436-200B**	-	0.17	0.20	Ω

DYNAMIC CHARACTERISTICS

Tmb = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 10 A	8.5	16	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1500	2000	pF
C_{oss}	Output capacitance		-	300	400	pF
C_{rss}	Feedback capacitance		-	60	100	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	20	30	ns
t_r	Turn-on rise time	V_{GS} = 10 V;	-	40	60	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω;	-	145	185	ns
t_f	Turn-off fall time	R_{GS} = 50 Ω	-	50	70	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	12.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

Tmb = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	19	A
I_{DRM}	Pulsed reverse drain current	-	-	-	76	A
V_{SD}	Diode forward voltage	I_F = 19 A ; V_{GS} = 0 V	-	1.0	1.7	V
t_{rr}	Reverse recovery time	I_F = 19 A; -dI_F/dt = 100 A/µs;	-	180	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	2.5	-	µC

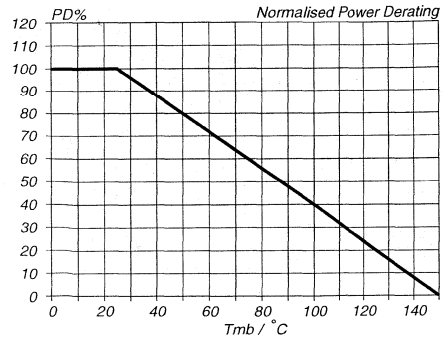


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

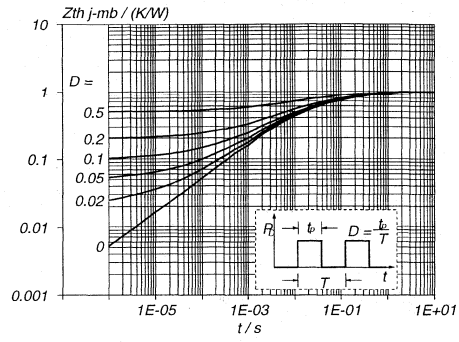


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

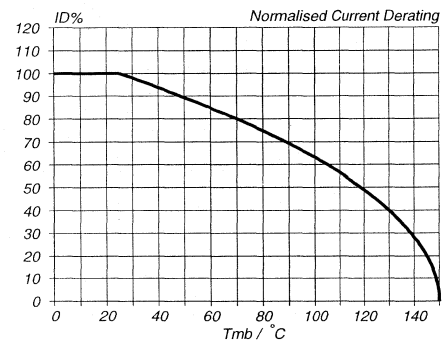


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

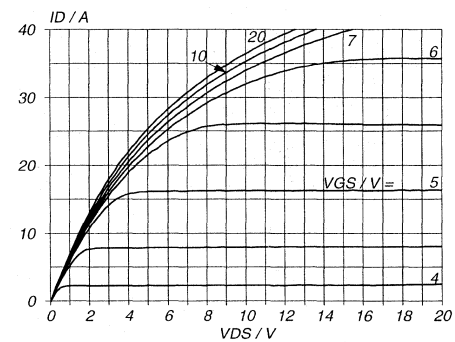


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

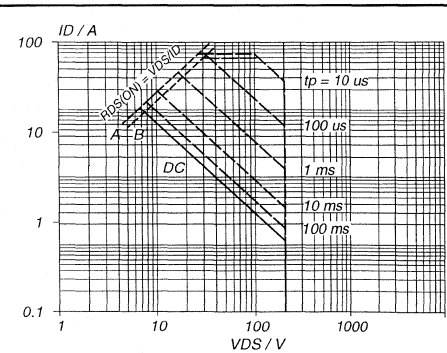


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

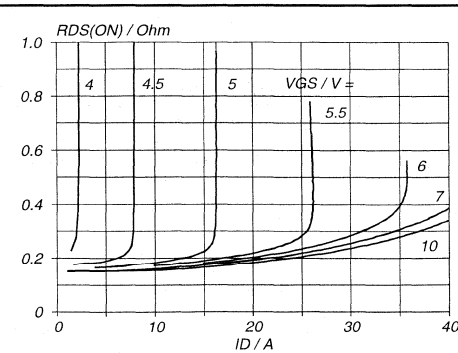


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

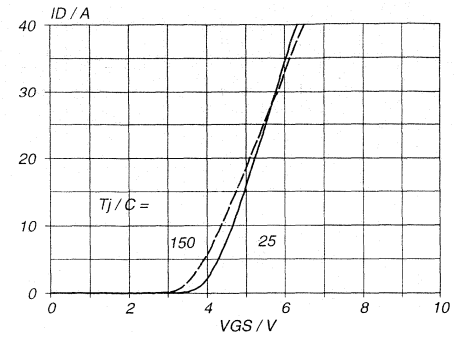


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

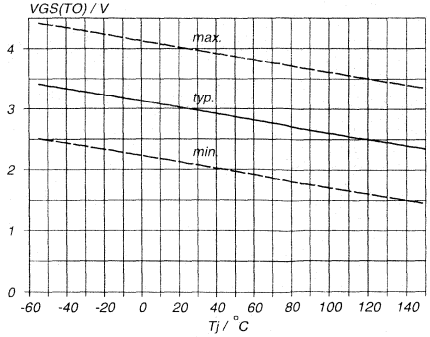


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

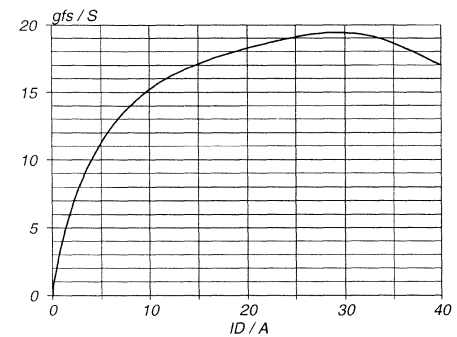


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

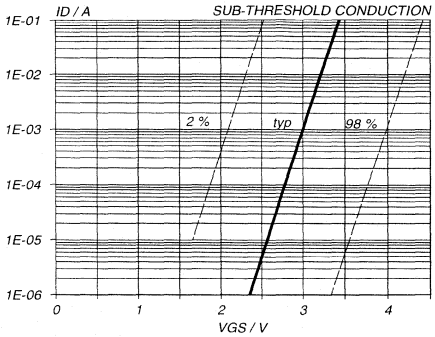


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

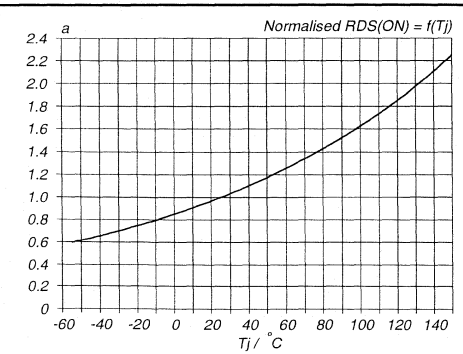


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 10 A; V_{GS} = 10 V

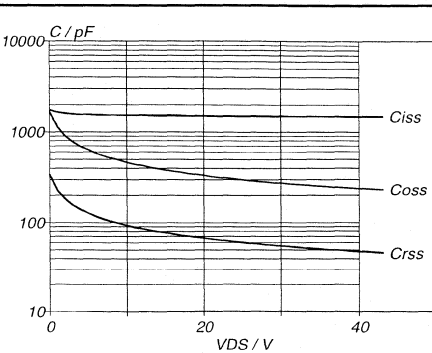


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

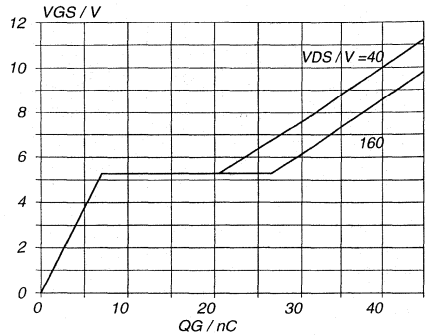


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 19$ A; parameter V_{DS}

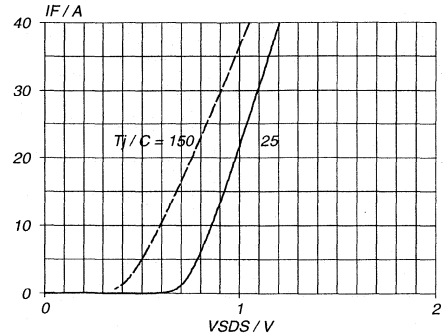


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

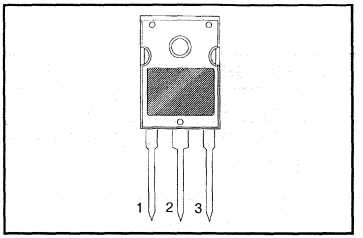
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK436	-800A	-800B	
V_{DS}	Drain-source voltage	800	800	V
I_D	Drain current (DC)	4	3.5	A
P_{tot}	Total power dissipation	125	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	3	4	Ω

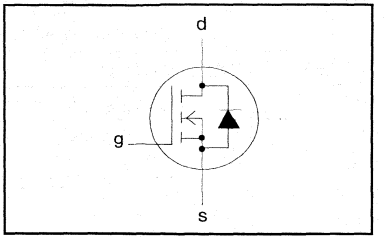
PINNING - SOT429 (TO247)

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	800		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	800		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-800A	-800B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	4.0	3.5	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	2.5	2.2	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	16	14	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	45	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	800	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j = 25 °C	-	2	20	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK436-800A**	-	2.7	3.0	Ω
		I_D = 1.5 A **BUK436-800B**	-	3.5	4.0	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1.5 A	3.0	4.3	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1000	1250	pF
C_{oss}	Output capacitance		-	80	120	pF
C_{rss}	Feedback capacitance		-	30	50	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.3 A;	-	10	25	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	130	150	ns
t_f	Turn-off fall time		-	40	60	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	12.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	4.0	A
I_{DRM}	Pulsed reverse drain current	-	-	-	16	A
V_{SD}	Diode forward voltage	I_F = 4.0 A ; V_{GS} = 0 V	-	1.0	1.3	V
t_{rr}	Reverse recovery time	I_F = 4.0 A; -dI_F/dt = 100 A/µs;	-	1800	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	12	-	µC

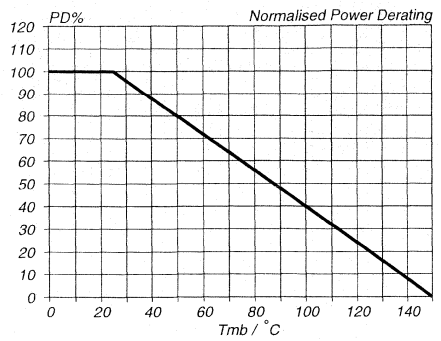


Fig.1. Normalised power dissipation.
PD% = 100·$P_D/P_{D\ 25\ °C}$ = f(T_{mb})

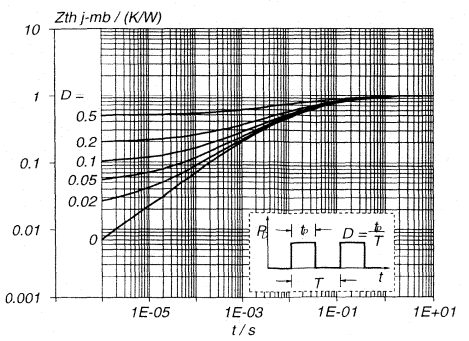


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

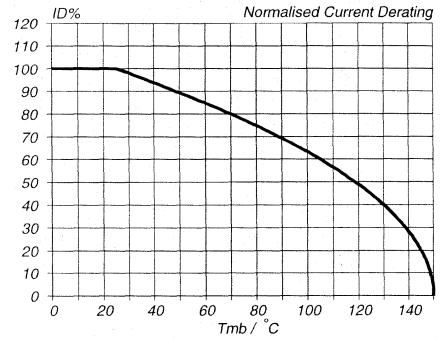


Fig.2. Normalised continuous drain current.
ID% = 100·$I_D/I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq 10$ V

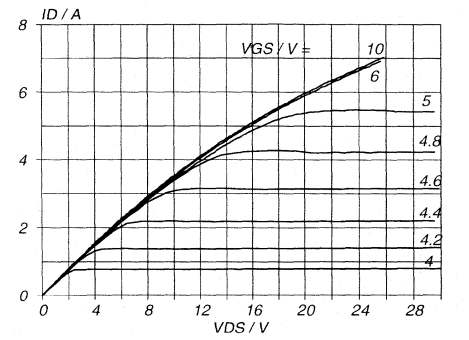


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

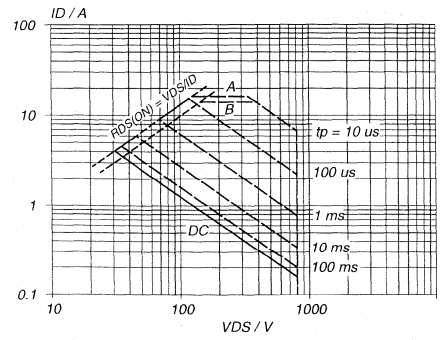


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

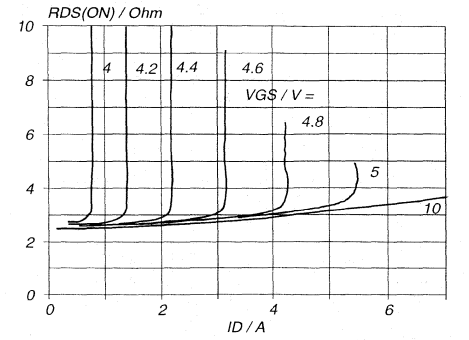


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

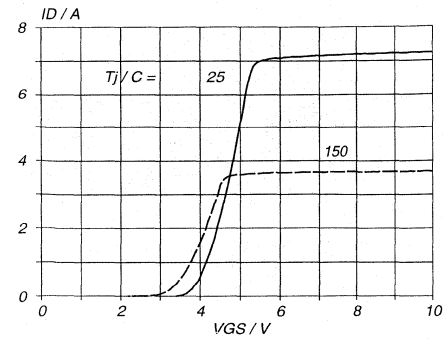


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

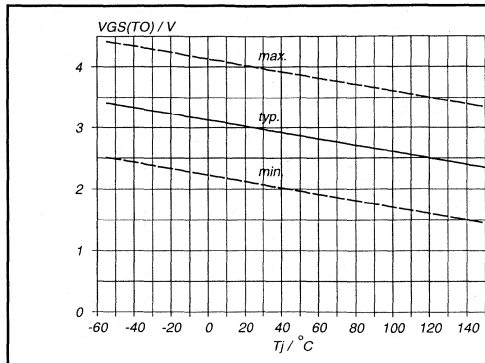


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

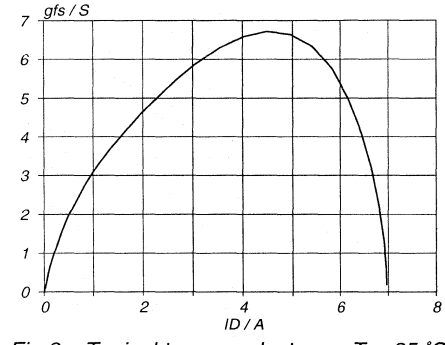


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

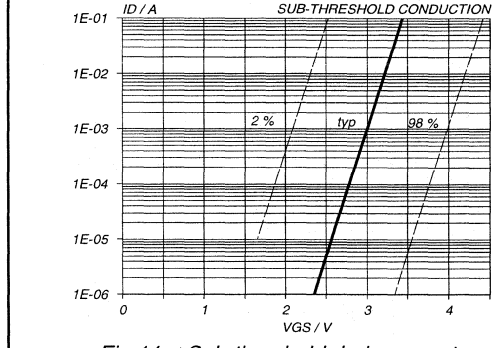


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

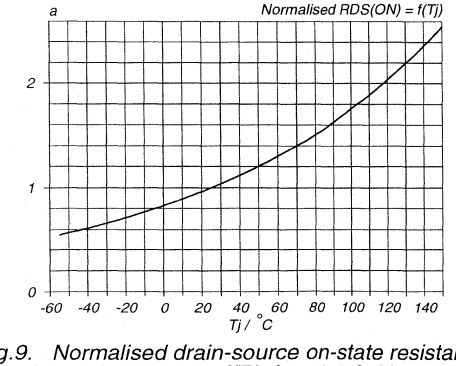


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ °C} = f(T_j)$; I_D = 1.5 A; V_{GS} = 10 V

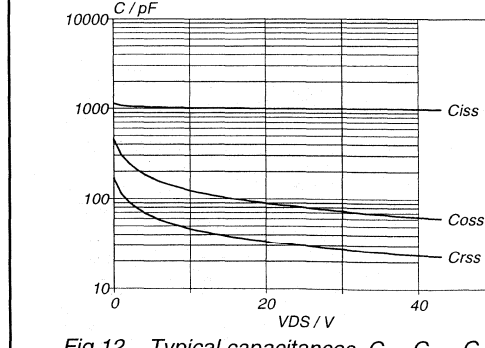


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

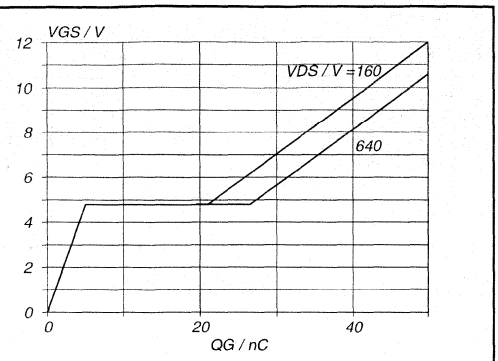


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 4$ A; parameter V_{DS}

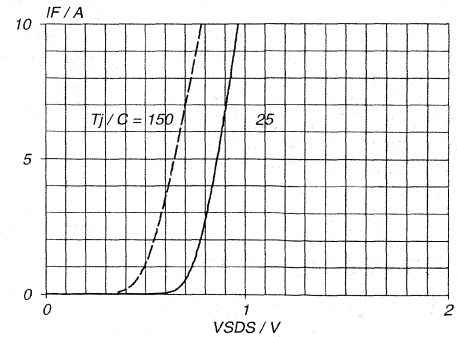


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

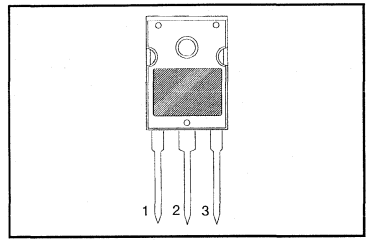
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	1000	V
I_D	Drain current (DC)	3.1	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	5	Ω

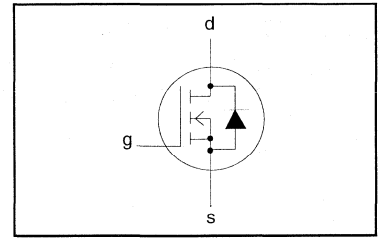
PINNING - SOT429 (TO247)

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	1000	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	1000	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	3.1	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	2.0	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	12	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Junction temperature	-	-	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	45	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	1000	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 1000 V; V_{GS} = 0 V; T_j = 25 °C	-	2	20	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 1000 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1.5 A	-	4.5	5.0	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1.5 A	3.0	4.3	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1000	1250	pF
C_{oss}	Output capacitance		-	80	120	pF
C_{rss}	Feedback capacitance		-	30	50	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.3 A;	-	10	25	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	130	150	ns
t_f	Turn-off fall time		-	40	60	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	12.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	3.5	A
I_{DRM}	Pulsed reverse drain current	-	-	-	14	A
V_{SD}	Diode forward voltage	I_F = 3.5 A ; V_{GS} = 0 V	-	1.0	1.3	V
t_{rr}	Reverse recovery time	I_F = 3.5 A; -dI_F/dt = 100 A/µs;	-	1800	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	12	-	µC

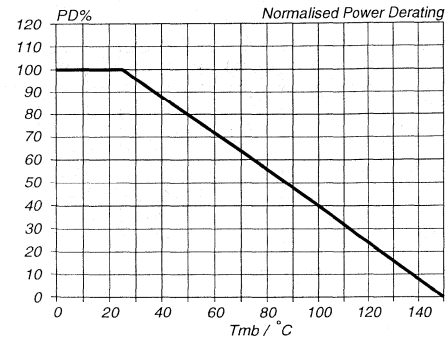


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

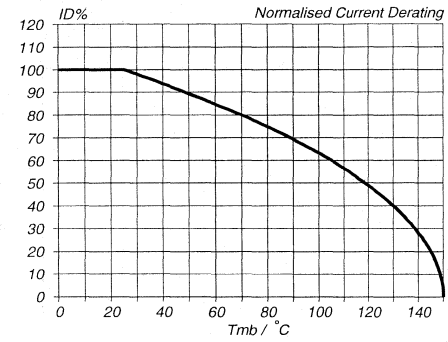


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

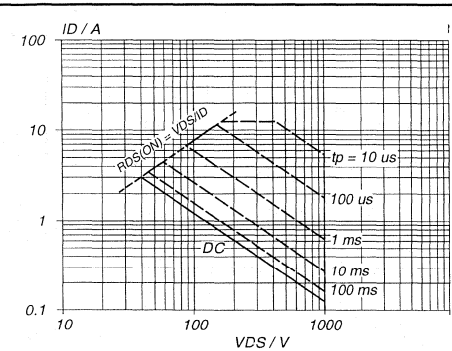


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

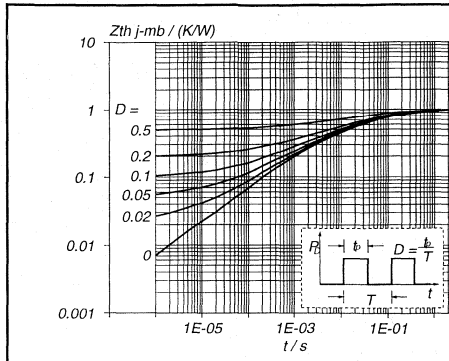


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

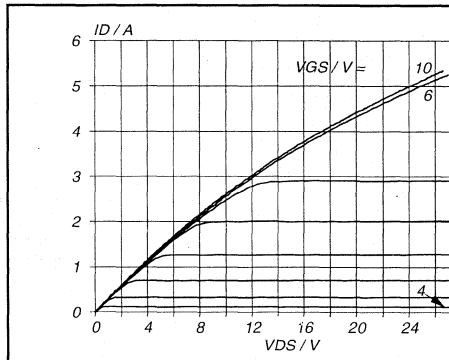


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

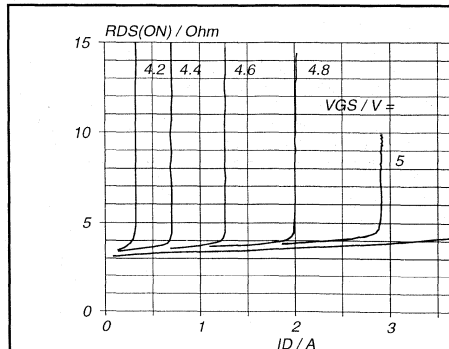


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

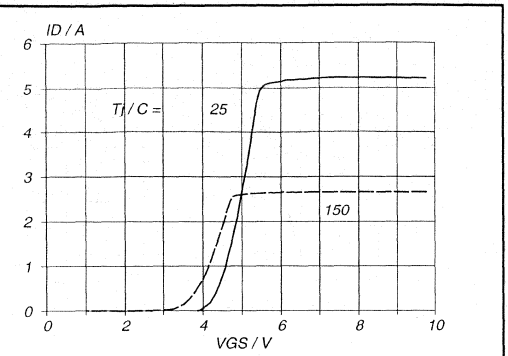


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

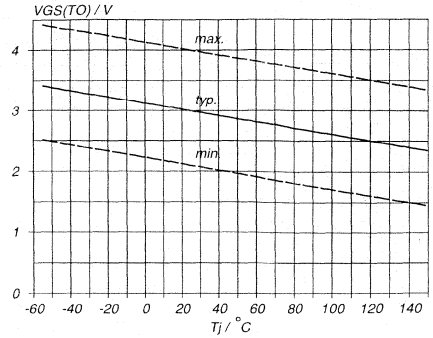


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

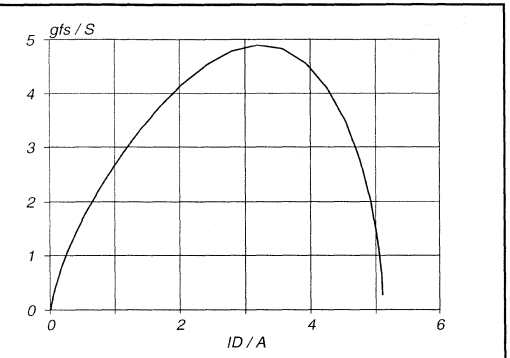


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

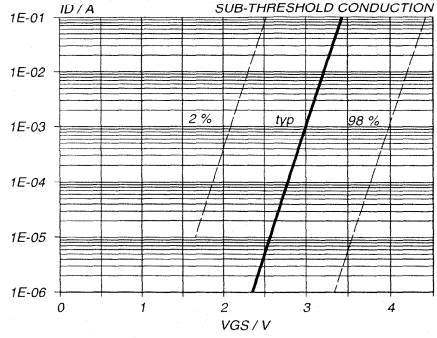


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

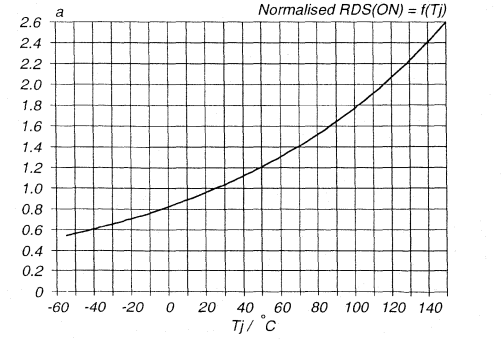


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 1.5 A; V_{GS} = 10 V

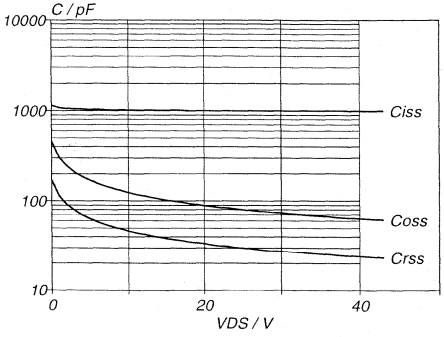


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

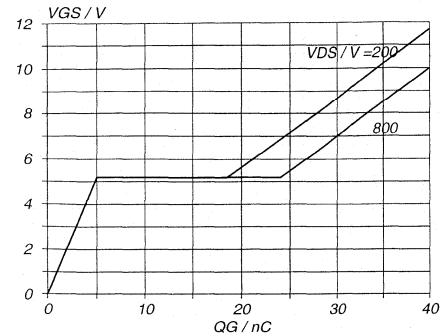


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 3.5$ A; parameter V_{DS}

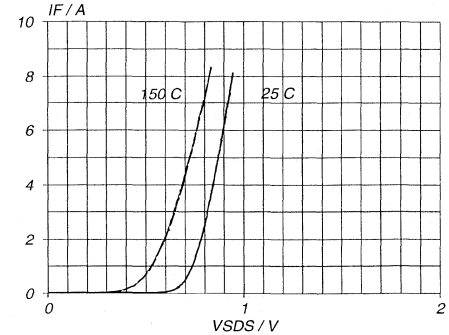


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

PowerMOS transistor — BUK438W-800A/B

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

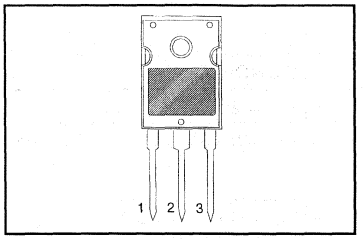
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK438	-800A	-800B	
V_{DS}	Drain-source voltage	800	800	V
I_D	Drain current (DC)	7.6	6.6	A
P_{tot}	Total power dissipation	220	220	W
$R_{DS(ON)}$	Drain-source on-state resistance	1.5	2.0	Ω

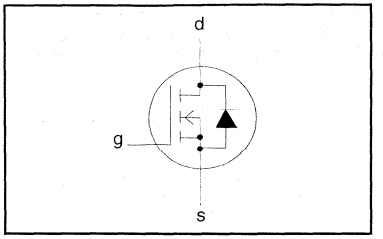
PINNING - SOT429 (TO247)

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	800		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	800		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-800A	-800B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	7.6	6.6	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	4.8	4.1	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	30	26	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	220		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	0.57	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	45	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	800	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j = 25 °C	-	5	50	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 4.0 A **BUK438-800A**	-	1.2	1.5	Ω
		BUK438-800B	-	1.6	2.0	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 4.0 A	3.0	7.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	2000	3000	pF
C_{oss}	Output capacitance		-	200	300	pF
C_{rss}	Feedback capacitance		-	100	200	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.6 A;	-	40	90	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	100	140	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	300	430	ns
t_f	Turn-off fall time		-	100	140	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	12.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	7.6	A
I_{DRM}	Pulsed reverse drain current	-	-	-	30	A
V_{SD}	Diode forward voltage	I_F = 7.6 A ;V_{GS} = 0 V	-	0.9	1.3	V
t_{rr}	Reverse recovery time	I_F = 7.6 A; -dI_F/dt = 100 A/µs;	-	1.5	-	µs
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	20	-	µC

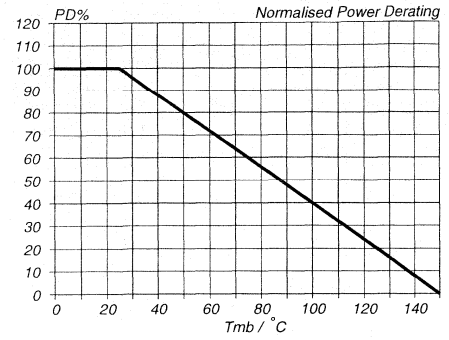


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

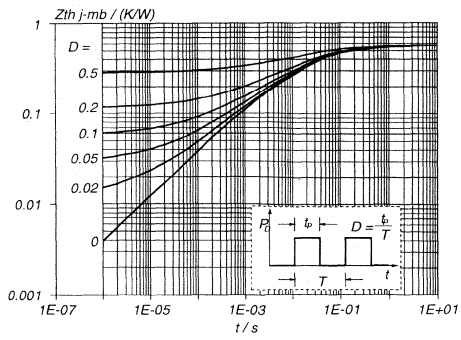


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

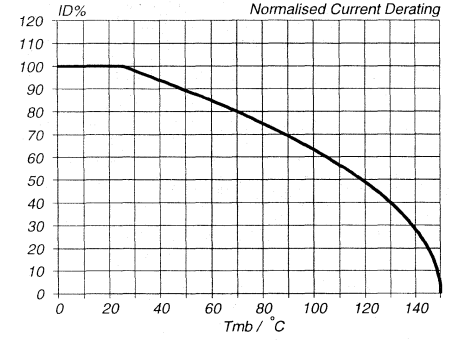


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq 10$ V

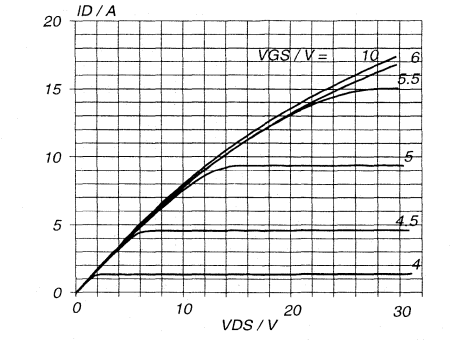


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

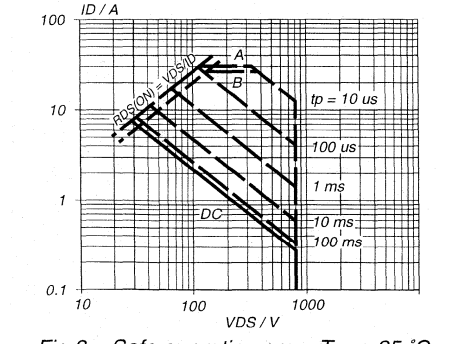


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

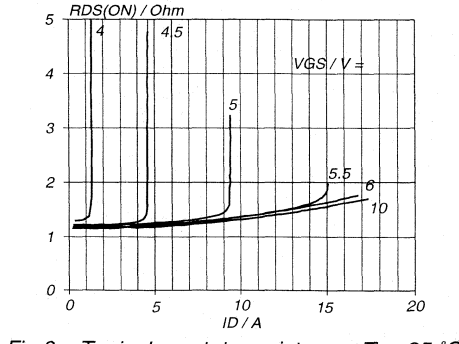


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

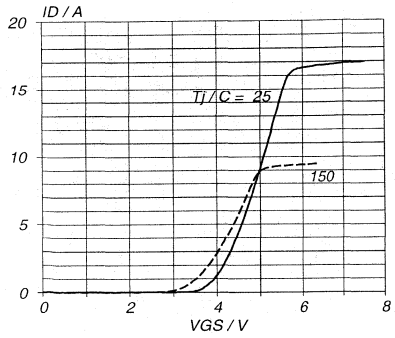


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

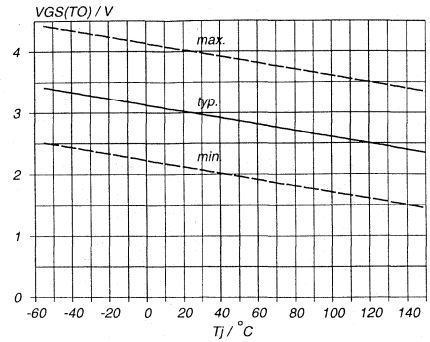


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

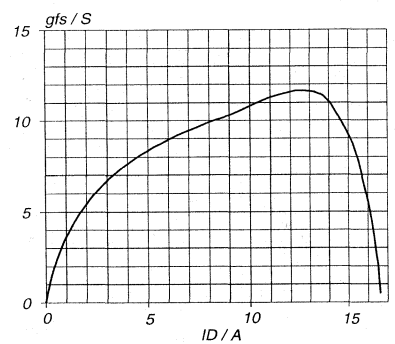


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

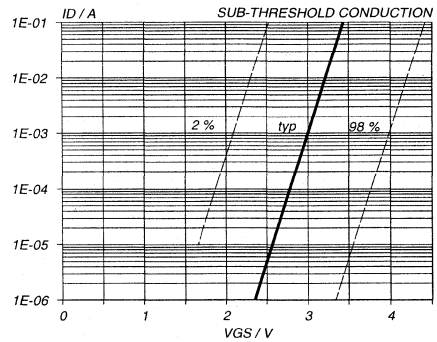


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

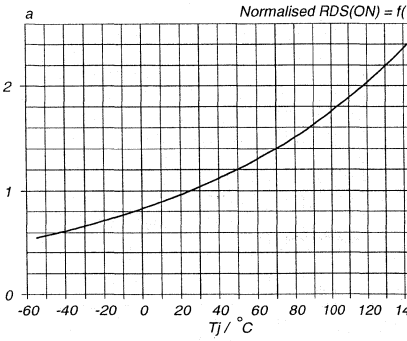


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 4 A; V_{GS} = 10 V

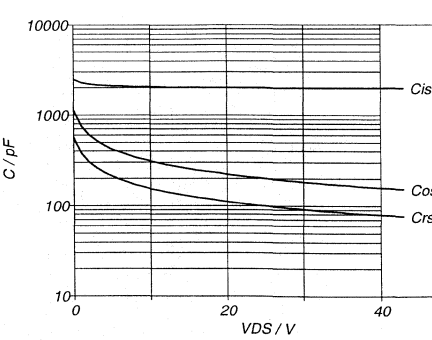


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

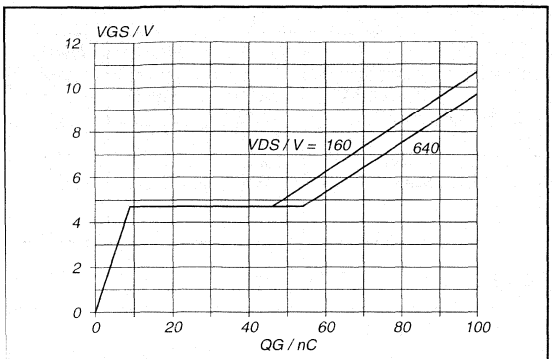


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 7.6$ A; parameter V_{DS}

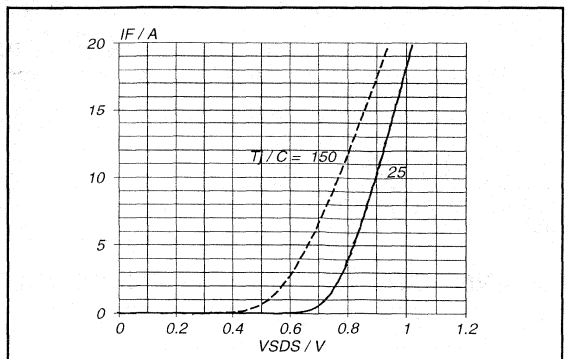


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic full-pack envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

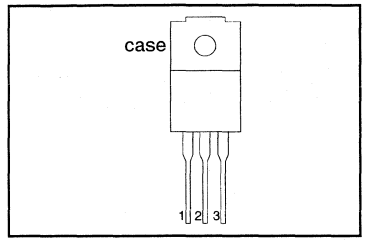
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK444	-200A	-200B	
V_{DS}	Drain-source voltage	200	200	V
I_D	Drain current (DC)	5.3	4.7	A
P_{tot}	Total power dissipation	25	25	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.4	0.5	Ω

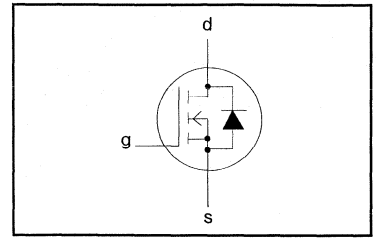
PINNING - SOT186

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	200		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-200A	-200B	
I_D	Drain current (DC)	T_{hs} = 25 °C	-	5.3	4.7	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	3.3	3.0	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	21	19	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	25		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction Temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK444-200A**	-	0.35	0.4	Ω
		I_D = 3.5 A **BUK444-200B**	-	0.4	0.5	Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 3.5 A	3.5	5.0	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	700	850	pF
C_{oss}	Output capacitance		-	100	160	pF
C_{rss}	Feedback capacitance		-	50	80	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.9 A;	-	12	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	45	70	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	80	120	ns
t_f	Turn-off fall time		-	40	60	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	5.3	A
I_{DRM}	Pulsed reverse drain current	-	-	-	21	A
V_{SD}	Diode forward voltage	I_F = 5.3 A ; V_{GS} = 0 V	-	1.1	1.3	V
t_{rr}	Reverse recovery time	I_F = 5.3 A; -dI_F/dt = 100 A/µs;	-	150	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.9	-	µC

AVALANCHE LIMITING VALUE

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 9 A ; $V_{DD} \leq$ 100 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	50	mJ

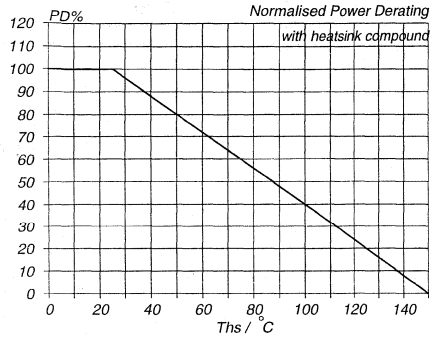


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{hs})

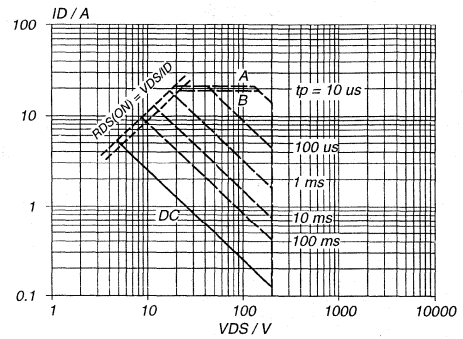


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

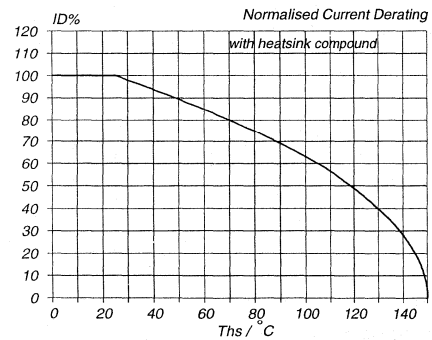


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{hs}); conditions: $V_{GS} \geq$ 10 V

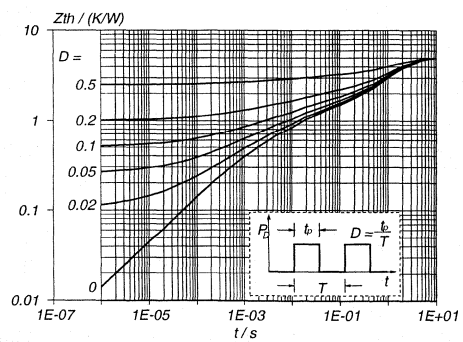


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}hs}$ = f(t); parameter D = t_p/T

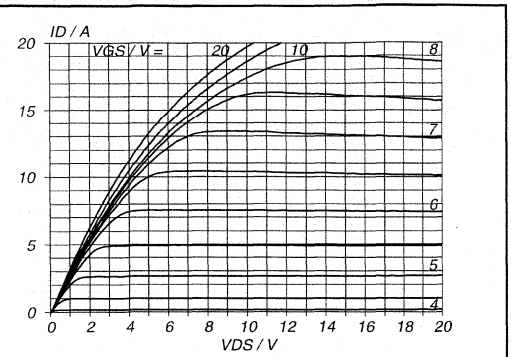


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

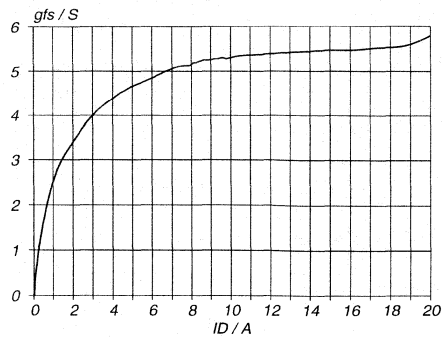


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

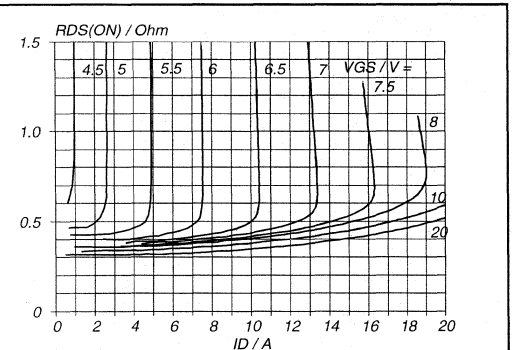


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

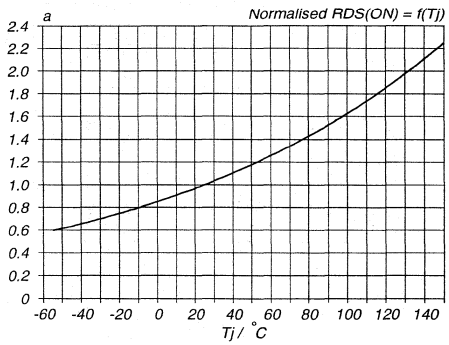


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,˚C} = f(T_j)$; I_D = 3.5 A; V_{GS} = 10 V

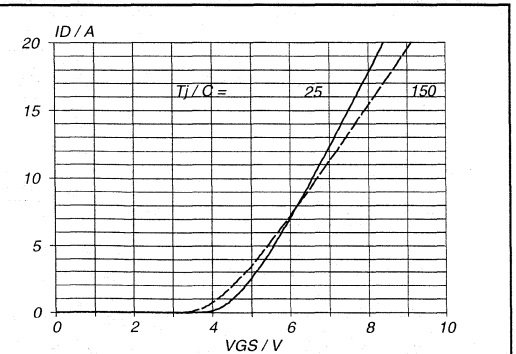


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

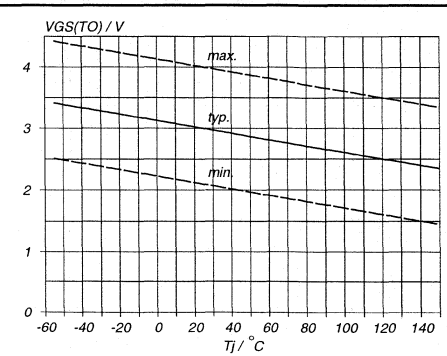


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

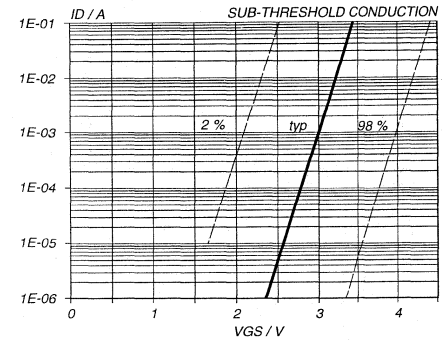


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; *conditions:* $T_j = 25$ °C; $V_{DS} = V_{GS}$

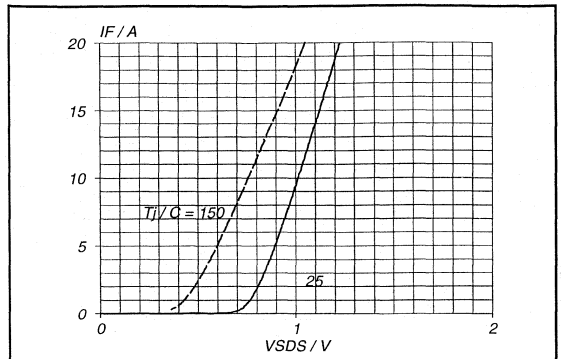


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; *conditions:* $V_{GS} = 0$ V; *parameter* T_j

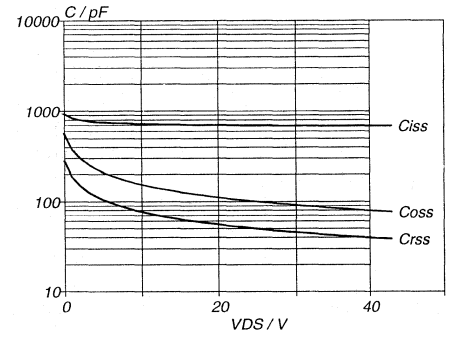


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; *conditions:* $V_{GS} = 0$ V; $f = 1$ MHz

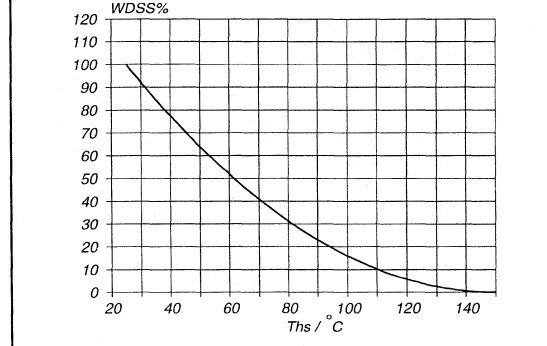


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{hs})$; *conditions:* $I_D = 9$ A

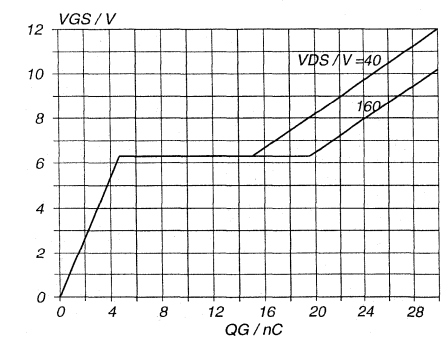


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; *conditions:* $I_D = 9$ A; *parameter* V_{DS}

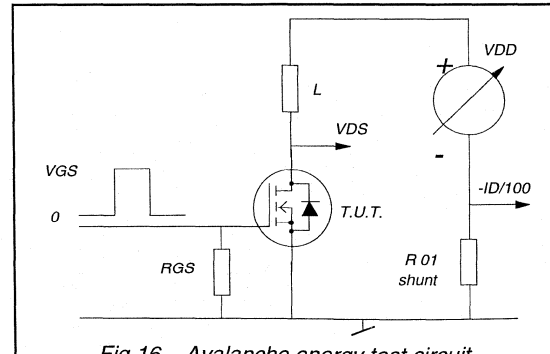


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic full-pack envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

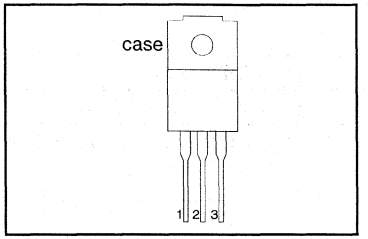
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK444	-800A	-800B	
V_{DS}	Drain-source voltage	800	800	V
I_D	Drain current (DC)	1.4	1.2	A
P_{tot}	Total power dissipation	30	30	W
$R_{DS(ON)}$	Drain-source on-state resistance	6.0	8.0	Ω

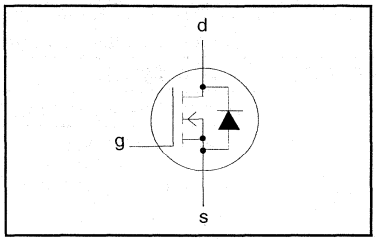
PINNING - SOT186

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	800		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	800		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-800A	-800B	
I_D	Drain current (DC)	T_{hs} = 25 °C	-	1.4	1.2	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	0.9	0.75	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	5.6	4.8	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	30		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction Temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	4.17	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	800	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j = 25 °C	-	2	20	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1.0 A **BUK444-800A**	-	5.0	6.0	Ω
		BUK444-800B	-	6.0	8.0	Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1.0 A	1.0	2.3	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	450	750	pF
C_{oss}	Output capacitance		-	42	70	pF
C_{rss}	Feedback capacitance		-	15	30	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 1.9 A;	-	15	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	50	65	ns
t_f	Turn-off fall time		-	30	40	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	1.4	A
I_{DRM}	Pulsed reverse drain current	-	-	-	5.6	A
V_{SD}	Diode forward voltage	I_F = 1.4 A ; V_{GS} = 0 V	-	1.0	1.3	V
t_{rr}	Reverse recovery time	I_F = 1.4 A; -dI_F/dt = 100 A/µs;	-	230	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	1.9	-	µC

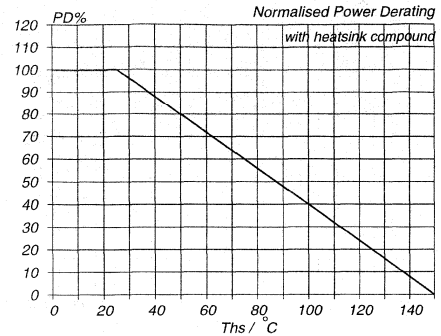


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{hs})

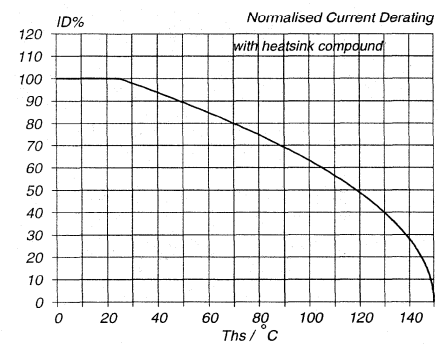


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{hs}); conditions: V_{GS} ≥ 10 V

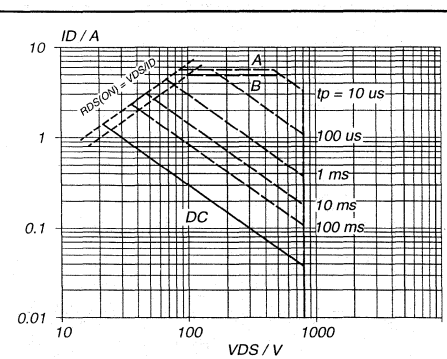


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

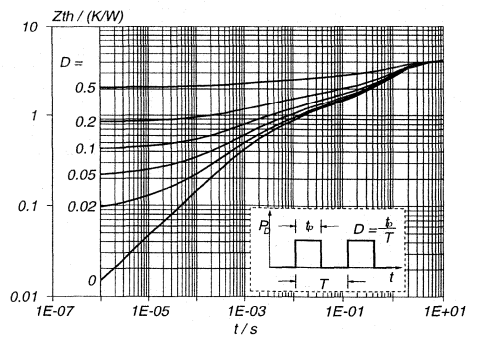


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}hs}$ = f(t); parameter D = t_p/T

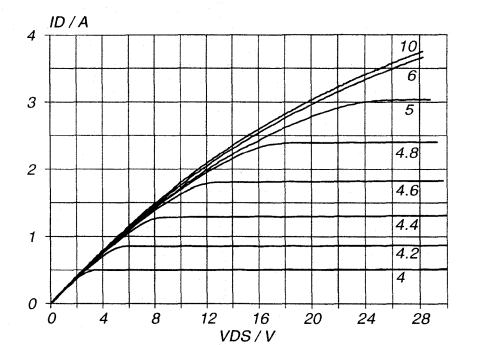


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

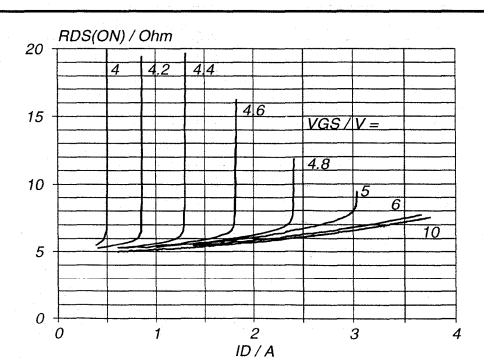


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

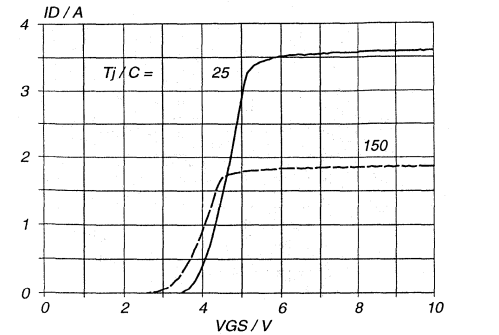


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

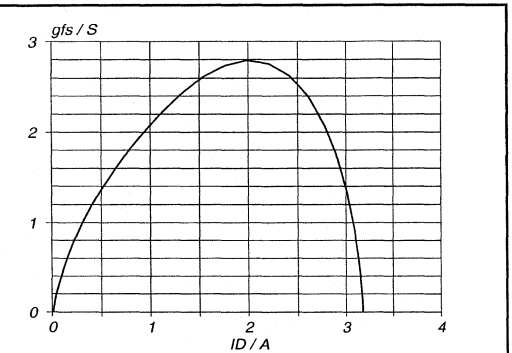


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

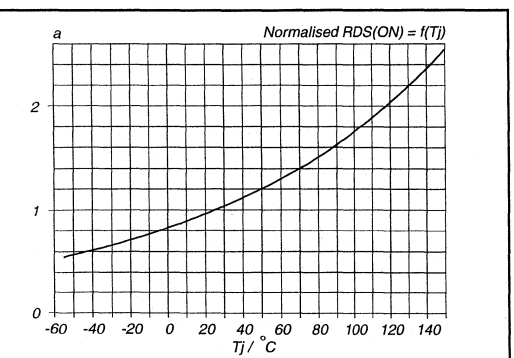


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ °C} = f(T_j)$; I_D = 1.0 A; V_{GS} = 10 V

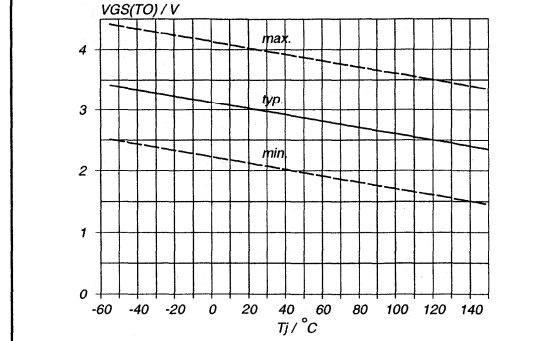


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

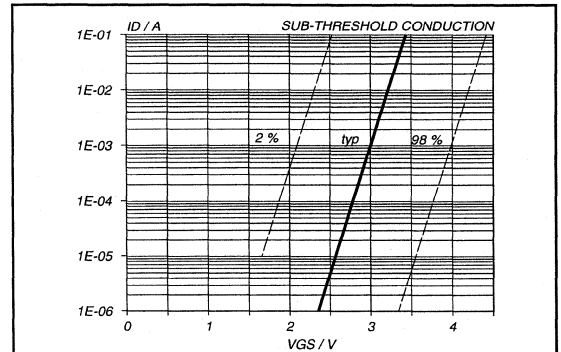


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

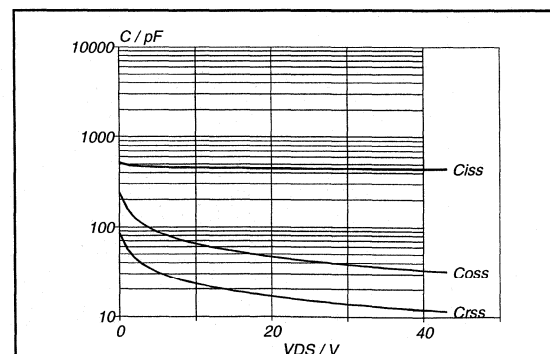


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

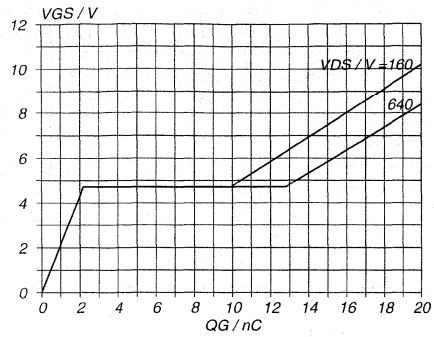


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 2.4$ A; parameter V_{DS}

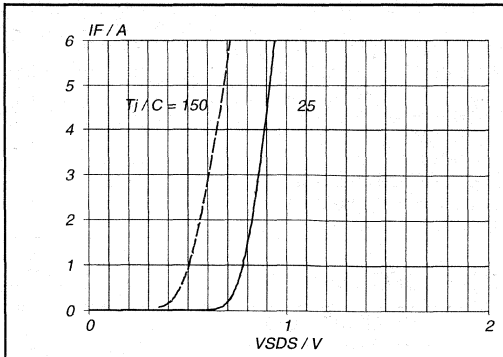


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic full-pack envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

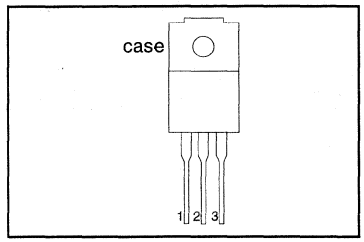
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK445	-200A	-200B	
V_{DS}	Drain-source voltage	200	200	V
I_D	Drain current (DC)	7.6	7	A
P_{tot}	Total power dissipation	30	30	W
T_j	Junction temperature	150	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.23	0.28	Ω

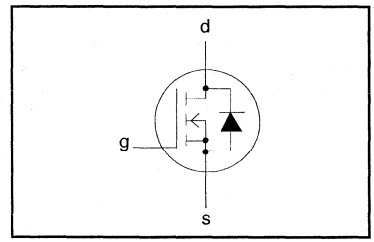
PINNING - SOT186

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	200		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-200A	-200B	
I_D	Drain current (DC)	T_{hs} = 25 °C	-	7.6	7	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	4.8	4.4	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	30	28	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	30		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction Temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	4.17	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK445-200A**	-	0.2	0.23	Ω
		I_D = 7 A **BUK445-200B**	-	0.22	0.28	Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 7 A	6	8.4	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1400	1750	pF
C_{oss}	Output capacitance		-	190	250	pF
C_{rss}	Feedback capacitance		-	55	80	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	18	30	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	35	60	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	85	120	ns
t_f	Turn-off fall time		-	35	50	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	7.6	A
I_{DRM}	Pulsed reverse drain current	-	-	-	30	A
V_{SD}	Diode forward voltage	I_F = 7.6 A ; V_{GS} = 0 V	-	1.0	1.5	V
t_{rr}	Reverse recovery time	I_F = 7.6 A; -dI_F/dt = 100 A/µs;	-	150	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	1.3	-	µC

AVALANCHE LIMITING VALUE

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 14 A ; $V_{DD} \leq$ 100 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	100	mJ

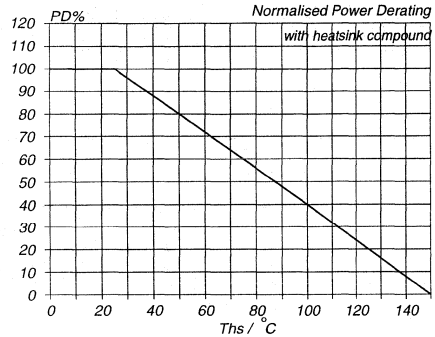


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{hs})

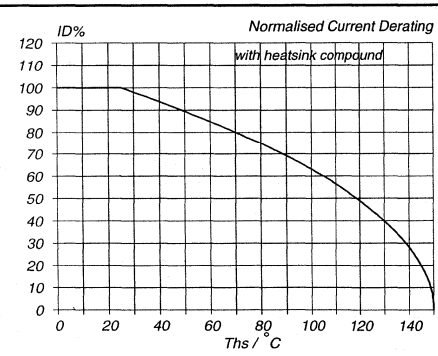


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{hs}); conditions: $V_{GS} \geq$ 10 V

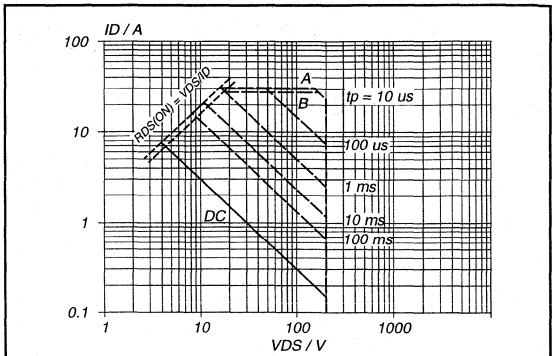


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

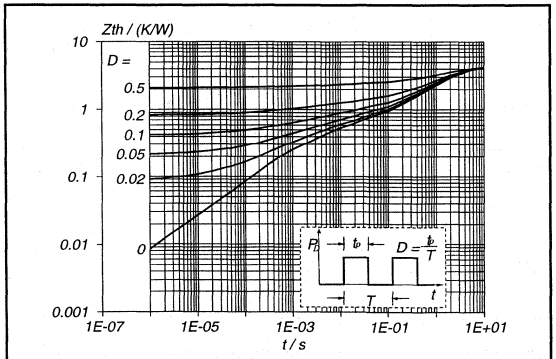


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}hs}$ = f(t); parameter D = t_p/T

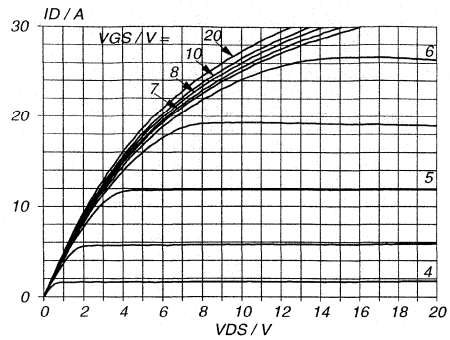


Fig.5. Typical output characteristics, T_j = 25 °C. $I_D = f(V_{DS})$; parameter V_{GS}

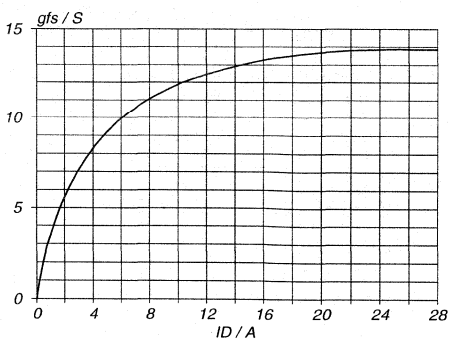


Fig.8. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

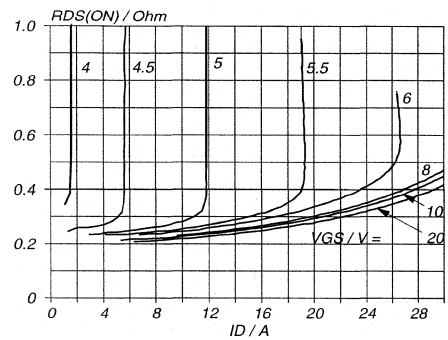


Fig.6. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

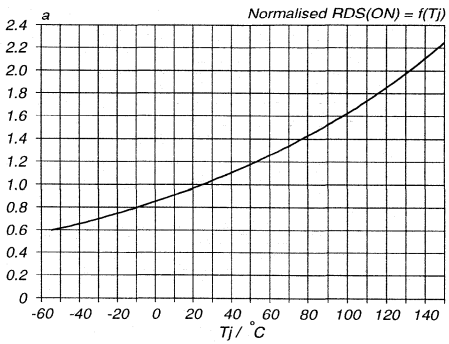


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 7 A; V_{GS} = 10 V

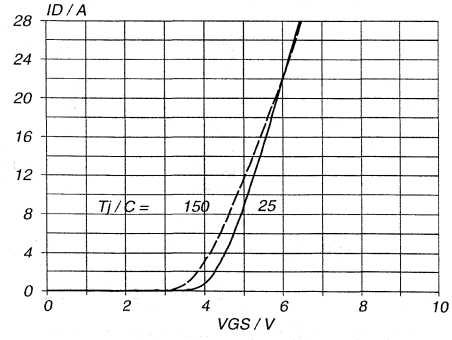


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

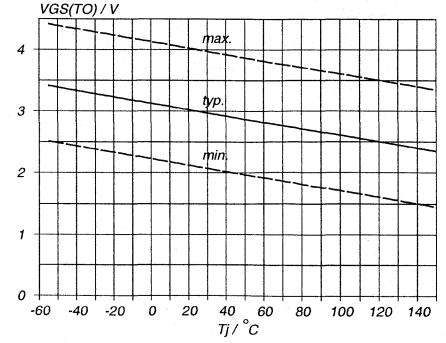


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

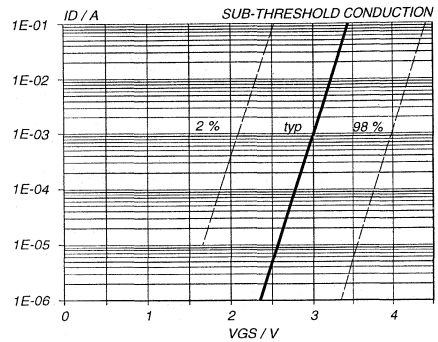


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

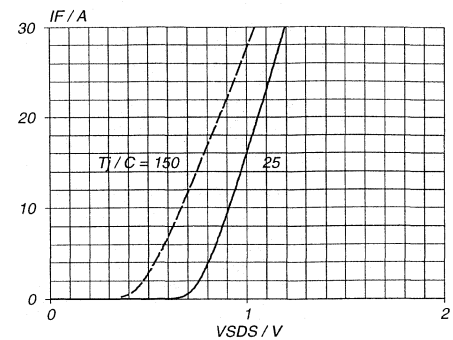


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

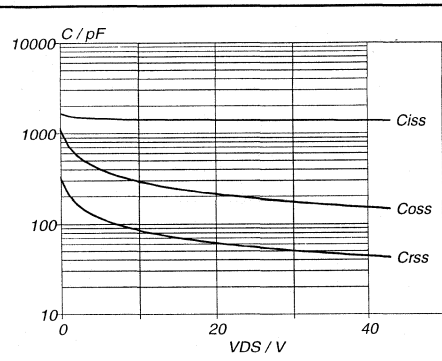


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

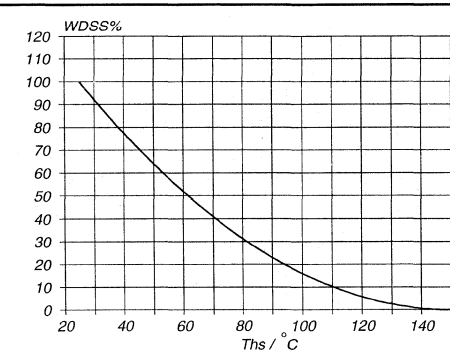


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{hs})$; conditions: I_D = 14 A

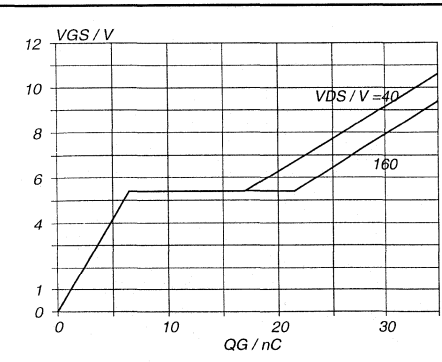


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 14 A; parameter V_{DS}

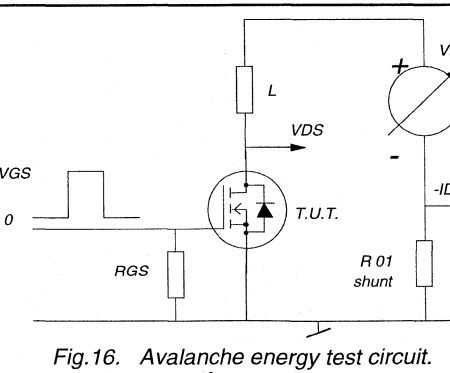


Fig.16. Avalanche energy test circuit.
$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic full-pack envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

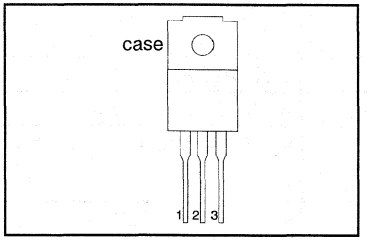
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK446	-800A	-800B	
V_{DS}	Drain-source voltage	800	800	V
I_D	Drain current (DC)	2.0	1.7	A
P_{tot}	Total power dissipation	30	30	W
$R_{DS(ON)}$	Drain-source on-state resistance	3	4	Ω

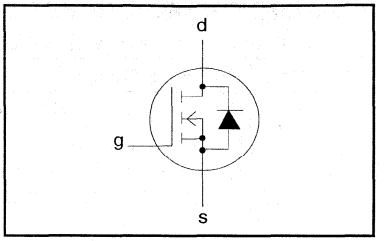
PINNING - SOT186

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	800		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	800		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-800A	-800B	
I_D	Drain current (DC)	T_{hs} = 25 °C	-	2.0	1.7	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	1.3	1.1	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	8	6.8	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	30		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction Temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	4.16	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	800	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j = 25 °C	-	2	20	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK446-800A**	-	2.7	3.0	Ω
		I_D = 1.5 A **BUK446-800B**	-	3.5	4.0	Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1.5 A	3.0	4.3	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1000	1250	pF
C_{oss}	Output capacitance		-	80	120	pF
C_{rss}	Feedback capacitance		-	30	50	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.3 A;	-	10	25	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	50	70	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	130	150	ns
t_f	Turn-off fall time		-	40	60	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	2.0	A
I_{DRM}	Pulsed reverse drain current	-	-	-	8	A
V_{SD}	Diode forward voltage	I_F = 2.0 A ; V_{GS} = 0 V	-	1.0	1.3	V
t_{rr}	Reverse recovery time	I_F = 2.0 A; -dI_F/dt = 100 A/µs;	-	1800	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	12	-	µC

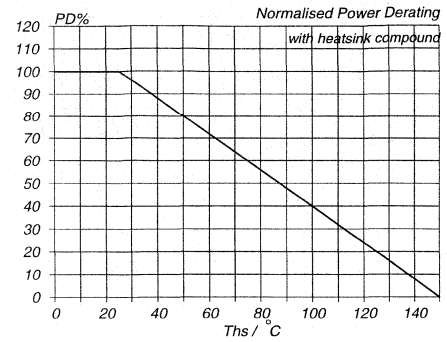


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{hs})

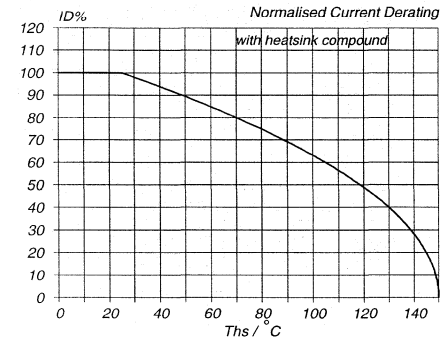


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{hs}); conditions: $V_{GS} \geq 10$ V

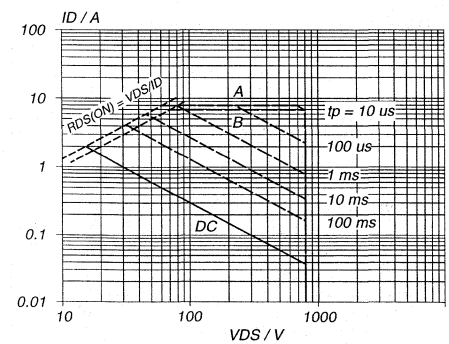


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

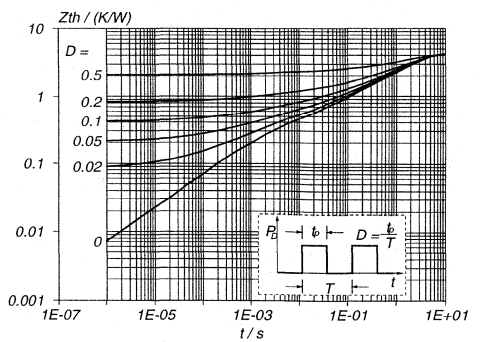


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}hs}$ = f(t); parameter D = t_p/T

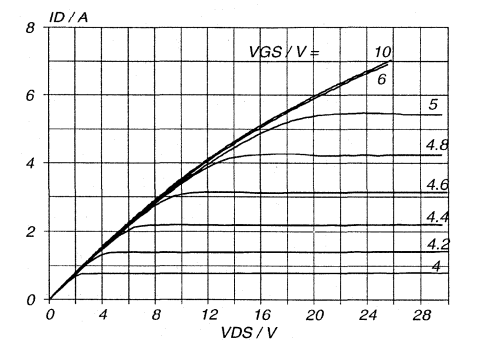


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

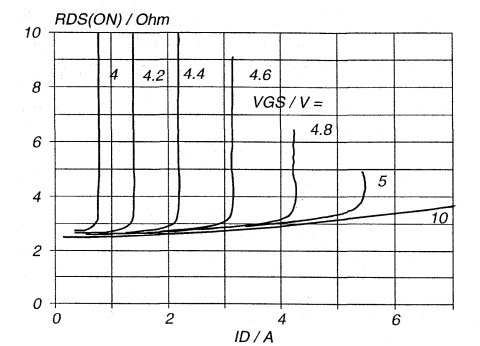


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

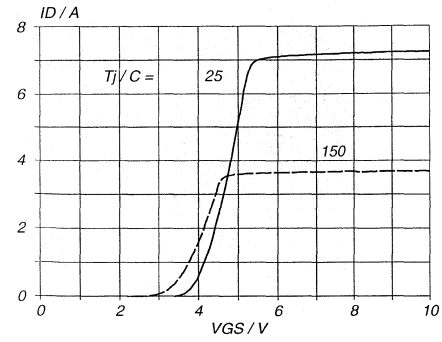


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

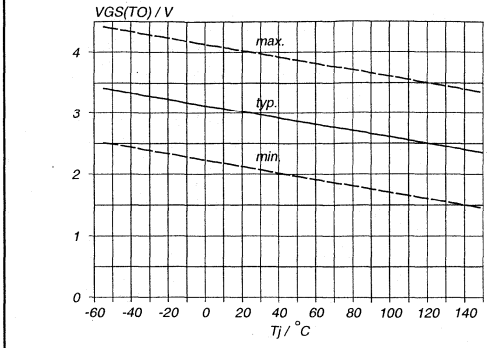


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

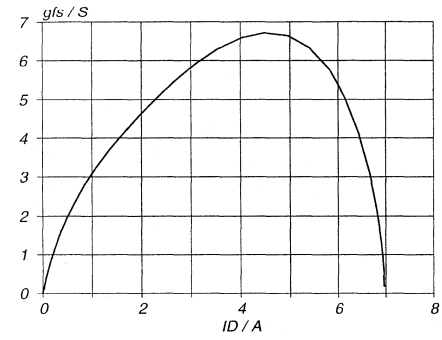


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

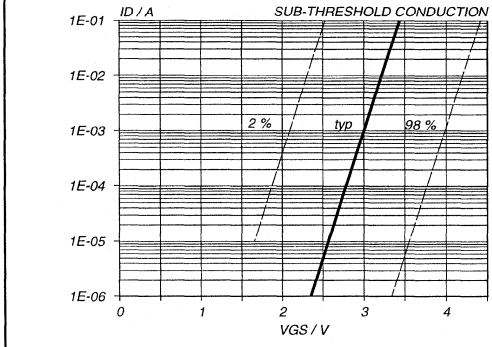


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

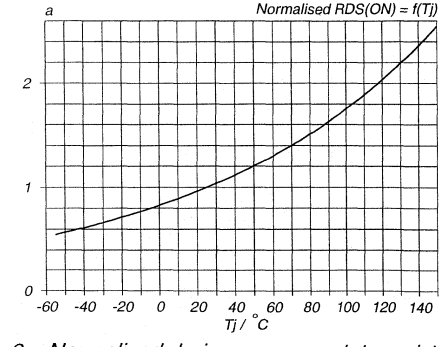


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ °C} = f(T_j)$; I_D = 1.5 A; V_{GS} = 10 V

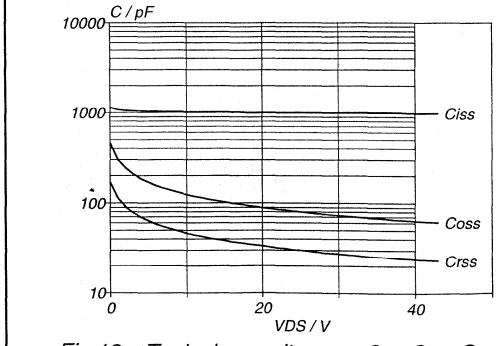


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

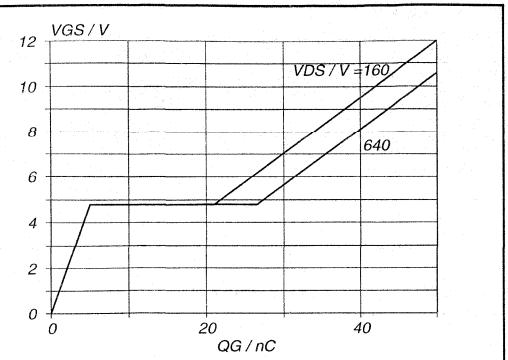


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 4$ A; parameter V_{DS}

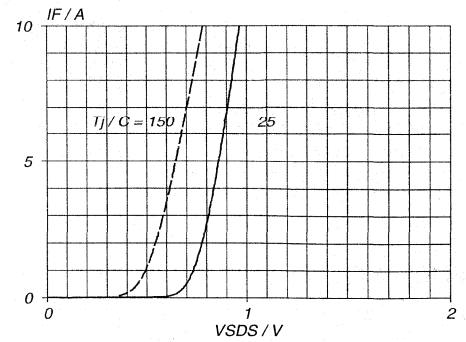


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic full-pack envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

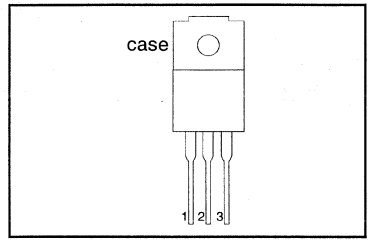
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	1000	V
I_D	Drain current (DC)	1.5	A
P_{tot}	Total power dissipation	30	W
$R_{DS(ON)}$	Drain-source on-state resistance	5	Ω

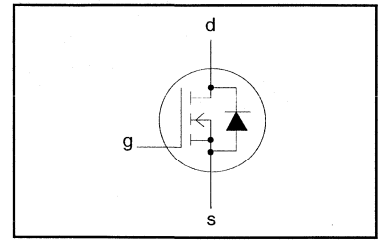
PINNING - SOT186

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	1000	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	1000	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{hs} = 25 °C	-	1.5	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	1.0	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	6	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	30	W
T_{stg}	Storage temperature	-	- 55	150	°C
T_j	Junction Temperature	-	-	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	4.16	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	1000	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 1000 V; V_{GS} = 0 V; T_j = 25 °C	-	2	20	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 1000 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1.5 A	-	4.5	5.0	Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1.5 A	3.0	4.3	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1000	1250	pF
C_{oss}	Output capacitance		-	80	120	pF
C_{rss}	Feedback capacitance		-	30	50	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.3 A;	-	10	25	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	50	70	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	130	150	ns
t_f	Turn-off fall time		-	40	60	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	1.7	A
I_{DRM}	Pulsed reverse drain current	-	-	-	6.8	A
V_{SD}	Diode forward voltage	I_F = 1.7 A ; V_{GS} = 0 V	-	1.0	1.3	V
t_{rr}	Reverse recovery time	I_F = 1.7 A; -dI_F/dt = 100 A/µs;	-	1800	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	12	-	µC

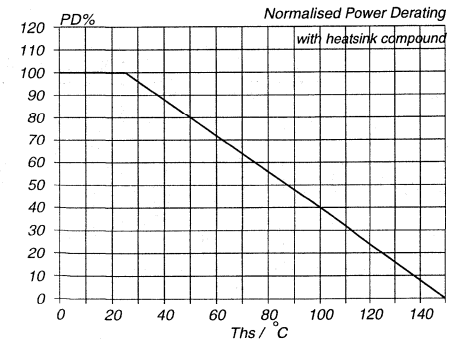


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{hs})

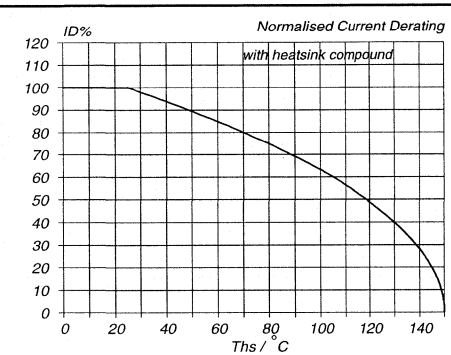


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{hs}); conditions: V_{GS} ≥ 10 V

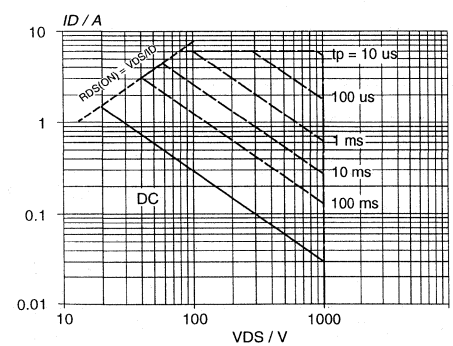


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

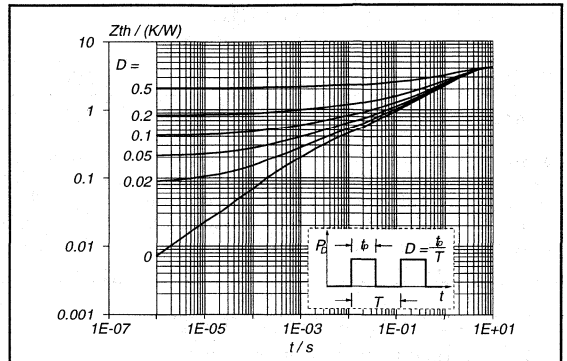


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}hs}$ = f(t); parameter D = t_p/T

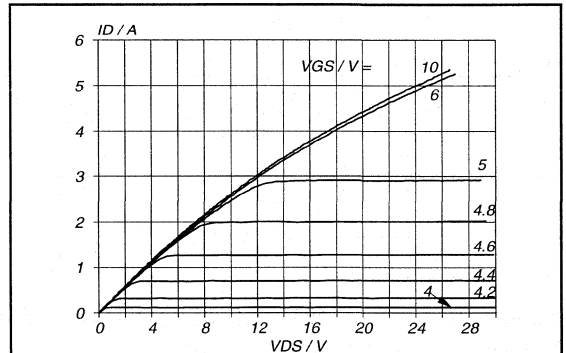


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

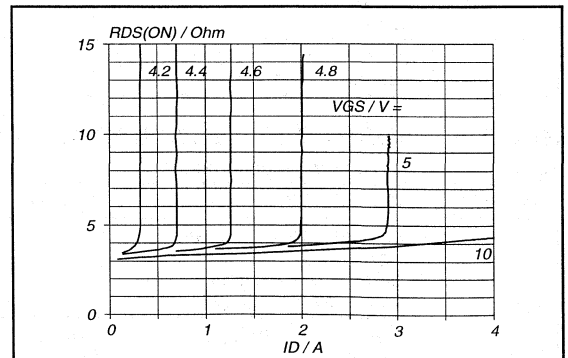


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

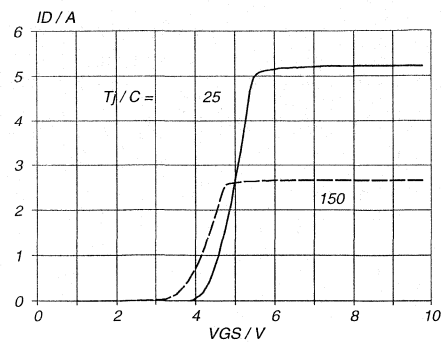


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

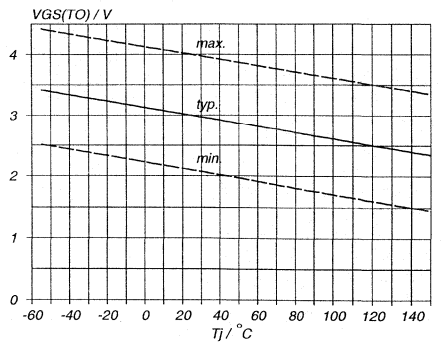


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

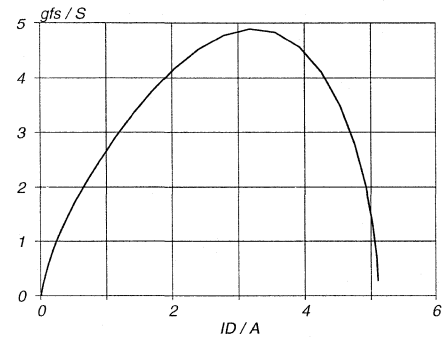


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

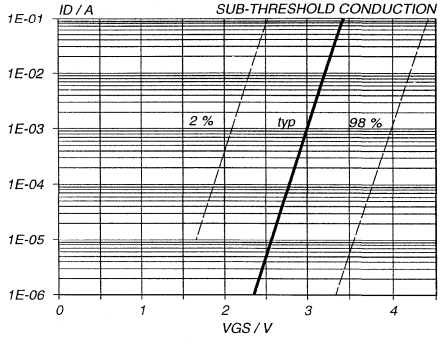


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

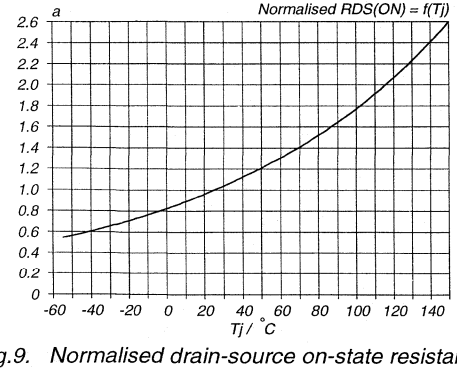


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 1.5 A; V_{GS} = 10 V

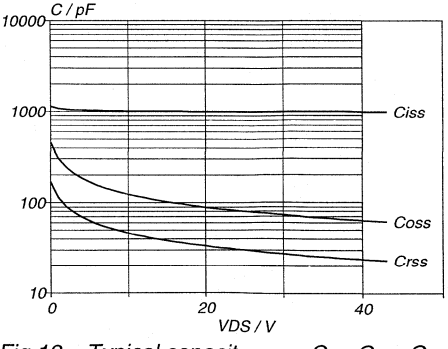


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

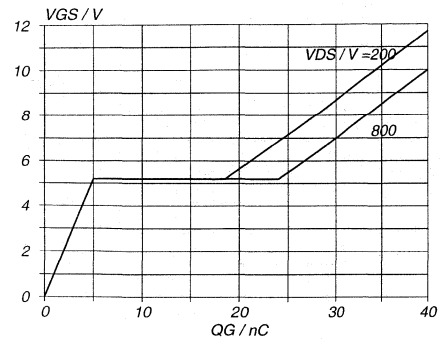


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 3.5$ A; parameter V_{DS}

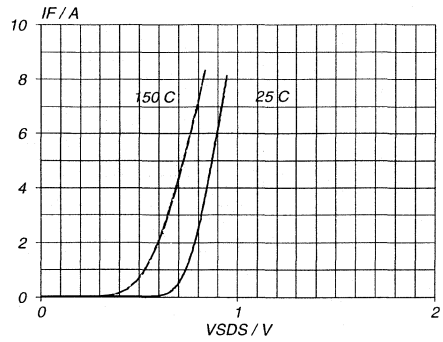


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

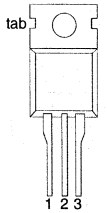
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK452	-100A	-100B	
V_{DS}	Drain-source voltage	100	100	V
I_D	Drain current (DC)	11	10	A
P_{tot}	Total power dissipation	60	60	W
T_j	Junction temperature	175	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.25	0.3	Ω

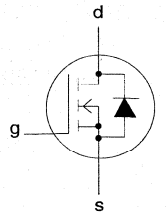
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	100		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-100A	-100B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	11	10	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	7.7	7	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	44	40	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	60		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction Temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK452-100A** I_D = 5.5 A **BUK452-100B**	- -	0.22 0.25	0.25 0.3	Ω Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5.5 A	3	4.2	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	400	500	pF
C_{oss}	Output capacitance		-	90	120	pF
C_{rss}	Feedback capacitance		-	35	50	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	9	14	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	30	45	ns
t_f	Turn-off fall time		-	20	40	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	11	A
I_{DRM}	Pulsed reverse drain current	-	-	-	44	A
V_{SD}	Diode forward voltage	I_F = 11 A ; V_{GS} = 0 V	-	1.2	1.5	V
t_{rr}	Reverse recovery time	I_F = 11 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.35	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 11 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	35	mJ

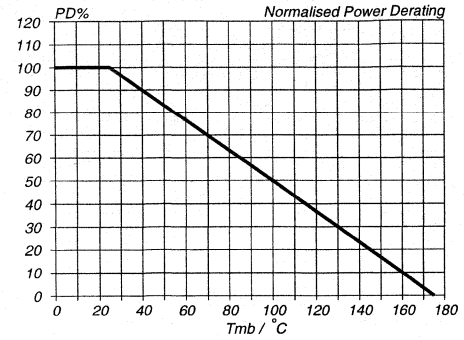


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

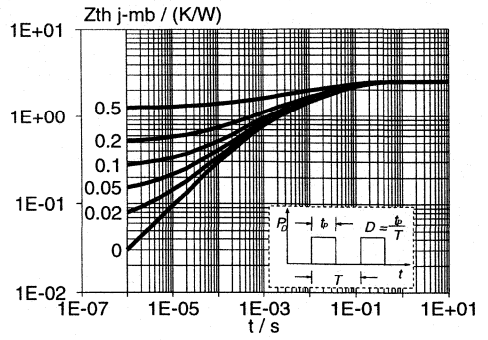


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

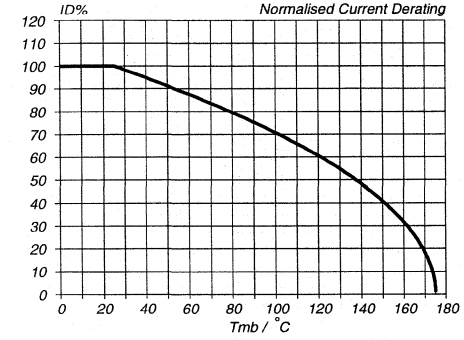


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

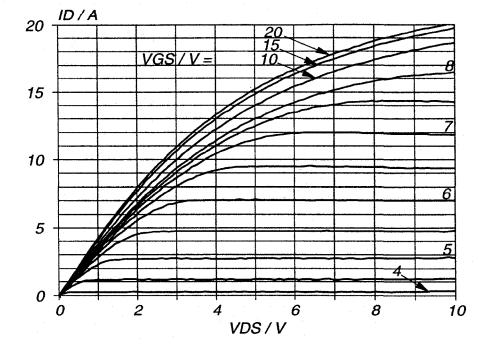


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

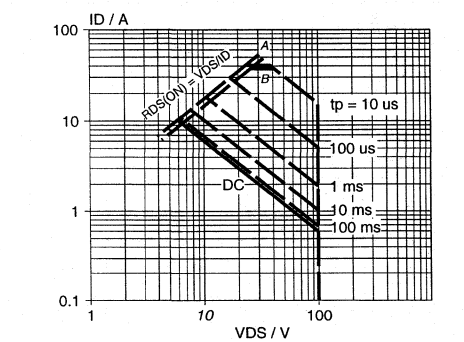


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

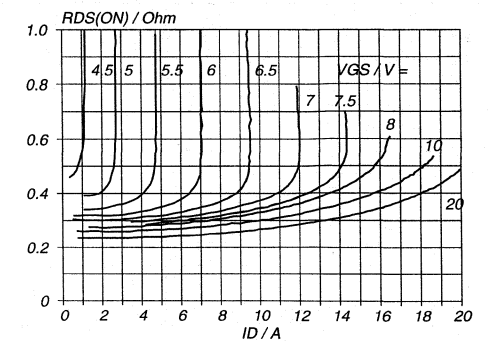


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

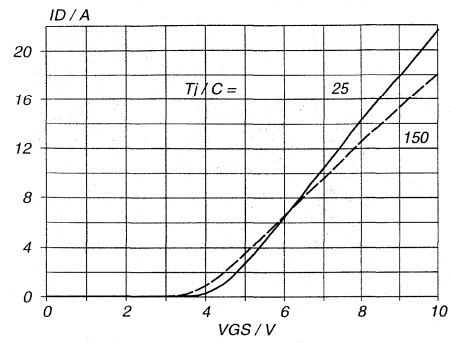


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

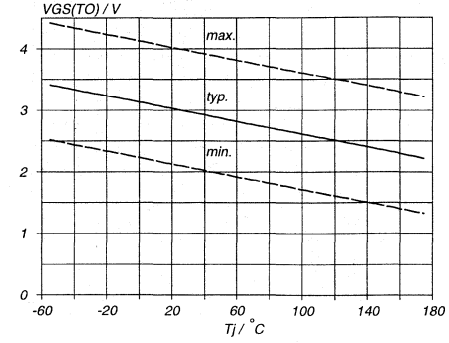


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

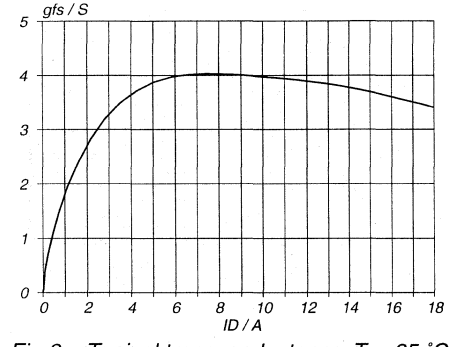


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

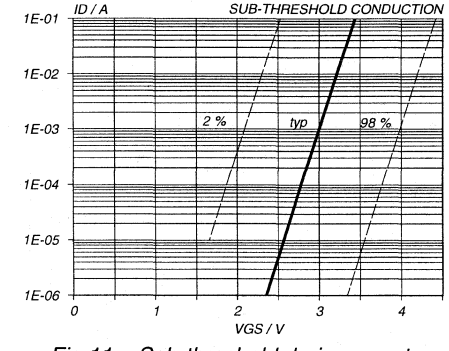


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

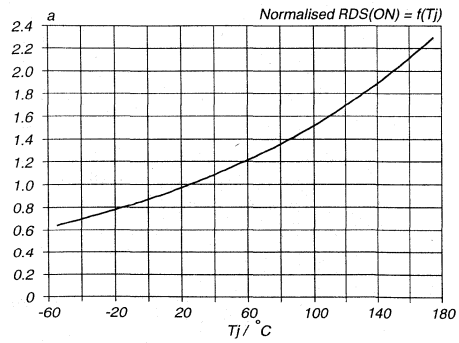


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ °C} = f(T_j)$; I_D = 5.5 A; V_{GS} = 10 V

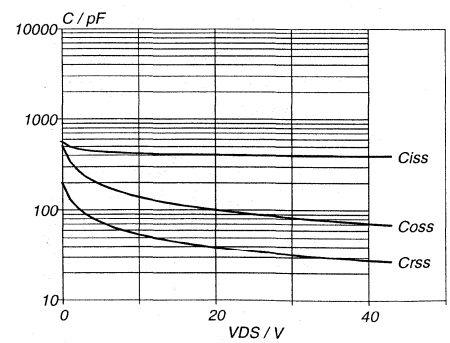


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

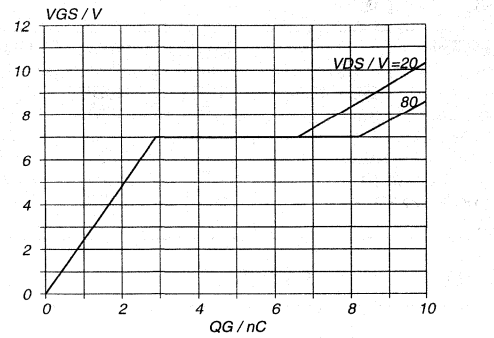


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 11 A; parameter V_{DS}

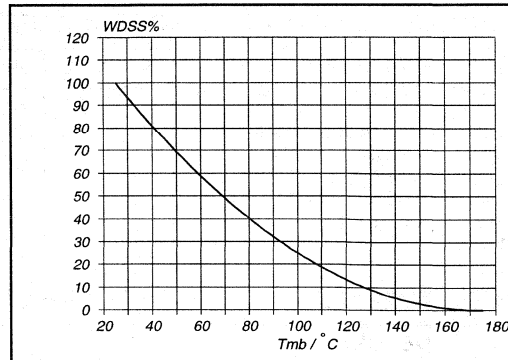


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: I_D = 11 A

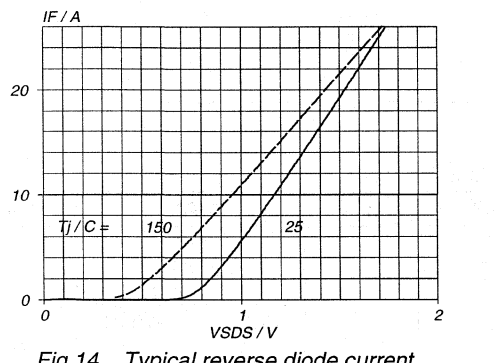


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

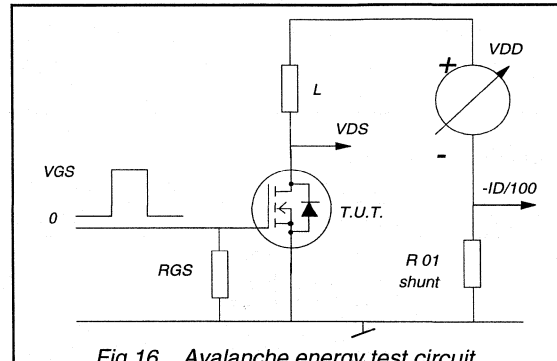


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

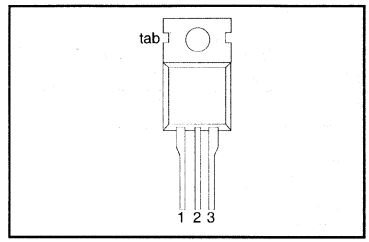
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK453	-100A	-100B	
V_{DS}	Drain-source voltage	100	100	V
I_D	Drain current (DC)	14	13	A
P_{tot}	Total power dissipation	75	75	W
T_j	Junction temperature	175	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.16	0.20	Ω

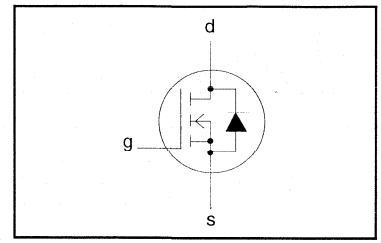
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	100		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-100A	-100B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	14	13	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	10	9	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	56	52	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	75		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction Temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK453-100A**	-	0.15	0.16	Ω
		I_D = 5 A **BUK453-100B**	-	0.15	0.20	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5 A	4.0	5.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	660	825	pF
C_{oss}	Output capacitance		-	140	200	pF
C_{rss}	Feedback capacitance		-	60	100	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	10	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	60	90	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	14	A
I_{DRM}	Pulsed reverse drain current	-	-	-	56	A
V_{SD}	Diode forward voltage	I_F = 14 A ; V_{GS} = 0 V	-	1.2	1.5	V
t_{rr}	Reverse recovery time	I_F = 14 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.6	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 14 A ; V_{DD} ≤ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	70	mJ

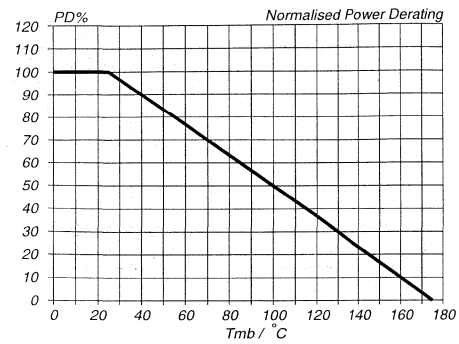


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

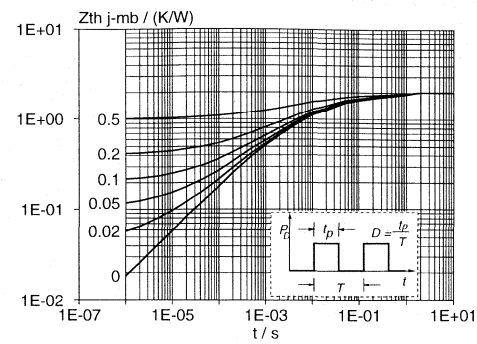


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

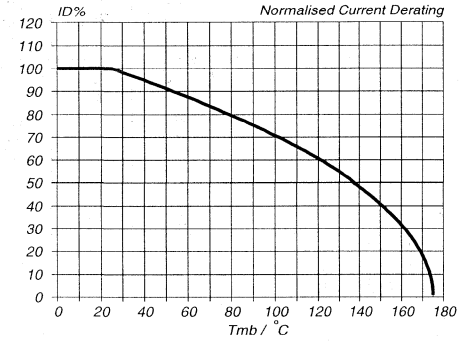


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

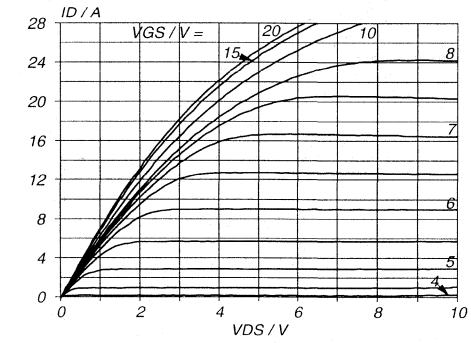


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

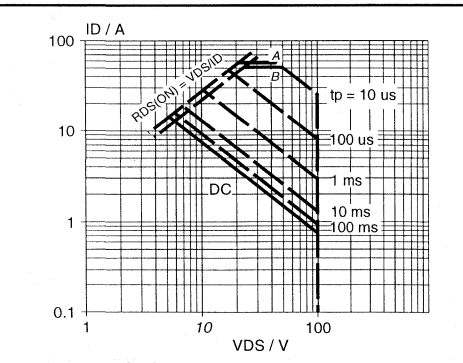


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

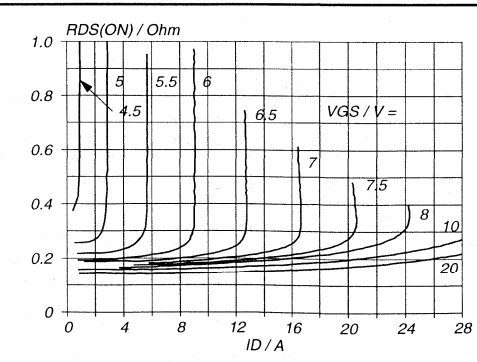


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

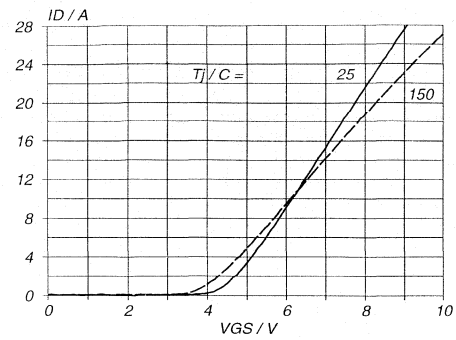


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

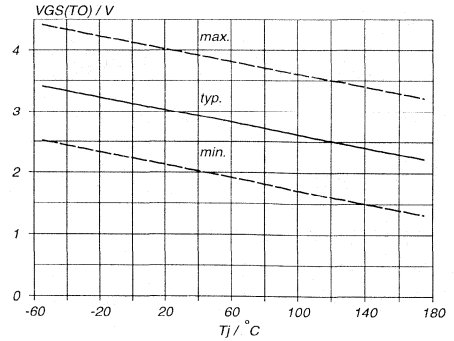


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

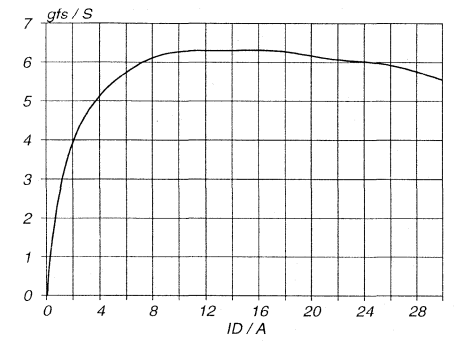


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

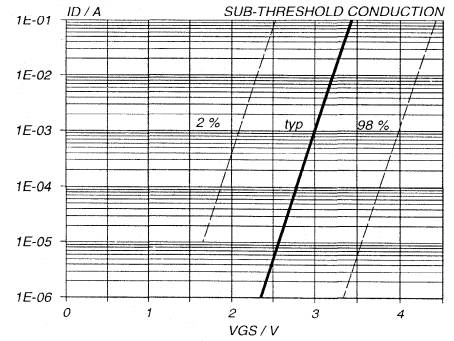


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

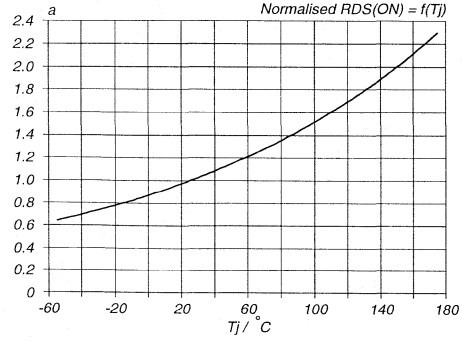


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ °C} = f(T_j)$; I_D = 5 A; V_{GS} = 10 V

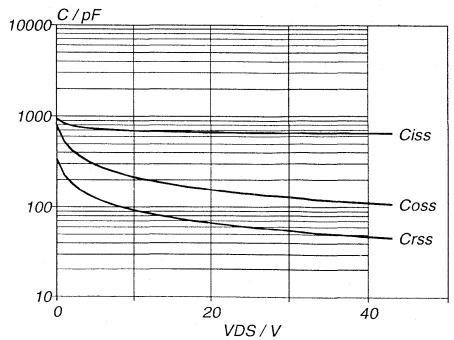


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

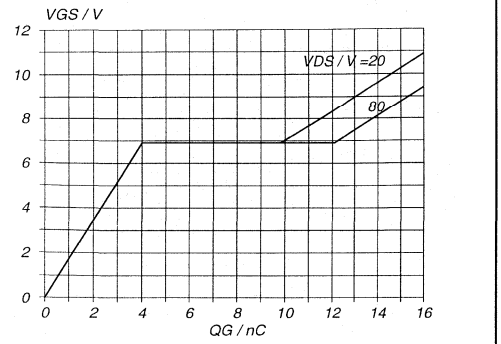


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 14 A; parameter V_{DS}

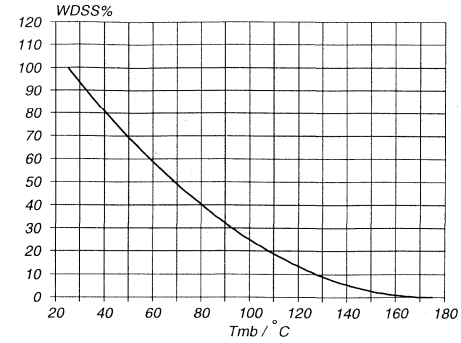


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: I_D = 14 A

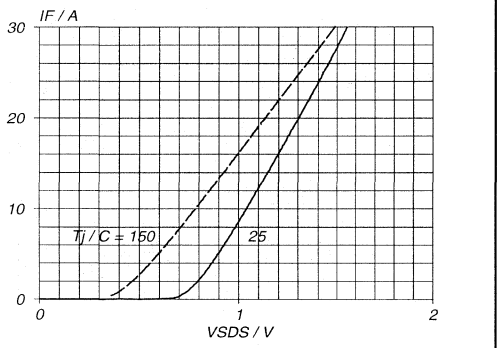


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

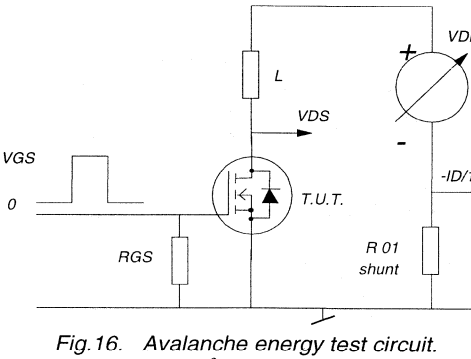


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor — BUK454-200A/B

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for use in surface mount applications.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

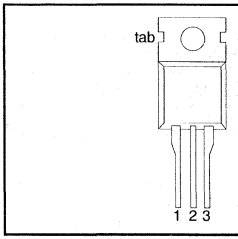
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (DC)	9.2	A
P_{tot}	Total power dissipation	90	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.4	Ω

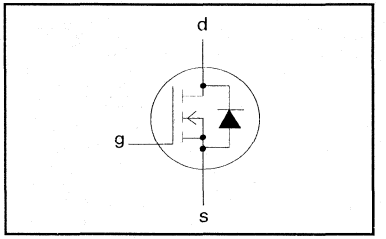
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	200		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-200A	**-200B**	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	9.2	8.2	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	6.5	5.8	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	36	33	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	90		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction Temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.67	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK454-200A**	-	0.35	0.4	Ω
		I_D = 3.5 A **BUK454-200B**	-	0.4	0.5	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 3.5 A	3.5	5.0	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	700	850	pF
C_{oss}	Output capacitance		-	100	160	pF
C_{rss}	Feedback capacitance		-	50	80	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.9 A;	-	12	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	45	70	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	80	120	ns
t_f	Turn-off fall time		-	40	60	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	9.2	A
I_{DRM}	Pulsed reverse drain current	-	-	-	36	A
V_{SD}	Diode forward voltage	I_F = 9.2 A ; V_{GS} = 0 V	-	1.1	1.3	V
t_{rr}	Reverse recovery time	I_F = 9.2 A; -dI_F/dt = 100 A/µs;	-	180	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	1.2	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 9 A ; $V_{DD} \leq$ 100 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	50	mJ

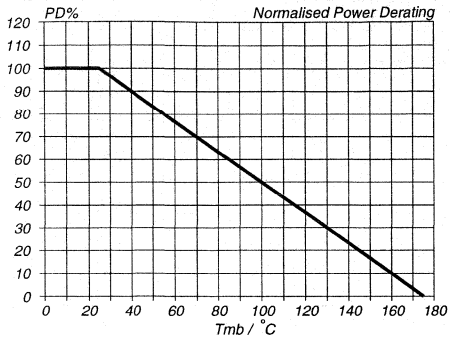


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D / P_{D\,25\,°C} = f(T_{mb})$

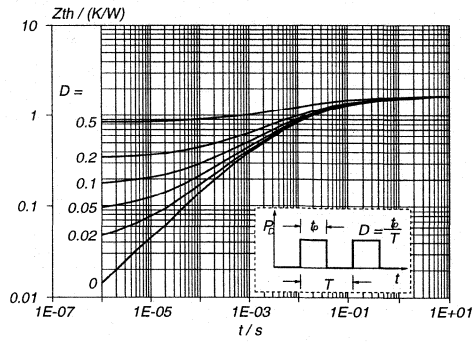


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb} = f(t)$; parameter $D = t_p/T$

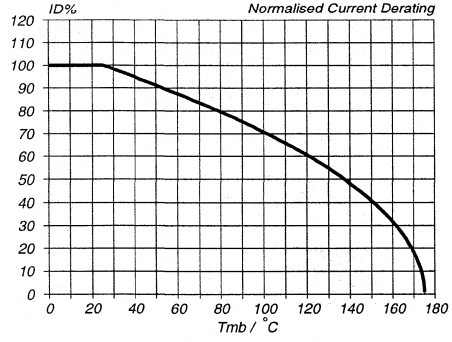


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D / I_{D\,25\,°C} = f(T_{mb})$; conditions: $V_{GS} \geq 10$ V

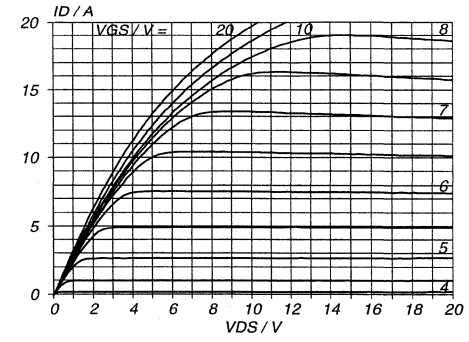


Fig.5. Typical output characteristics, $T_j = 25$ °C.
$I_D = f(V_{DS})$; parameter V_{GS}

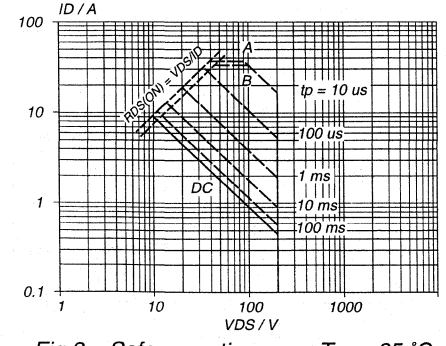


Fig.3. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

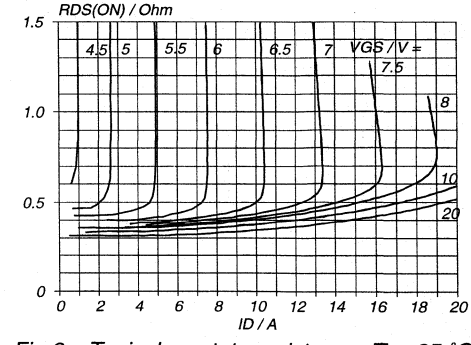


Fig.6. Typical on-state resistance, $T_j = 25$ °C.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

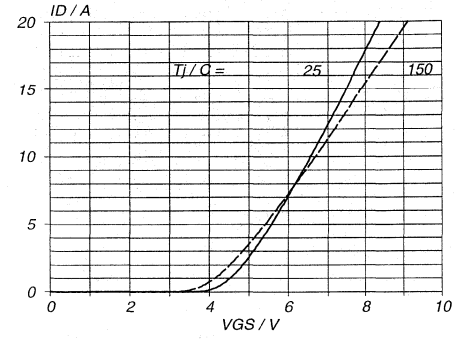


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

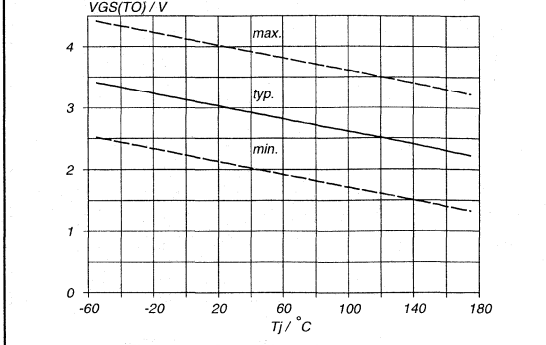


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

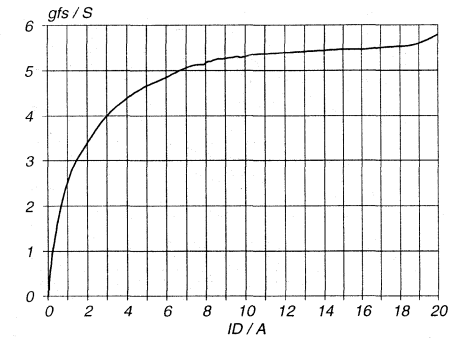


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

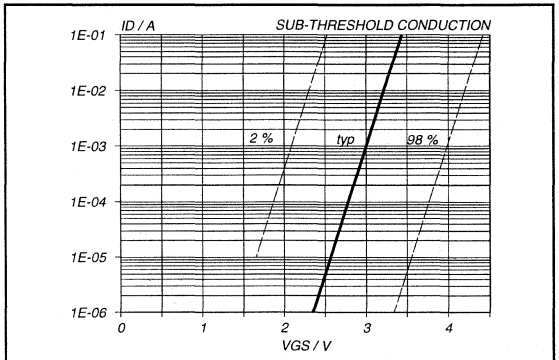


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

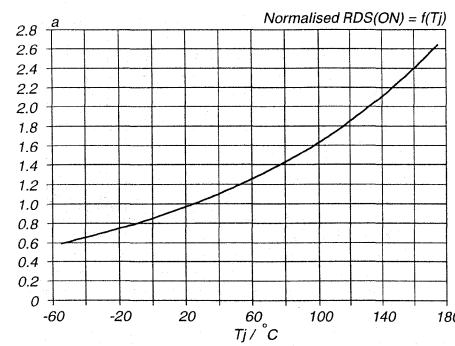


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 3.5 A; V_{GS} = 10 V

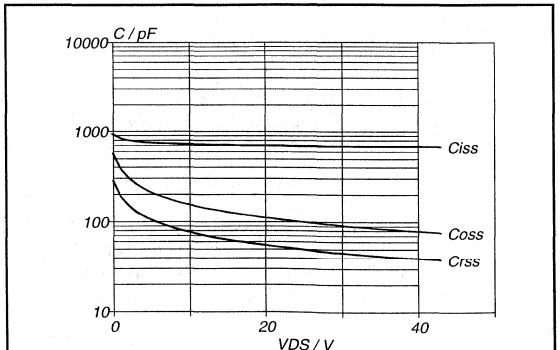


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

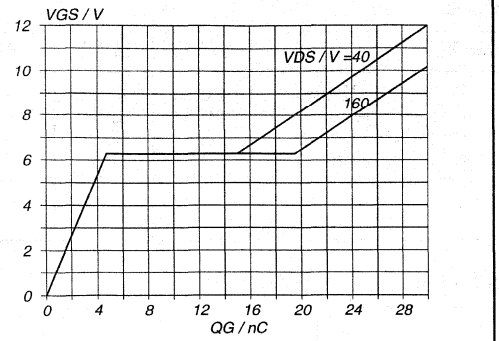


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 9$ A; parameter V_{DS}

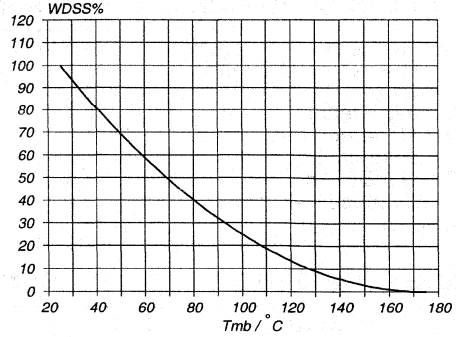


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 9$ A

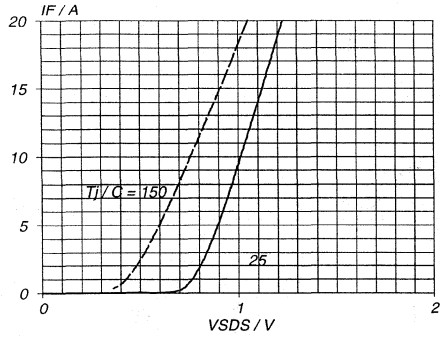


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

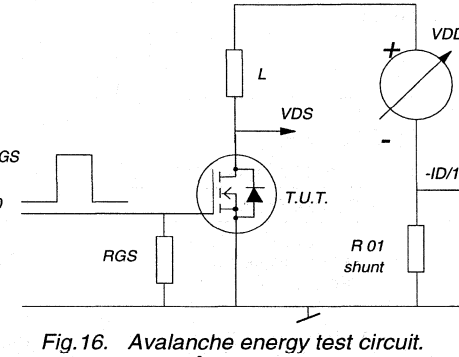


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

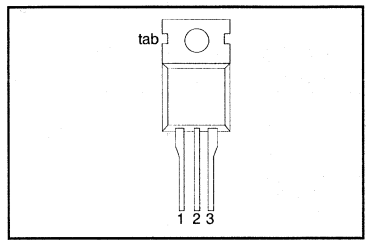
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK454	-800A	-800B	
V_{DS}	Drain-source voltage	800	800	V
I_D	Drain current (DC)	2.4	2.0	A
P_{tot}	Total power dissipation	85	85	W
$R_{DS(ON)}$	Drain-source on-state resistance	6	8	Ω

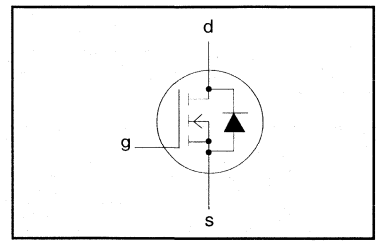
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	800		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	800		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-800A	-800B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	2.4	2.0	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	1.5	1.25	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	9.5	8	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	85		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction Temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.47	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	800	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j = 25 °C	-	2	20	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK454-800A**	-	5	6	Ω
		I_D = 1.0 A **BUK454-800B**	-	6	8	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1.0 A	1.0	2.3	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	450	750	pF
C_{oss}	Output capacitance		-	42	70	pF
C_{rss}	Feedback capacitance		-	15	30	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 1.9 A;	-	15	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	50	65	ns
t_f	Turn-off fall time		-	30	40	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	2.6	A
I_{DRM}	Pulsed reverse drain current	-	-	-	10	A
V_{SD}	Diode forward voltage	I_F = 2.6 A ; V_{GS} = 0 V	-	1.0	1.3	V
t_{rr}	Reverse recovery time	I_F = 2.6 A; -dI_F/dt = 100 A/µs;	-	230	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	1.9	-	µC

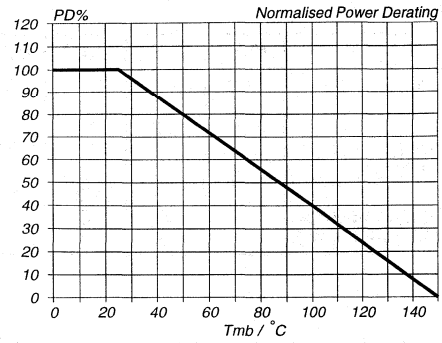


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

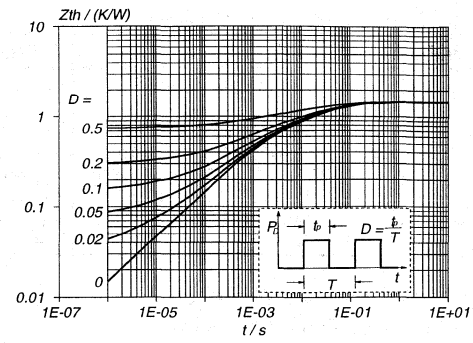


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

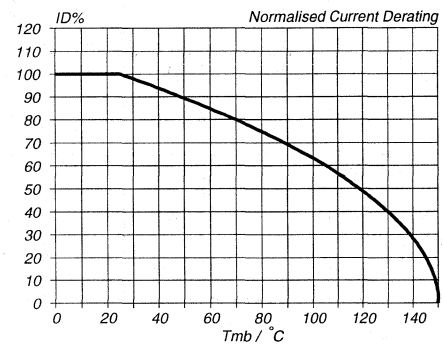


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

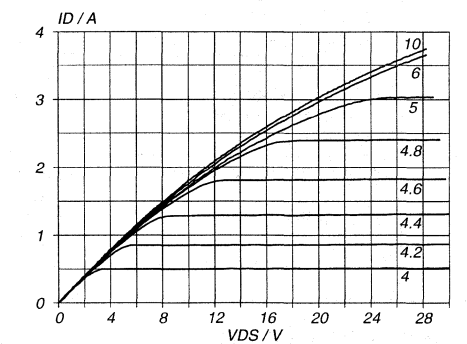


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

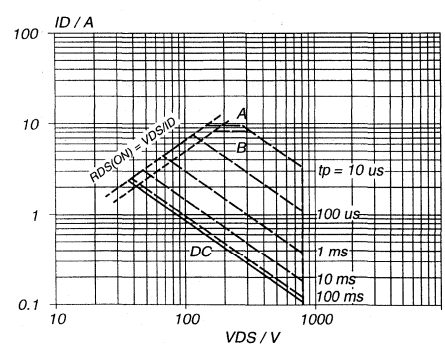


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

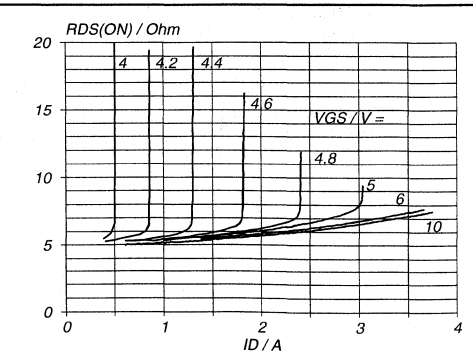


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

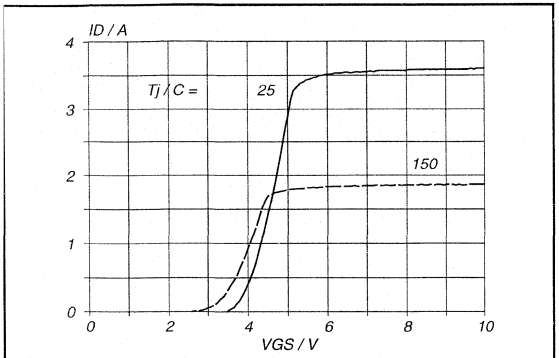


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

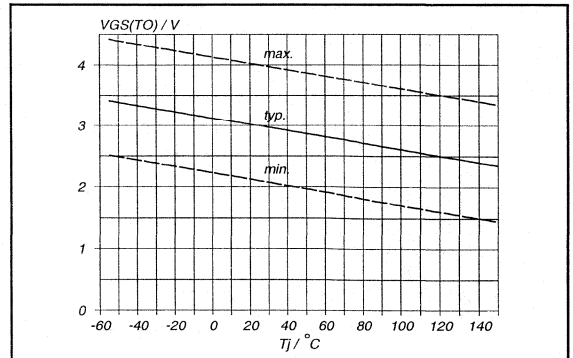


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

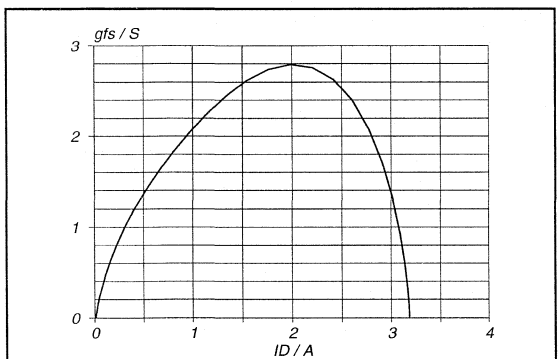


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

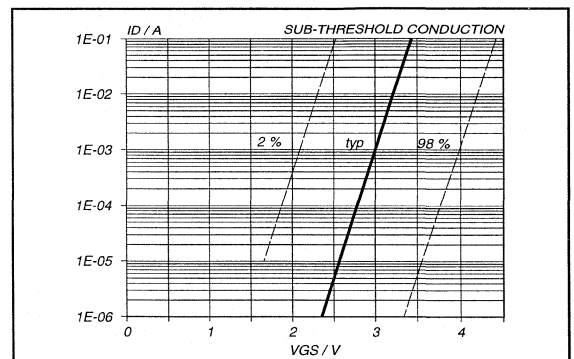


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

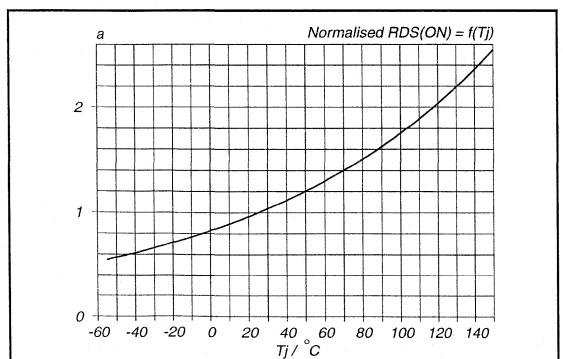


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ °C} = f(T_j)$; I_D = 1.0 A; V_{GS} = 10 V

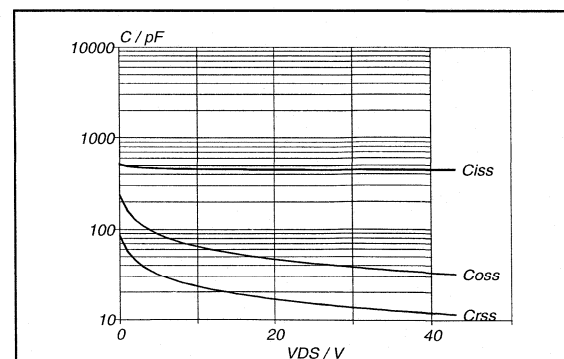


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

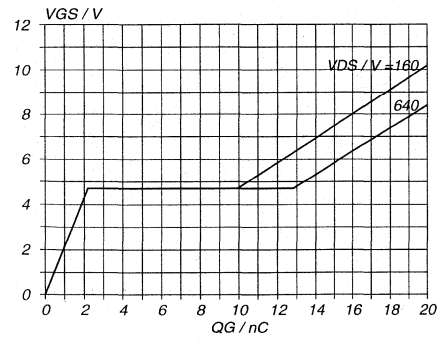


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 2.4$ A; parameter V_{DS}

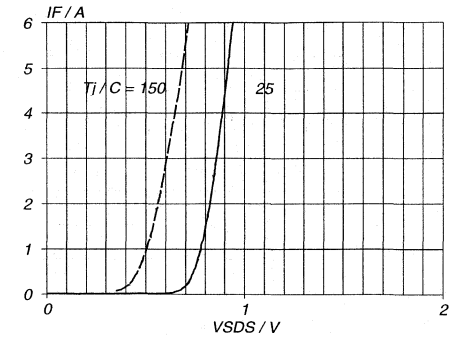


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

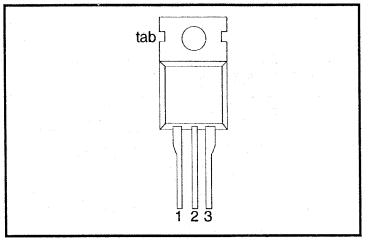
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK455	-100A	-100B	
V_{DS}	Drain-source voltage	100	100	V
I_D	Drain current (DC)	26	23	A
P_{tot}	Total power dissipation	125	125	W
T_j	Junction temperature	175	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.08	0.1	Ω

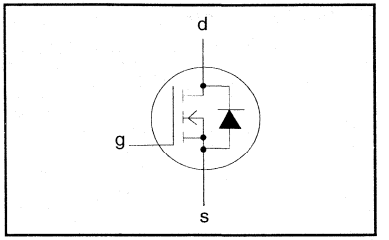
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	100		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-100A	-100B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	26	23	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	18	16	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	104	92	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction Temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK455-100A**	-	0.07	0.08	Ω
		I_D = 13 A **BUK455-100B**	-	0.08	0.1	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 13 A	7.0	13.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1650	2000	pF
C_{oss}	Output capacitance		-	350	500	pF
C_{rss}	Feedback capacitance		-	100	150	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	15	30	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	100	160	ns
t_f	Turn-off fall time		-	50	80	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	26	A
I_{DRM}	Pulsed reverse drain current	-	-	-	104	A
V_{SD}	Diode forward voltage	I_F = 26 A ; V_{GS} = 0 V	-	1.3	1.7	V
t_{rr}	Reverse recovery time	I_F = 26 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.8	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 26 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	100	mJ

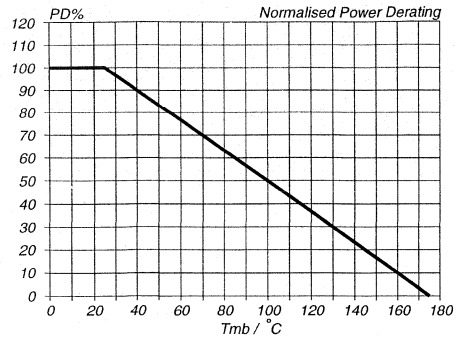


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

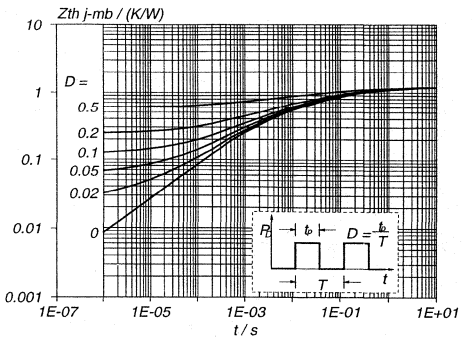


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

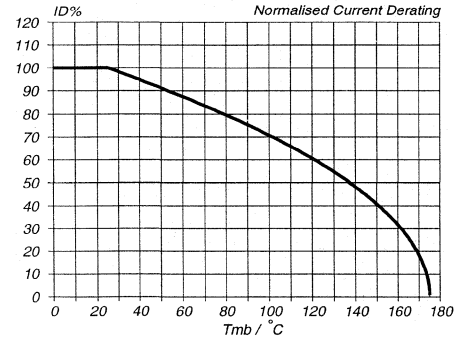


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

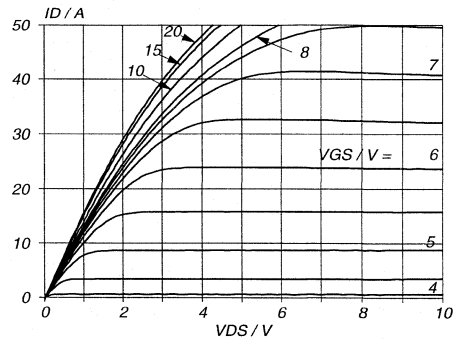


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

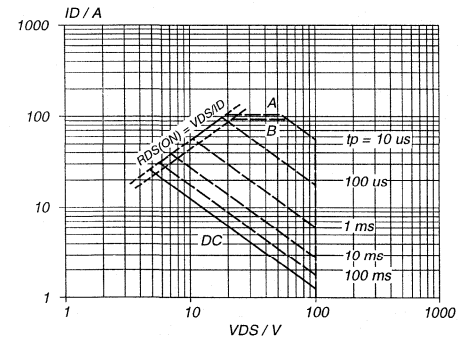


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

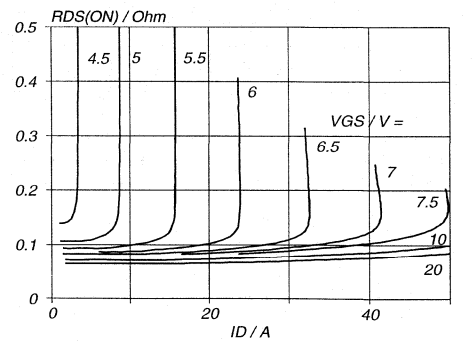


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

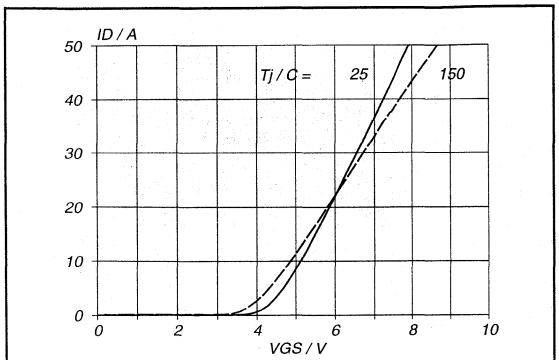


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

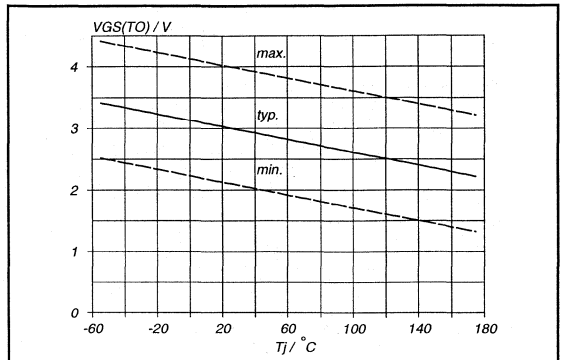


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

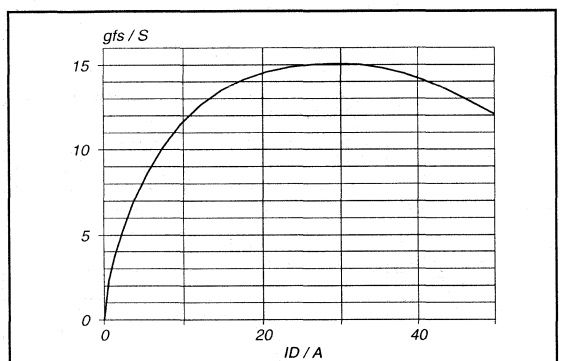


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

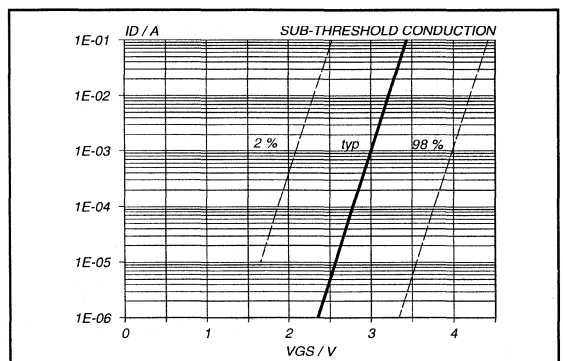


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

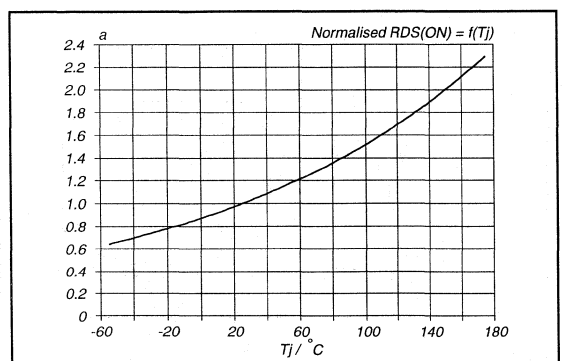


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 13 A; V_{GS} = 10 V

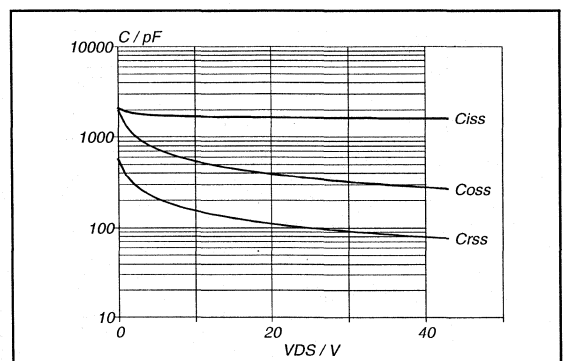


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

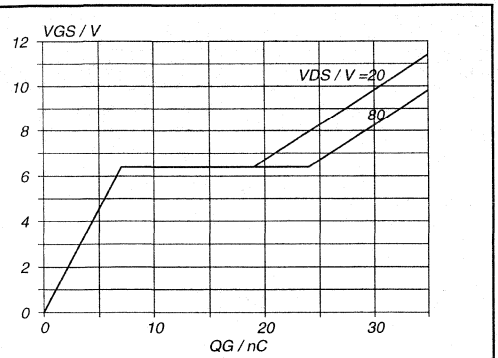


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 26$ A; parameter V_{DS}

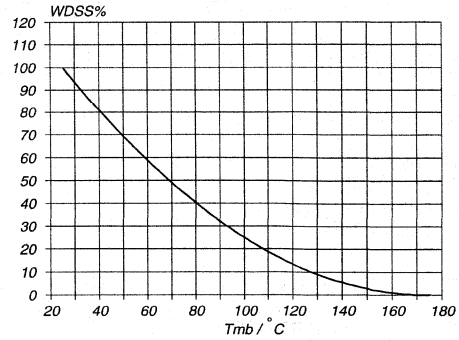


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 26$ A

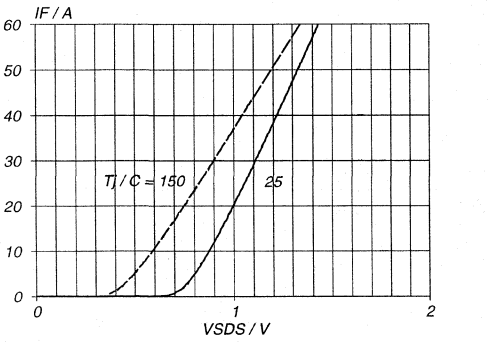


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

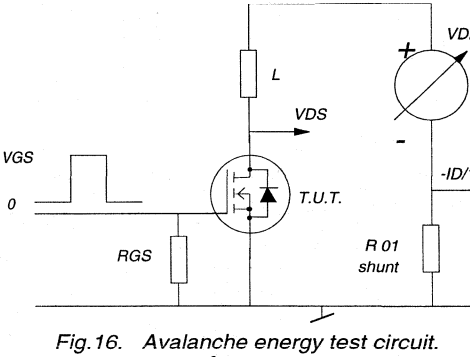


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor — BUK455-200A/B

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

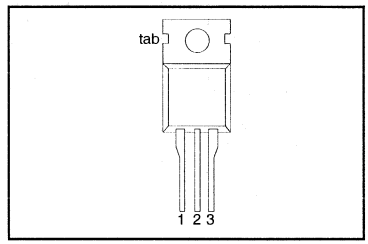
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK455	-200A	-200B	
V_{DS}	Drain-source voltage	200	200	V
I_D	Drain current (DC)	14	13	A
P_{tot}	Total power dissipation	125	125	W
T_j	Junction temperature	175	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance;	0.23	0.28	Ω

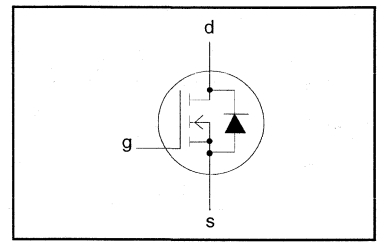
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	200		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-200A	-200B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	14	13	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	10	9	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	56	52	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction Temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK455-200A**	-	0.2	0.23	Ω
		I_D = 7 A **BUK455-200B**	-	0.22	0.28	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 7 A	6.0	8.4	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1400	1750	pF
C_{oss}	Output capacitance		-	190	250	pF
C_{rss}	Feedback capacitance		-	55	80	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	18	30	ns
t_r	Turn-on rise time	V_{GS} = 30 V; R_{GS} = 50 Ω;	-	35	60	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	85	120	ns
t_f	Turn-off fall time		-	35	50	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	14	A
I_{DRM}	Pulsed reverse drain current	-	-	-	56	A
V_{SD}	Diode forward voltage	I_F = 14 A ; V_{GS} = 0 V	-	1.0	1.5	V
t_{rr}	Reverse recovery time	I_F = 14 A; -dI_F/dt = 100 A/µs;	-	180	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	1.8	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 14 A ; V_{DD} ≤ 100 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	100	mJ

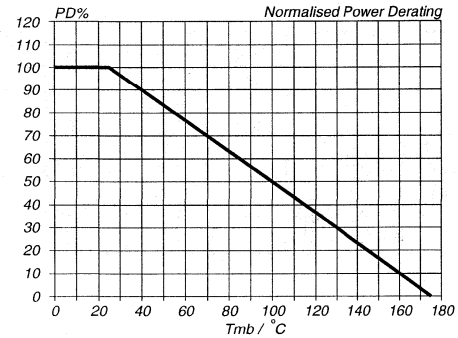


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

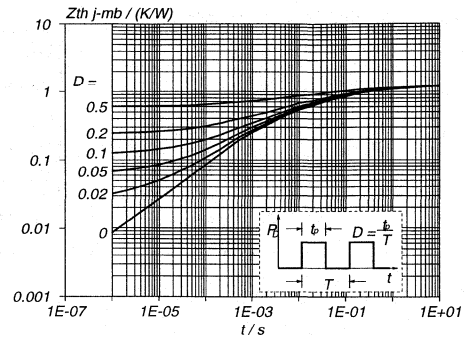


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

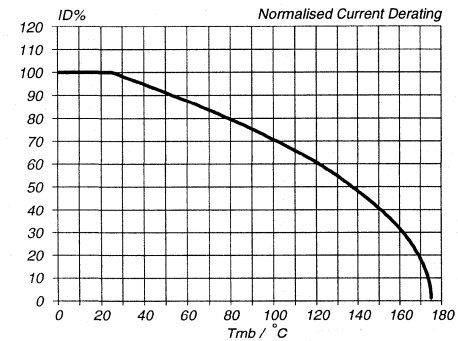


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

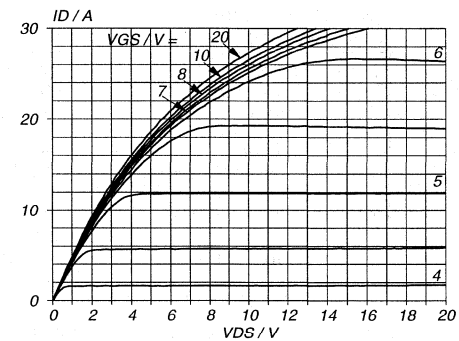


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

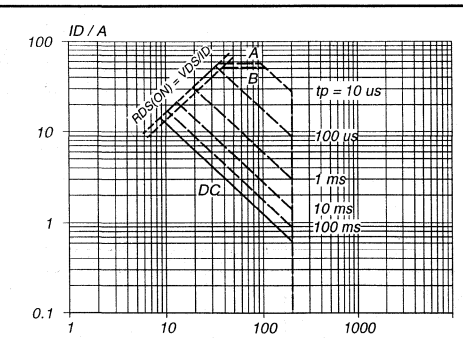


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

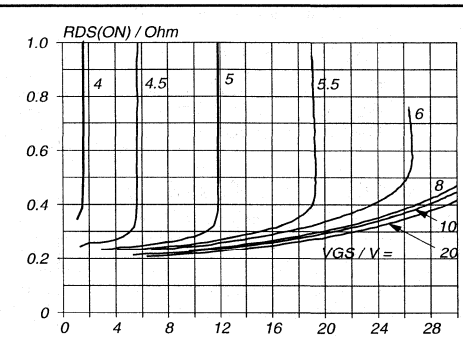


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

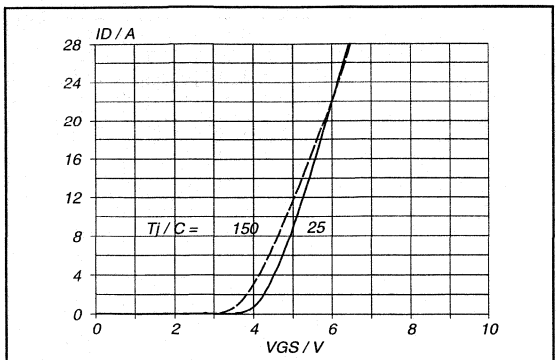


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

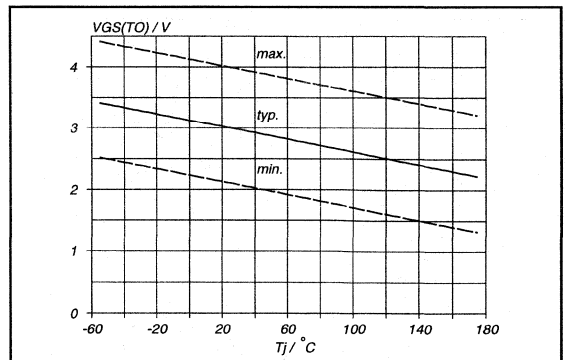


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

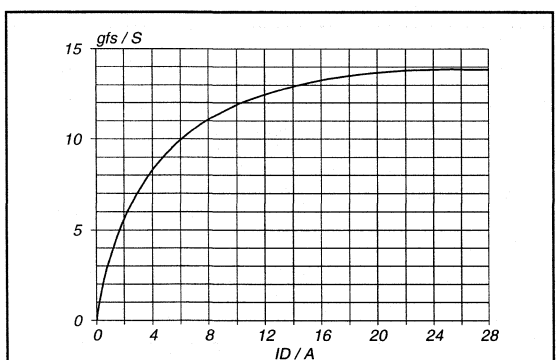


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

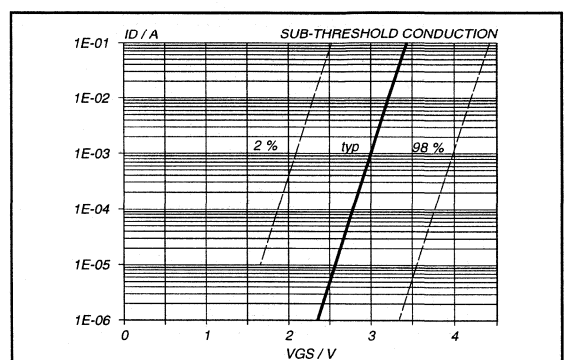


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

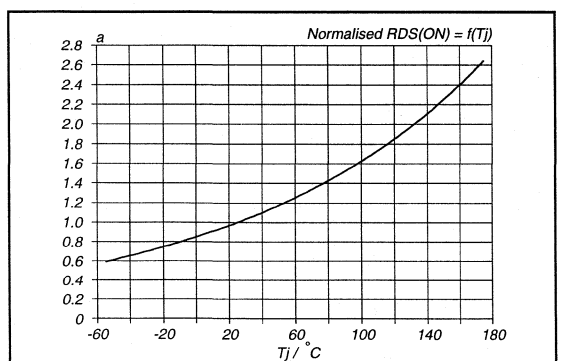


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 7 A; V_{GS} = 10 V

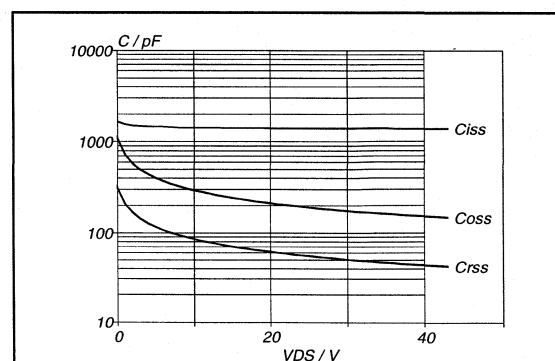


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

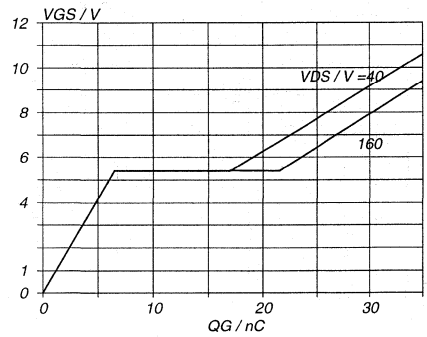


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 14$ A; parameter V_{DS}

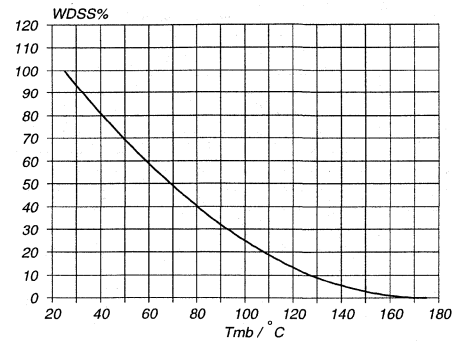


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 14$ A

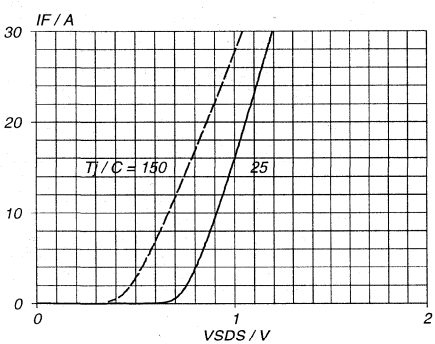


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

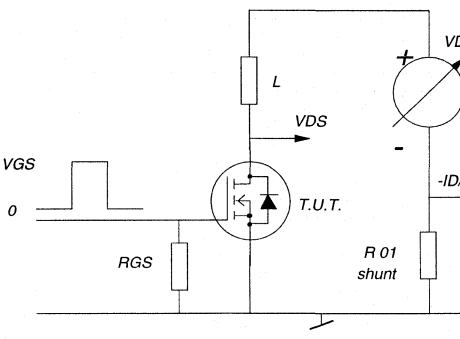


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

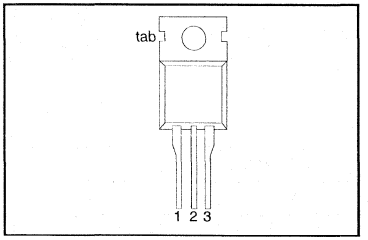
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK456	-100A	-100B	
V_{DS}	Drain-source voltage	100	100	V
I_D	Drain current (DC)	34	32	A
P_{tot}	Total power dissipation	150	150	W
T_j	Junction temperature	175	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.057	0.065	Ω

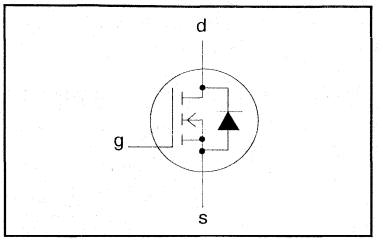
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	100		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-100A	-100B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	34	32	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	24	22	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	136	128	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	150		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK456-100A**	-	0.052	0.057	Ω
		I_D = 15 A **BUK456-100B**	-	0.06	0.065	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 15 A	12	16	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1500	2000	pF
C_{oss}	Output capacitance		-	450	600	pF
C_{rss}	Feedback capacitance		-	130	200	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	20	30	ns
t_r	Turn-on rise time	V_{GS} = 10 V;	-	40	60	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω;	-	150	200	ns
t_f	Turn-off fall time	R_{GS} = 50 Ω	-	65	85	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	34	A
I_{DRM}	Pulsed reverse drain current	-	-	-	136	A
V_{SD}	Diode forward voltage	I_F = 34 A ; V_{GS} = 0 V	-	1.8	2.5	V
t_{rr}	Reverse recovery time	I_F = 34 A; -dI_F/dt = 100 A/µs;	-	100	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	1.0	-	µC

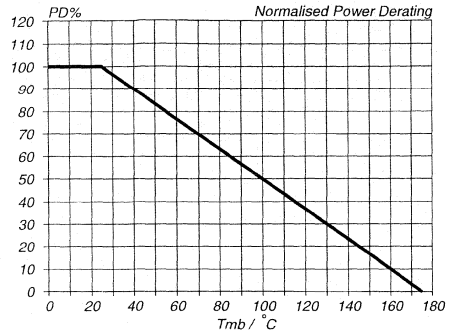


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

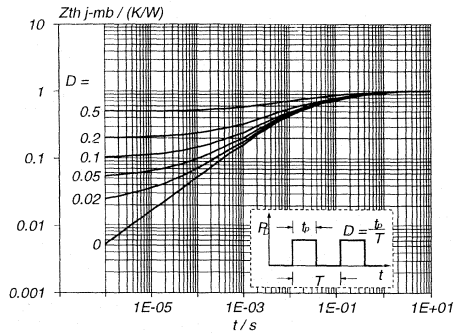


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

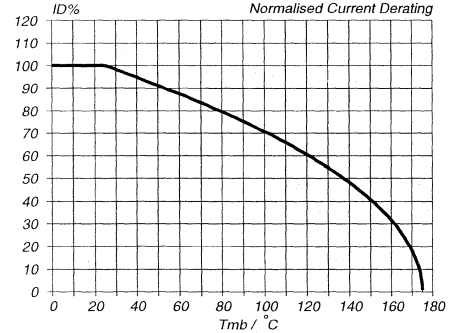


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

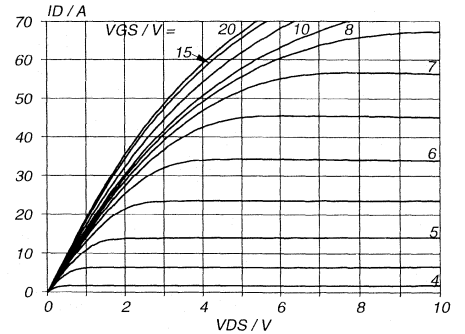


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

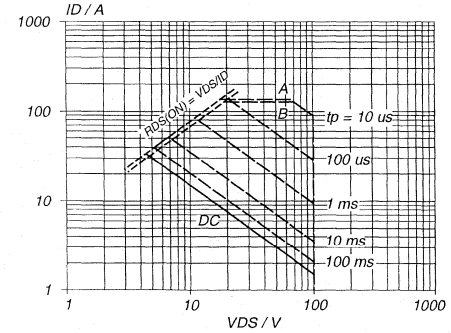


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

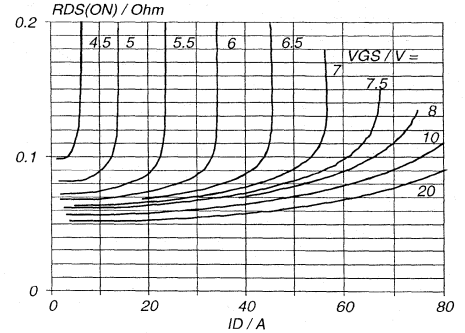


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

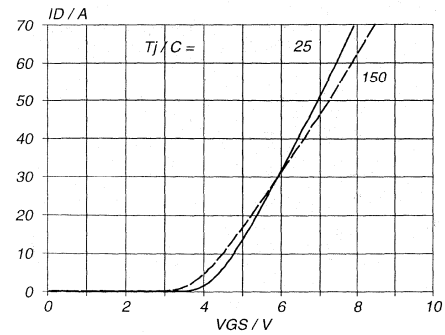


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

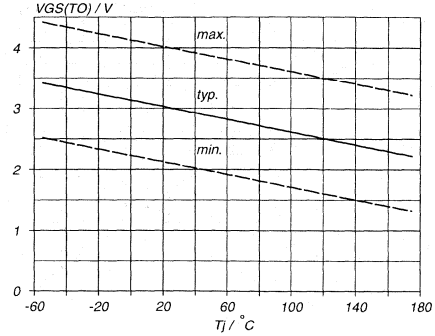


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

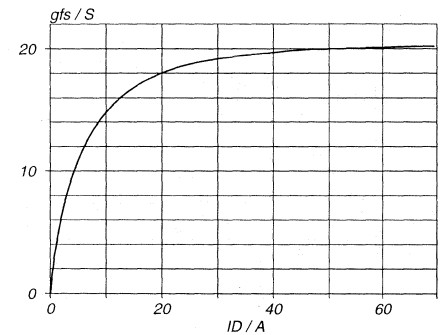


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

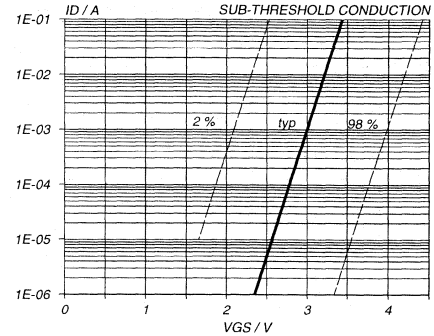


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

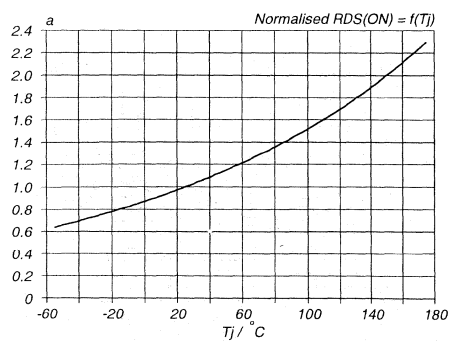


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ °C} = f(T_j)$; I_D = 15 A; V_{GS} = 10 V

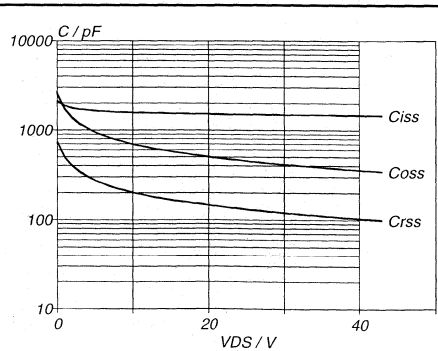


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

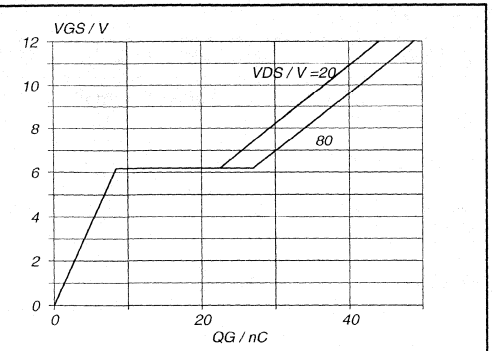


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 34$ A; parameter V_{DS}

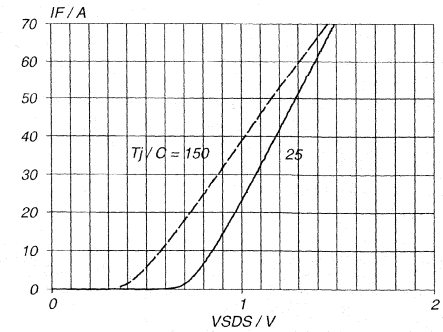


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

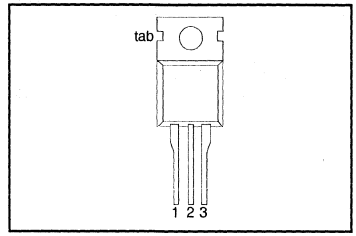
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK456	-200A	-200B	
V_{DS}	Drain-source voltage	200	200	V
I_D	Drain current (DC)	19	17	A
P_{tot}	Total power dissipation	150	150	W
T_j	Junction temperature	175	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.16	0.2	Ω

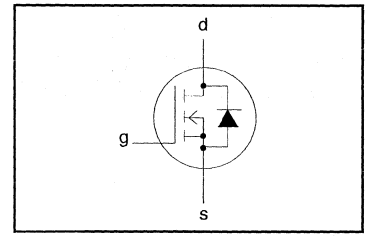
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	200		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-200A	-200B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	19	17	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	13	12	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	76	68	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	150		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction Temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK456-200A**	-	0.15	0.16	Ω
		I_D = 10 A **BUK456-200B**	-	0.18	0.20	Ω

DYNAMIC CHARACTERISTICS

Tmb = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 10 A	8.5	16	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1500	2000	pF
C_{oss}	Output capacitance		-	300	400	pF
C_{rss}	Feedback capacitance		-	60	100	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	20	30	ns
t_r	Turn-on rise time	V_{GS} = 10 V;	-	40	60	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω;	-	145	185	ns
t_f	Turn-off fall time	R_{GS} = 50 Ω	-	50	70	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

Tmb = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	19	A
I_{DRM}	Pulsed reverse drain current	-	-	-	76	A
V_{SD}	Diode forward voltage	I_F = 19 A ; V_{GS} = 0 V	-	1.0	1.7	V
t_{rr}	Reverse recovery time	I_F = 19 A; -dI_F/dt = 100 A/µs;	-	180	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	2.5	-	µC

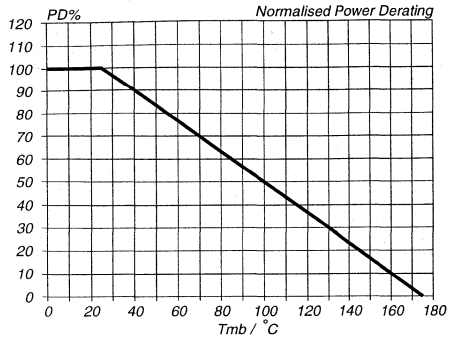


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

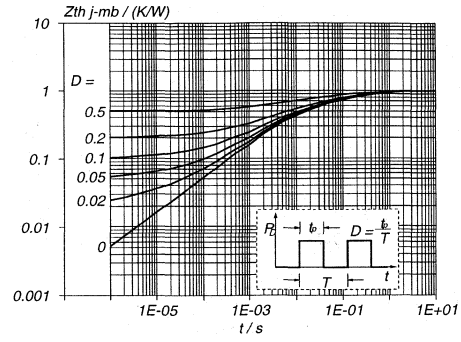


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

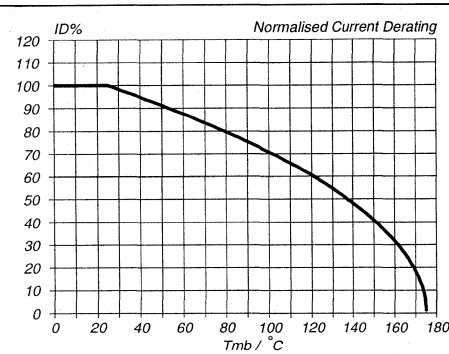


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

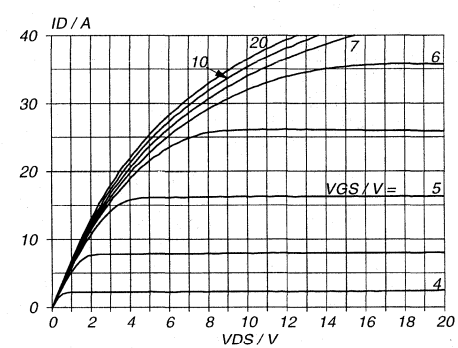


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

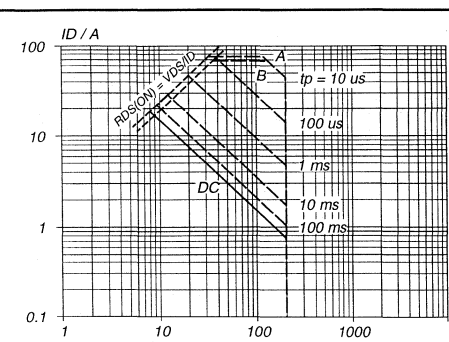


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

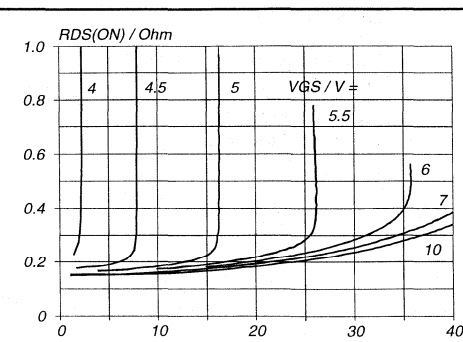


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

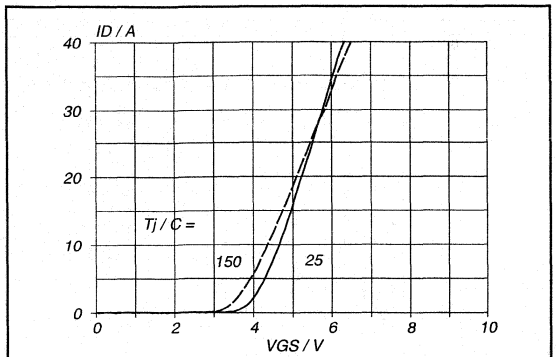


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

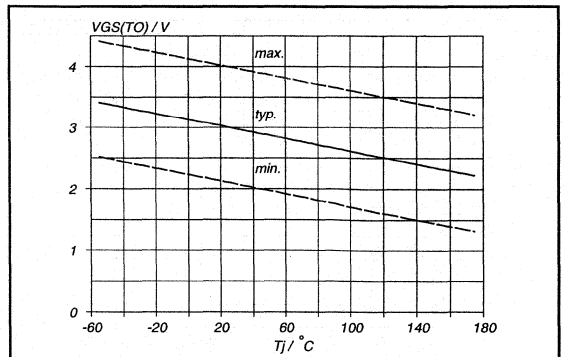


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

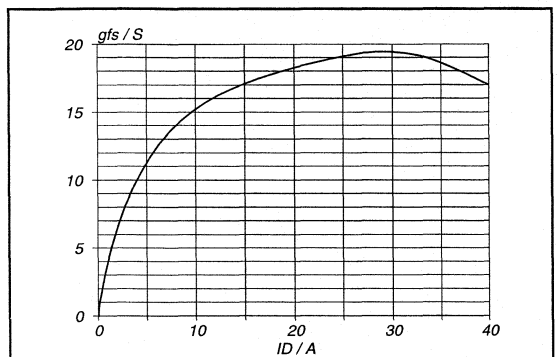


Fig.8. Typical transconductance, $T_j = 25$ °C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

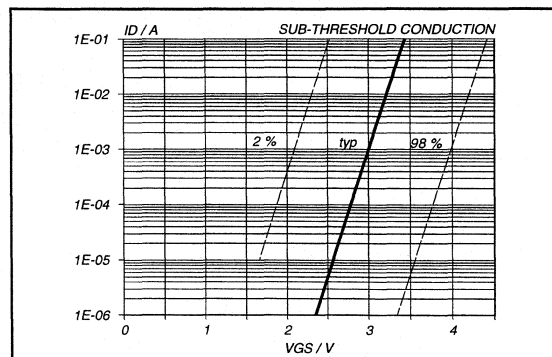


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

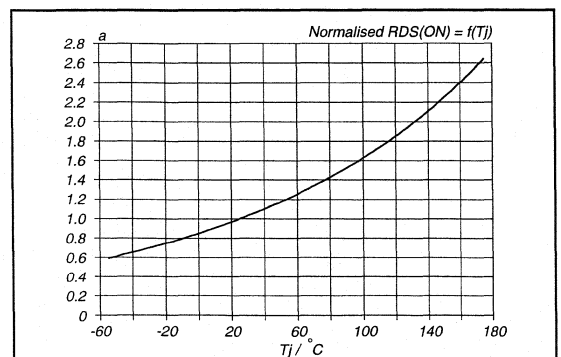


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 10$ A; $V_{GS} = 10$ V

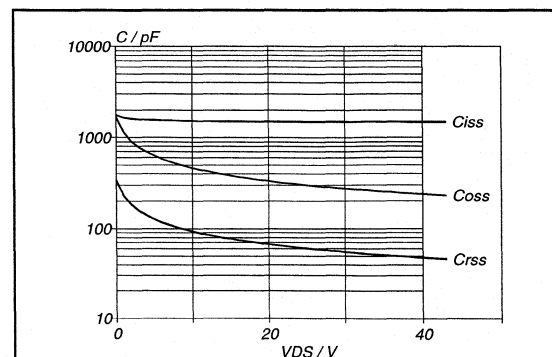


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

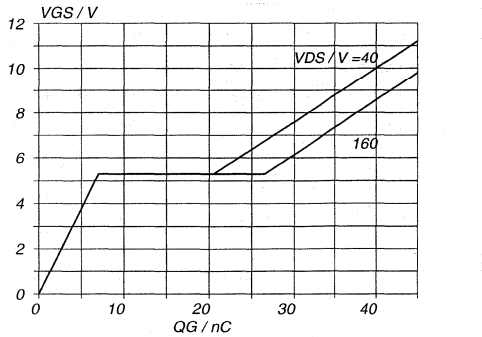


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 19$ A; parameter V_{DS}

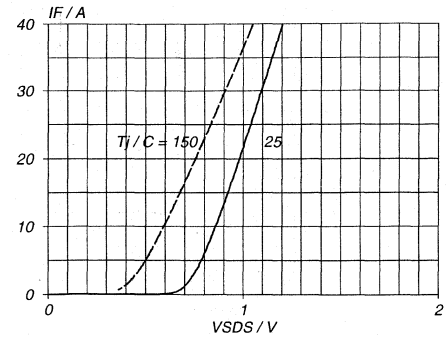


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

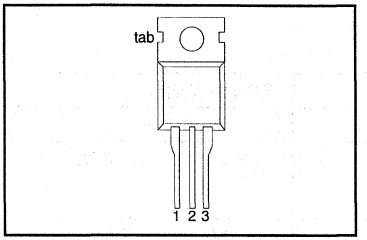
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK456	-800A	-800B	
V_{DS}	Drain-source voltage	800	800	V
I_D	Drain current (DC)	4	3.5	A
P_{tot}	Total power dissipation	125	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	3	4	Ω

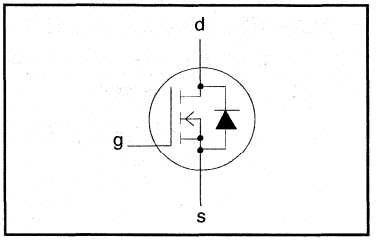
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	800		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	800		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-800A	-800B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	4.0	3.5	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	2.5	2.2	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	16	14	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction Temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	800	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j = 25 °C	-	2	20	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK456-800A** I_D = 1.5 A **BUK456-800B**	- -	2.7 3.5	3.0 4.0	Ω Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1.5 A	3.0	4.3	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1000	1250	pF
C_{oss}	Output capacitance		-	80	120	pF
C_{rss}	Feedback capacitance		-	30	50	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.3 A;	-	10	25	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	50	70	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	130	150	ns
t_f	Turn-off fall time		-	40	60	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	4.0	A
I_{DRM}	Pulsed reverse drain current	-	-	-	16	A
V_{SD}	Diode forward voltage	I_F = 4.0 A ; V_{GS} = 0 V	-	1.0	1.3	V
t_{rr}	Reverse recovery time	I_F = 4.0 A; -dI_F/dt = 100 A/µs;	-	1800	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	12	-	µC

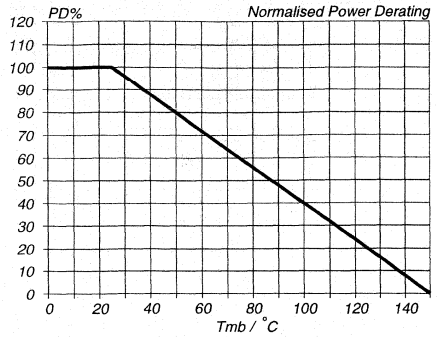


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

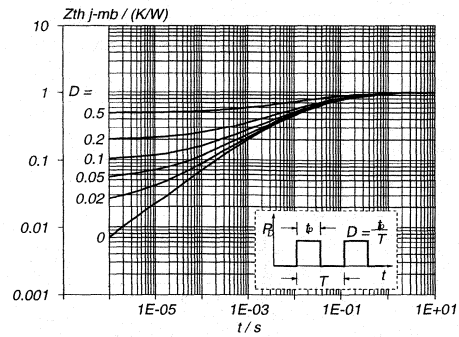


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

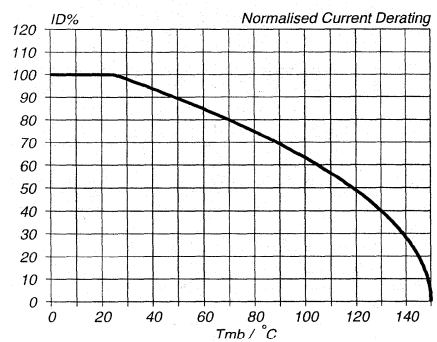


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

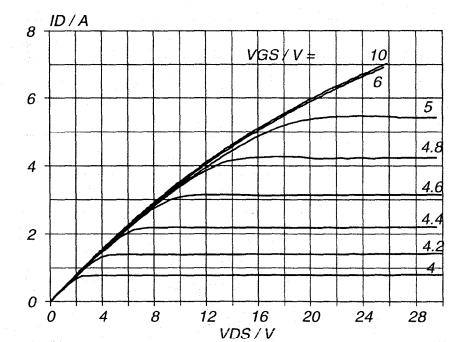


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

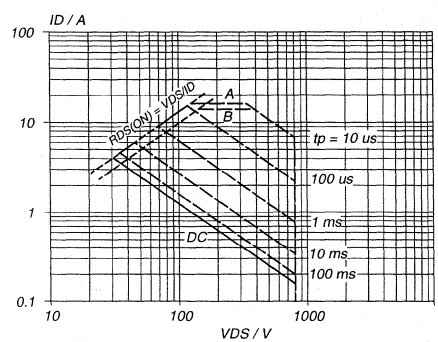


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

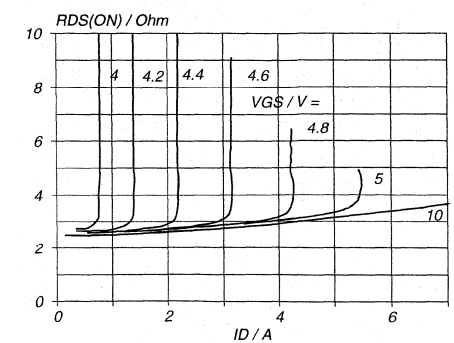


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

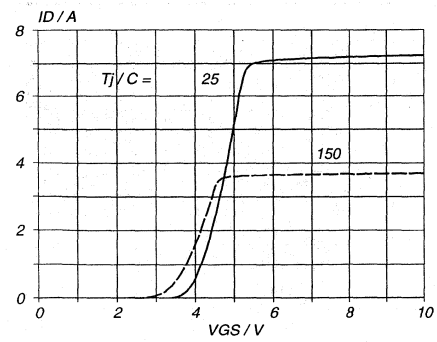


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

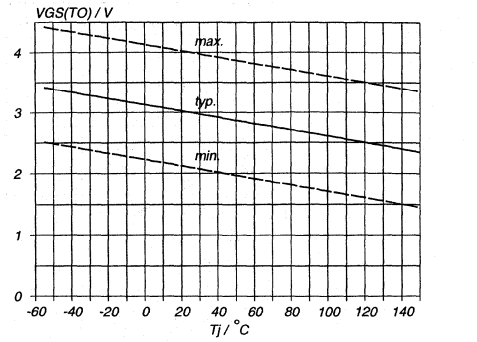


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

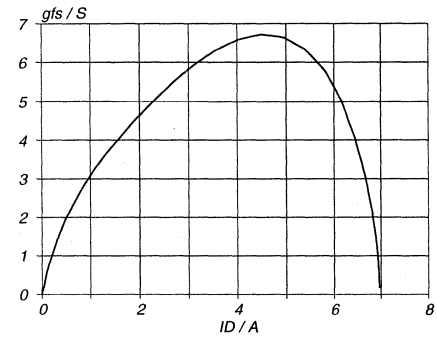


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

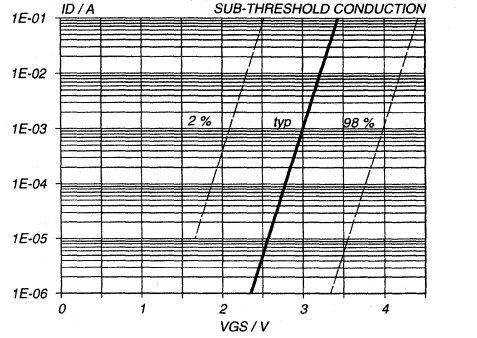


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

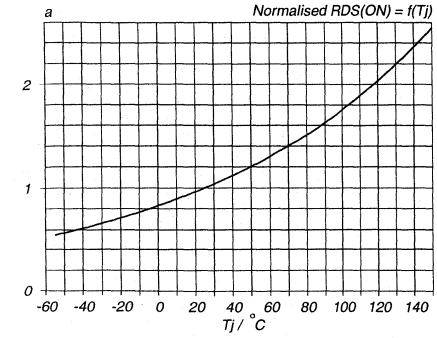


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ °C} = f(T_j)$; I_D = 1.5 A; V_{GS} = 10 V

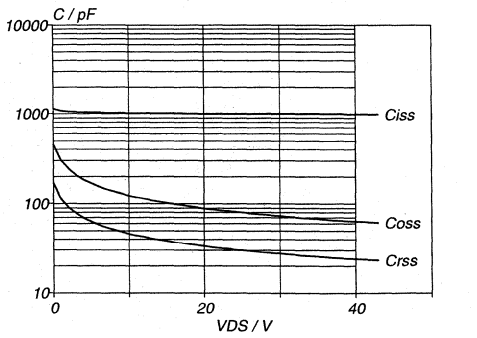


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

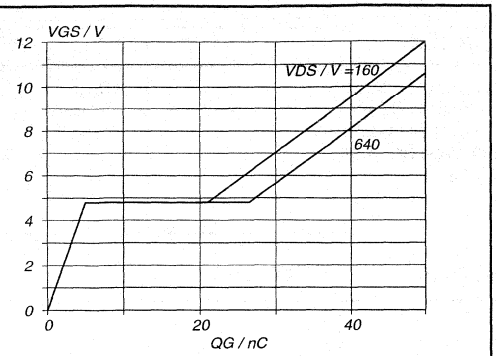


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 4$ A; parameter V_{DS}

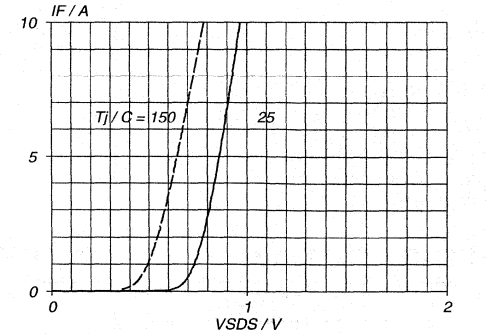


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

PowerMOS transistor — BUK456-1000B

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

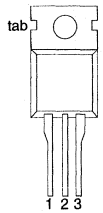
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	1000	V
I_D	Drain current (DC)	3.1	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	5	Ω

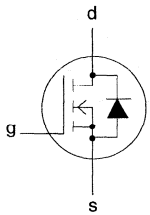
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	1000	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	1000	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	3.1	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	2.0	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	12	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}	Storage temperature	-	- 55	150	°C
T_j	Junction Temperature	-	-	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	1000	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 1000 V; V_{GS} = 0 V; T_j = 25 °C	-	2	20	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 1000 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1.5 A	-	4.5	5.0	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1.5 A	3.0	4.3	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1000	1250	pF
C_{oss}	Output capacitance		-	80	120	pF
C_{rss}	Feedback capacitance		-	30	50	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.3 A;	-	10	25	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	50	70	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	130	150	ns
t_f	Turn-off fall time		-	40	60	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	3.5	A
I_{DRM}	Pulsed reverse drain current	-	-	-	14	A
V_{SD}	Diode forward voltage	I_F = 3.5 A ; V_{GS} = 0 V	-	1.0	1.3	V
t_{rr}	Reverse recovery time	I_F = 3.5 A; -dI_F/dt = 100 A/µs;	-	1800	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	12	-	µC

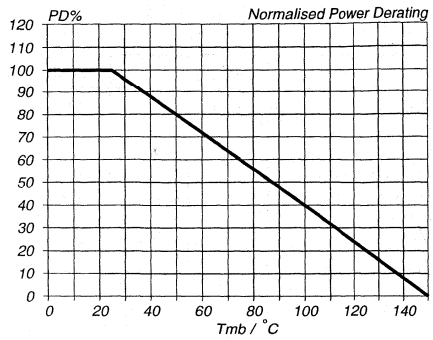


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

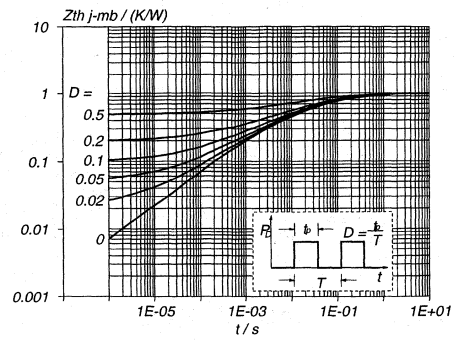


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

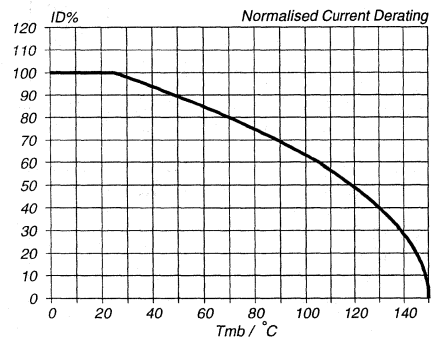


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

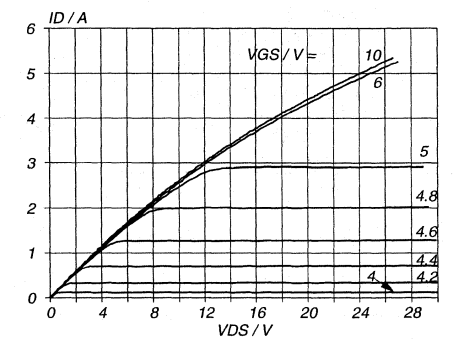


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

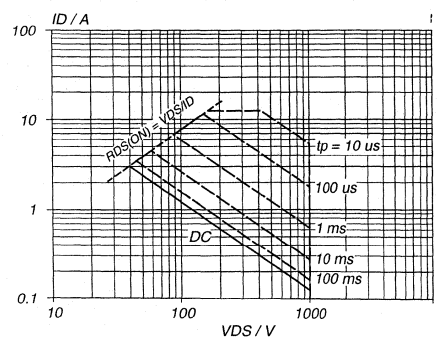


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

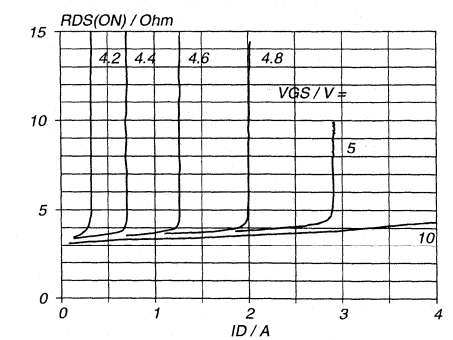


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

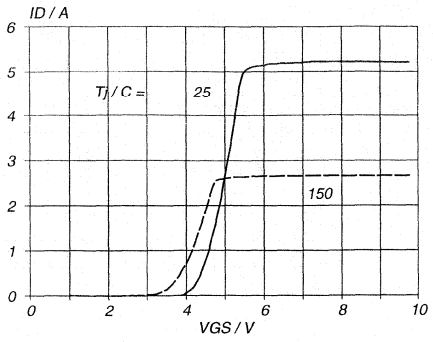


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

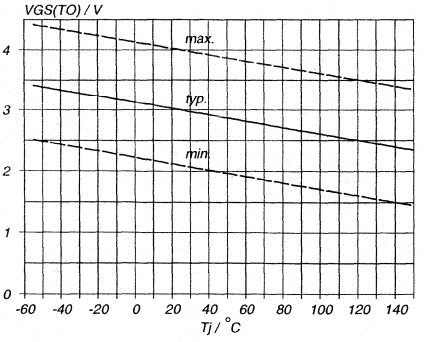


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

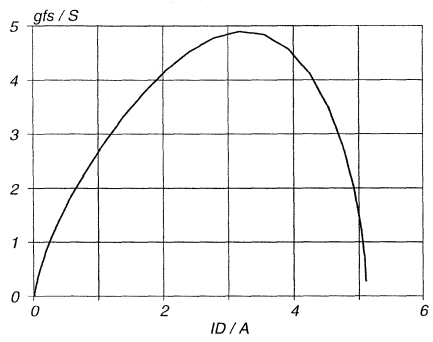


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

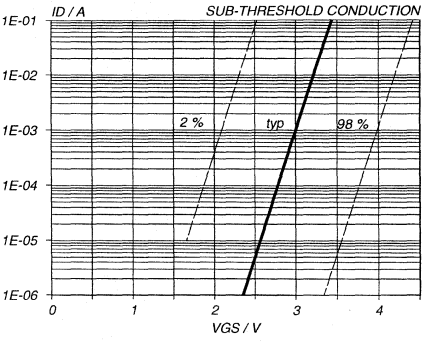


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

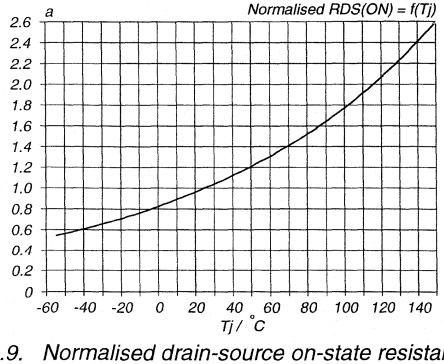


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ °C} = f(T_j)$; I_D = 1.5 A; V_{GS} = 10 V

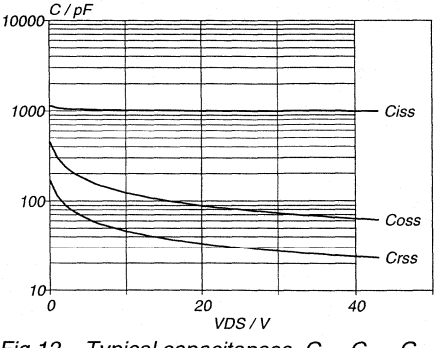


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

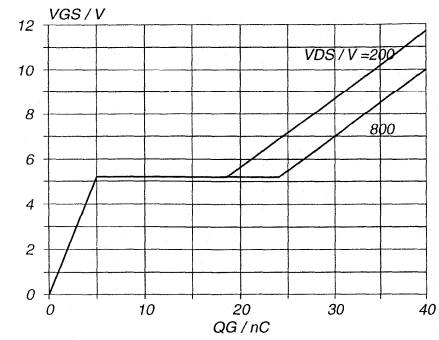


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 3.5$ A; parameter V_{DS}

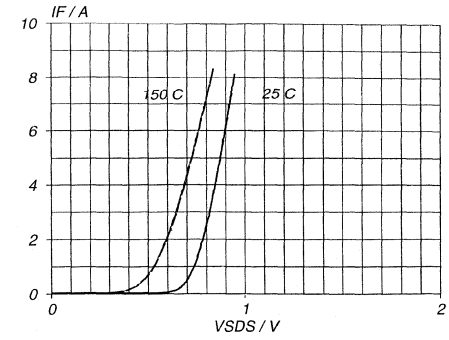


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

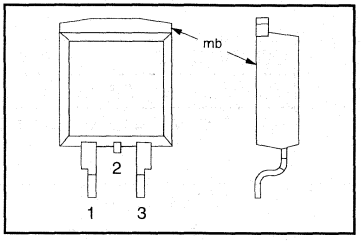
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	11	A
P_{tot}	Total power dissipation	60	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.25	Ω

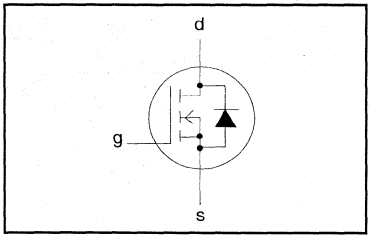
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain (no connection possible)
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	11	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	7.7	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	44	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	60	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint FR4 board (see fig. 18.)	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 5.5 A	-	0.22	0.25	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5.5 A	3	4.2	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	400	500	pF
C_{oss}	Output capacitance		-	90	120	pF
C_{rss}	Feedback capacitance		-	35	50	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	9	14	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	30	45	ns
t_f	Turn-off fall time		-	20	40	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	11	A
I_{DRM}	Pulsed reverse drain current	-	-	-	44	A
V_{SD}	Diode forward voltage	I_F = 11 A ; V_{GS} = 0 V	-	1.2	1.5	V
t_{rr}	Reverse recovery time	I_F = 11 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.35	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 11 A ; V_{DD} ≤ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	35	mJ

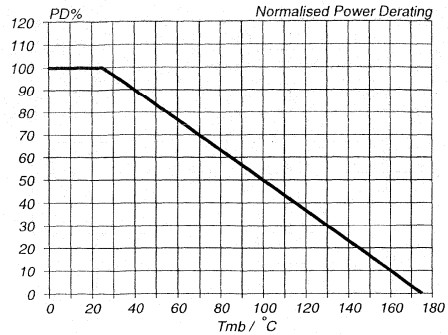


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

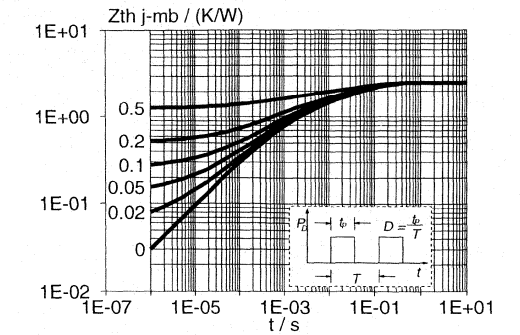


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

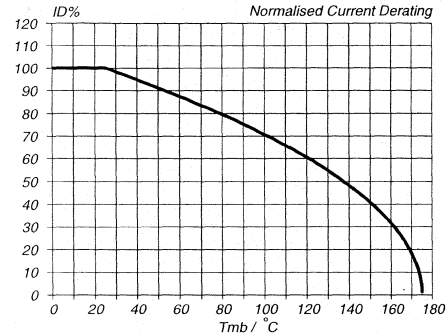


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

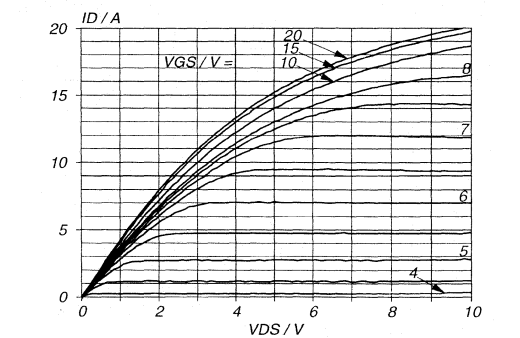


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

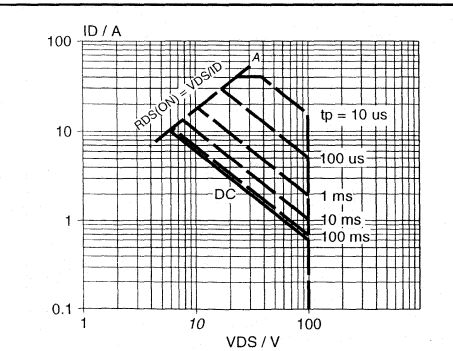


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

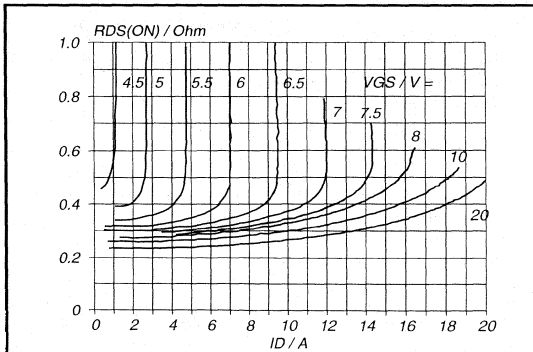


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

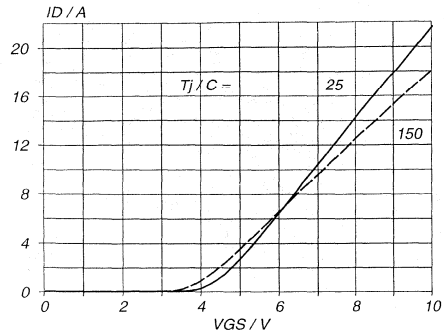


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

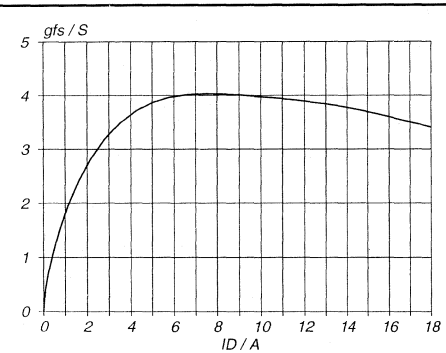


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

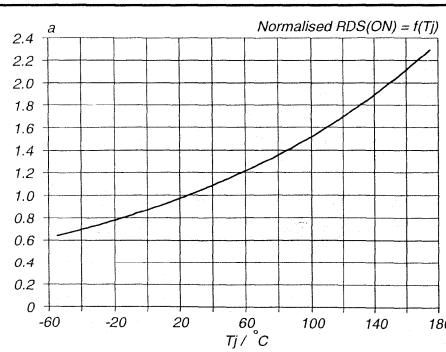


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 5.5 A; V_{GS} = 10 V

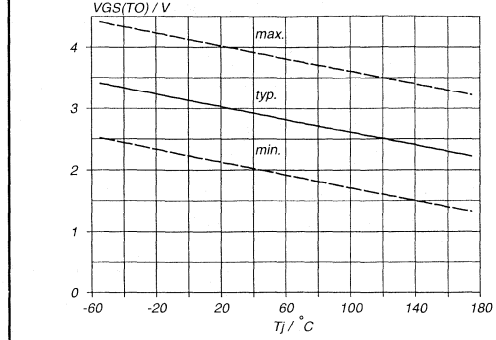


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

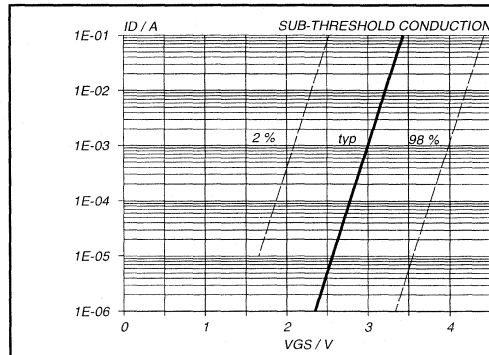


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

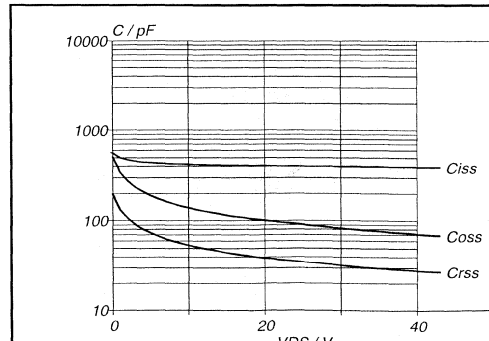


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

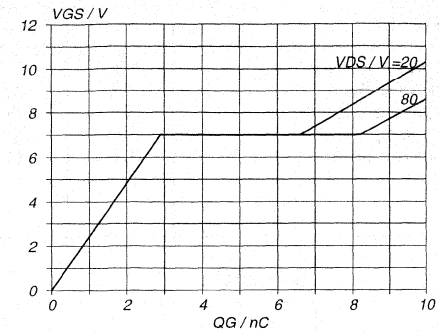


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 11$ A; parameter V_{DS}

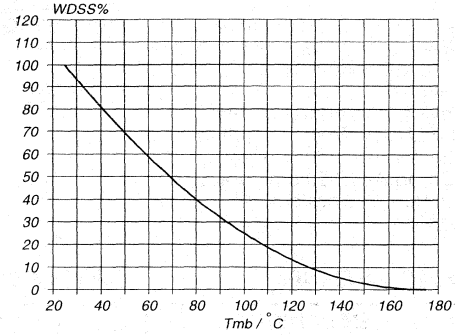


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 11$ A

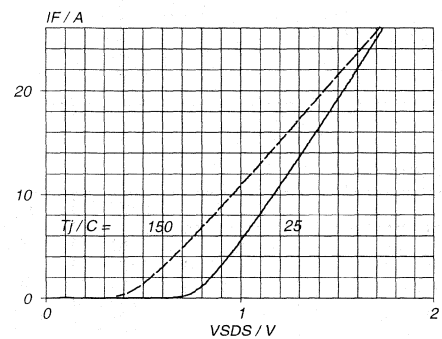


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

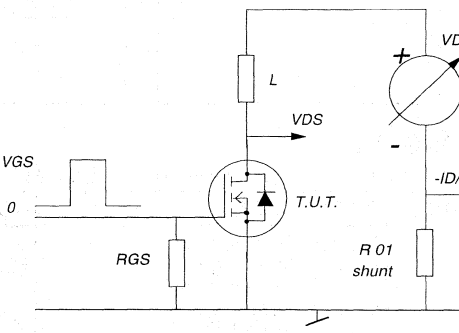


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

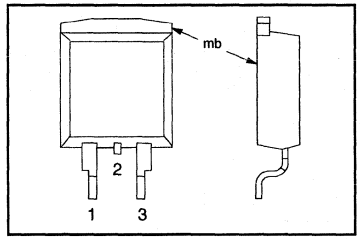
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
	Drain-source voltage	100	V
V_{DS}	Drain current (DC)	14	A
I_D	Total power dissipation	75	W
P_{tot}	Junction temperature	175	°C
T_j	Drain-source on-state resistance	0.16	Ω
$R_{DS(ON)}$			

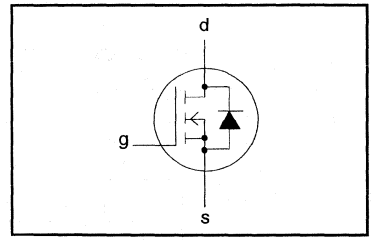
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	14	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	10	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	56	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	75	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint FR4 board (see fig. 18)	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A	-	0.15	0.16	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5 A	4.0	5.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	660	825	pF
C_{oss}	Output capacitance		-	140	200	pF
C_{rss}	Feedback capacitance		-	60	100	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	10	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	60	90	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	14	A
I_{DRM}	Pulsed reverse drain current	-	-	-	56	A
V_{SD}	Diode forward voltage	I_F = 14 A ; V_{GS} = 0 V	-	1.2	1.5	V
t_{rr}	Reverse recovery time	I_F = 14 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.6	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 14 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	70	mJ

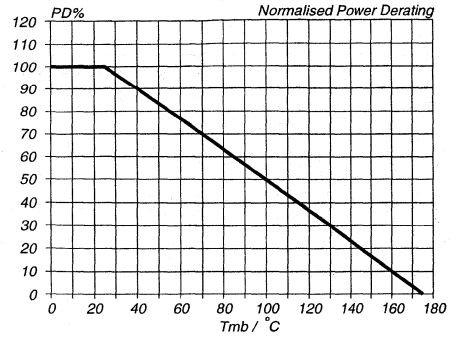


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

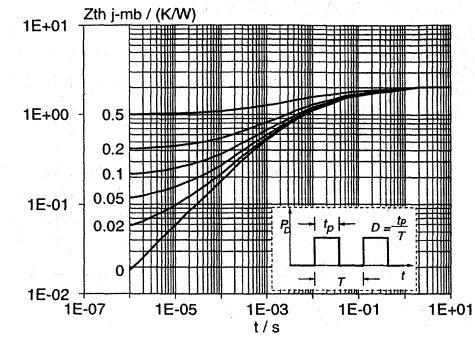


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

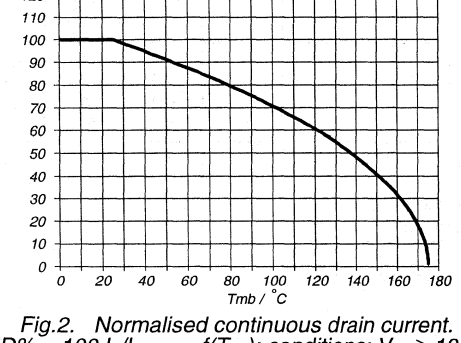


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

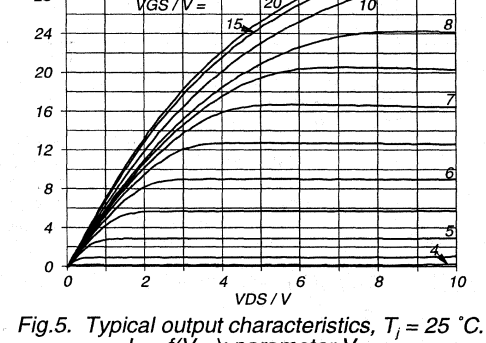


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

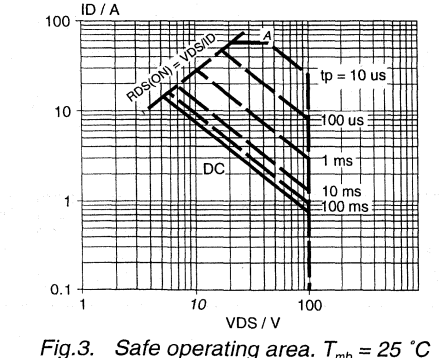


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

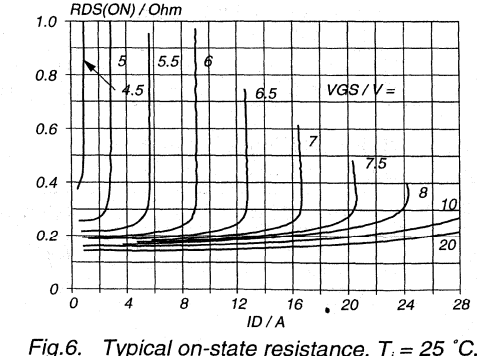


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

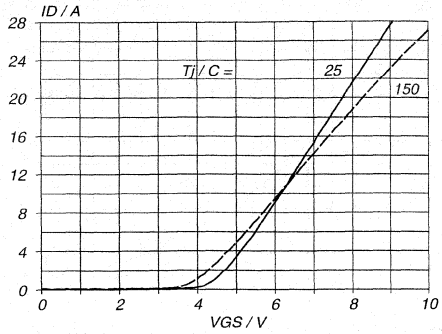


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

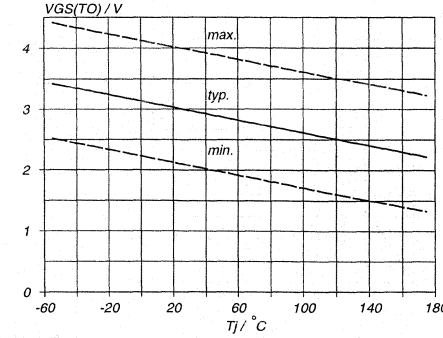


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

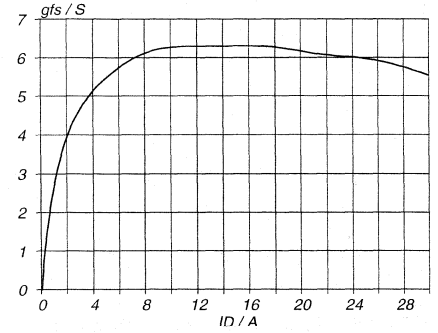


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

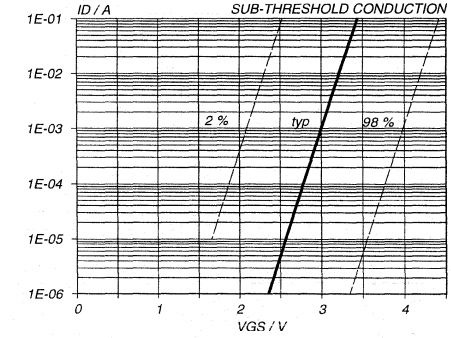


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

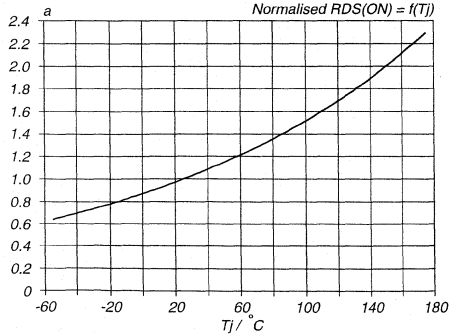


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 5 A; V_{GS} = 10 V

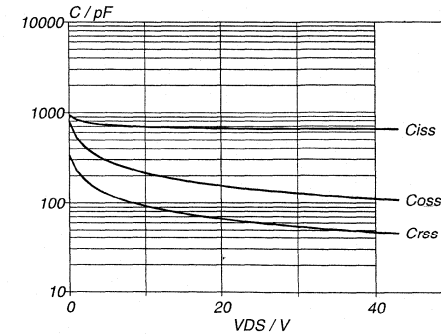


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

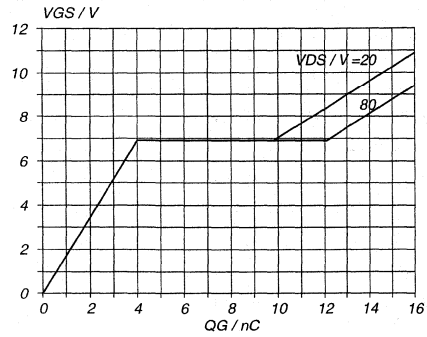


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: I_D = 14 A; parameter V_{DS}

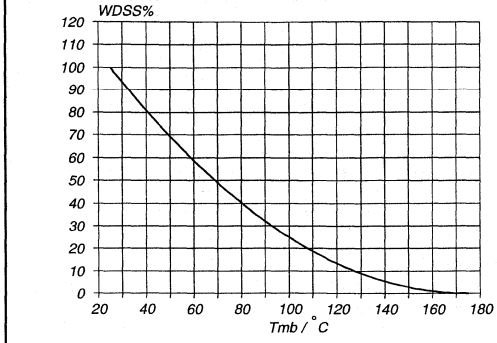


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: I_D = 14 A

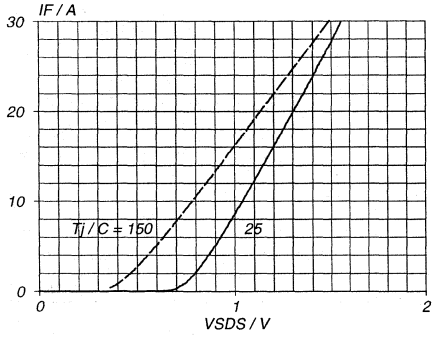


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

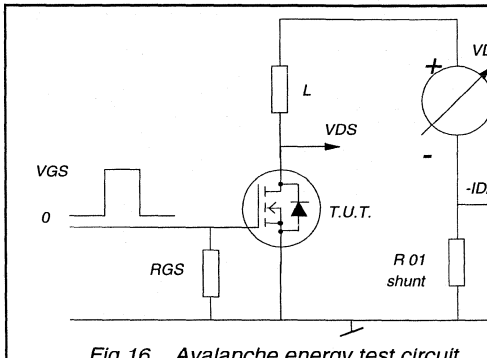


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PowerMOS transistor | BUK464-200A

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

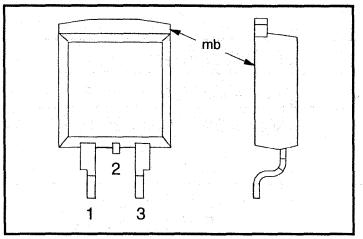
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (DC)	9.2	A
P_{tot}	Total power dissipation	90	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.4	Ω

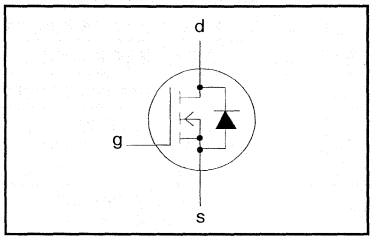
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	200	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	9.2	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	6.5	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	36	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	90	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.67	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board (see Fig. 18).	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 3.5 A	-	0.35	0.4	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 3.5 A	3.5	5.0	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	700	850	pF
C_{oss}	Output capacitance		-	100	160	pF
C_{rss}	Feedback capacitance		-	50	80	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.9 A;	-	12	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	45	70	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	80	120	ns
t_f	Turn-off fall time		-	40	60	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	9.2	A
I_{DRM}	Pulsed reverse drain current	-	-	-	36	A
V_{SD}	Diode forward voltage	I_F = 9.2 A ; V_{GS} = 0 V	-	1.1	1.3	V
t_{rr}	Reverse recovery time	I_F = 9.2 A; -dI_F/dt = 100 A/µs;	-	180	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	1.2	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 9 A ; $V_{DD} \leq$ 100 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	50	mJ

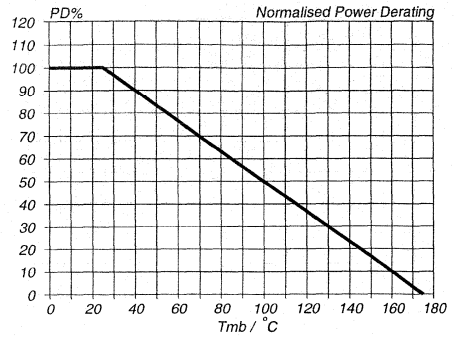


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

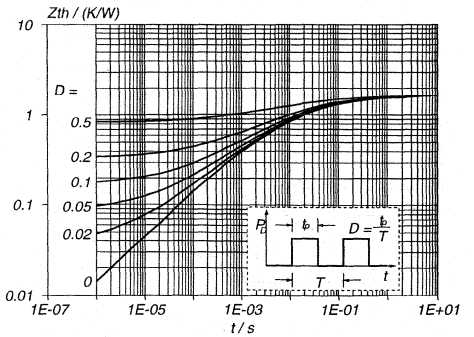


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

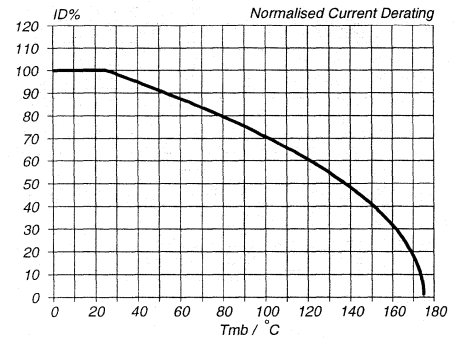


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

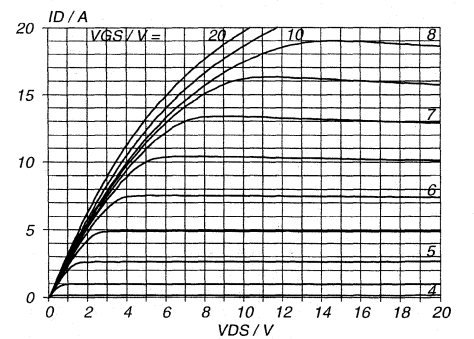


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

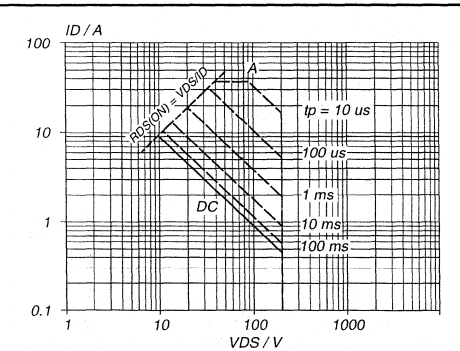


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

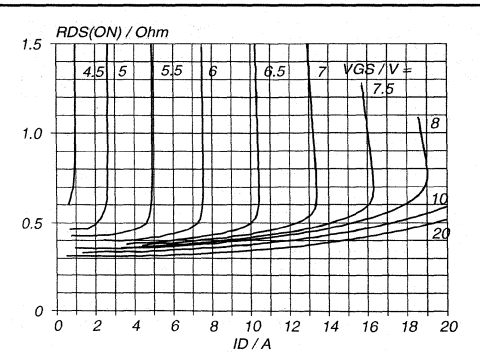


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

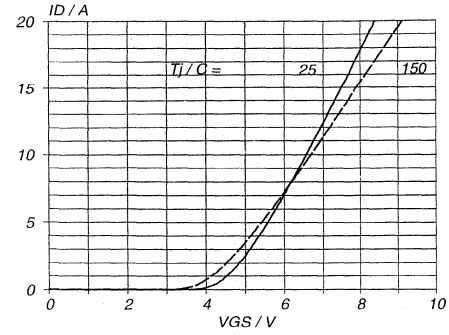


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

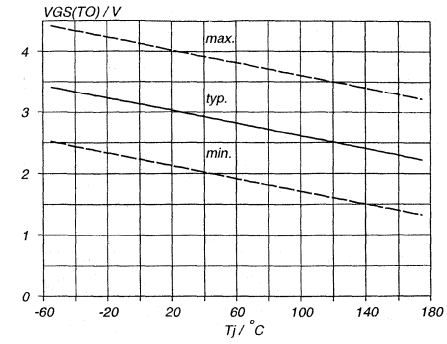


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

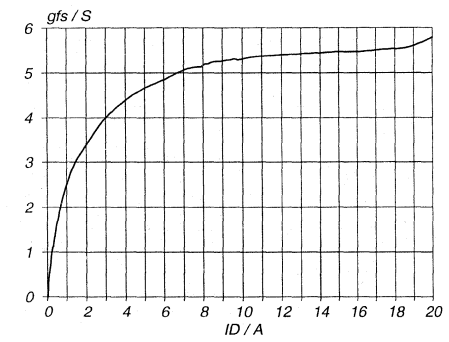


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

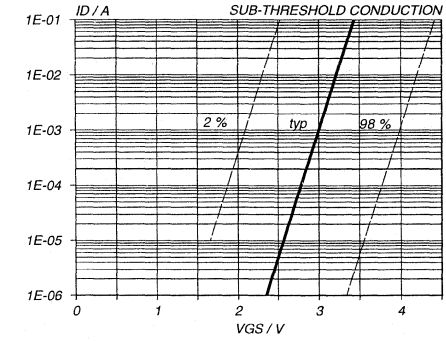


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

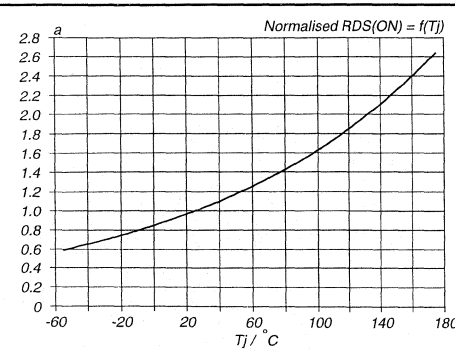


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 3.5 A; V_{GS} = 10 V

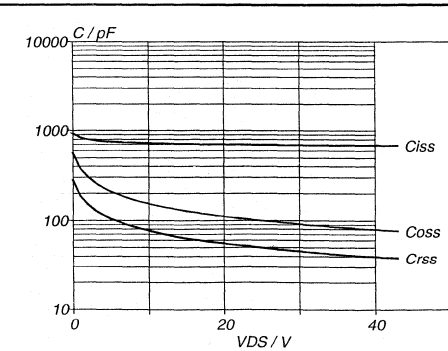


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

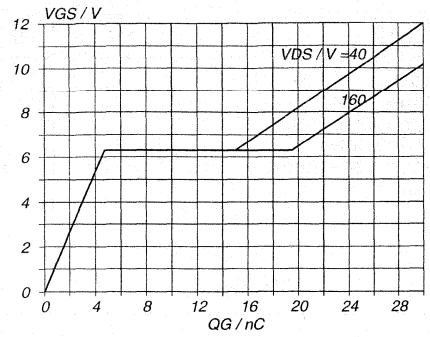


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 9.2$ A; parameter V_{DS}

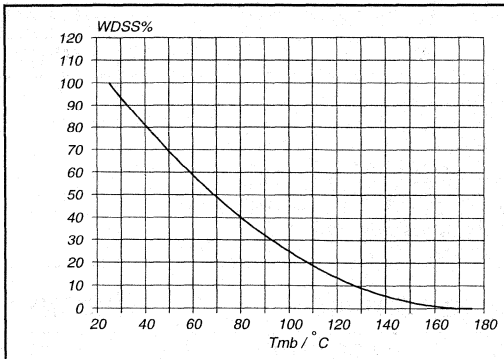


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 9$ A

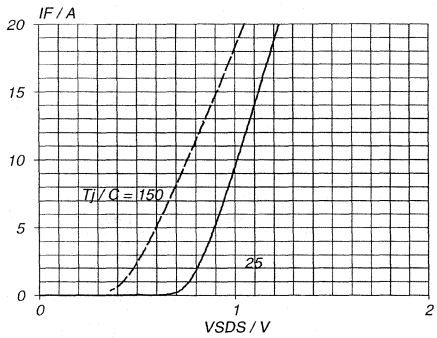


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

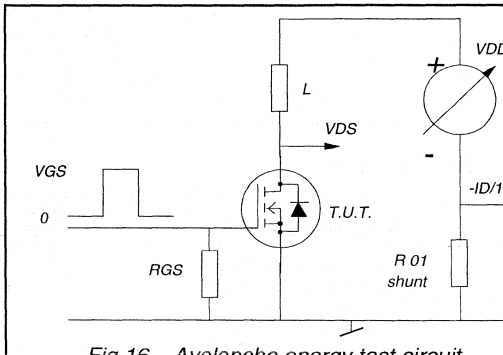


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor — BUK465-100A

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

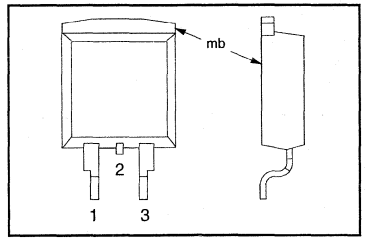
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	26	A
P_{tot}	Total power dissipation	125	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.08	Ω

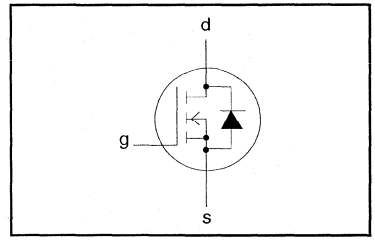
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	26	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	18	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	104	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint FR4 board (see Fig 18).	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 13 A	-	0.07	0.08	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 13 A	7.0	13.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1650	2000	pF
C_{oss}	Output capacitance		-	350	500	pF
C_{rss}	Feedback capacitance		-	100	150	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	15	30	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	100	160	ns
t_f	Turn-off fall time		-	50	80	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	26	A
I_{DRM}	Pulsed reverse drain current	-	-	-	104	A
V_{SD}	Diode forward voltage	I_F = 26 A ; V_{GS} = 0 V	-	1.3	1.7	V
t_{rr}	Reverse recovery time	I_F = 26 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.8	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 26 A ; V_{DD} ≤ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	100	mJ

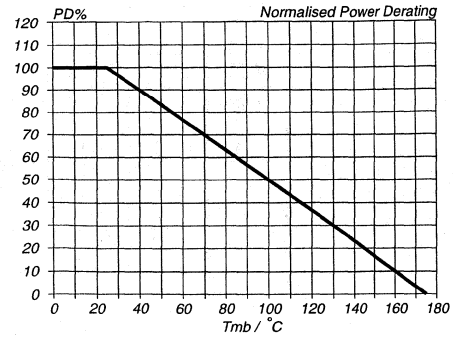


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

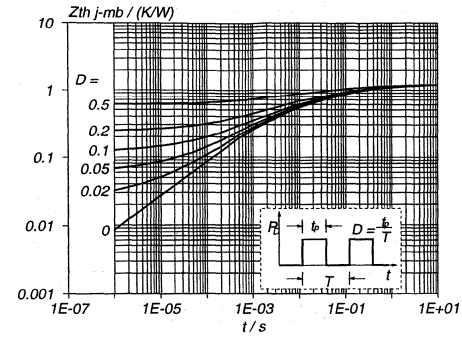


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

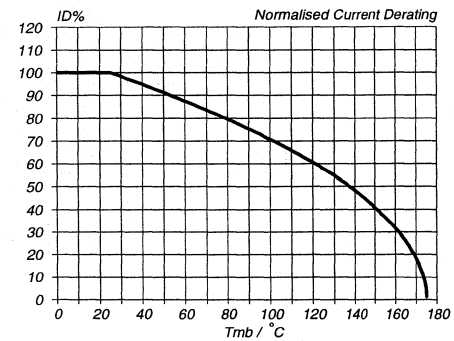


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

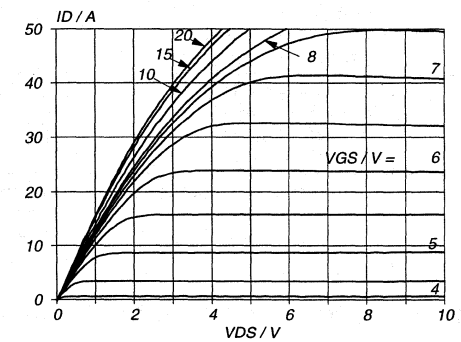


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

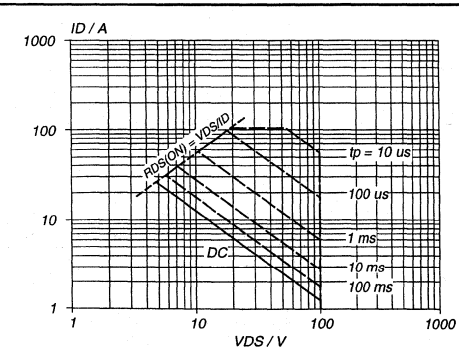


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

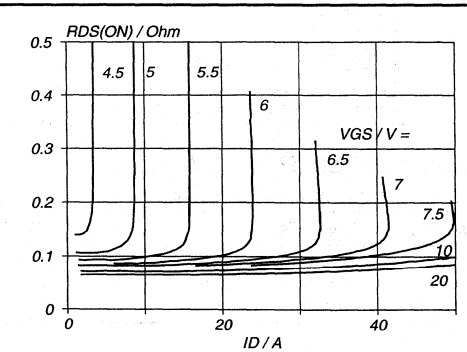


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

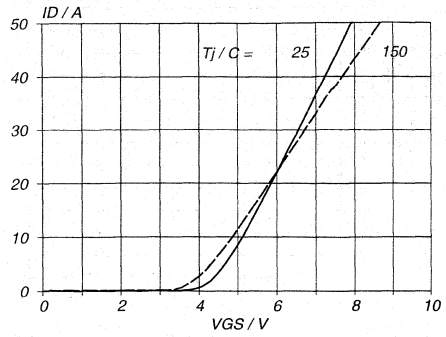


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

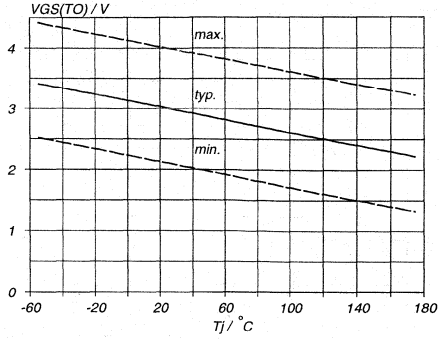


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

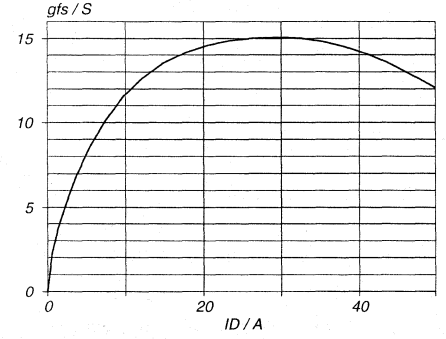


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

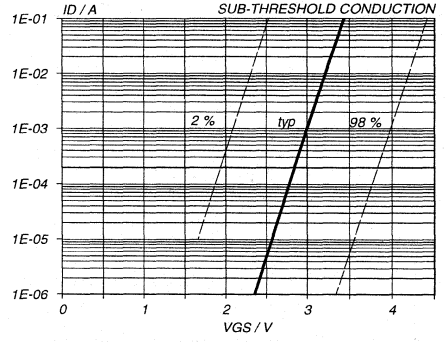


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

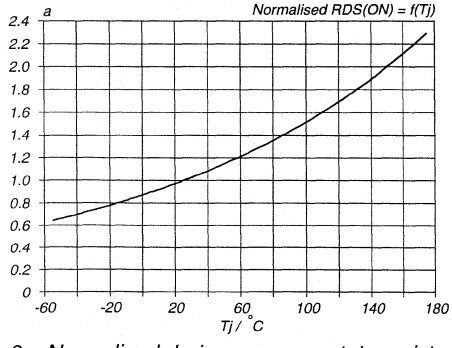


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ °C} = f(T_j)$; I_D = 13 A; V_{GS} = 10 V

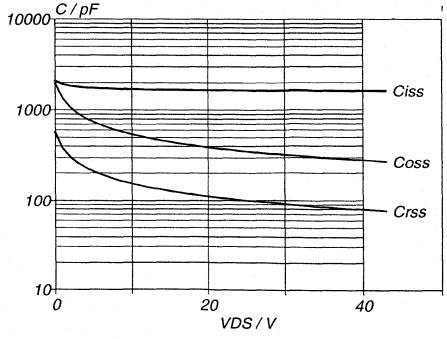


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

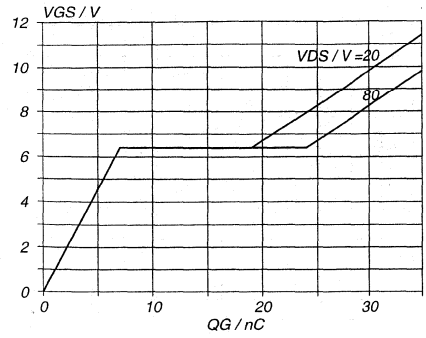


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 26$ A; parameter V_{DS}

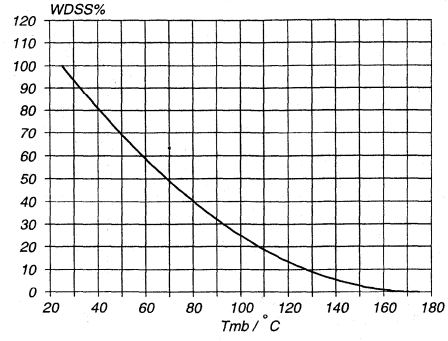


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 26$ A

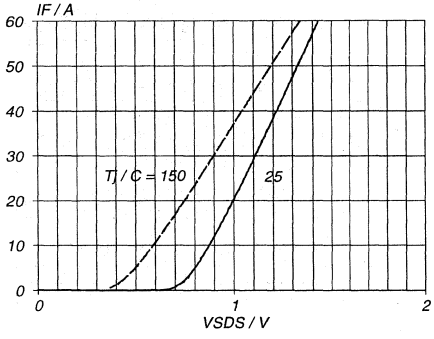


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

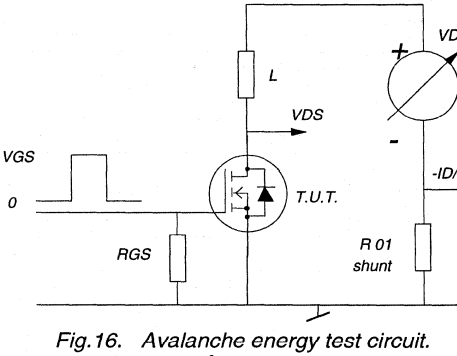


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

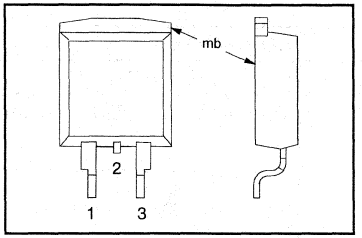
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (DC)	14	A
P_{tot}	Total power dissipation	125	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.23	Ω

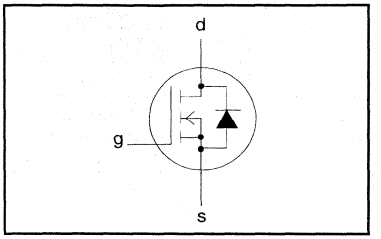
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	200	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	14	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	10	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	56	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board (see Fig. 18.)	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 7 A	-	0.2	0.23	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 7 A	6	8.4	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1400	1750	pF
C_{oss}	Output capacitance		-	190	250	pF
C_{rss}	Feedback capacitance		-	55	80	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	18	30	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	35	60	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	85	120	ns
t_f	Turn-off fall time		-	35	50	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	14	A
I_{DRM}	Pulsed reverse drain current	-	-	-	56	A
V_{SD}	Diode forward voltage	I_F = 14 A ; V_{GS} = 0 V	-	1.0	1.5	V
t_{rr}	Reverse recovery time	I_F = 14 A; -dI_F/dt = 100 A/µs;	-	180	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	1.8	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 14 A ; V_{DD} ≤ 100 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	100	mJ

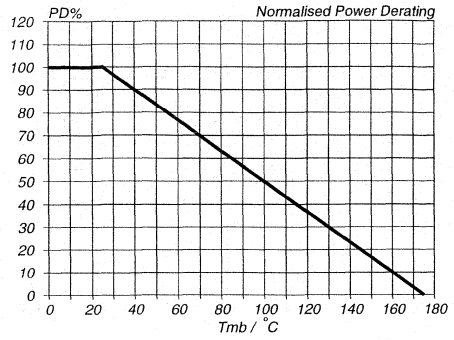


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

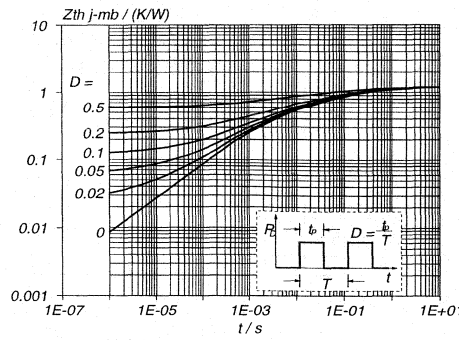


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

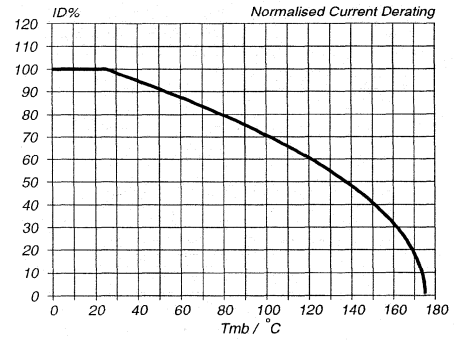


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

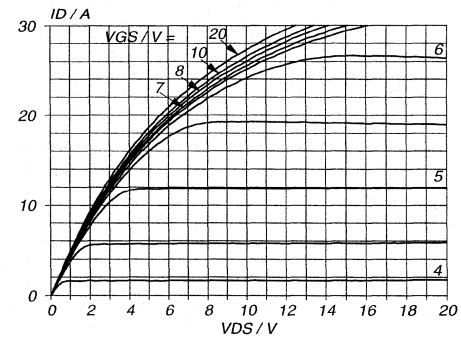


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

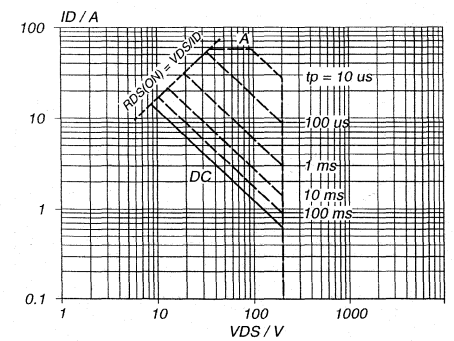


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

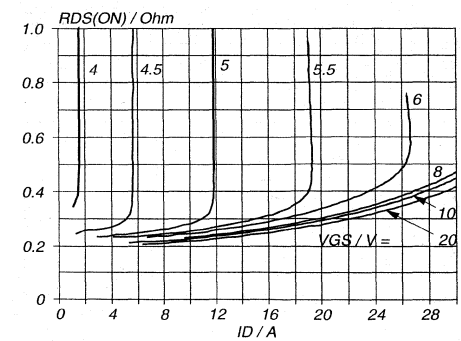


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

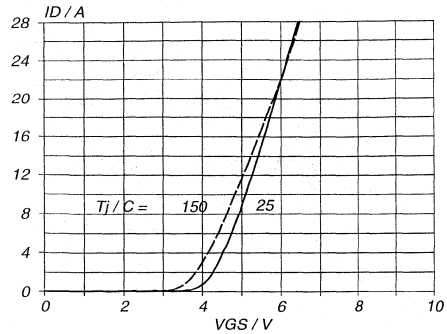


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

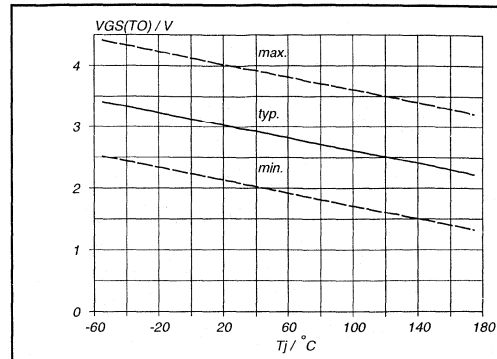


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

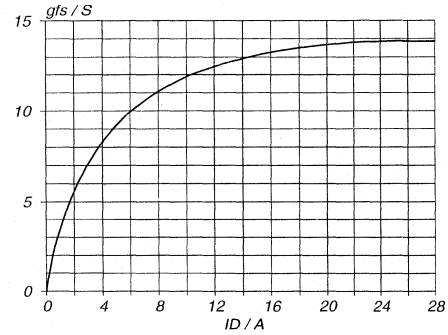


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

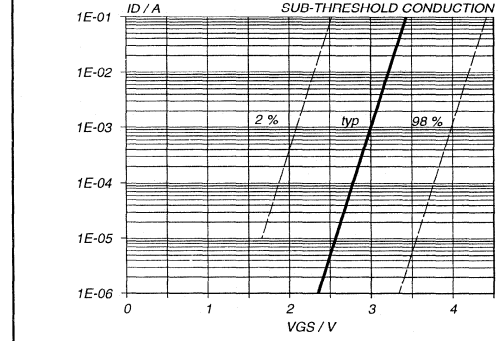


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

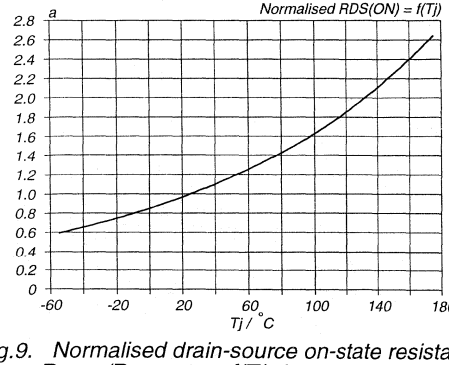


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 7 A; V_{GS} = 10 V

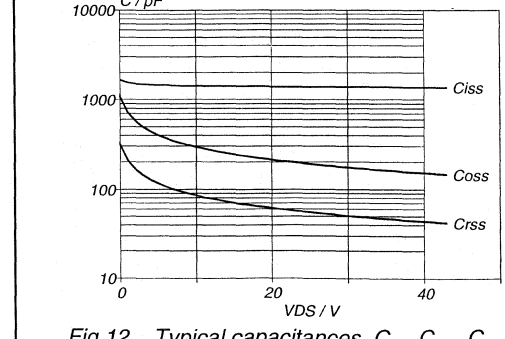


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

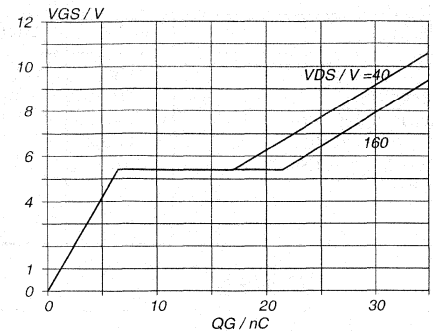


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 14 A; parameter V_{DS}

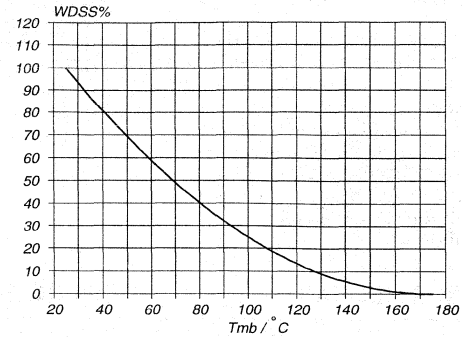


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: I_D = 14 A

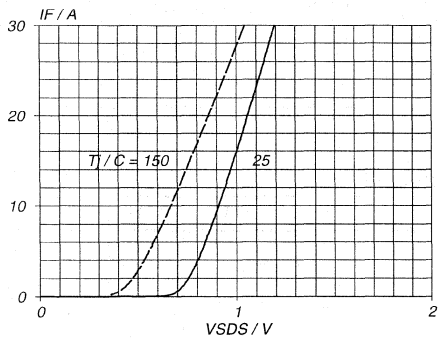


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

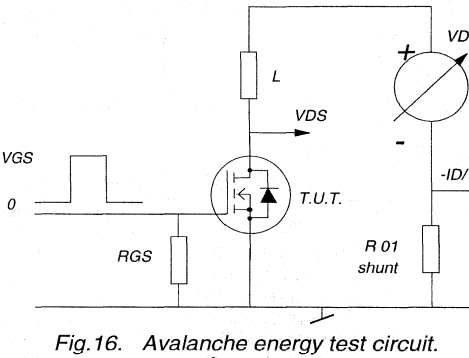


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

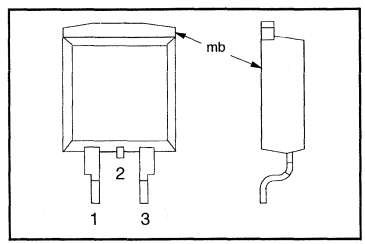
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	34	A
P_{tot}	Total power dissipation	150	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.057	Ω

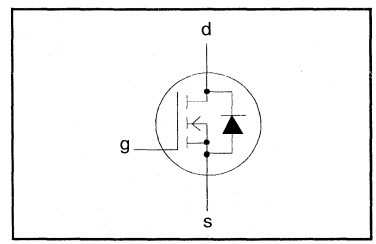
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	34	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	24	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	136	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	150	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board (see Fig. 18).	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 15 A	-	0.052	0.057	Ω

DYNAMIC CHARACTERISTICS

Tmb = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 15 A	12	16	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1500	2000	pF
C_{oss}	Output capacitance		-	450	600	pF
C_{rss}	Feedback capacitance		-	130	200	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	20	30	ns
t_r	Turn-on rise time	V_{GS} = 10 V;	-	40	60	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω;	-	150	200	ns
t_f	Turn-off fall time	R_{GS} = 50 Ω	-	65	85	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

Tmb = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	34	A
I_{DRM}	Pulsed reverse drain current	-	-	-	136	A
V_{SD}	Diode forward voltage	I_F = 34 A ; V_{GS} = 0 V	-	1.8	2.5	V
t_{rr}	Reverse recovery time	I_F = 34 A; -dI_F/dt = 100 A/µs;	-	100	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	1.0	-	µC

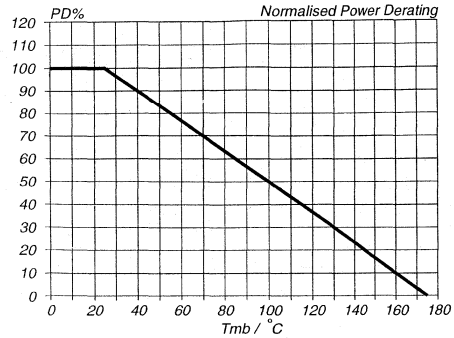


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

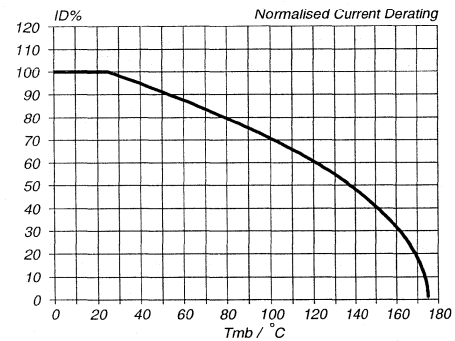


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

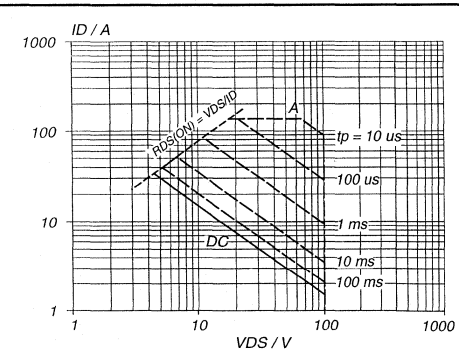


Fig.3. Safe operating area. T_{mb} = 25 ˚C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

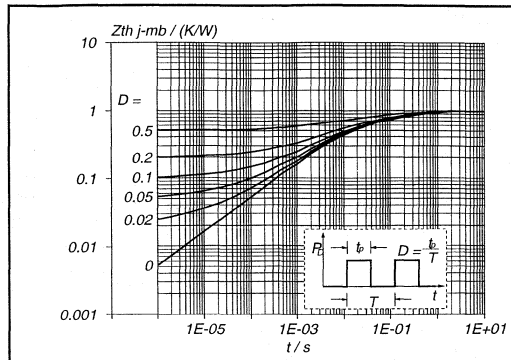


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

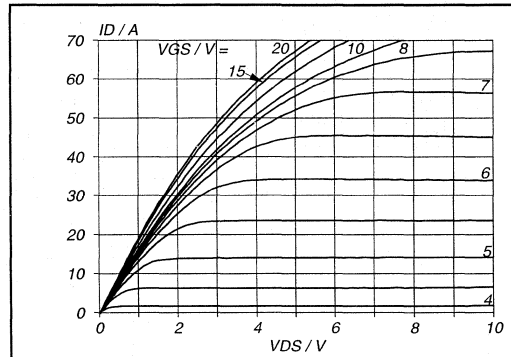


Fig.5. Typical output characteristics, T_j = 25 ˚C.
I_D = f(V_{DS}); parameter V_{GS}

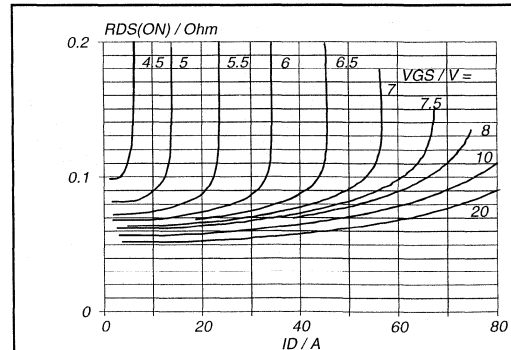


Fig.6. Typical on-state resistance, T_j = 25 ˚C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

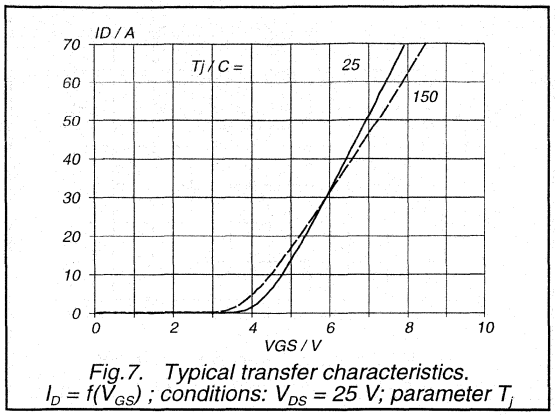


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

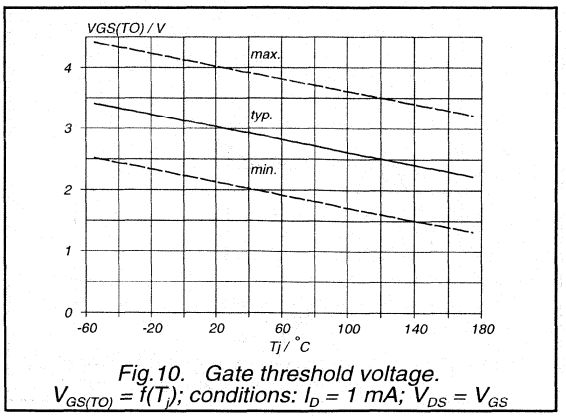


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

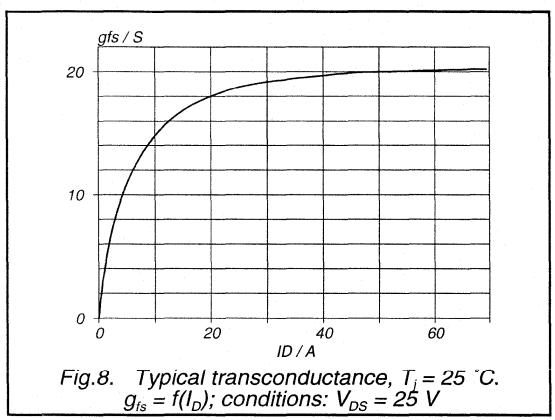


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

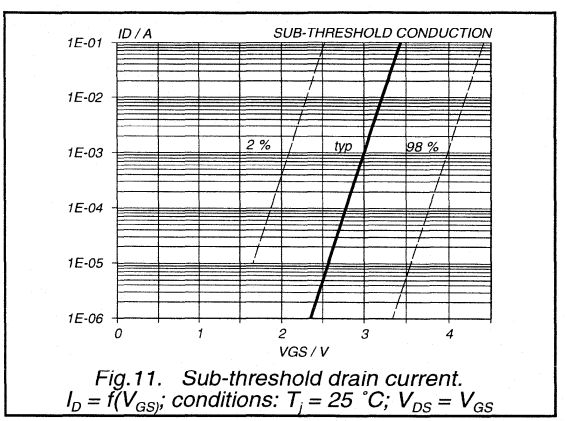


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

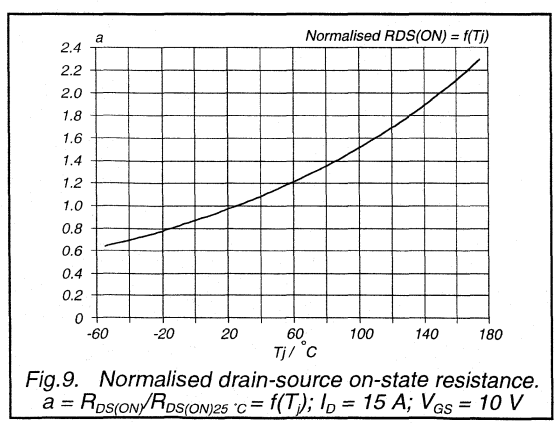


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 15 A; V_{GS} = 10 V

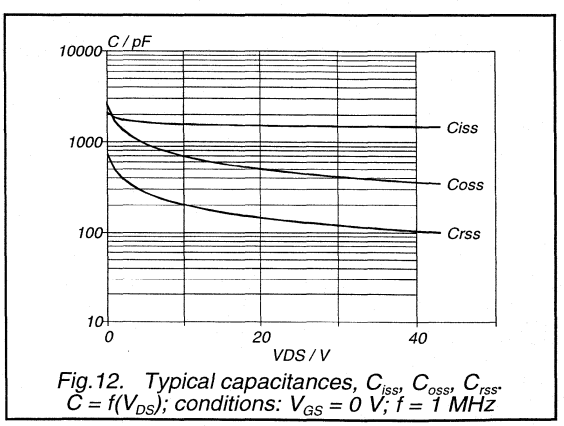


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

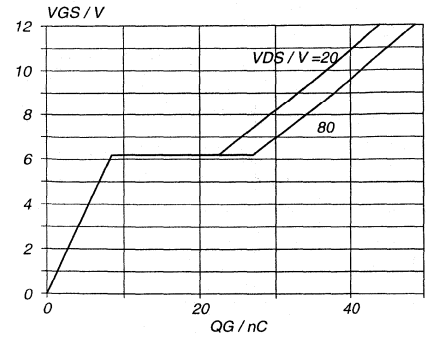


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 34$ A; parameter V_{DS}

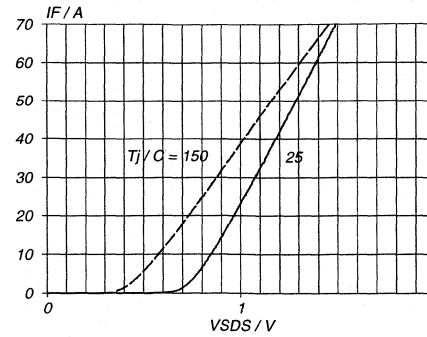


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

PowerMOS transistor — BUK466-200A

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for use in surface mount applications.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

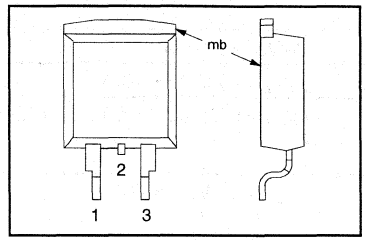
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (DC)	19	A
P_{tot}	Total power dissipation	150	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.16	Ω

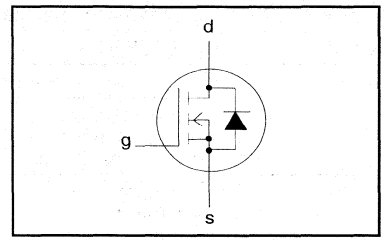
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	200	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	19	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	13	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	76	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	150	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board (see Fig. 18).	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 10 A	-	0.15	0.16	Ω

DYNAMIC CHARACTERISTICS

Tmb = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 10 A	8.5	16	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1500	2000	pF
C_{oss}	Output capacitance		-	300	400	pF
C_{rss}	Feedback capacitance		-	60	100	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	20	30	ns
t_r	Turn-on rise time	V_{GS} = 10 V;	-	40	60	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω;	-	145	185	ns
t_f	Turn-off fall time	R_{GS} = 50 Ω	-	50	70	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

Tmb = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	19	A
I_{DRM}	Pulsed reverse drain current	-	-	-	76	A
V_{SD}	Diode forward voltage	I_F = 19 A ; V_{GS} = 0 V	-	1.0	1.7	V
t_{rr}	Reverse recovery time	I_F = 19 A; -dI_F/dt = 100 A/µs;	-	180	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	2.5	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 19 A ; V_{DD} ≤ 30 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	150	mJ

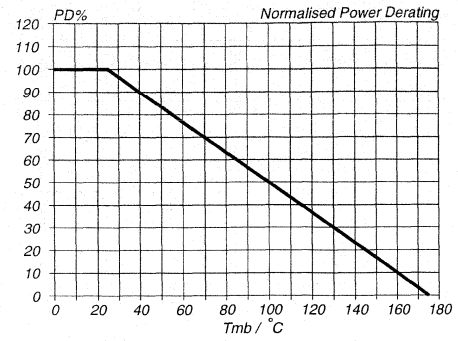


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

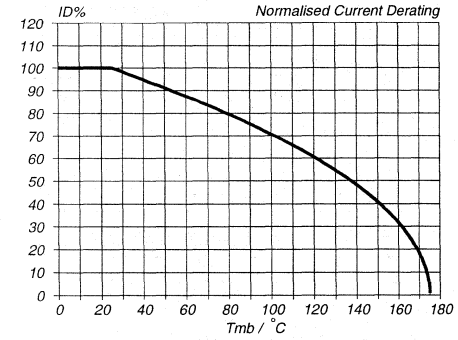


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

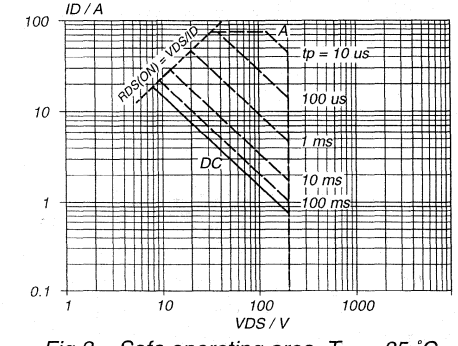


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

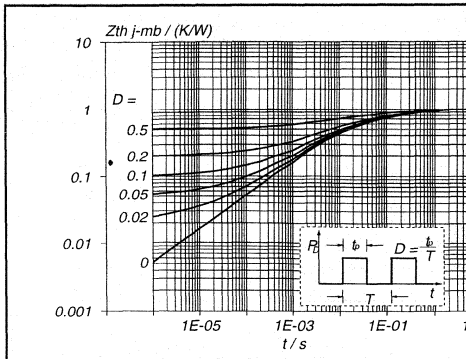


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

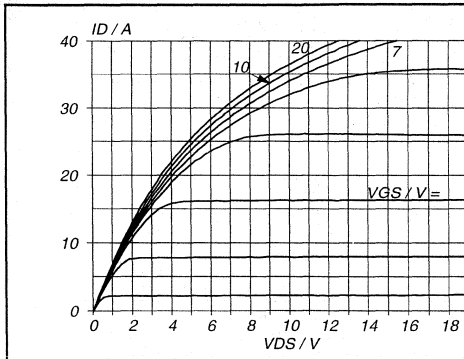


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

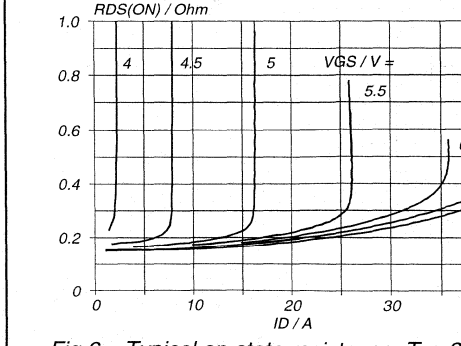


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

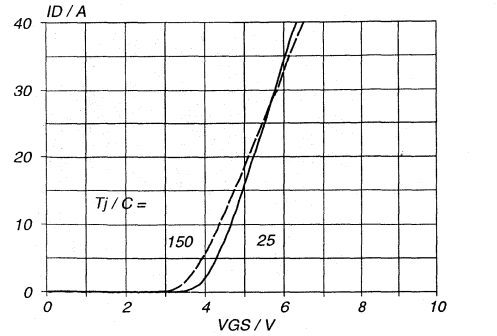


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

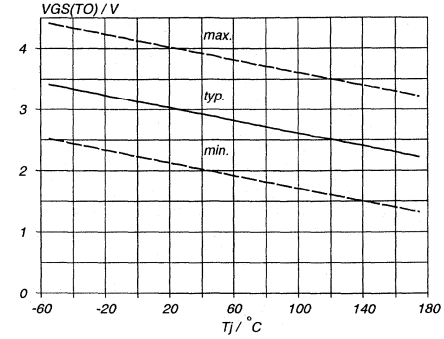


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

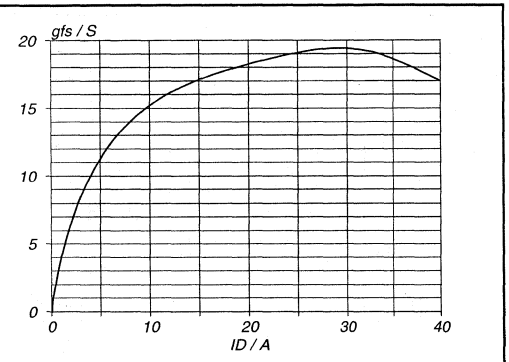


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

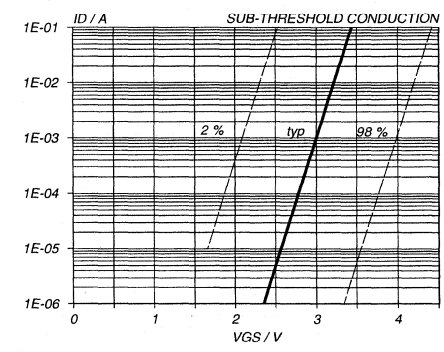


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

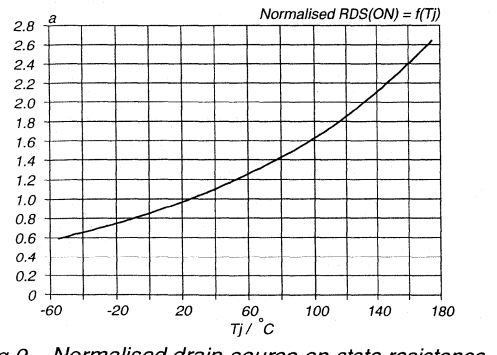


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 10 A; V_{GS} = 10 V

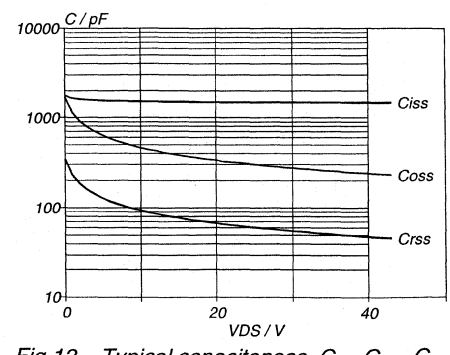


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

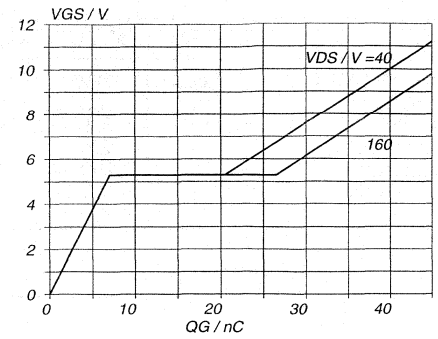


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 19$ A; parameter V_{DS}

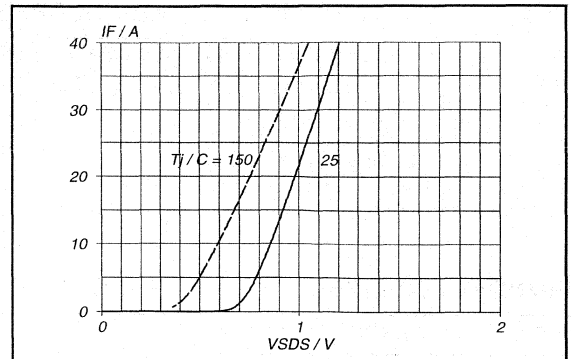


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

PowerMOS transistor
Isolated version of BUK452-100A/B

BUK472-100A/B

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic full-pack envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

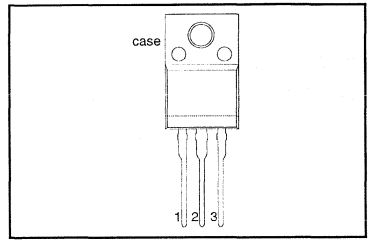
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK472	-100A	-100B	
V_{DS}	Drain-source voltage	100	100	V
I_D	Drain current (DC)	6.6	6.1	A
P_{tot}	Total power dissipation	22	22	W
T_j	Junction temperature	150	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.25	0.3	Ω

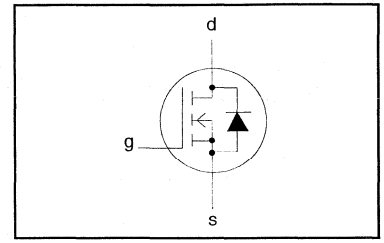
PINNING - SOT186A

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	100		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-100A	-100B	
I_D	Drain current (DC)	T_{hs} = 25 °C	-	6.6	6.1	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	4.1	3.8	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	26	24	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	22		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	5.68	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK472-100A**	-	0.22	0.25	Ω
		I_D = 5.5 A **BUK472-100B**	-	0.25	0.3	Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5.5 A	3	4.2	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	400	500	pF
C_{oss}	Output capacitance		-	90	120	pF
C_{rss}	Feedback capacitance		-	35	50	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	9	14	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	30	45	ns
t_f	Turn-off fall time		-	20	40	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	6.6	A
I_{DRM}	Pulsed reverse drain current	-	-	-	26	A
V_{SD}	Diode forward voltage	I_F = 6.6 A ; V_{GS} = 0 V	-	1.2	1.5	V
t_{rr}	Reverse recovery time	I_F = 6.6 A; -dI_F/dt = 100 A/µs;	-	80	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.30	-	µC

AVALANCHE LIMITING VALUE

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 11 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	35	mJ

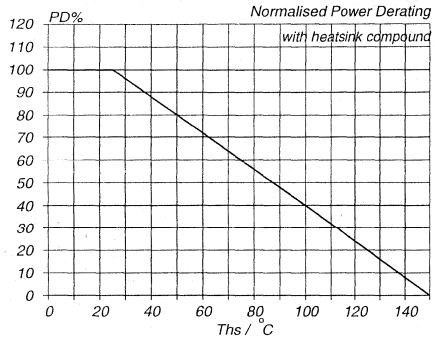


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{hs})

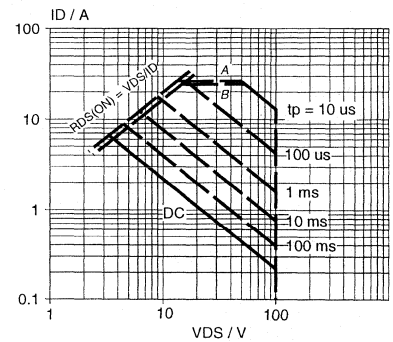


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

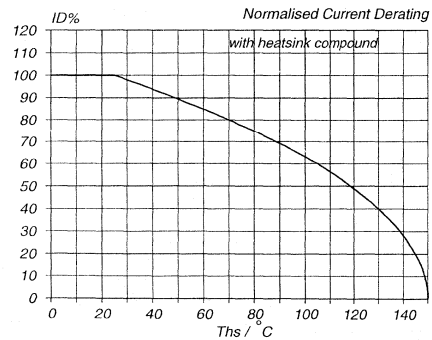


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{hs}); conditions: $V_{GS} \geq$ 10 V

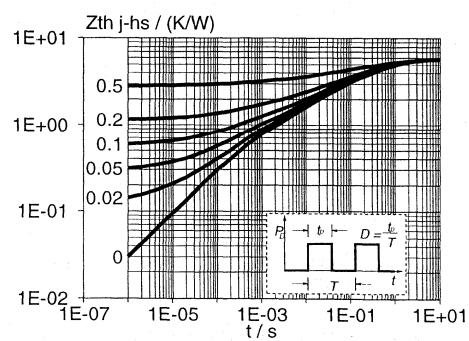


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}hs}$ = f(t); parameter D = t_p/T

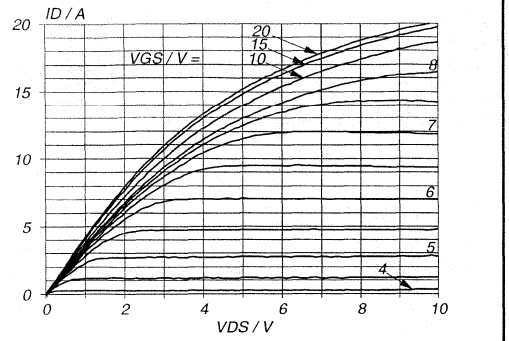


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

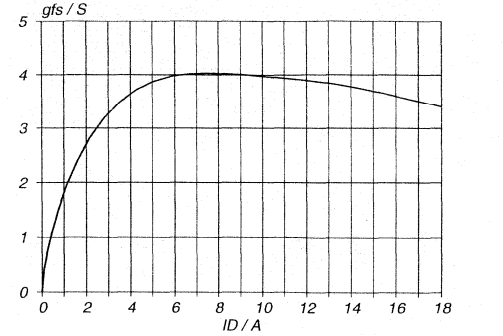


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

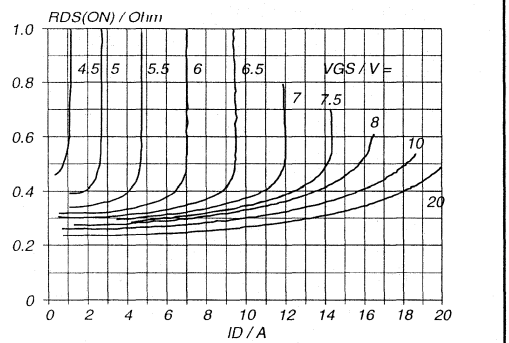


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

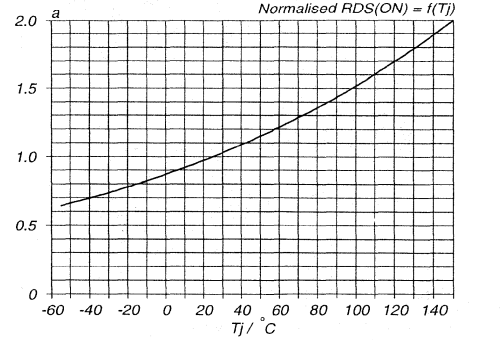


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,˚C} = f(T_j)$; I_D = 5.5 A; V_{GS} = 10 V

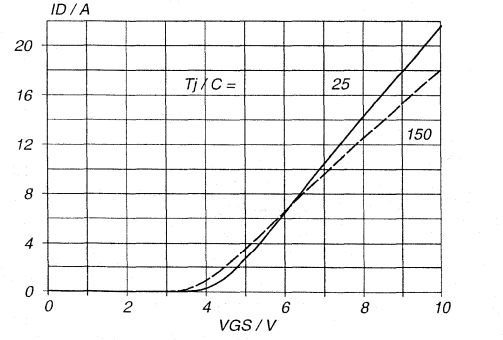


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

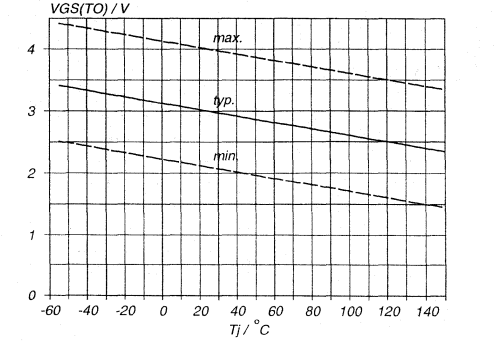


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

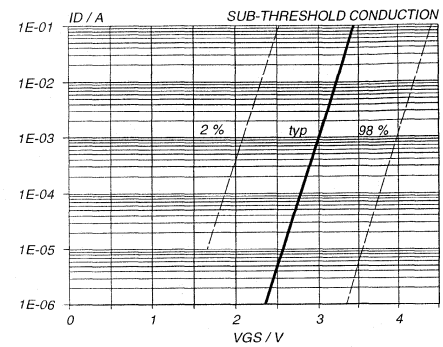


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

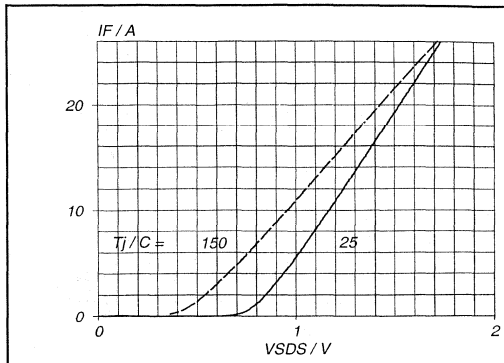


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

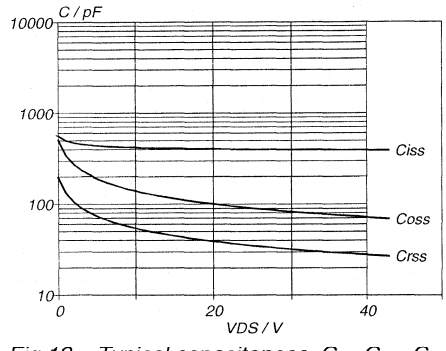


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

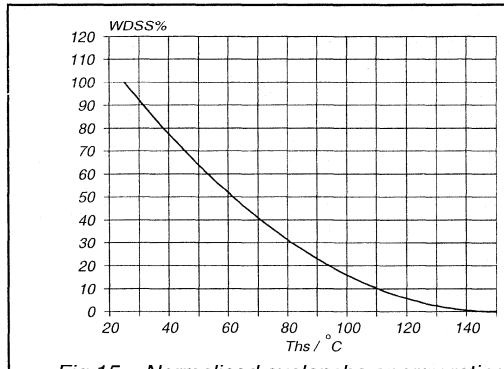


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{hs})$; conditions: $I_D = 11$ A

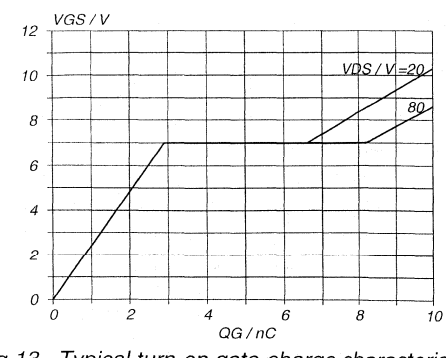


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 11$ A; parameter V_{DS}

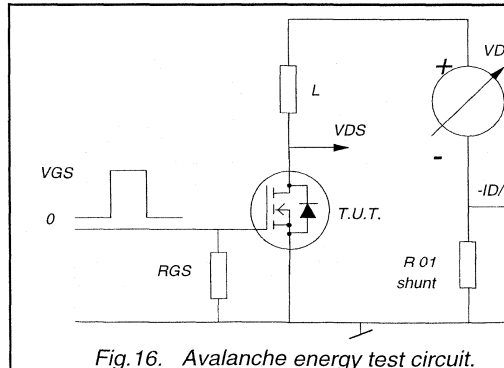


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PowerMOS transistor
Isolated version of BUK453-100A/B

BUK473-100A/B

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic full-pack envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

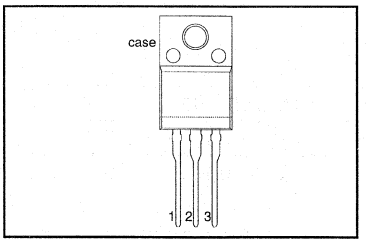
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK473	-100A	-100B	
V_{DS}	Drain-source voltage	100	100	V
I_D	Drain current (DC)	9	8	A
P_{tot}	Total power dissipation	25	25	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.16	0.2	Ω

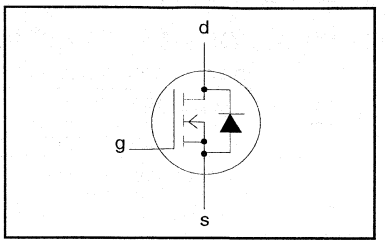
PINNING - SOT186A

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	100		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-100A	-100B	
I_D	Drain current (DC)	T_{hs} = 25 °C	-	9	8	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	5.7	5	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	36	32	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	25		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A **BUK473-100A**	-	0.15	0.16	Ω
		BUK473-100B	-	0.17	0.2	Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5 A	4.0	5.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	660	825	pF
C_{oss}	Output capacitance		-	140	200	pF
C_{rss}	Feedback capacitance		-	60	100	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.9 A;	-	10	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	60	90	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	9	A
I_{DRM}	Pulsed reverse drain current	-	-	-	36	A
V_{SD}	Diode forward voltage	I_F = 9 A ; V_{GS} = 0 V	-	1.1	1.3	V
t_{rr}	Reverse recovery time	I_F = 9 A; -dI_F/dt = 100 A/µs;	-	80	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.5	-	µC

AVALANCHE LIMITING VALUE

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 14 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	70	mJ

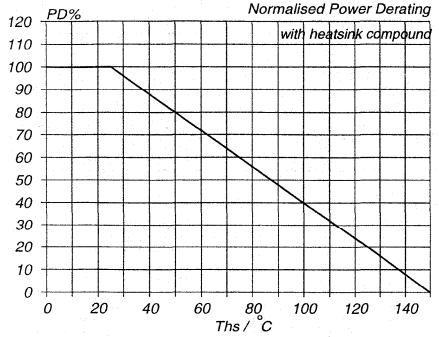


Fig.1. Normalised power dissipation. PD% = 100·P_D/$P_{D\ 25\ ˚C}$ = f(T_{hs})

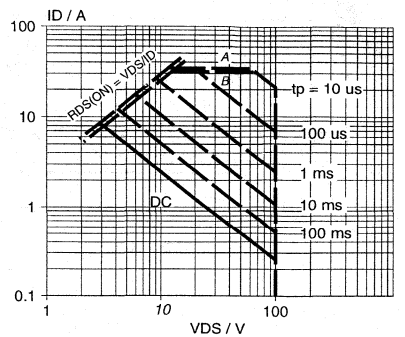


Fig.3. Safe operating area. T_{hs} = 25 ˚C I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

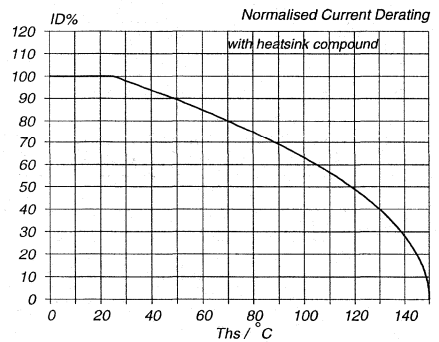


Fig.2. Normalised continuous drain current. ID% = 100·I_D/$I_{D\ 25\ ˚C}$ = f(T_{hs}); conditions: $V_{GS} \geq$ 10 V

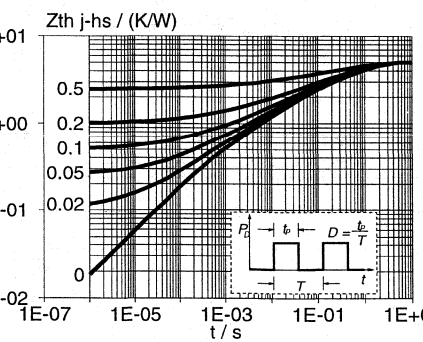


Fig.4. Transient thermal impedance. $Z_{th\ j\text{-}hs}$ = f(t); parameter D = t_p/T

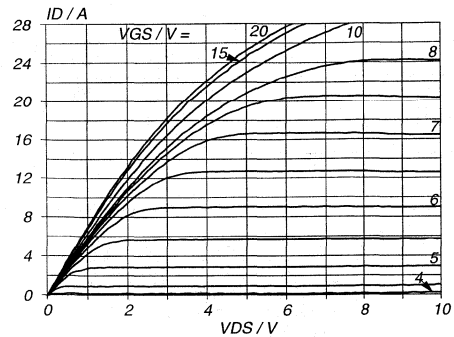


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

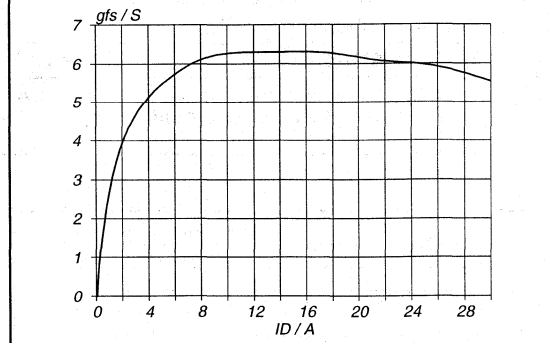


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

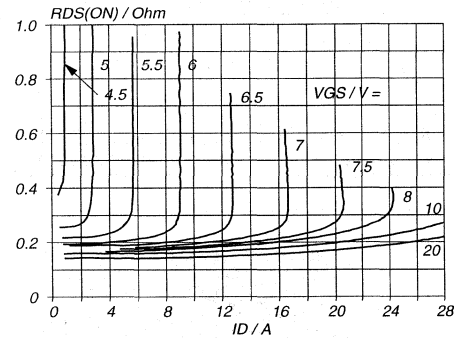


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

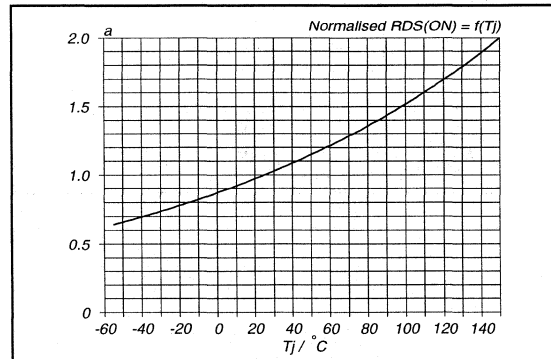


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,^{\circ}C} = f(T_j)$; I_D = 5 A; V_{GS} = 10 V

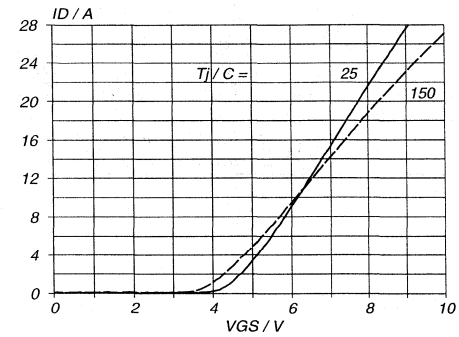


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

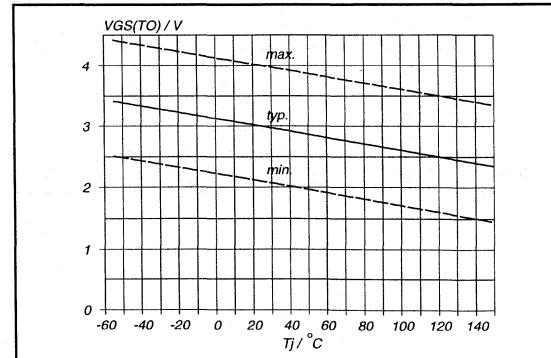


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

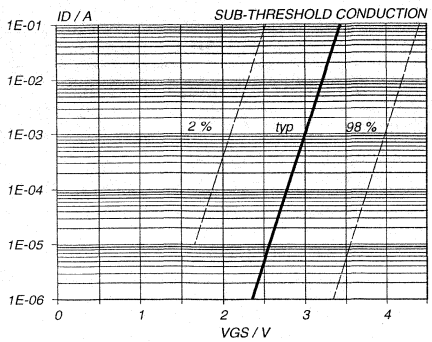


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

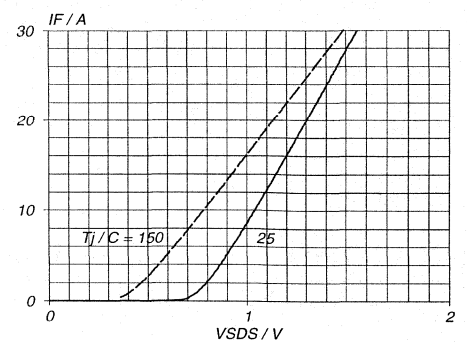


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

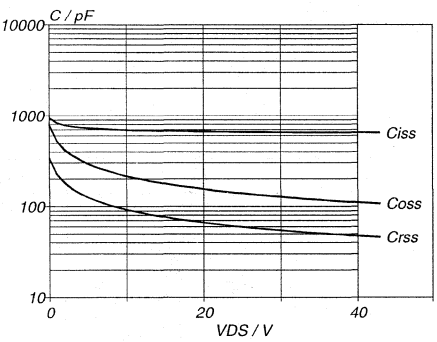


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

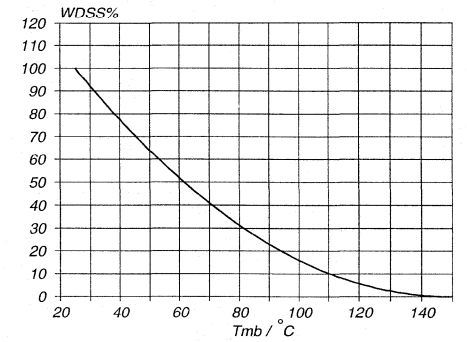


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{hs})$; conditions: I_D = 14 A

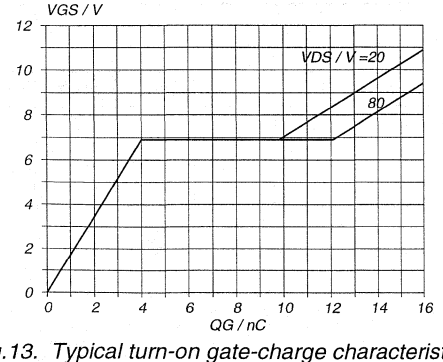


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 14 A; parameter V_{DS}

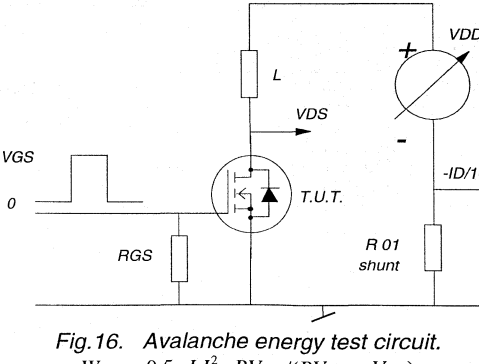


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor
Isolated version of BUK454-200A/B

BUK474-200A/B

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic full-pack envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

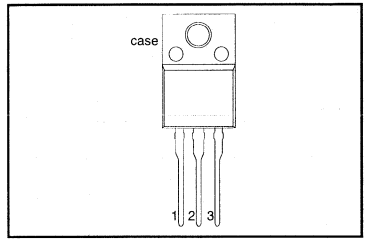
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK474	-200A	-200B	
V_{DS}	Drain-source voltage	200	200	V
I_D	Drain current (DC)	5.3	4.7	A
P_{tot}	Total power dissipation	25	25	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.4	0.5	Ω

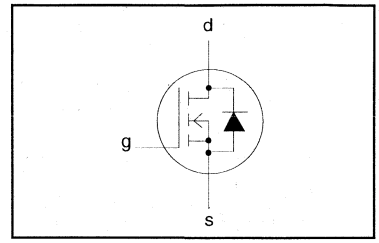
PINNING - SOT186A

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
				-200A	-200B	
V_{DS}	Drain-source voltage	-	-	200		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
I_D	Drain current (DC)	T_{hs} = 25 °C	-	5.3	4.7	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	3.3	3.0	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	21	19	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	25		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK474-200A**	-	0.35	0.4	Ω
		I_D = 3.5 A **BUK474-200B**	-	0.4	0.5	Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 3.5 A	3.5	5.0	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	700	850	pF
C_{oss}	Output capacitance		-	100	160	pF
C_{rss}	Feedback capacitance		-	50	80	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.9 A;	-	12	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	45	70	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	80	120	ns
t_f	Turn-off fall time		-	40	60	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	5.3	A
I_{DRM}	Pulsed reverse drain current	-	-	-	21	A
V_{SD}	Diode forward voltage	I_F = 5.3 A ; V_{GS} = 0 V	-	1.1	1.3	V
t_{rr}	Reverse recovery time	I_F = 5.3 A; -dI_F/dt = 100 A/µs;	-	150	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.9	-	µC

AVALANCHE LIMITING VALUE

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 9 A ; $V_{DD} \leq$ 100 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	50	mJ

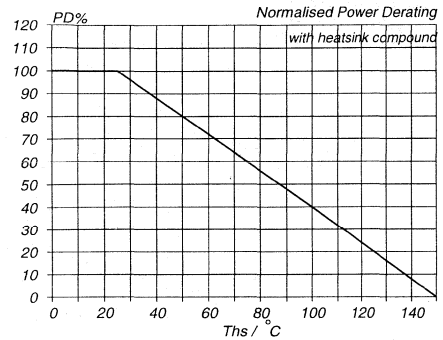


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{hs})

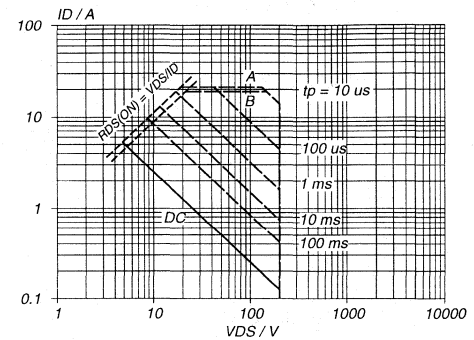


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

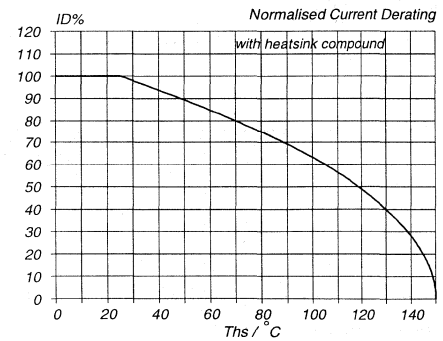


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{hs}); conditions: $V_{GS} \geq$ 10 V

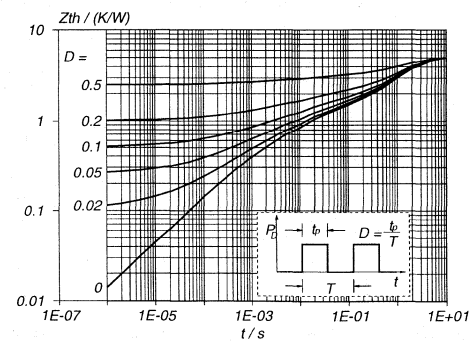


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}hs}$ = f(t); parameter D = t_p/T

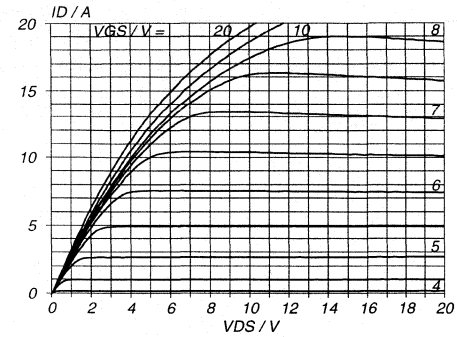


Fig.5. Typical output characteristics, T_j = 25 °C. $I_D = f(V_{DS})$; parameter V_{GS}

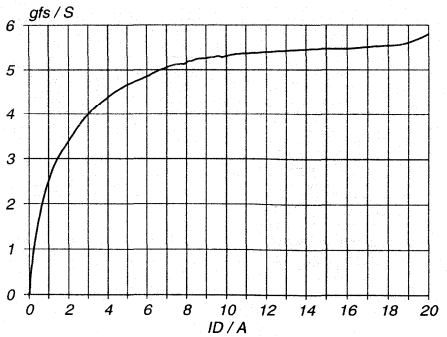


Fig.8. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

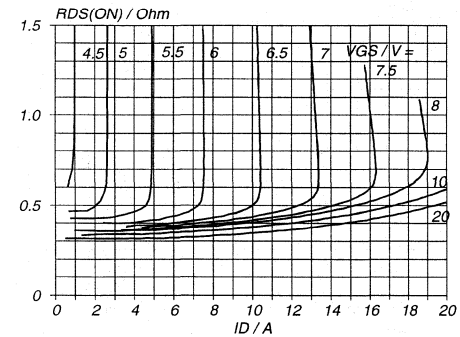


Fig.6. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

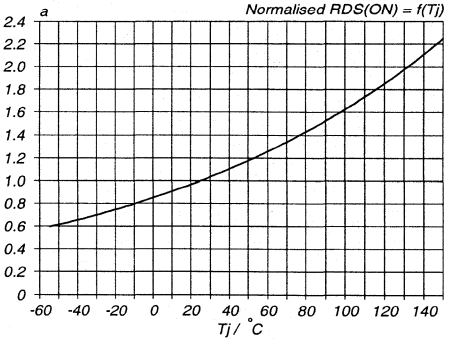


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 3.5 A; V_{GS} = 10 V

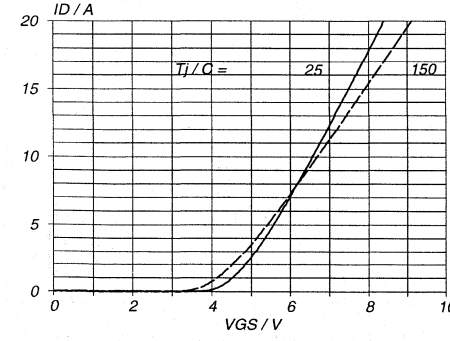


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

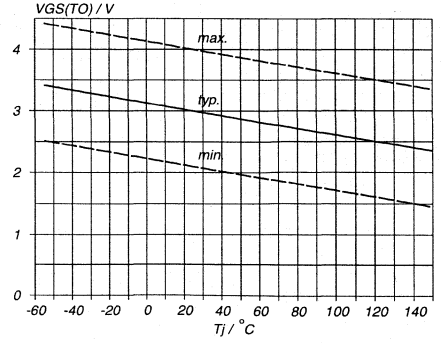


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

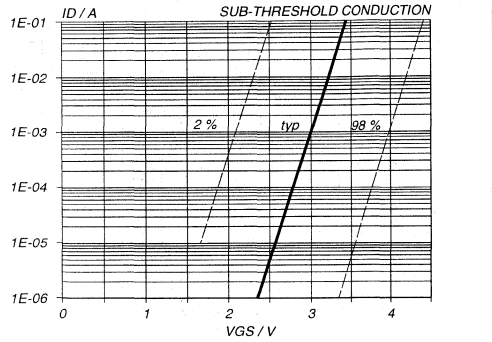


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

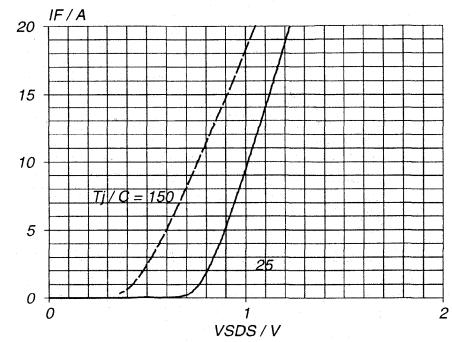


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

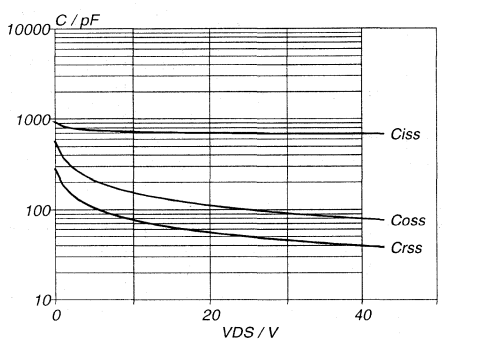


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

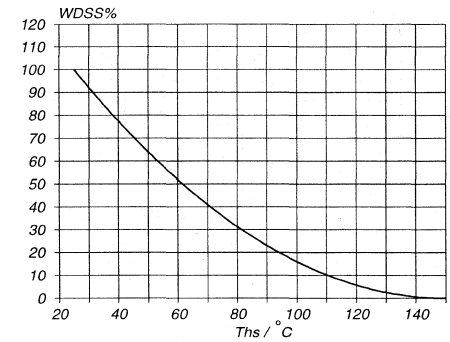


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{hs})$; conditions: $I_D = 9$ A

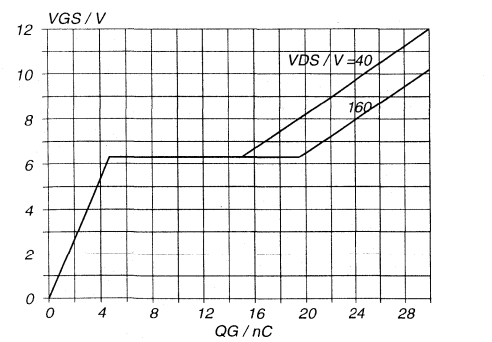


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 9$ A; parameter V_{DS}

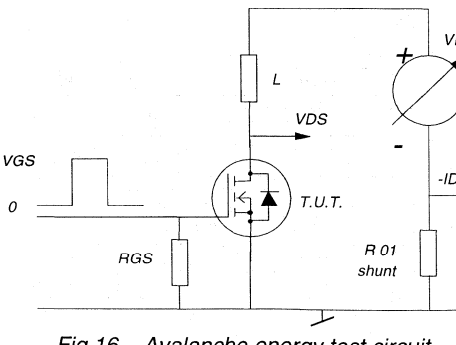


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PowerMOS transistor
Isolated version of BUK455-200A/B

BUK475-200A/B

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic full-pack envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

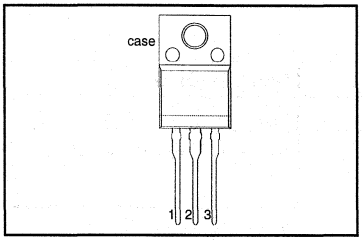
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK475	-200A	-200B	
V_{DS}	Drain-source voltage	200	200	V
I_D	Drain current (DC)	7.6	7	A
P_{tot}	Total power dissipation	30	30	W
T_j	Junction temperature	150	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.23	0.28	Ω

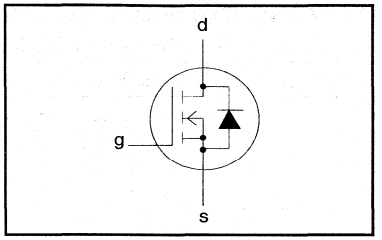
PINNING - SOT186A

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	200		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-200A	-200B	
I_D	Drain current (DC)	T_{hs} = 25 °C	-	7.6	7	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	4.8	4.4	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	30	28	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	30		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	4.17	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK475-200A**	-	0.2	0.23	Ω
		I_D = 7 A **BUK475-200B**	-	0.22	0.28	Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 7 A	6	8.4	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1400	1750	pF
C_{oss}	Output capacitance		-	190	250	pF
C_{rss}	Feedback capacitance		-	55	80	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	18	30	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	35	60	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	85	120	ns
t_f	Turn-off fall time		-	35	50	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	7.6	A
I_{DRM}	Pulsed reverse drain current	-	-	-	30	A
V_{SD}	Diode forward voltage	I_F = 7.6 A ; V_{GS} = 0 V	-	1.0	1.5	V
t_{rr}	Reverse recovery time	I_F = 7.6 A; -dI_F/dt = 100 A/µs;	-	150	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	1.3	-	µC

AVALANCHE LIMITING VALUE

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 14 A ; $V_{DD} \leq$ 100 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	100	mJ

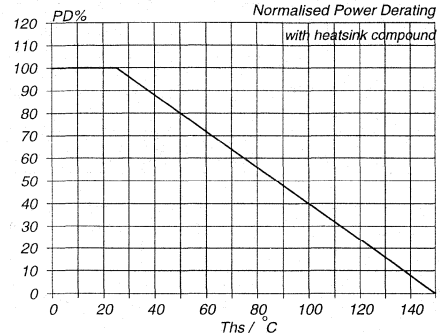


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{hs})

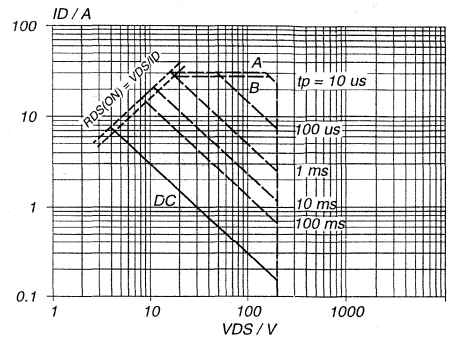


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

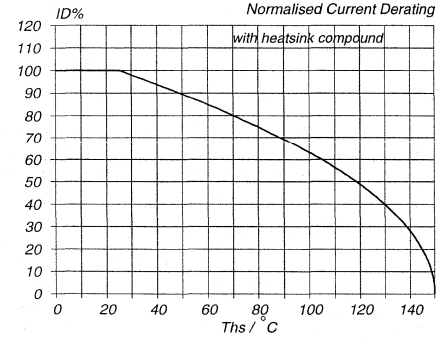


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{hs}); conditions: $V_{GS} \geq$ 10 V

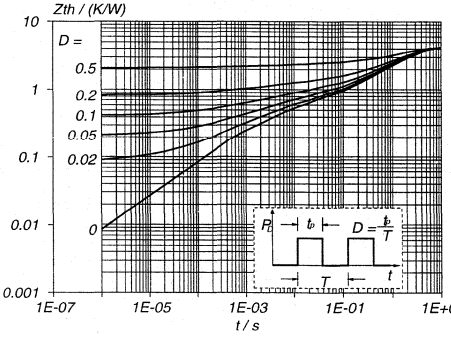


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}hs}$ = f(t); parameter D = t_p/T

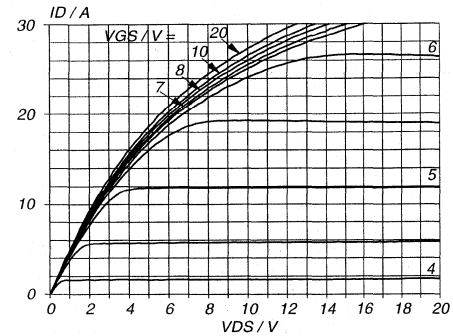


Fig.5. Typical output characteristics, T_j = 25 °C. $I_D = f(V_{DS})$; parameter V_{GS}

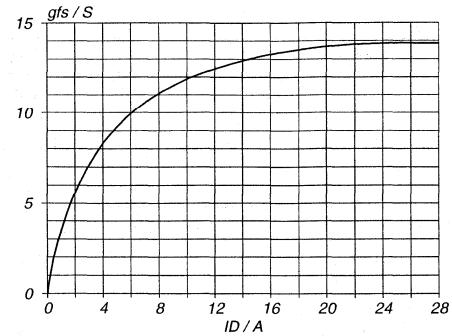


Fig.8. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

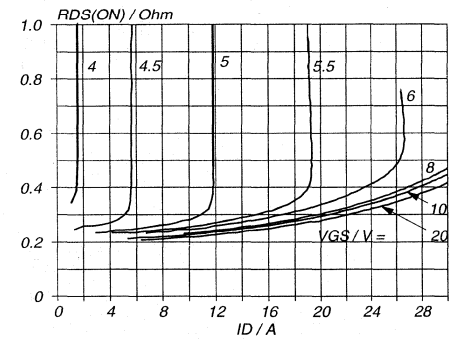


Fig.6. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

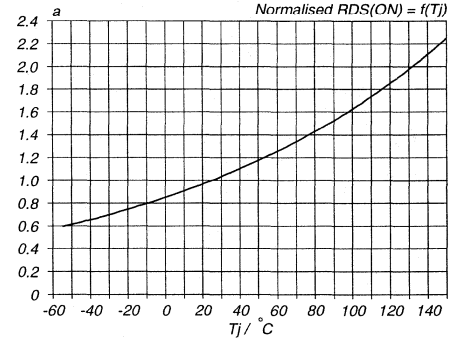


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 7 A; V_{GS} = 10 V

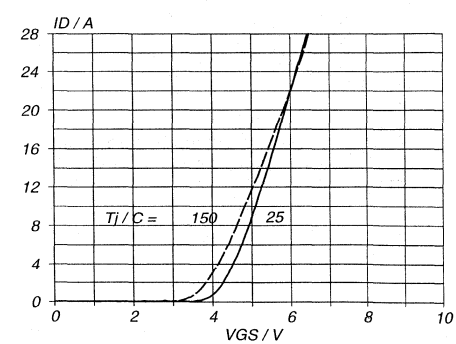


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

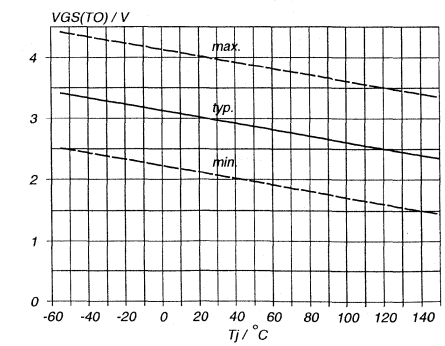


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

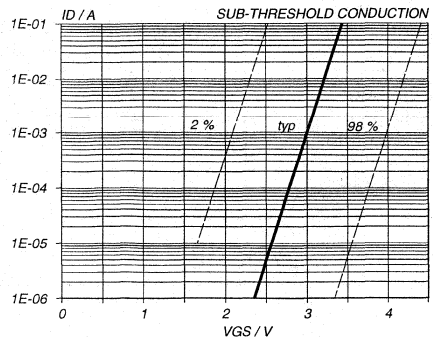


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

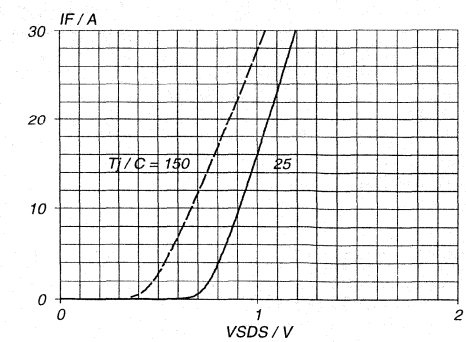


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

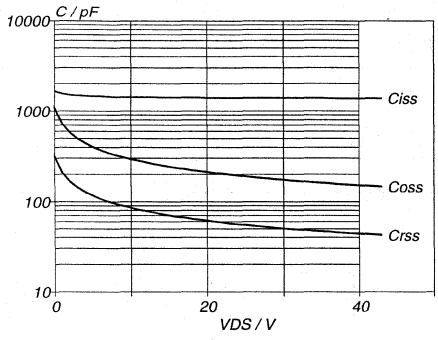


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

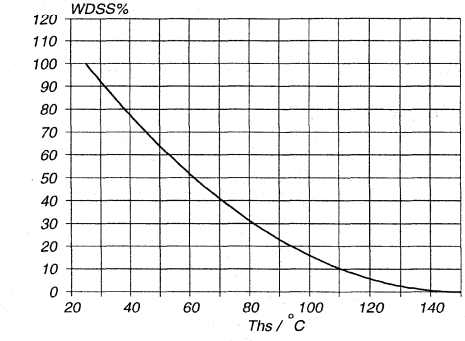


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{hs})$; conditions: $I_D = 14$ A

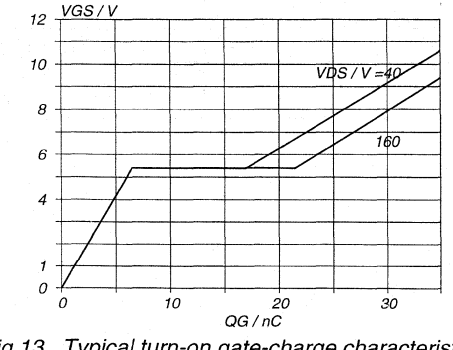


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 14$ A; parameter V_{DS}

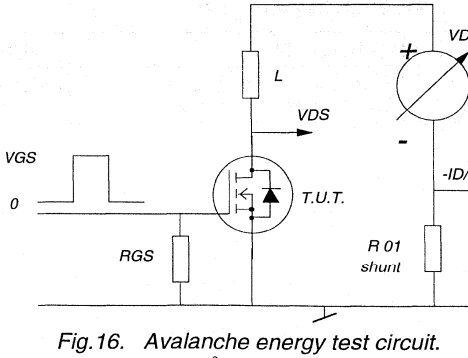


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in automotive and general purpose switching applications.

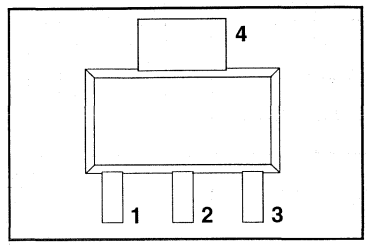
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	1.0	A
P_{tot}	Total power dissipation	1.5	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 10 V	0.80	Ω

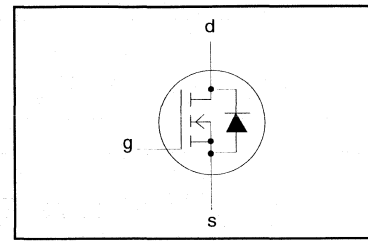
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{amb} = 25 °C	-	1	A
I_D	Drain current (DC)	T_{amb} = 100 °C	-	0.6	A
I_{DM}	Drain current (pulse peak value)	T_{amb} = 25 °C	-	4	A
P_{tot}	Total power dissipation	T_{amb} = 25 °C	-	1.5	W
T_{stg}	Storage temperature	-	- 55	150	°C
T_j	Junction Temperature	-	-	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}b}$	From junction to board[1]	Mounted on any PCB	-	50	-	K/W
$R_{th\ j\text{-}amb}$	From junction to ambient	Mounted on PCB of Fig.17	-	-	85	K/W

1 Temperature measured 1-3 mm from tab.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V;	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1 A	-	0.48	0.80	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1 A	0.8	1.1	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	140	240	pF
C_{oss}	Output capacitance		-	40	60	pF
C_{rss}	Feedback capacitance		-	16	25	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	5	10	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	35	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	10	20	ns
t_f	Turn-off fall time		-	10	20	ns

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	1	A
I_{DRM}	Pulsed reverse drain current	-	-	-	4	A
V_{SD}	Diode forward voltage	I_F = 1 A; V_{GS} = 0 V	-	0.85	1.1	V
t_{rr}	Reverse recovery time	I_F = 1 A; -dI_F/dt = 100 A/µs;	-	40	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	100	-	nC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 1 A; $V_{DD} \leq$ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{amb} = 25 °C	-	-	10	mJ

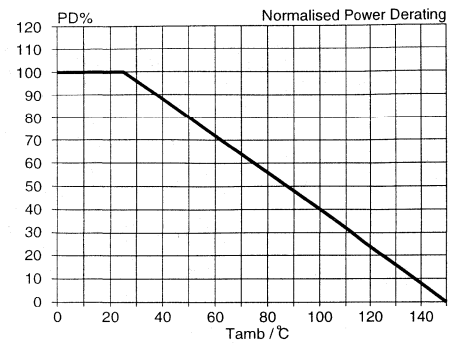


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{amb})

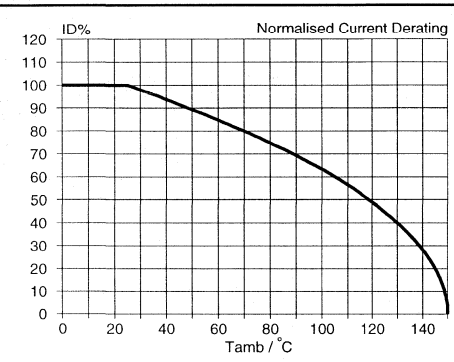


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{amb}); conditions: V_{GS} ≥ 10 V

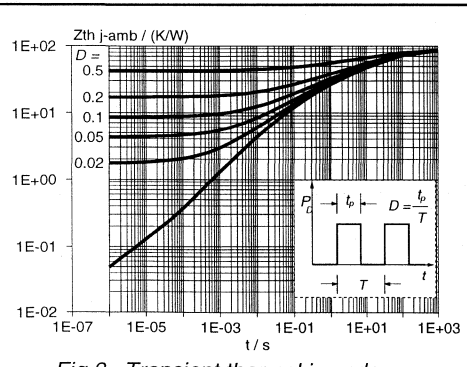


Fig.3. Transient thermal impedance.
$Z_{th\ j\text{-}amb}$ = f(t); parameter D = t_p/T

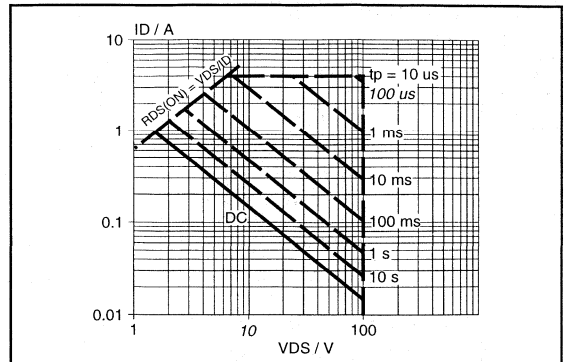


Fig.4. Safe operating area T_{amb} = 25 ˚C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

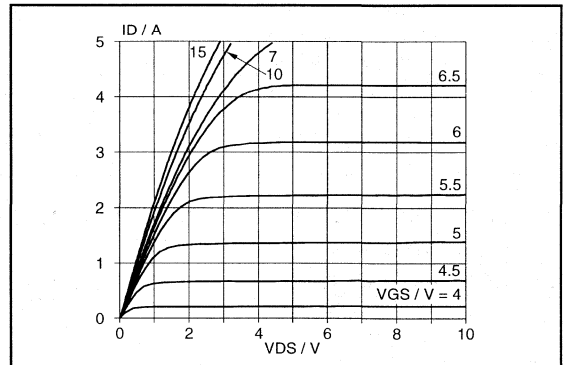


Fig.5. Typical output characteristics, T_j = 25 ˚C.
I_D = f(V_{DS}); parameter V_{GS}

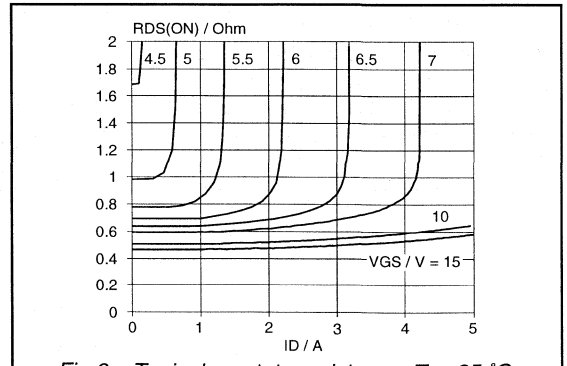


Fig.6. Typical on-state resistance, T_j = 25 ˚C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

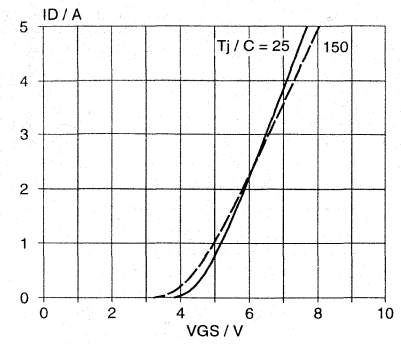


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

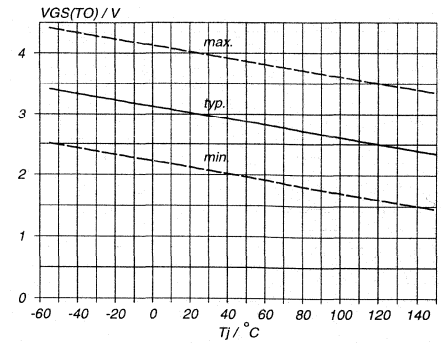


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.1 mA; $V_{DS} = V_{GS}$

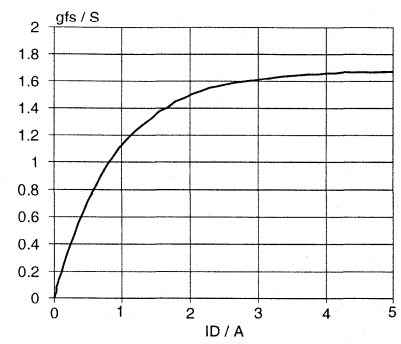


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

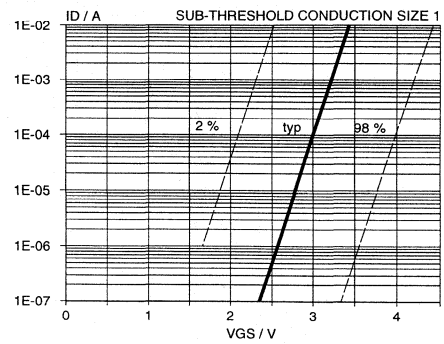


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

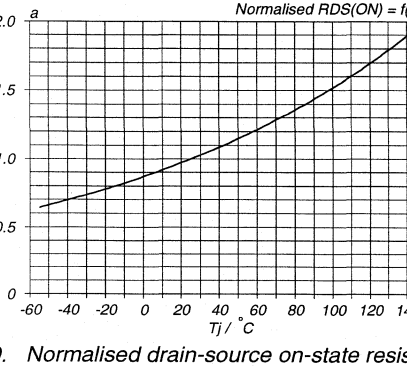


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ °C} = f(T_j)$; I_D = 1 A; V_{GS} = 10 V

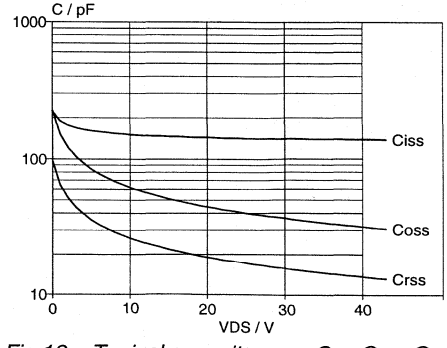


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

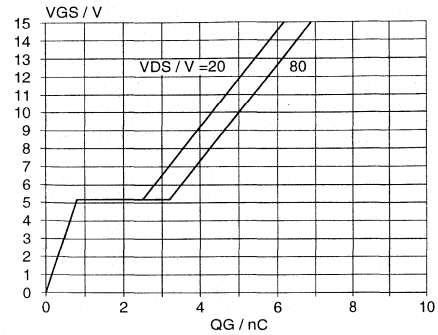


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 1 A; parameter V_{DS}

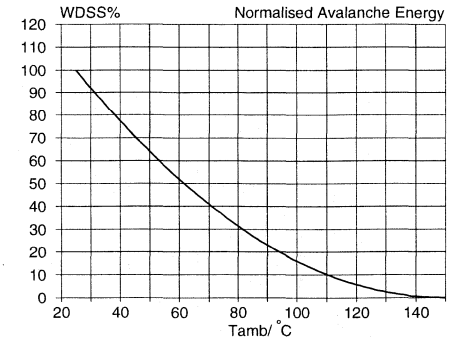


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{amb})$; conditions: I_D = 1 A

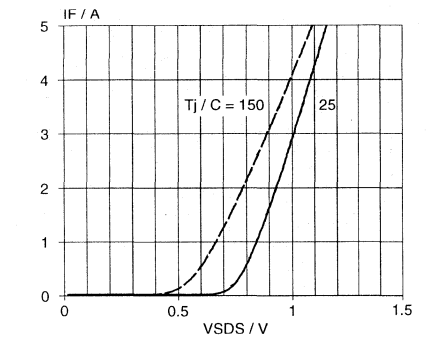


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

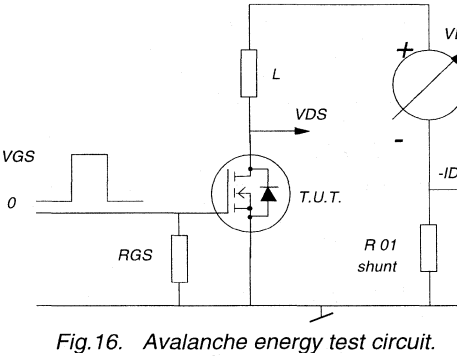


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PRINTED CIRCUIT BOARD

Dimensions in mm.

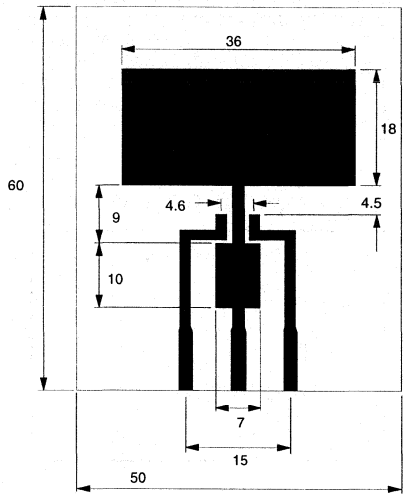


Fig.17. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in automotive and general purpose switching applications.

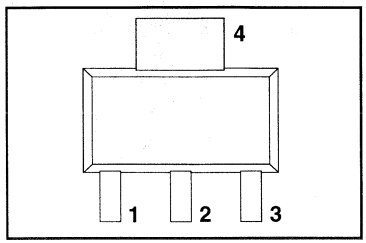
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	1.8	A
P_{tot}	Total power dissipation	1.8	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 10 V	0.28	Ω

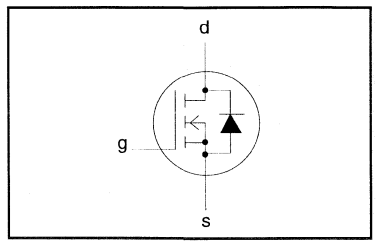
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{amb} = 25 °C	-	1.8	A
I_D	Drain current (DC)	T_{amb} = 100 °C	-	1.1	A
I_{DM}	Drain current (pulse peak value)	T_{amb} = 25 °C	-	7.2	A
P_{tot}	Total power dissipation	T_{amb} = 25 °C	-	1.8	W
T_{stg}	Storage temperature	-	- 55	150	°C
T_j	Junction Temperature	-	-	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}b}$	From junction to board[1]	Mounted on any PCB	-	40	-	K/W
$R_{th\ j\text{-}amb}$	From junction to ambient	Mounted on PCB of Fig.17	-	-	70	K/W

1 Temperature measured 1-3 mm from tab.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V;	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1.8 A	-	0.21	0.28	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1.8 A	1.5	2.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	300	500	pF
C_{oss}	Output capacitance		-	90	120	pF
C_{rss}	Feedback capacitance		-	35	50	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	9	14	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	30	45	ns
t_f	Turn-off fall time		-	20	40	ns

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	1.8	A
I_{DRM}	Pulsed reverse drain current	-	-	-	7.2	A
V_{SD}	Diode forward voltage	I_F = 1.8 A; V_{GS} = 0 V	-	0.85	1.1	V
t_{rr}	Reverse recovery time	I_F = 1.8 A; -dI_F/dt = 100 A/µs;	-	80	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.30	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 1.8 A; V_{DD} ≤ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{amb} = 25 °C	-	-	40	mJ

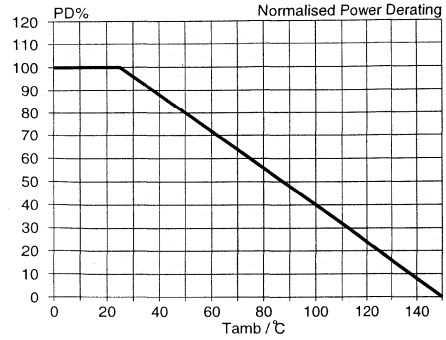


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ ˚C}$ = f(T_{amb})

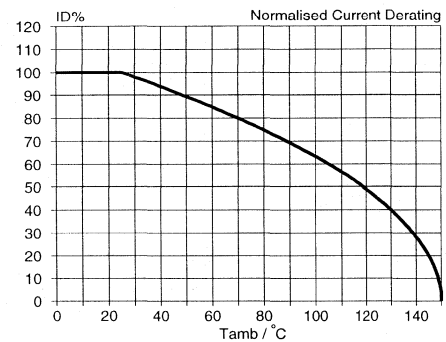


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ ˚C}$ = f(T_{amb}); conditions: $V_{GS} \geq$ 10 V

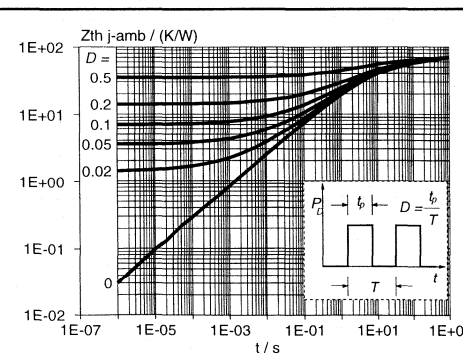


Fig.3. Transient thermal impedance.
$Z_{th\ j\text{-}amb}$ = f(t); parameter D = t_p/T

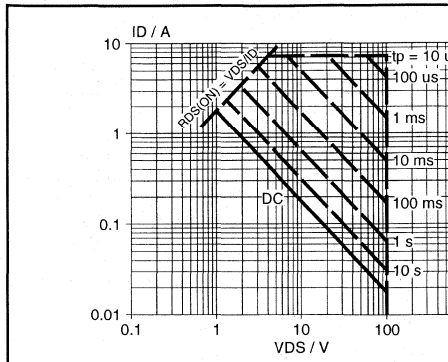


Fig.4. Safe operating area. T_{amb} = 25 ˚C.
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

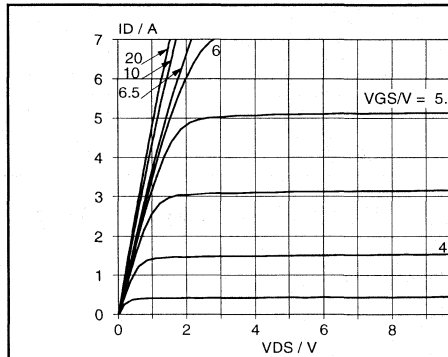


Fig.5. Typical output characteristics, T_j = 25 ˚C.
I_D = f(V_{DS}); parameter V_{GS}

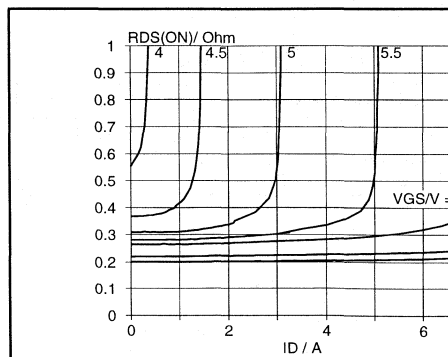


Fig.6. Typical on-state resistance, T_j = 25 ˚C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

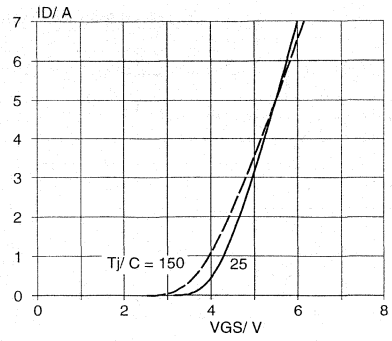


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

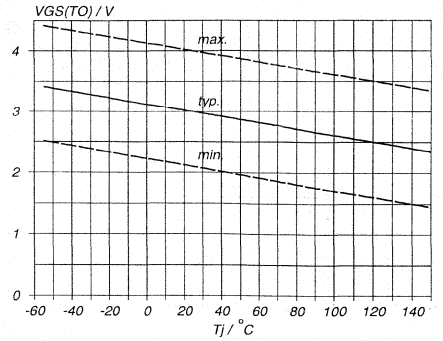


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

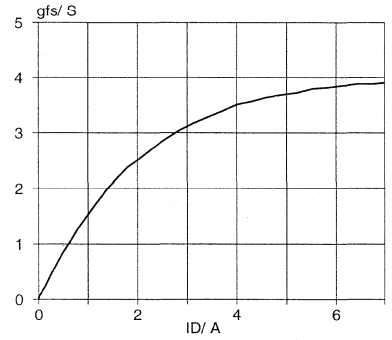


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

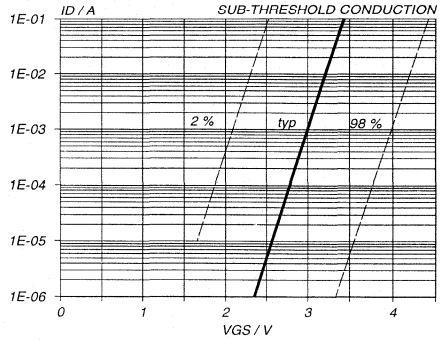


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

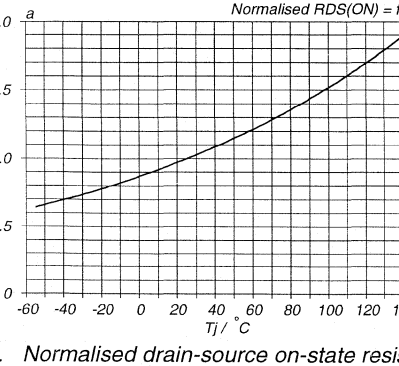


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 1.8 A; V_{GS} = 10 V

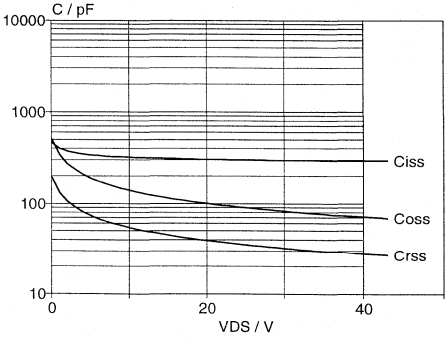


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

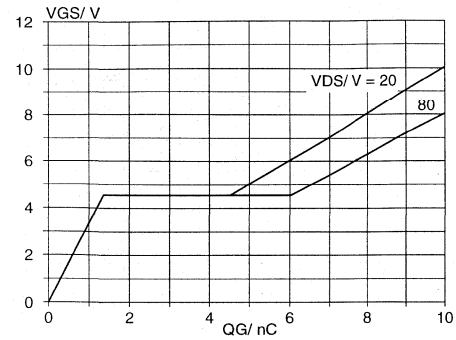


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 1.8$ A; parameter V_{DS}

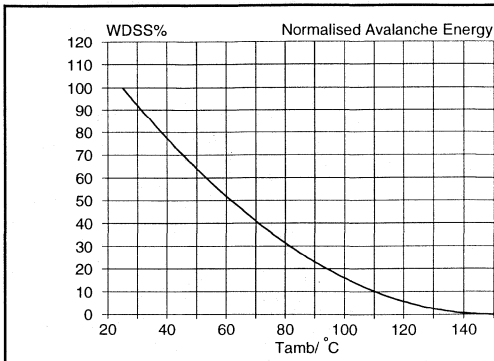


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{amb})$; conditions: $I_D = 1.8$ A

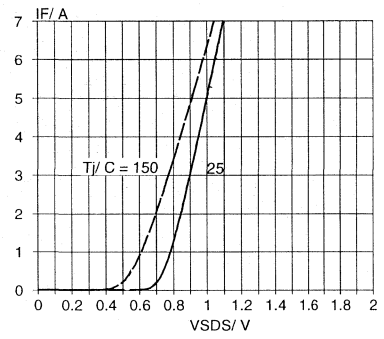


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

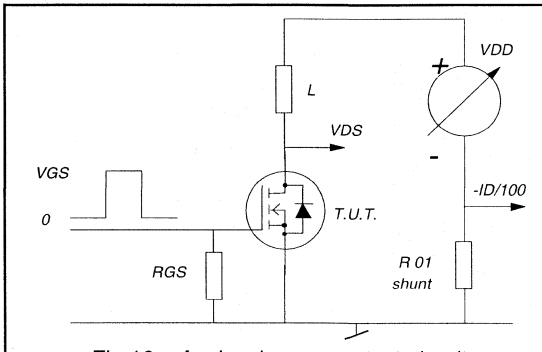


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PRINTED CIRCUIT BOARD

Dimensions in mm.

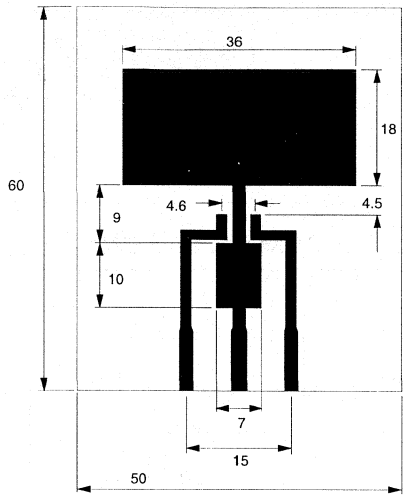


Fig.17. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mounting featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance. Intended for use in Switched Mode Power Supplies (SMPS) and general purpose switching applications.

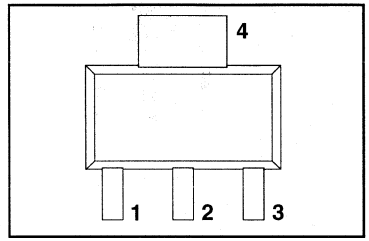
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (DC)	2.0	A
P_{tot}	Total power dissipation	8.3	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.9	Ω

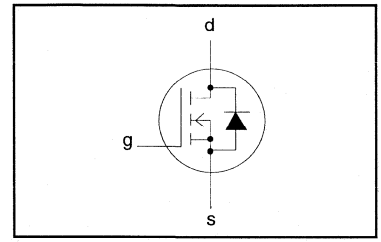
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	200	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
I_D	Drain current (DC)	T_{sp} = 25 °C	-	2.0	A
		T_{sp} = 100 °C	-	1.3	A
I_{DM}	Drain current (pulse peak value)	T_{sp} = 25 °C	-	8.0	A
I_{DR}	Source-drain diode current (DC)	T_{sp} = 25 °C	-	2.0	A
I_{DRM}	Source-drain diode current (pulse peak value)	T_{sp} = 25 °C	-	8.0	A
P_{tot}	Total power dissipation	T_{sp} = 25 °C	-	8.3	W
T_{stg}	Storage temperature		-55	150	°C
T_j	Junction Temperature		-	150	°C

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 2 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω			
		T_j = 25°C prior to surge	-	50	mJ
		T_j = 100°C prior to surge	-	8	mJ

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}sp}$	Thermal resistance junction to solder point		-	-	15	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	pcb mounted; minimum footprint	-	156	-	K/W
		pcb mounted; pad area as in fig:17	-	70	-	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	0.1	10	µA
		V_{DS} = 200 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 2 A	-	0.53	0.9	Ω
V_{SD}	Source-drain diode forward voltage	I_F = 2 A ;V_{GS} = 0 V	-	0.87	1.0	V

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 2 A	0.5	2.6	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	305	400	pF
C_{oss}	Output capacitance		-	60	100	pF
C_{rss}	Feedback capacitance		-	24	50	pF
$Q_{g(tot)}$	Total gate charge	V_{GS} = 10 V; I_D = 2 A; V_{DS} = 160 V	-	13	-	nC
Q_{gs}	Gate to source charge		-	2	-	nC
Q_{gd}	Gate to drain (Miller) charge		-	5	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.75 A;	-	10	15	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	30	45	ns
$t_{d\ off}$	Turn-off delay time	R_{GEN} = 50 Ω	-	30	40	ns
t_f	Turn-off fall time		-	20	30	ns
t_{rr}	Source-drain diode reverse recovery time	I_F = 2 A; -dI_F/dt = 100 A/µs;	-	88	-	ns
Q_{rr}	Source-drain diode reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	370	-	nC

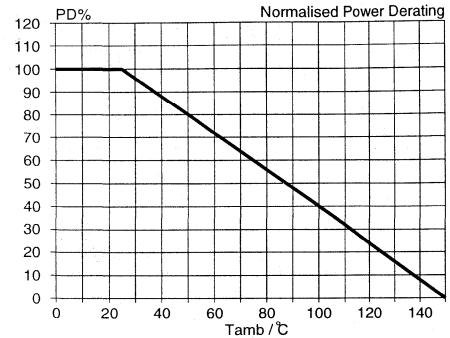


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ ^\circ C}$ = f(T_{amb})

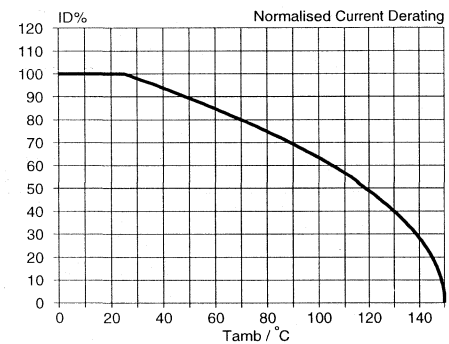


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ ^\circ C}$ = f(T_{amb}); conditions: $V_{GS} \geq 10$ V

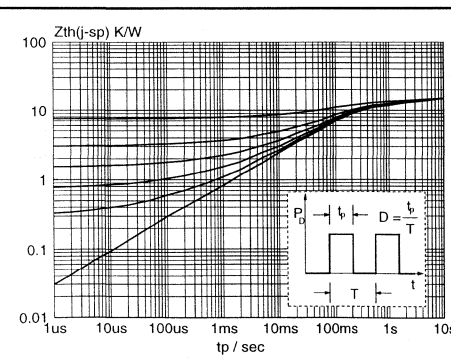


Fig.3. Transient thermal impedance.
$Z_{th\ j\text{-}sp}$ = f(t); parameter D = t_p/T

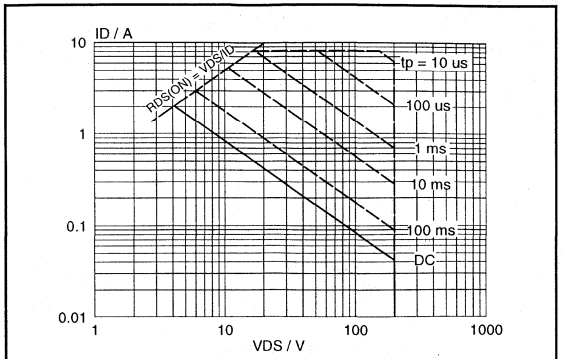


Fig.4. Safe operating area. T_{amb} = 25 ˚C.
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

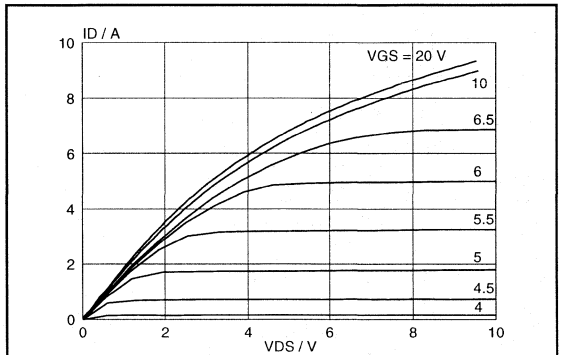


Fig.5. Typical output characteristics, T_j = 25 ˚C.
I_D = f(V_{DS}); parameter V_{GS}

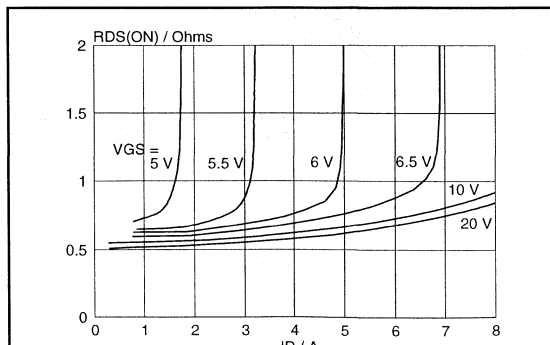


Fig.6. Typical on-state resistance, T_j = 25 ˚C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

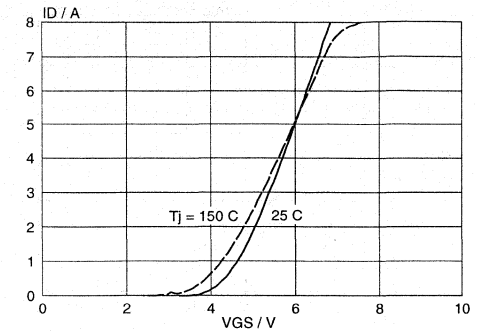


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

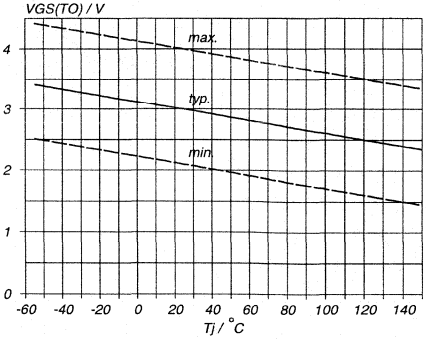


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

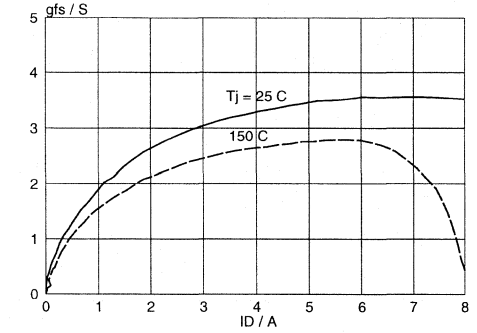


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

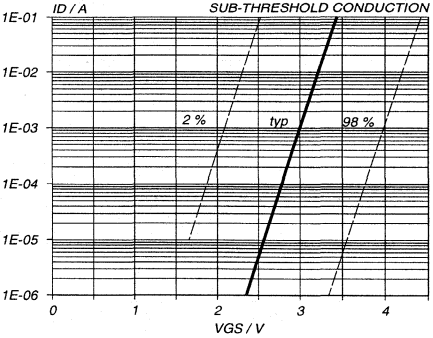


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

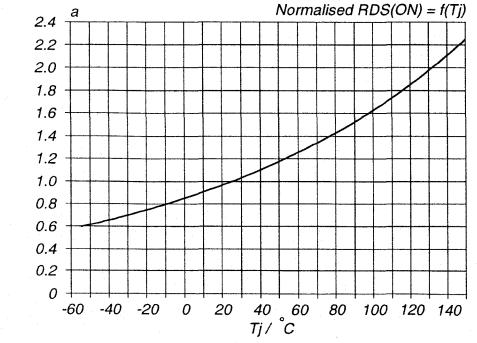


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 2 A; V_{GS} = 10 V

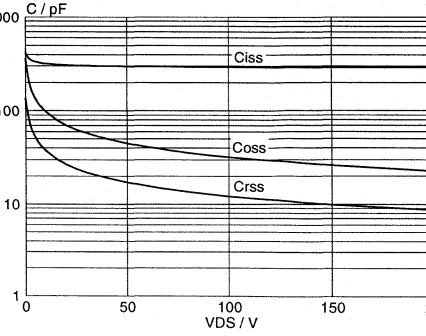


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

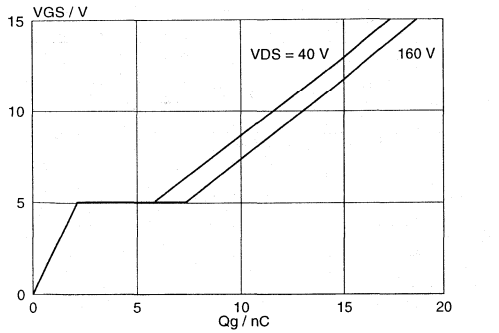


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 2$ A; parameter V_{DS}

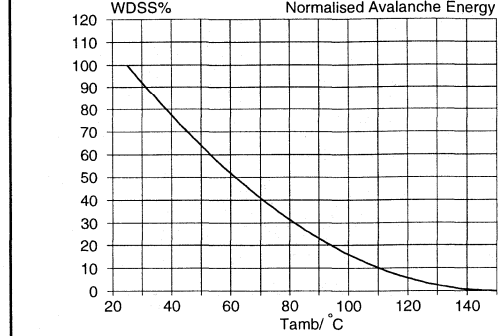


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{amb})$; conditions: $I_D = 2$ A

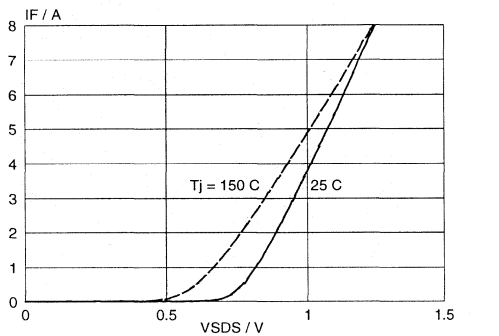


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

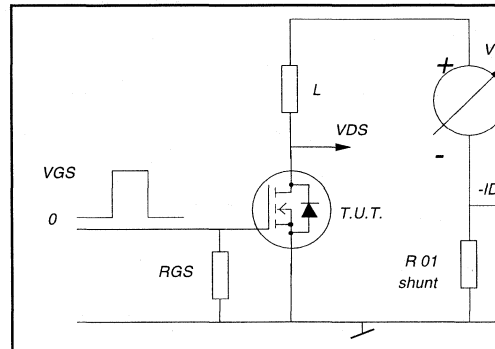


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PRINTED CIRCUIT BOARD

Dimensions in mm.

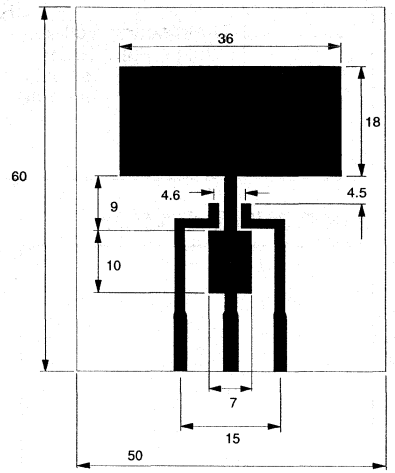


Fig.17. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).

PowerMOS transistor Logic level FET

BUK543-100A/B

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic full-pack envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

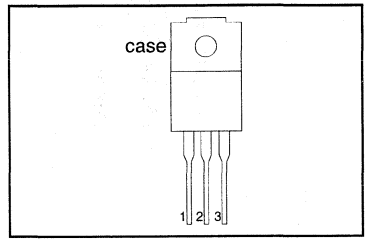
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK543	-100A	-100B	
V_{DS}	Drain-source voltage	100	100	V
I_D	Drain current (DC)	8.3	7.5	A
P_{tot}	Total power dissipation	25	25	W
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.18	0.22	Ω

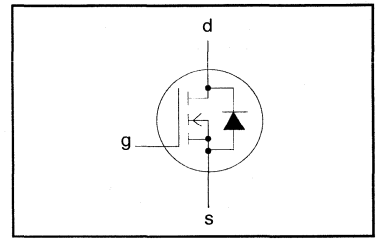
PINNING - SOT186

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	100		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100		V
$\pm V_{GS}$	Gate-source voltage	-	-	15		V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20		V
				-100A	-100B	
I_D	Drain current (DC)	T_{hs} = 25 °C	-	8.3	7.5	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	5.2	4.7	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	33	30	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	25		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction Temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	5.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 5 A **BUK543-100A**	-	0.17	0.18	Ω
		BUK543-100B	-	0.20	0.22	Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5 A	6.0	8.0	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	620	825	pF
C_{oss}	Output capacitance		-	180	250	pF
C_{rss}	Feedback capacitance		-	90	120	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	10	20	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	45	60	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	90	115	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	8.3	A
I_{DRM}	Pulsed reverse drain current	-	-	-	33	A
V_{SD}	Diode forward voltage	I_F = 8.3 A ; V_{GS} = 0 V	-	1.1	1.3	V
t_{rr}	Reverse recovery time	I_F = 8.3 A; -dI_F/dt = 100 A/µs;	-	80	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.5	-	µC

AVALANCHE LIMITING VALUE

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 13 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	70	mJ

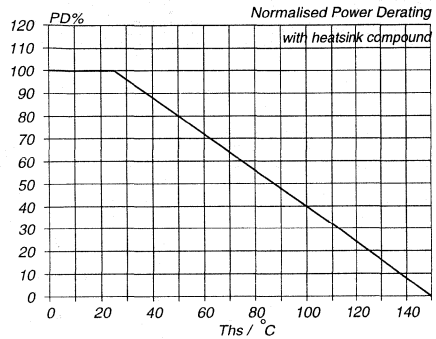


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{hs})

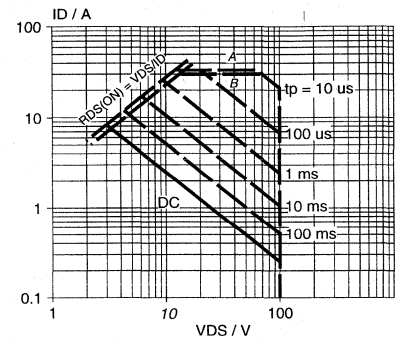


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

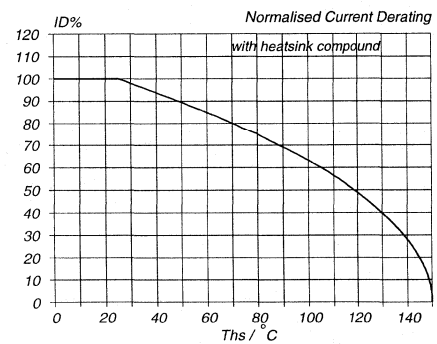


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{hs}); conditions: $V_{GS} \geq$ 5 V

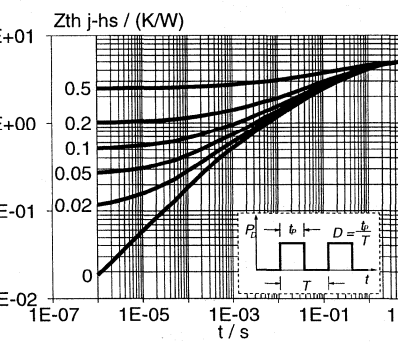


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}hs}$ = f(t); parameter D = t_p/T

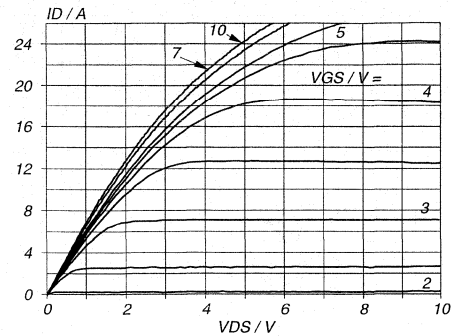


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

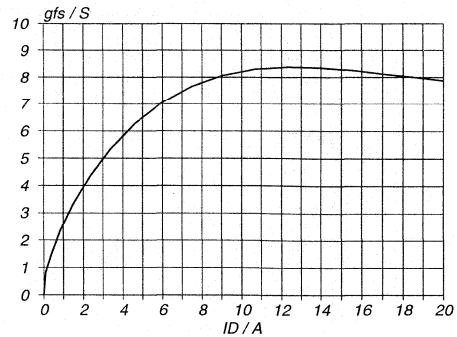


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

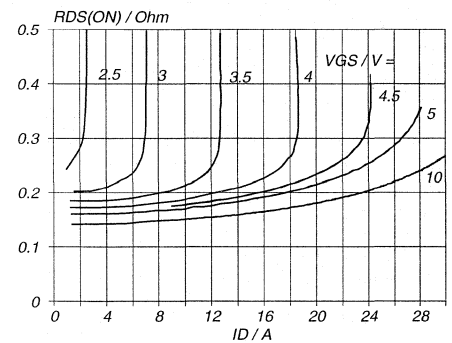


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

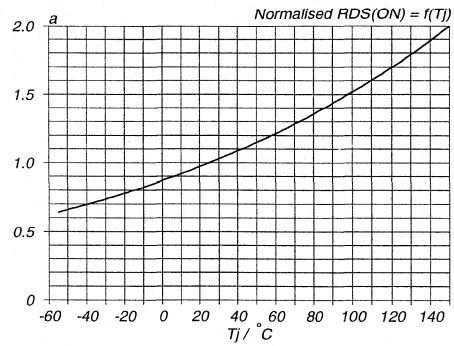


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\ ˚C} = f(T_j)$; I_D = 5 A; V_{GS} = 5 V

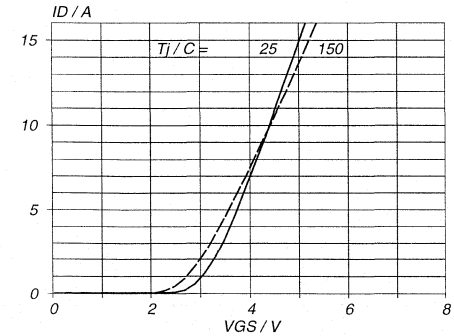


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

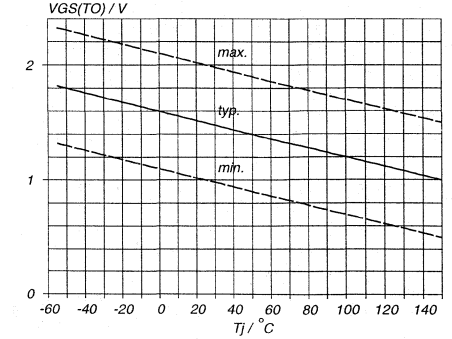


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

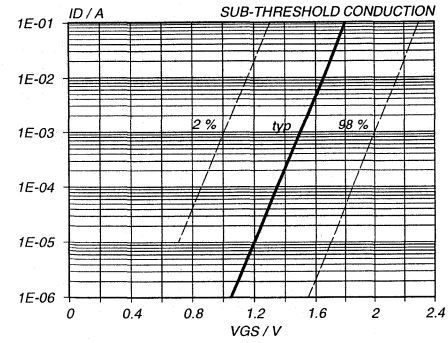


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

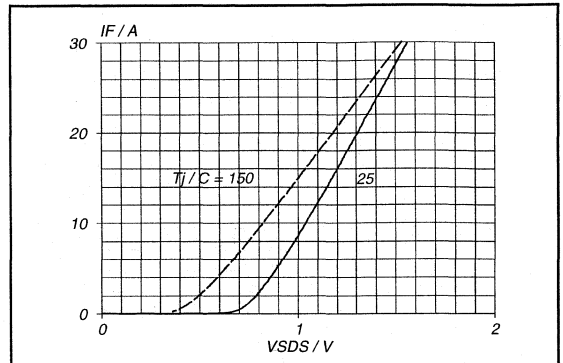


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

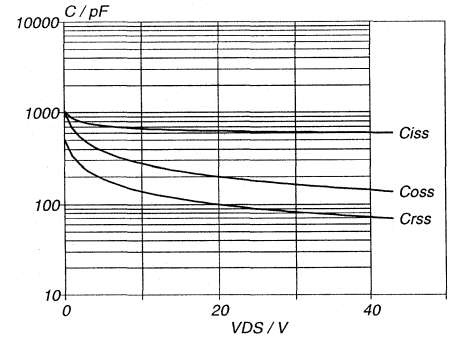


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

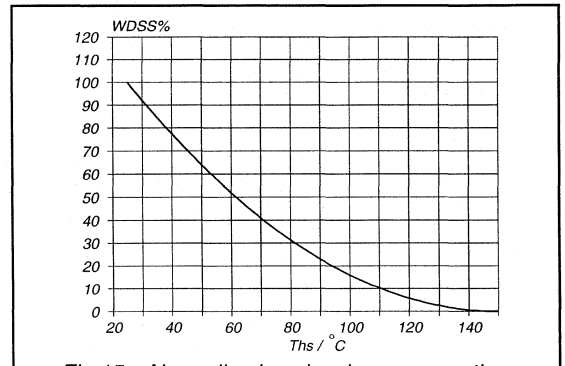


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{hs})$; conditions: I_D = 13 A

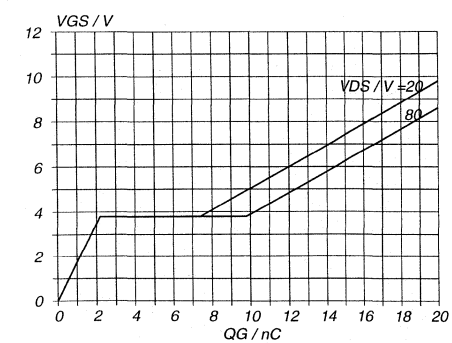


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 13 A; parameter V_{DS}

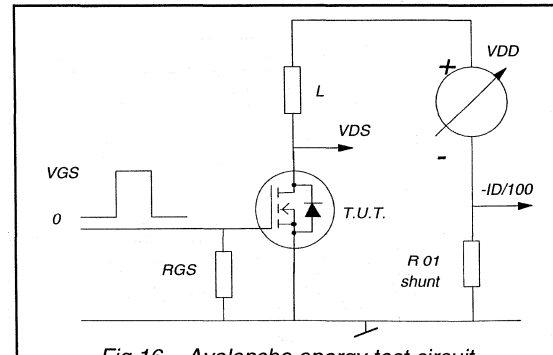


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor Logic level FET

BUK545-100A/B

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic full-pack envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

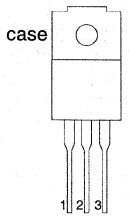
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK545	-100A	-100B	
V_{DS}	Drain-source voltage	100	100	V
I_D	Drain current (DC)	13	12	A
P_{tot}	Total power dissipation	30	30	W
T_j	Junction temperature	150	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance; $V_{GS} = 5$ V	0.085	0.11	Ω

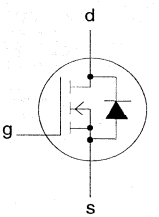
PINNING - SOT186

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	100		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100		V
$\pm V_{GS}$	Gate-source voltage	-	-	15		V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ μs	-	20		V
				-100A	-100B	
I_D	Drain current (DC)	T_{hs} = 25 °C	-	13	12	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	8.2	7.5	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	52	48	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	30		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction Temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	4.17	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; **BUK545-100A** I_D = 13 A **BUK545-100B**	- -	0.075 0.09	0.085 0.11	Ω Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 13 A	10	13.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1450	1750	pF
C_{oss}	Output capacitance		-	280	350	pF
C_{rss}	Feedback capacitance		-	100	150	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	25	40	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	65	85	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	135	180	ns
t_f	Turn-off fall time		-	80	110	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	13	A
I_{DRM}	Pulsed reverse drain current	-	-	-	52	A
V_{SD}	Diode forward voltage	I_F = 13 A ; V_{GS} = 0 V	-	1.3	1.7	V
t_{rr}	Reverse recovery time	I_F = 13 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.70	-	µC

AVALANCHE LIMITING VALUE

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 25 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	140	mJ

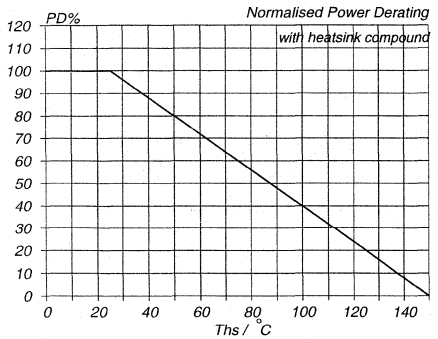


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{hs})

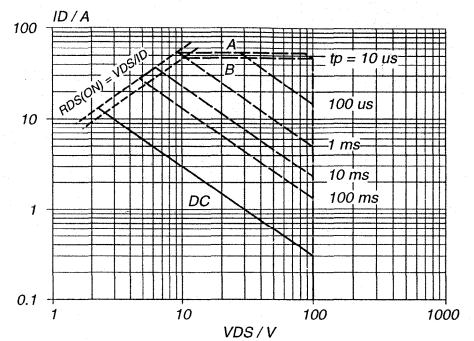


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

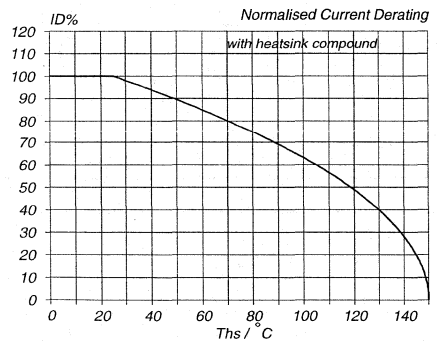


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{hs}); conditions: $V_{GS} \geq$ 5 V

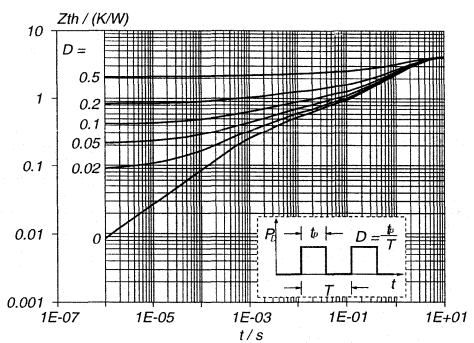


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}hs}$ = f(t); parameter D = t_p/T

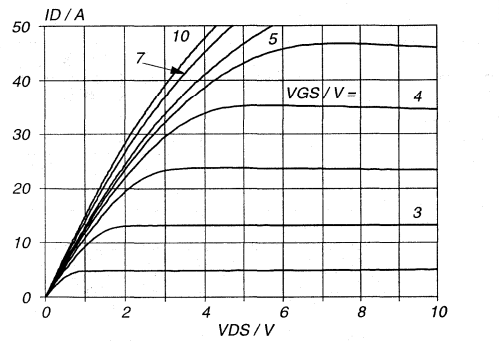


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

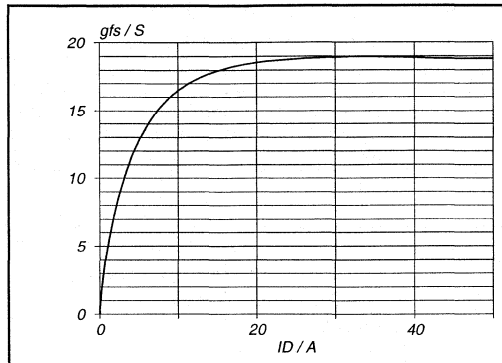


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

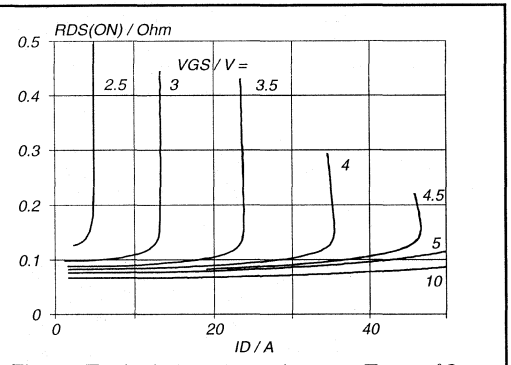


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

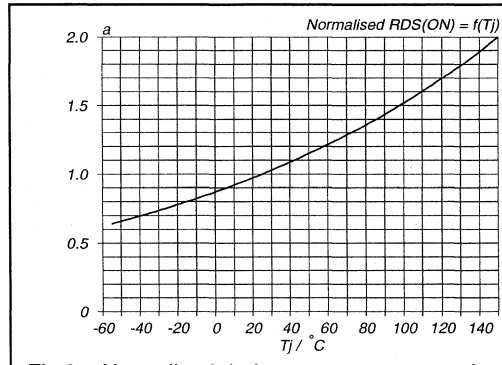


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\ ˚C} = f(T_j)$; I_D = 13 A; V_{GS} = 5 V

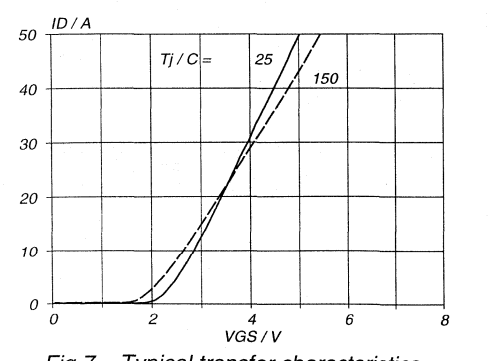


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

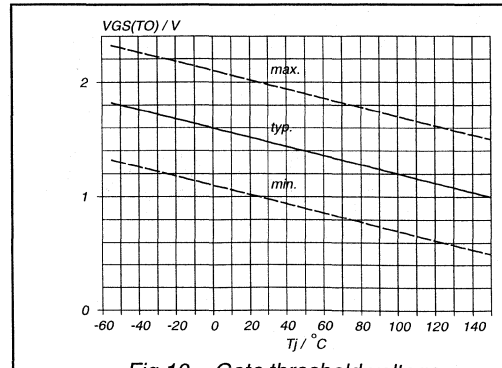


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

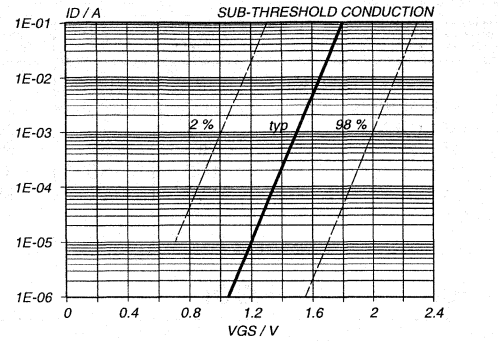


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

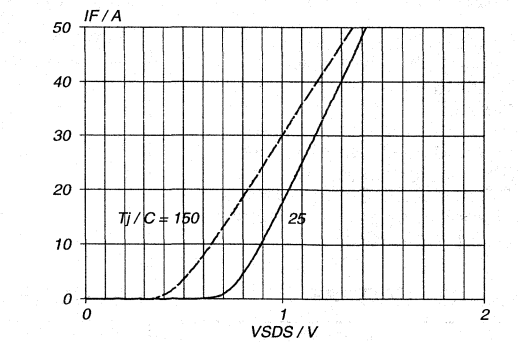


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

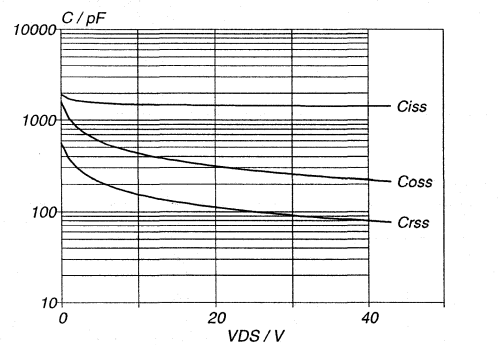


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
C = f(V_{DS}); conditions: V_{GS} = 0 V; f = 1 MHz

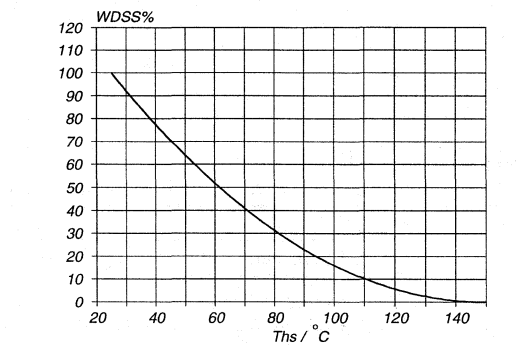


Fig.15. Normalised avalanche energy rating.
W_{DSS}% = f(T_{hs}); conditions: I_D = 25 A

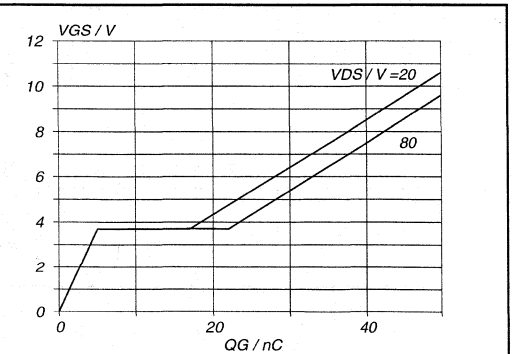


Fig.13. Typical turn-on gate-charge characteristics.
V_{GS} = f(Q_G); conditions: I_D = 25 A; parameter V_{DS}

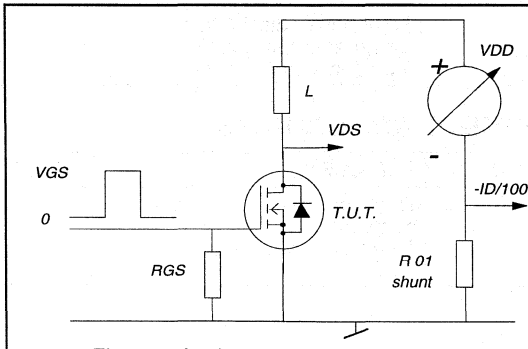


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PowerMOS transistor Logic level FET

BUK545-200A/B

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic full-pack envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

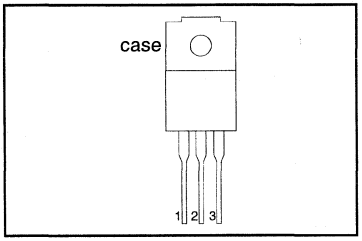
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK545	-200A	-200B	
V_{DS}	Drain-source voltage	200	200	V
I_D	Drain current (DC)	7.6	7	A
P_{tot}	Total power dissipation	30	30	W
T_j	Junction temperature	150	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.23	0.28	Ω

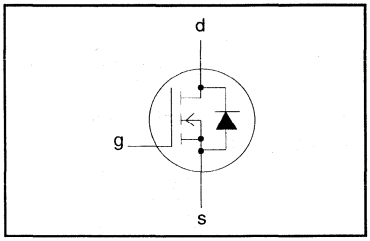
PINNING - SOT186

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	200		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200		V
$\pm V_{GS}$	Gate-source voltage	-	-	15		V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20		V
				-200A	-200B	
I_D	Drain current (DC)	T_{hs} = 25 °C	-	7.6	7	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	4.8	4.4	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	30	28	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	30		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction Temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	4.17	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; **BUK545-200A**	-	0.2	0.23	Ω
		I_D = 7 A **BUK545-200B**	-	0.24	0.28	Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 7 A	8.0	15	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1600	2000	pF
C_{oss}	Output capacitance		-	180	250	pF
C_{rss}	Feedback capacitance		-	55	80	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	25	40	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	45	75	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	140	180	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	7.6	A
I_{DRM}	Pulsed reverse drain current	-	-	-	30	A
V_{SD}	Diode forward voltage	I_F = 7.6 A ; V_{GS} = 0 V	-	1.0	1.5	V
t_{rr}	Reverse recovery time	I_F = 7.6 A; -dI_F/dt = 100 A/µs;	-	150	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	1.3	-	µC

AVALANCHE LIMITING VALUE

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 14 A ; $V_{DD} \leq$ 100 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	100	mJ

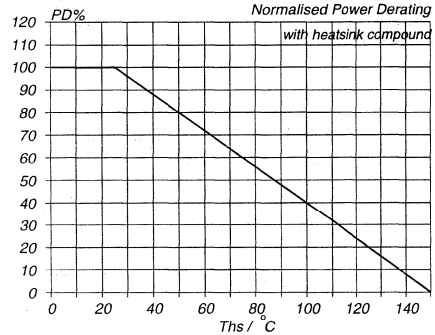


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{hs})

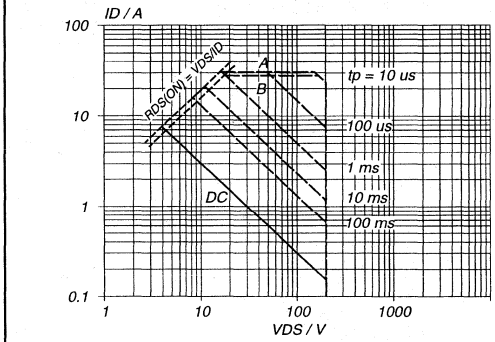


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

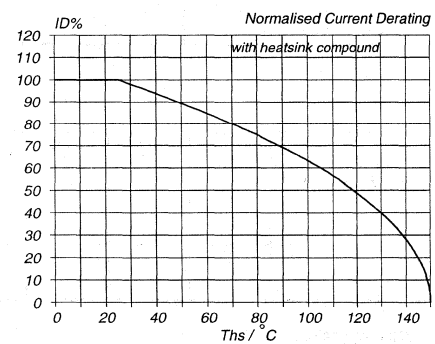


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{hs}); conditions: $V_{GS} \geq$ 5 V

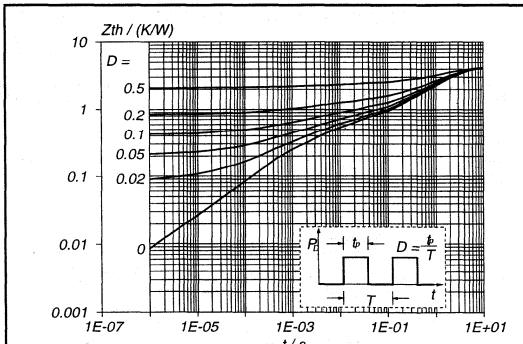


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}hs}$ = f(t); parameter D = t_p/T

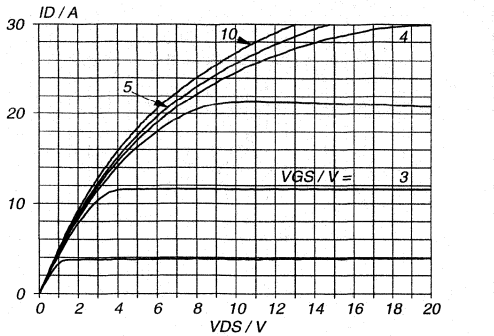


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

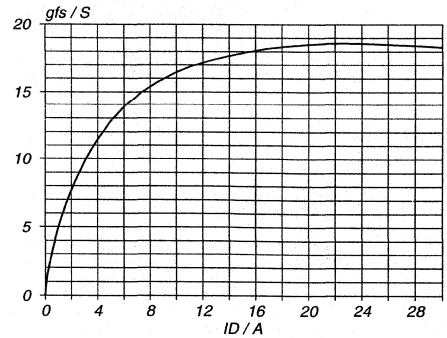


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

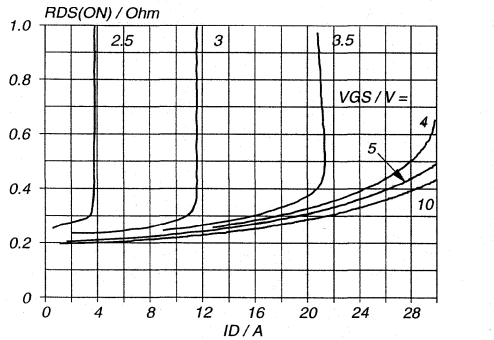


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

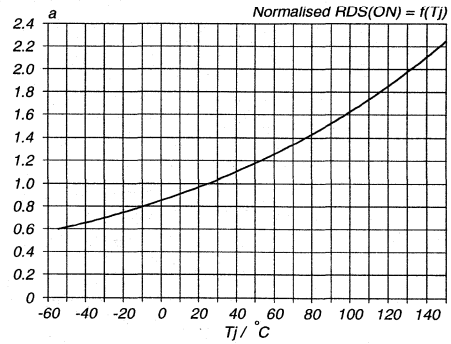


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\ ˚C} = f(T_j)$; I_D = 7 A; V_{GS} = 5 V

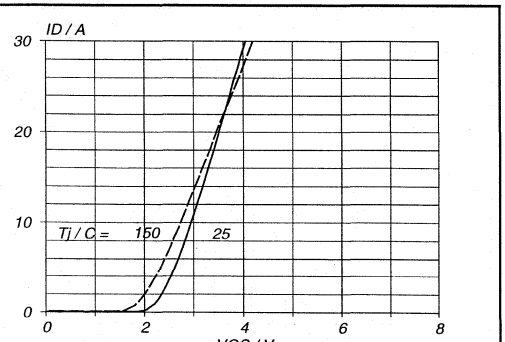


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

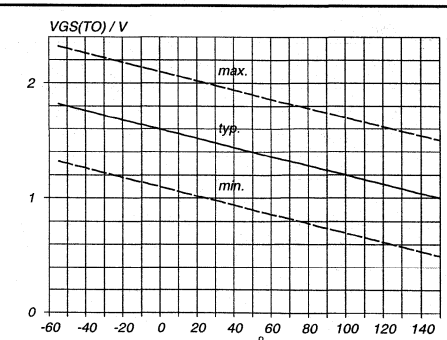


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

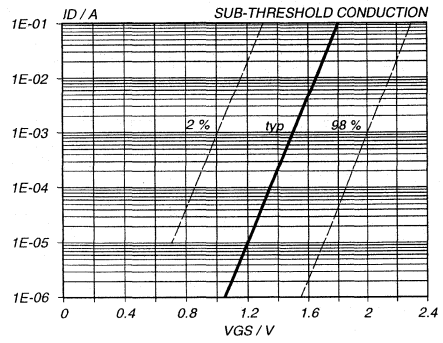


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

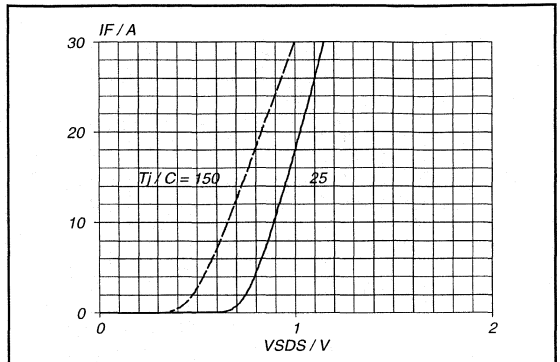


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

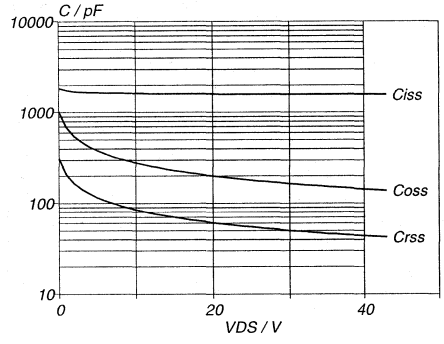


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

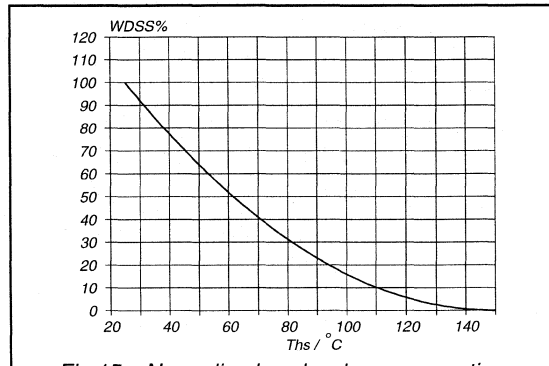


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{hs})$; conditions: $I_D = 14$ A

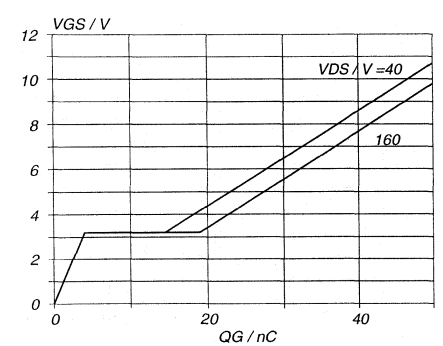


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 14$ A; parameter V_{DS}

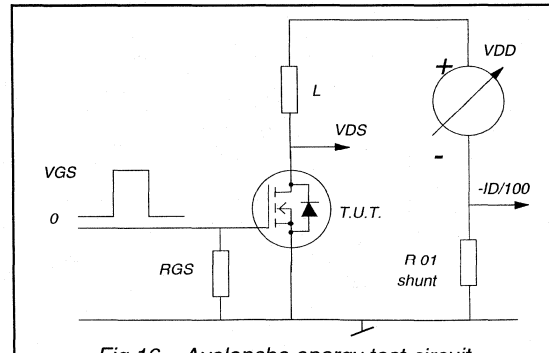


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PowerMOS transistor Logic level FET

BUK552-60A/B

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

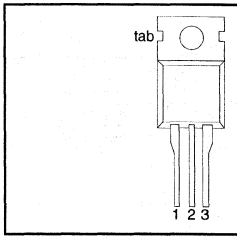
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK552	-60A	-60B	
V_{DS}	Drain-source voltage	60	60	V
I_D	Drain current (DC)	14	13	A
P_{tot}	Total power dissipation	60	60	W
T_j	Junction temperature	175	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.15	0.18	Ω

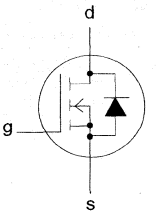
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	60		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60		V
$\pm V_{GS}$	Gate-source voltage	-	-	15		V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20		V
				-60A	-60B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	14	13	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	10	9	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	56	52	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	60		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction Temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; **BUK552-60A**	-	0.12	0.15	Ω
		I_D = 8.5 A **BUK552-60B**	-	0.15	0.18	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 8.5 A	5	6.7	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	400	600	pF
C_{oss}	Output capacitance		-	150	200	pF
C_{rss}	Feedback capacitance		-	65	100	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	12	18	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	60	80	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	50	70	ns
t_f	Turn-off fall time		-	45	70	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	14	A
I_{DRM}	Pulsed reverse drain current	-	-	-	56	A
V_{SD}	Diode forward voltage	I_F = 14 A ; V_{GS} = 0 V	-	1.3	1.7	V
t_{rr}	Reverse recovery time	I_F = 14 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.18	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 14 A ; V_{DD} ≤ 25 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	30	mJ

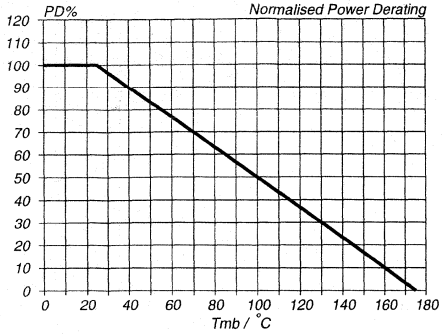


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

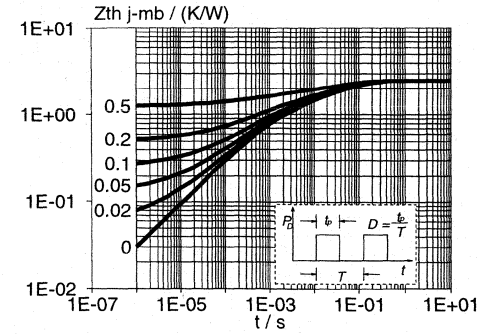


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

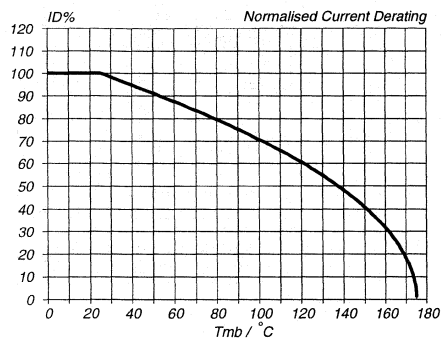


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: V_{GS} ≥ 5 V

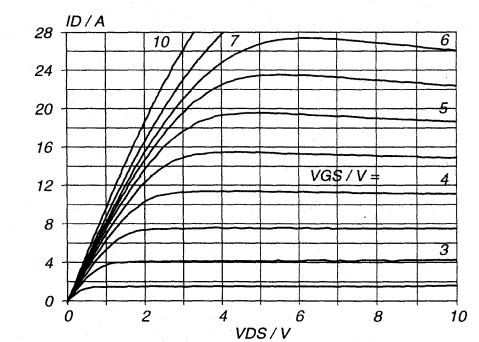


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

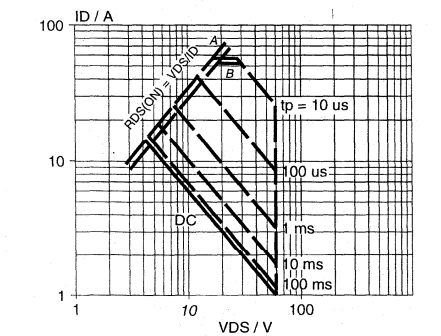


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

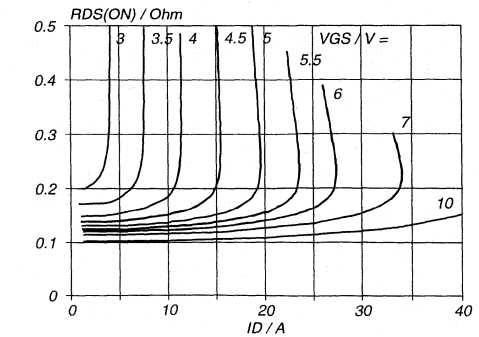


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

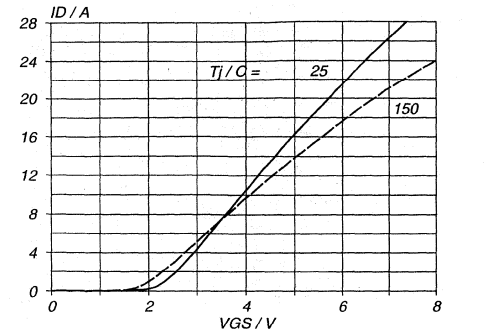


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

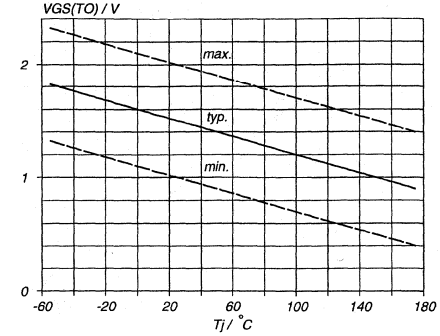


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

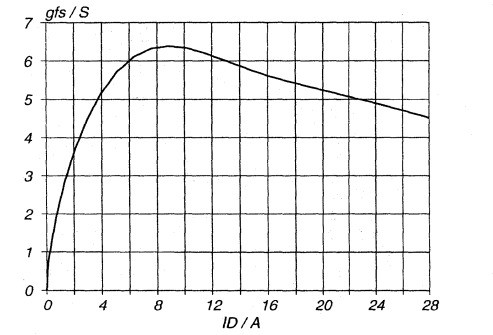


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

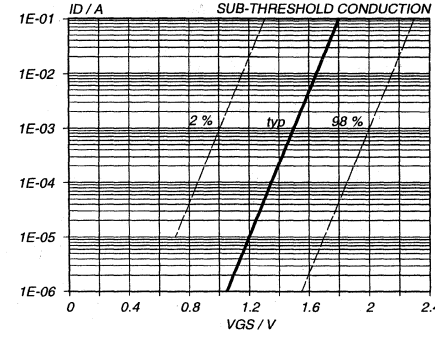


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

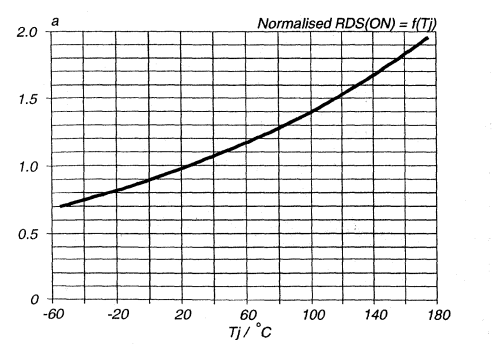


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 8.5 A; V_{GS} = 5 V

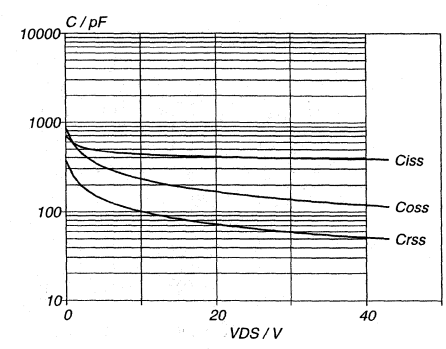


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

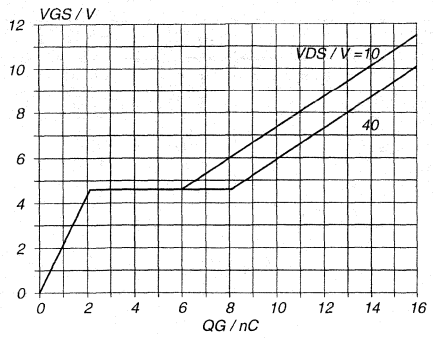


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: I_D = 14 A; parameter V_{DS}

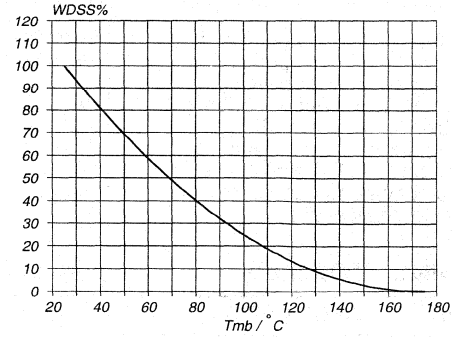


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: I_D = 14 A

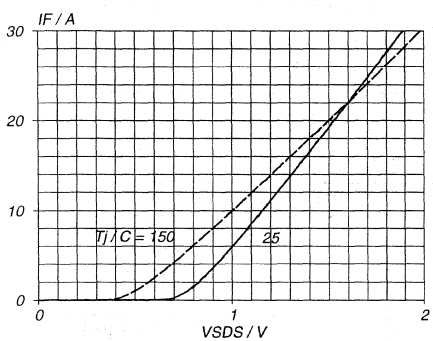


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

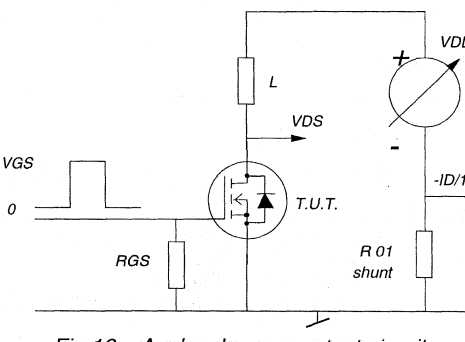


Fig.16. Avalanche energy test circuit.
$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PowerMOS transistor Logic level FET

BUK552-100A/B

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

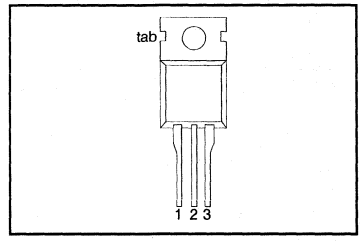
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK552	-100A	-100B	
V_{DS}	Drain-source voltage	100	100	V
I_D	Drain current (DC)	10	8.5	A
P_{tot}	Total power dissipation	60	60	W
T_j	Junction temperature	175	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.28	0.35	Ω

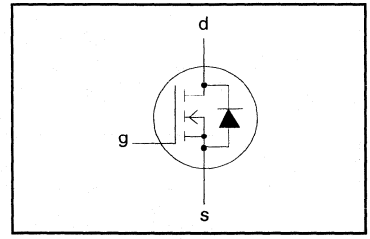
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	100		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100		V
$\pm V_{GS}$	Gate-source voltage	-	-	15		V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20		V
				-100A	-100B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	10	8.5	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	7	6	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	40	34	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	60		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction Temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; **BUK552-100A**	-	0.25	0.28	Ω
		I_D = 5.5 A **BUK552-100B**	-	0.3	0.35	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5.5 A	4.5	6	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	400	600	pF
C_{oss}	Output capacitance		-	90	120	pF
C_{rss}	Feedback capacitance		-	35	50	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	12	18	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	45	70	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	50	70	ns
t_f	Turn-off fall time		-	30	45	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	10	A
I_{DRM}	Pulsed reverse drain current	-	-	-	40	A
V_{SD}	Diode forward voltage	I_F = 10 A ; V_{GS} = 0 V	-	1.2	1.5	V
t_{rr}	Reverse recovery time	I_F = 10 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.35	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 10 A ; V_{DD} ≤ 50 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	30	mJ

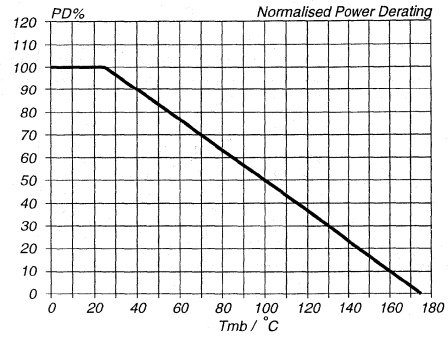


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

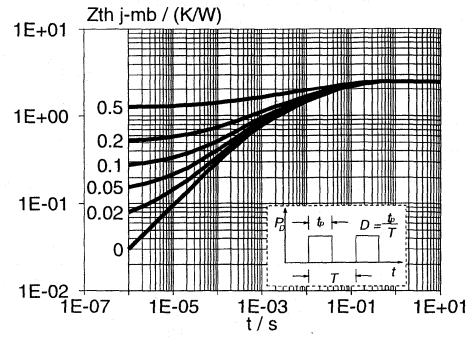


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

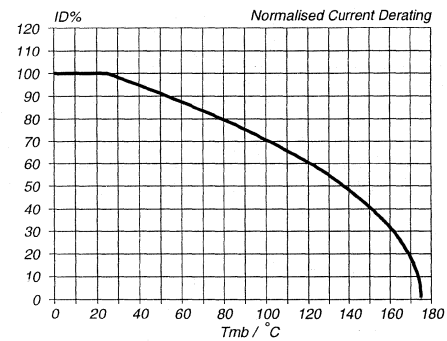


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 5 V

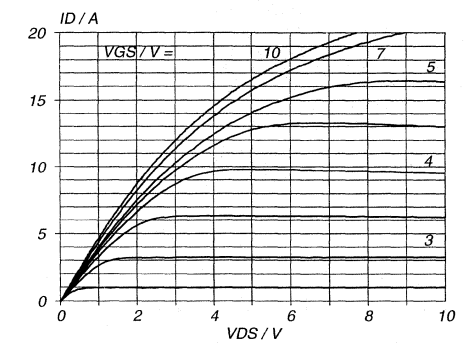


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

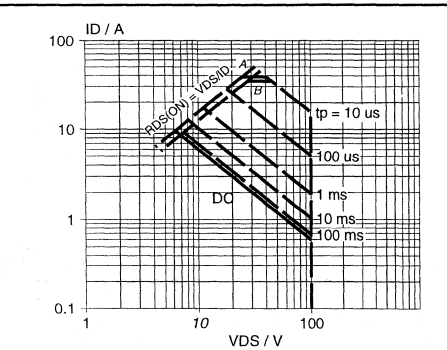


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

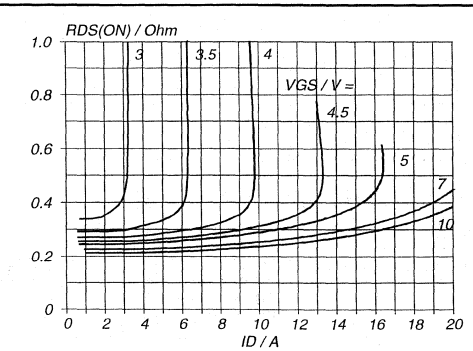


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

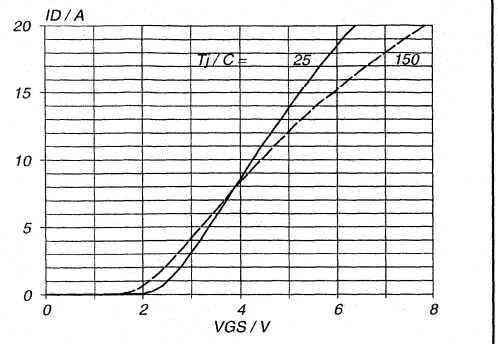


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

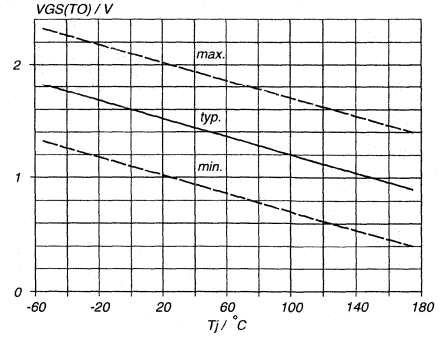


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

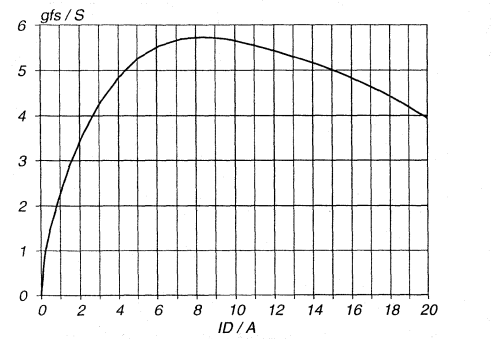


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

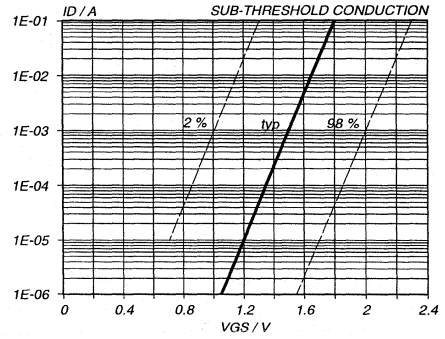


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

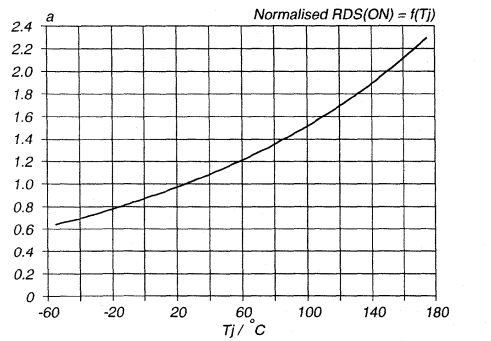


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 5.5 A; V_{GS} = 5 V

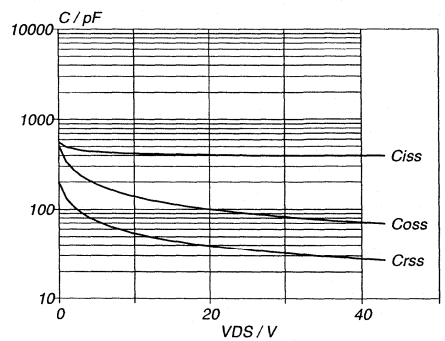


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

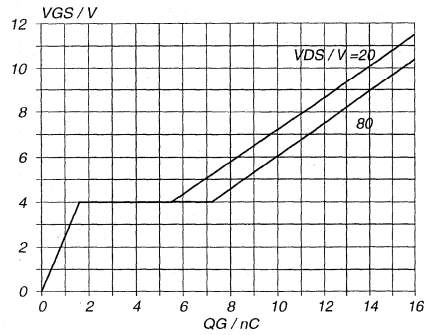


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 10 A; parameter V_{DS}

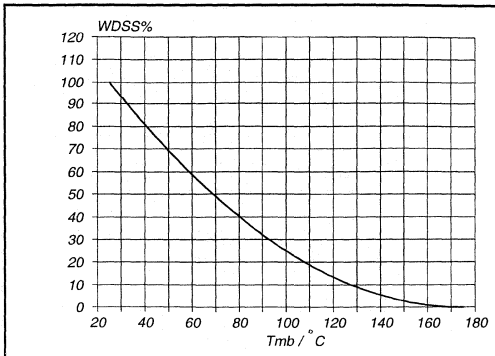


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: I_D = 10 A

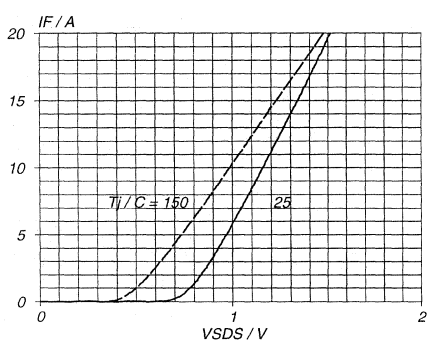


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

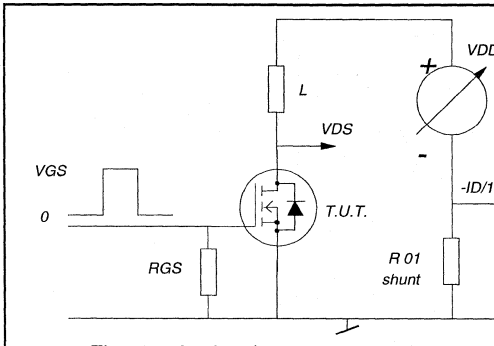


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor Logic level FET

BUK553-100A/B

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

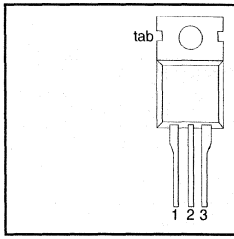
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK553	-100A	-100B	
V_{DS}	Drain-source voltage	100	100	V
I_D	Drain current (DC)	13	12	A
P_{tot}	Total power dissipation	75	75	W
T_j	Junction temperature	175	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.18	0.22	Ω

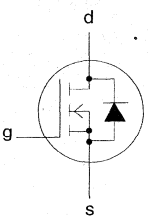
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	100		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100		V
$\pm V_{GS}$	Gate-source voltage	-	-	15		V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20		V
				-100A	-100B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	13	12	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	9	8.5	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	52	48	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	75		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction Temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; **BUK553-100A** I_D = 6.5 A **BUK553-100B**	- -	0.17 0.20	0.18 0.22	Ω Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 6.5 A	6.0	8.0	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	620	825	pF
C_{oss}	Output capacitance		-	180	250	pF
C_{rss}	Feedback capacitance		-	90	120	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	10	20	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	45	60	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	90	115	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	13	A
I_{DRM}	Pulsed reverse drain current	-	-	-	52	A
V_{SD}	Diode forward voltage	I_F = 13 A ; V_{GS} = 0 V	-	1.2	1.5	V
t_{rr}	Reverse recovery time	I_F = 13 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.6	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 13 A ; V_{DD} ≤ 50 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	70	mJ

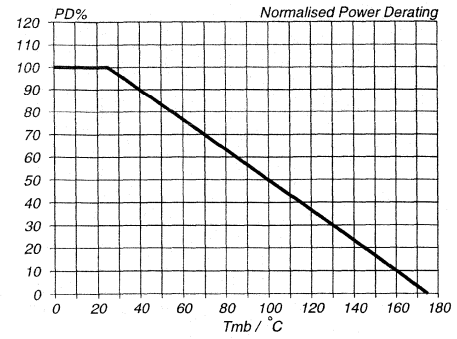


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

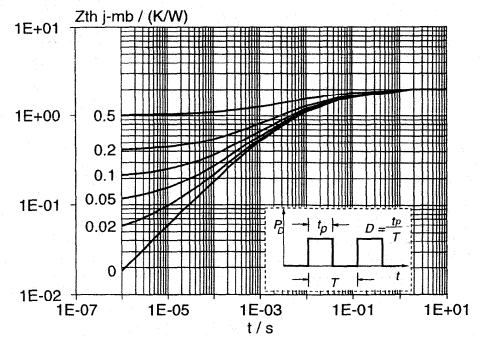


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

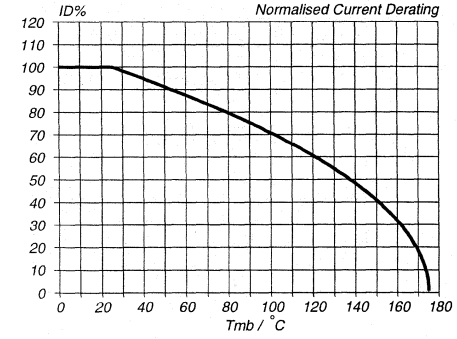


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 5 V

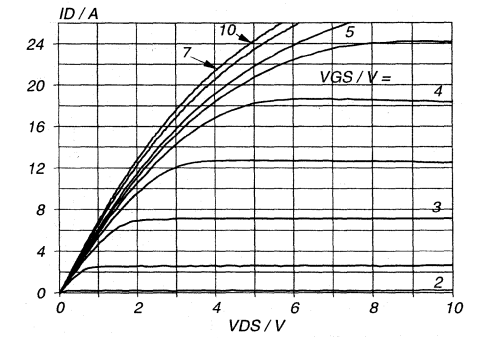


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

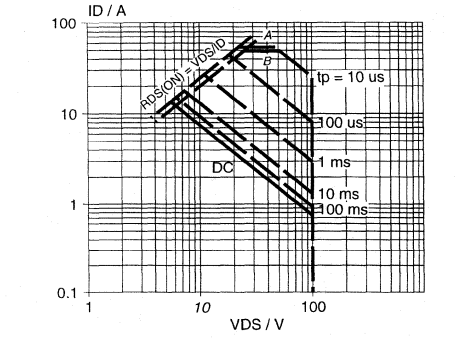


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

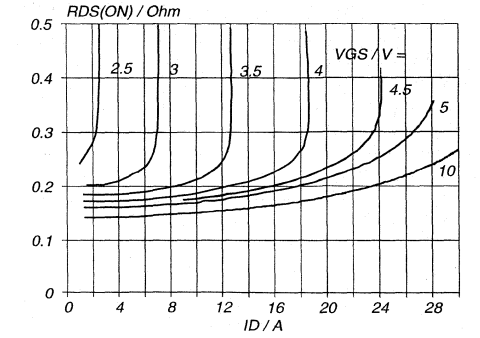


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

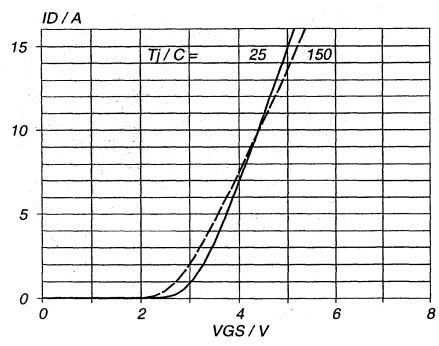


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

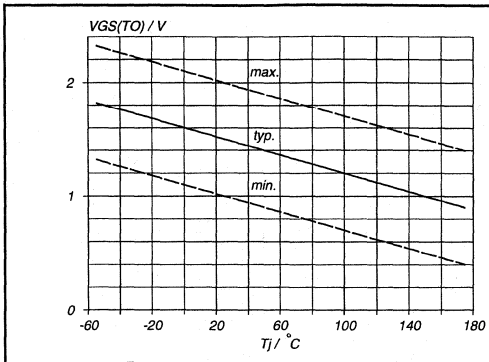


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

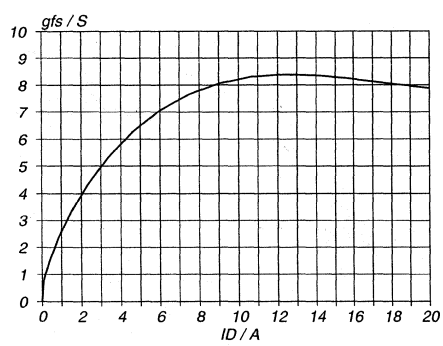


Fig.8. Typical transconductance, $T_j = 25$ °C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

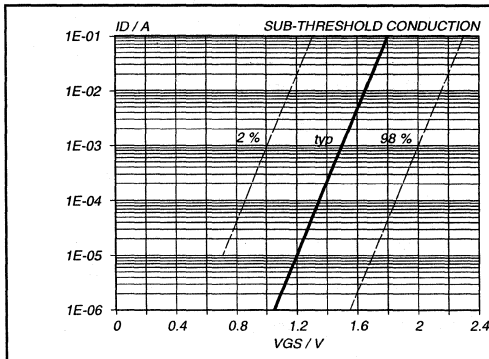


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

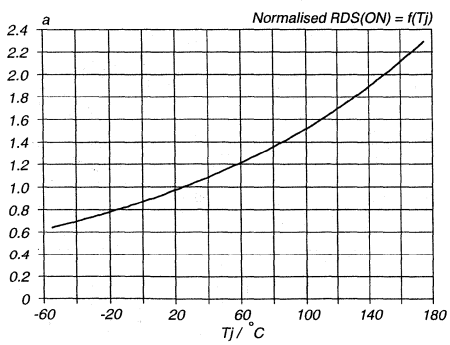


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ °C} = f(T_j)$; $I_D = 6.5$ A; $V_{GS} = 5$ V

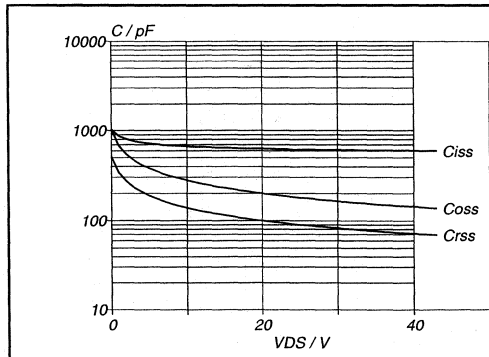


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

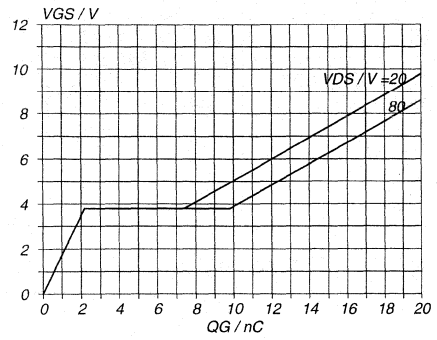


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 13 A; parameter V_{DS}

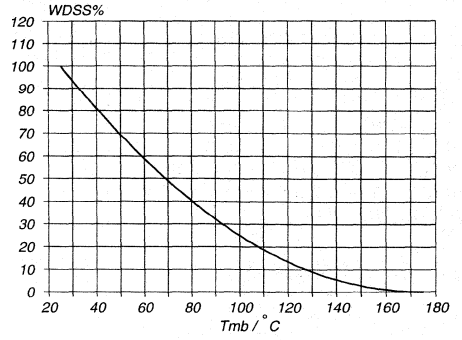


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: I_D = 13 A

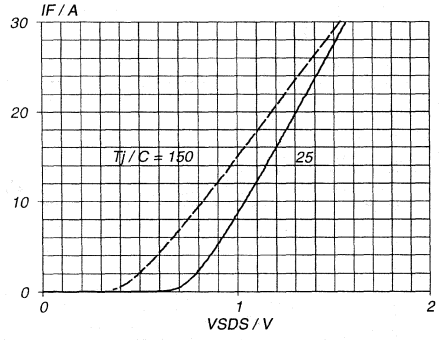


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

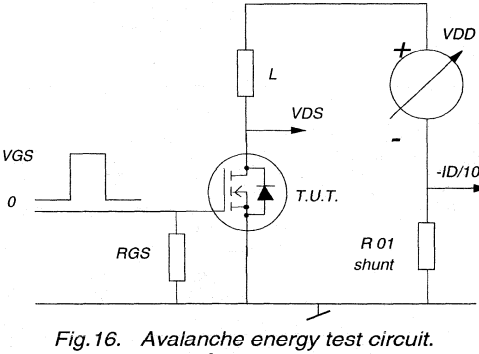


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor Logic level FET

BUK554-200A/B

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

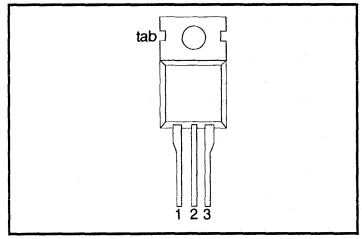
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK554	-200A	-200B	
V_{DS}	Drain-source voltage	200	200	V
I_D	Drain current (DC)	9.2	8.2	A
P_{tot}	Total power dissipation	90	90	W
T_j	Junction temperature	175	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.4	0.5	Ω

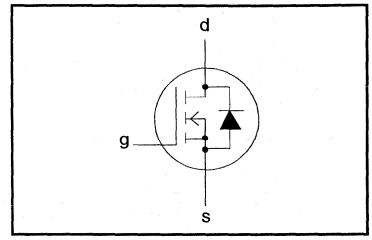
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	200		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200		V
$\pm V_{GS}$	Gate-source voltage	-	-	15		V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20		V
				-200A	-200B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	9.2	8.2	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	6.5	5.8	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	36	33	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	90		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction Temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.67	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; **BUK554-200A**	-	0.35	0.4	Ω
		I_D = 3.5 A **BUK554-200B**	-	0.4	0.5	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 3.5 A	3.5	6.0	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	800	1000	pF
C_{oss}	Output capacitance		-	120	160	pF
C_{rss}	Feedback capacitance		-	65	90	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.9 A;	-	16	30	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	75	110	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	120	180	ns
t_f	Turn-off fall time		-	50	75	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	9.2	A
I_{DRM}	Pulsed reverse drain current	-	-	-	36	A
V_{SD}	Diode forward voltage	I_F = 9.2 A ; V_{GS} = 0 V	-	1.1	1.3	V
t_{rr}	Reverse recovery time	I_F = 9.2 A; -dI_F/dt = 100 A/µs;	-	200	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	0.6	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 9 A ; $V_{DD} \leq$ 100 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	50	mJ

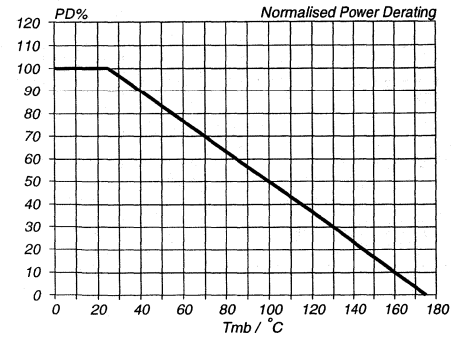


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

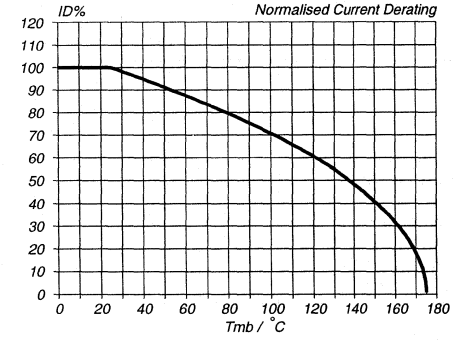


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: $V_{GS} \geq 5$ V

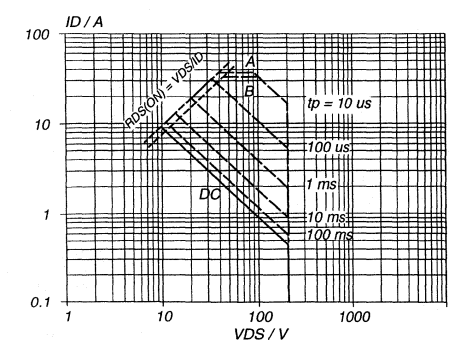


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

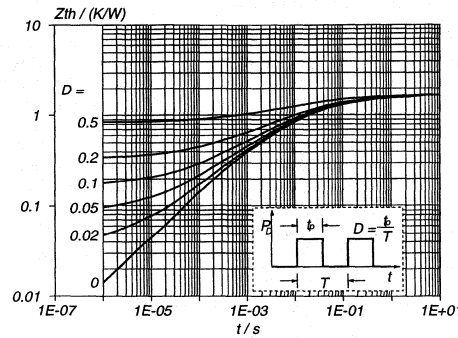


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

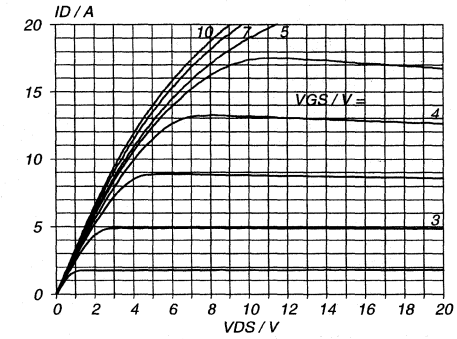


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

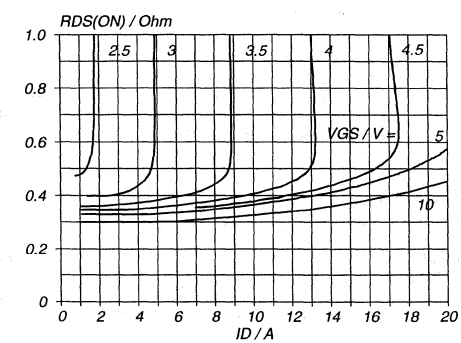


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

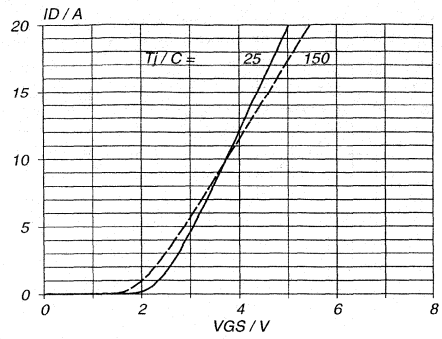


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

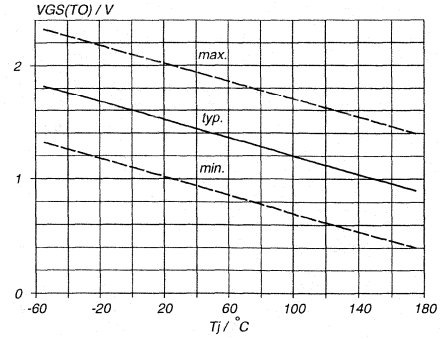


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

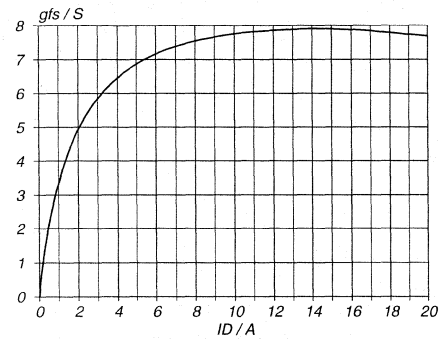


Fig.8. Typical transconductance, T_j = 25 ˚C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

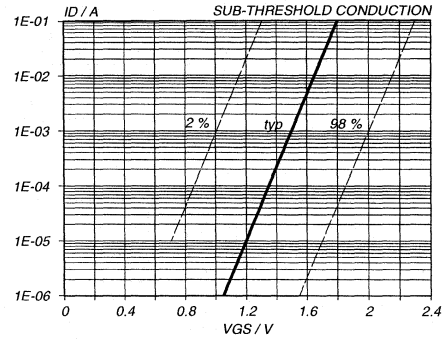


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

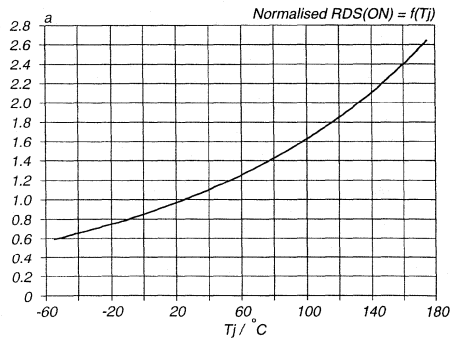


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,^{\circ}C} = f(T_j)$; I_D = 3.5 A; V_{GS} = 5 V

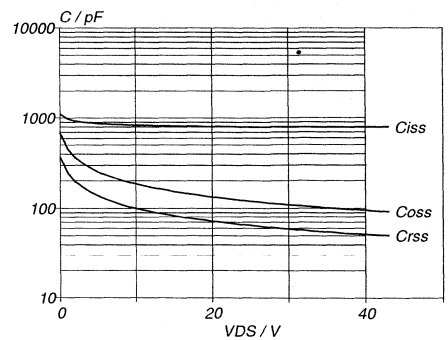


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

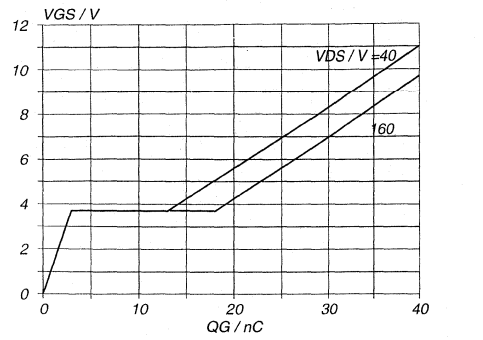


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 9.2$ A; parameter V_{DS}

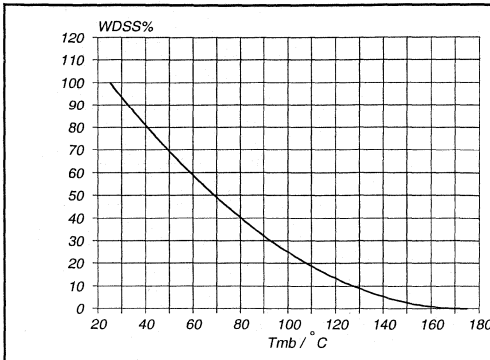


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 9$ A

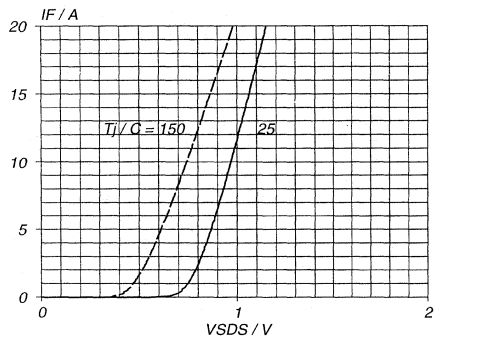


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

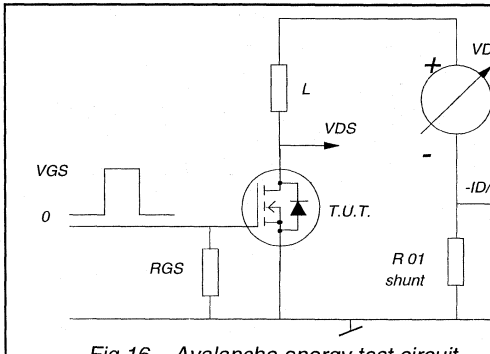


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor Logic level FET

BUK555-100A/B

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

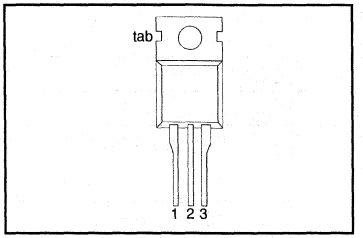
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK555	-100A	-100B	
V_{DS}	Drain-source voltage	100	100	V
I_D	Drain current (DC)	25	22	A
P_{tot}	Total power dissipation	125	125	W
T_j	Junction temperature	175	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.085	0.11	Ω

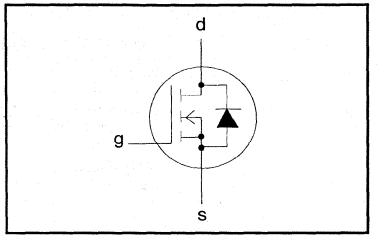
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	100		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100		V
$\pm V_{GS}$	Gate-source voltage	-	-	15		V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20		V
				-100A	-100B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	25	22	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	18	15	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	100	88	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction Temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; **BUK555-100A**	-	0.075	0.085	Ω
		I_D = 13 A **BUK555-100B**	-	0.09	0.11	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 13 A	10	13.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1450	1750	pF
C_{oss}	Output capacitance		-	280	350	pF
C_{rss}	Feedback capacitance		-	100	150	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	25	40	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	65	85	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	135	180	ns
t_f	Turn-off fall time		-	80	110	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	25	A
I_{DRM}	Pulsed reverse drain current	-	-	-	100	A
V_{SD}	Diode forward voltage	I_F = 25 A ; V_{GS} = 0 V	-	1.3	1.7	V
t_{rr}	Reverse recovery time	I_F = 25 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.8	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 25 A ; V_{DD} ≤ 50 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	140	mJ

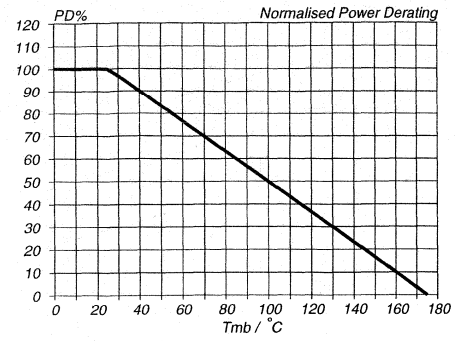


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

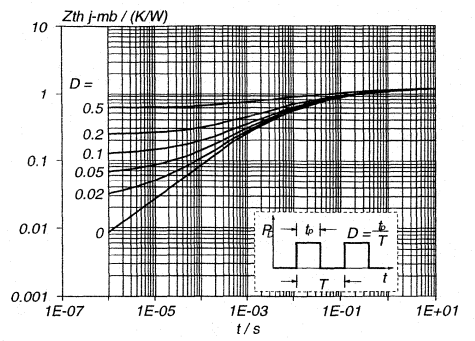


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

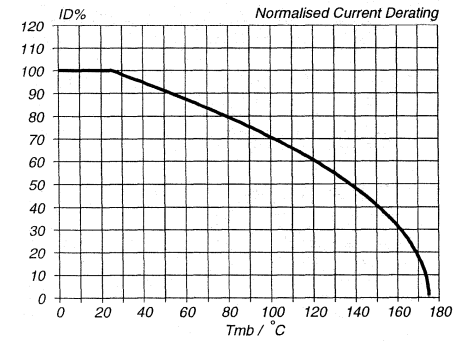


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 5 V

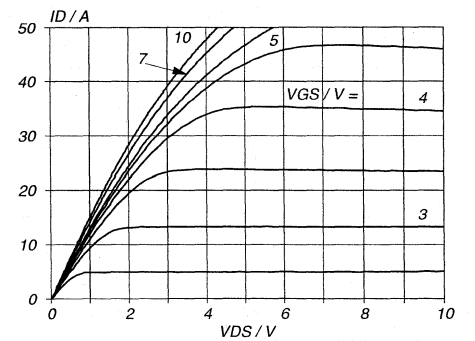


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

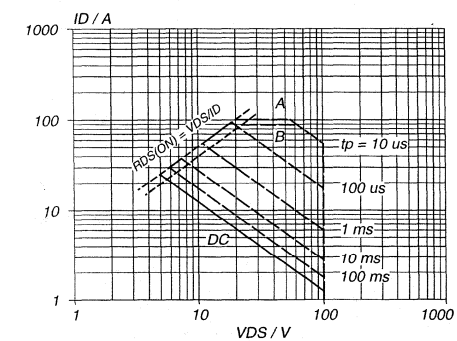


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

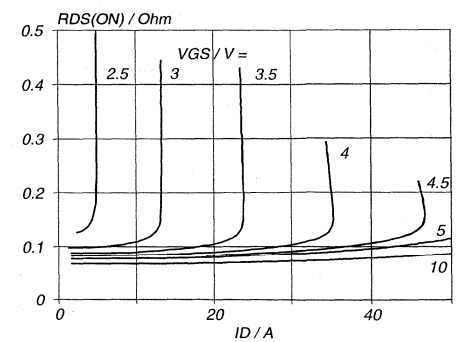


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

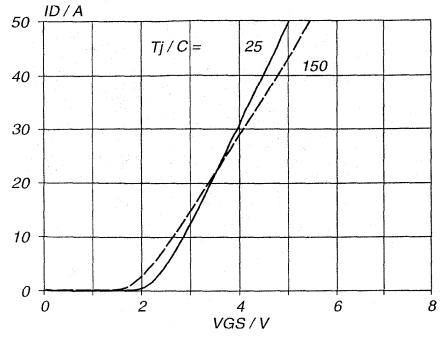


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

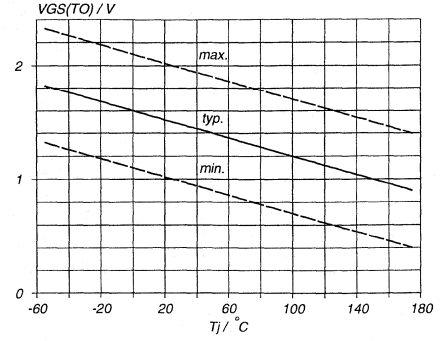


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

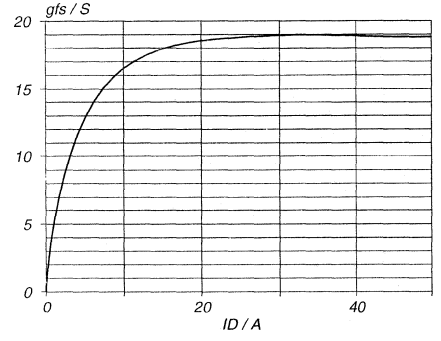


Fig.8. Typical transconductance, $T_j = 25$ °C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

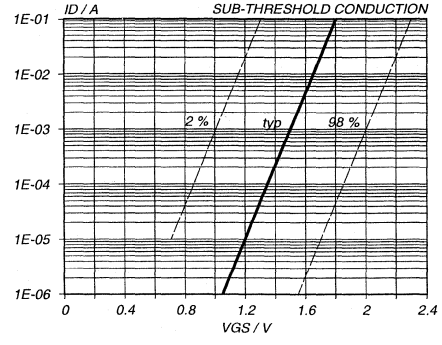


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

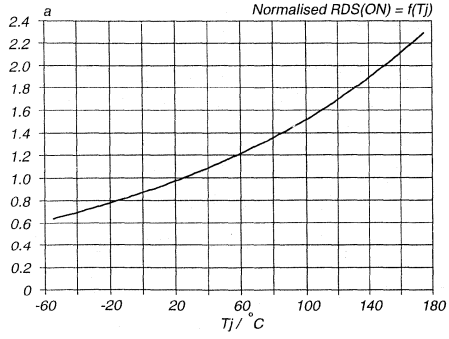


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 13$ A; $V_{GS} = 5$ V

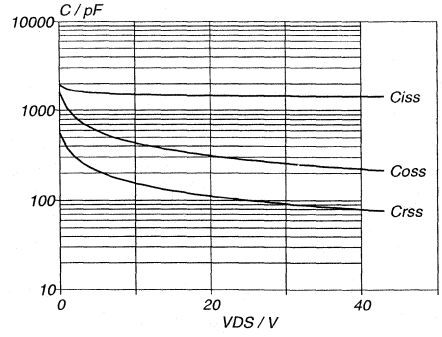


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

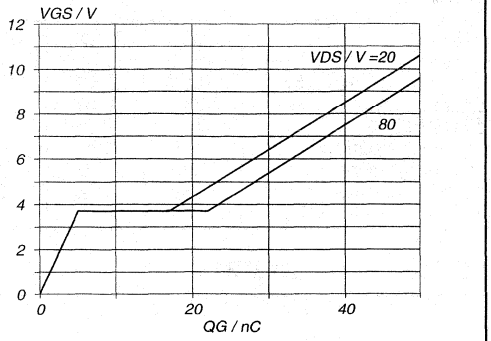


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 25$ A; parameter V_{DS}

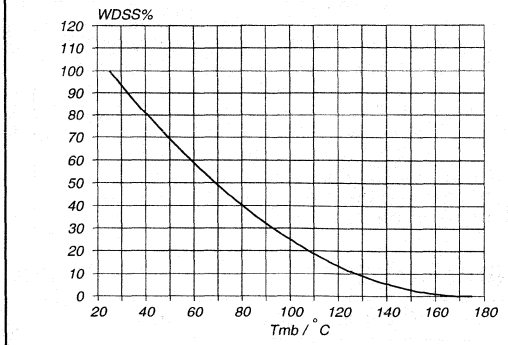


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 25$ A

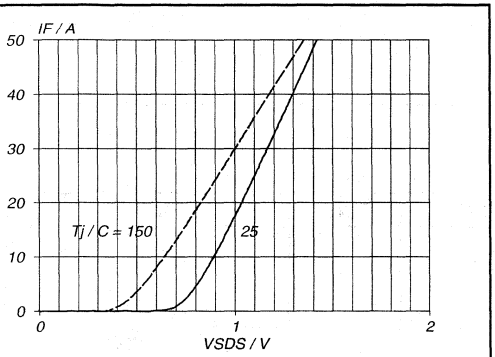


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

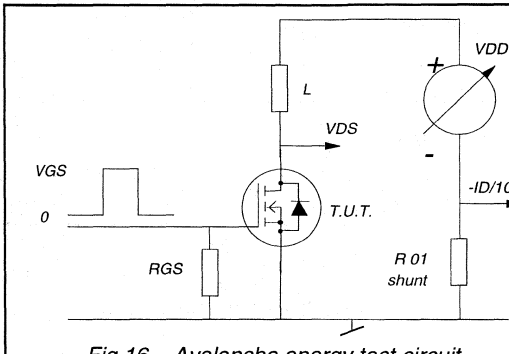


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PowerMOS transistor Logic level FET

BUK555-200A/B

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

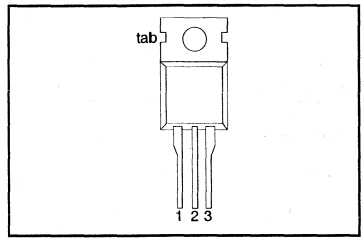
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK555	-200A	-200B	
V_{DS}	Drain-source voltage	200	200	V
I_D	Drain current (DC)	14	13	A
P_{tot}	Total power dissipation	125	125	W
T_j	Junction temperature	175	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.23	0.28	Ω

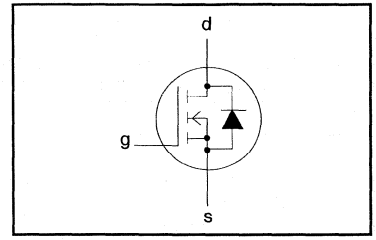
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	200		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200		V
$\pm V_{GS}$	Gate-source voltage	-	-	15		V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20		V
				-200A	-200B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	14	13	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	10	9.2	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	56	52	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction Temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; **BUK555-200A** I_D = 7 A **BUK555-200B**	- -	0.2 0.24	0.23 0.28	Ω Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 7 A	8.0	15	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1600	2000	pF
C_{oss}	Output capacitance		-	180	250	pF
C_{rss}	Feedback capacitance		-	55	80	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	25	40	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	45	75	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	140	180	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	14	A
I_{DRM}	Pulsed reverse drain current	-	-	-	56	A
V_{SD}	Diode forward voltage	I_F = 14 A ; V_{GS} = 0 V	-	1.0	1.5	V
t_{rr}	Reverse recovery time	I_F = 14 A; -dI_F/dt = 100 A/µs;	-	200	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.25	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 14 A ; V_{DD} ≤ 100 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	100	mJ

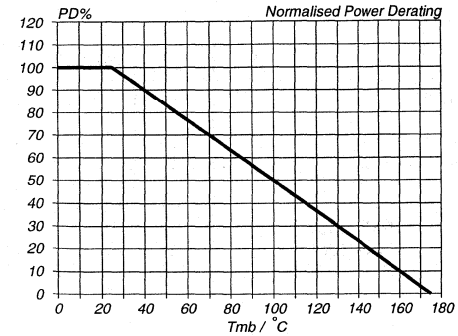


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D / P_{D\,25\,°C} = f(T_{mb})$

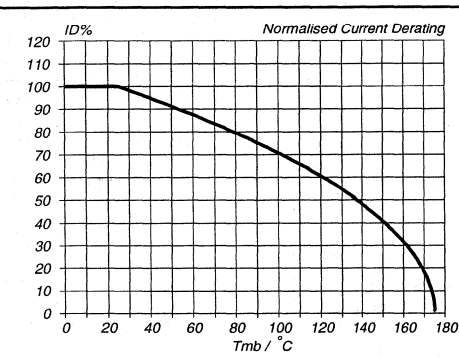


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D / I_{D\,25\,°C} = f(T_{mb})$; *conditions:* $V_{GS} \geq 5$ V

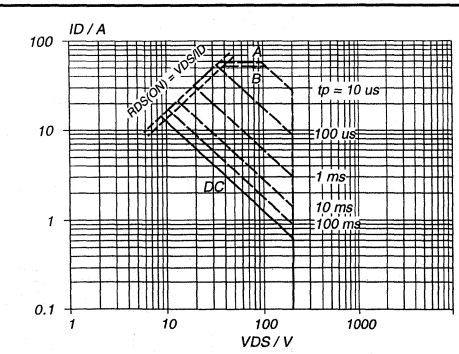


Fig.3. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} *single pulse; parameter* t_p

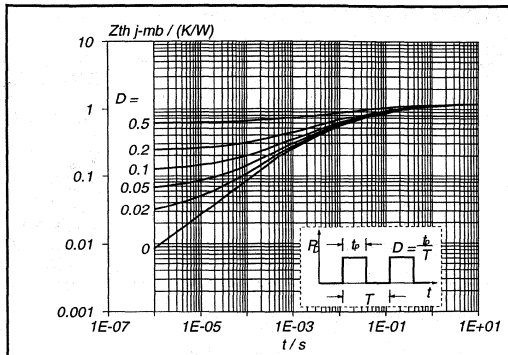


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb} = f(t)$; *parameter* $D = t_p/T$

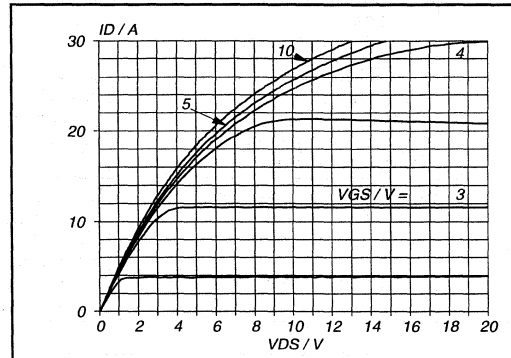


Fig.5. Typical output characteristics, $T_j = 25$ °C.
$I_D = f(V_{DS})$; *parameter* V_{GS}

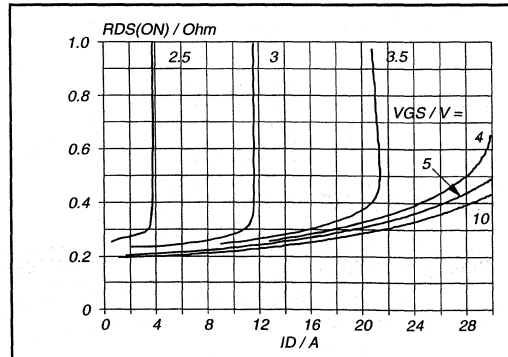


Fig.6. Typical on-state resistance, $T_j = 25$ °C.
$R_{DS(ON)} = f(I_D)$; *parameter* V_{GS}

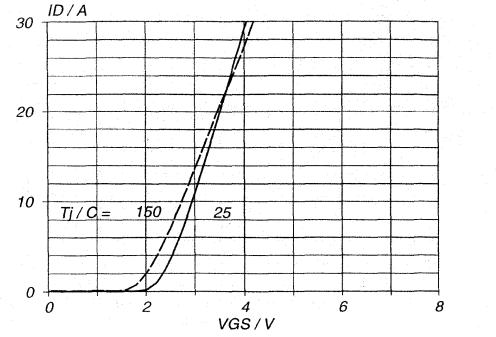


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

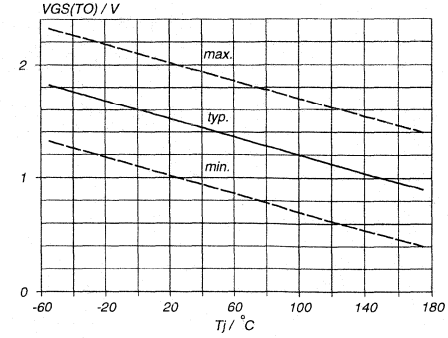


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

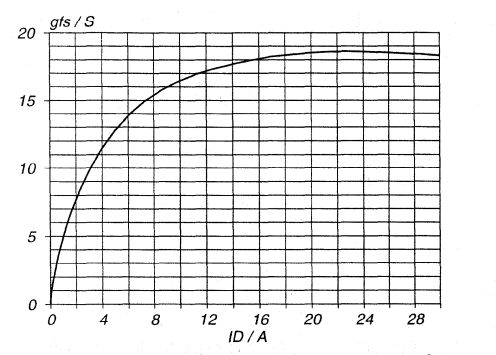


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

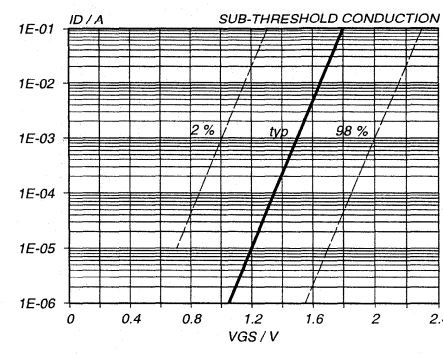


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

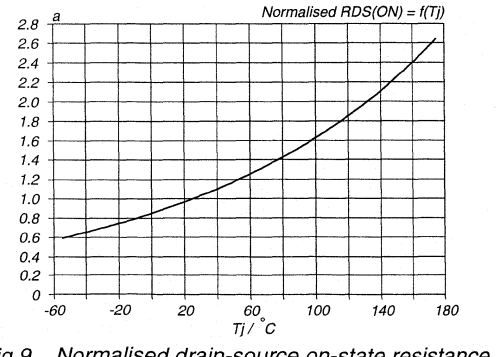


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 7 A; V_{GS} = 5 V

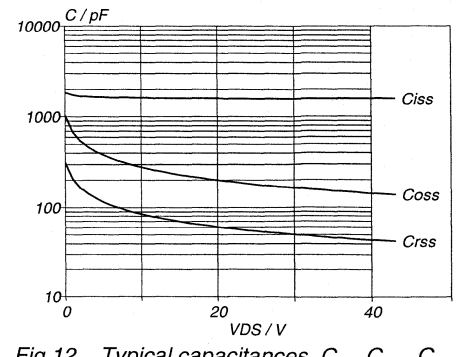


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

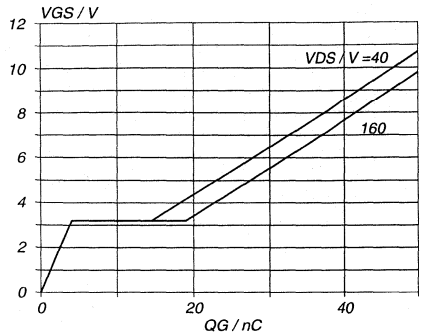


Fig.13. Typical turn-on gate-charge characteristics.
V_{GS} = f(Q_G); conditions: I_D = 14 A; parameter V_{DS}

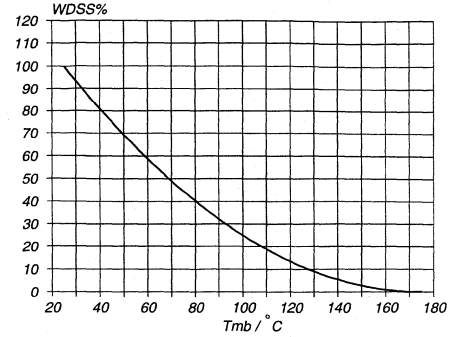


Fig.15. Normalised avalanche energy rating.
W_{DSS}% = f(T_{mb}); conditions: I_D = 14 A

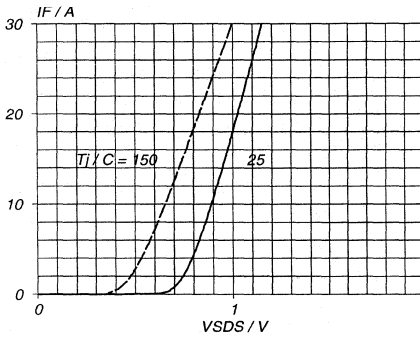


Fig.14. Typical reverse diode current.
I_F = f(V_{SDS}); conditions: V_{GS} = 0 V; parameter T_j

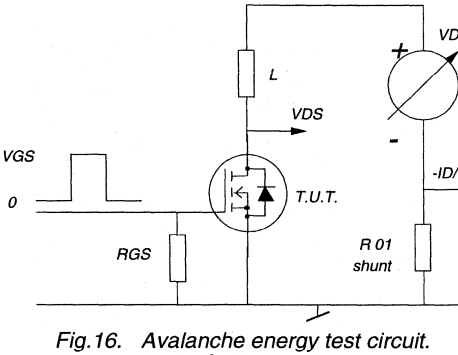


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor Logic level FET

BUK562-100A

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

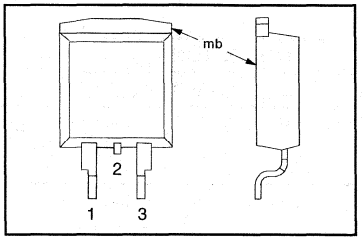
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	10	A
P_{tot}	Total power dissipation	60	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.28	Ω

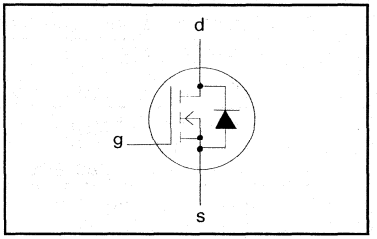
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	10	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	7	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	40	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	60	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board (see fig. 18).	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 5.5 A	-	0.25	0.28	Ω
						Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5.5 A	4.5	6	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	400	600	pF
C_{oss}	Output capacitance		-	90	120	pF
C_{rss}	Feedback capacitance		-	35	50	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	12	18	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	45	70	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	50	70	ns
t_f	Turn-off fall time		-	30	45	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	10	A
I_{DRM}	Pulsed reverse drain current	-	-	-	40	A
V_{SD}	Diode forward voltage	I_F = 10 A ; V_{GS} = 0 V	-	1.2	1.5	V
t_{rr}	Reverse recovery time	I_F = 10 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.35	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 10 A ; V_{DD} ≤ 50 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	30	mJ

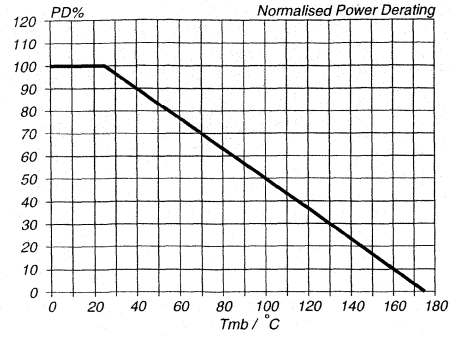


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

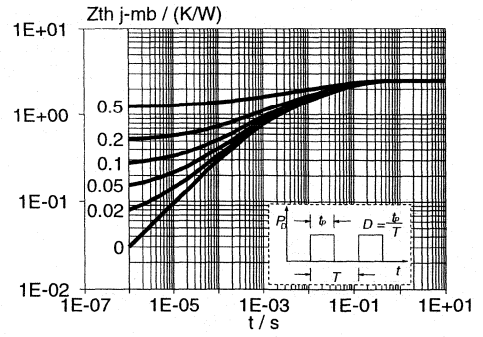


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

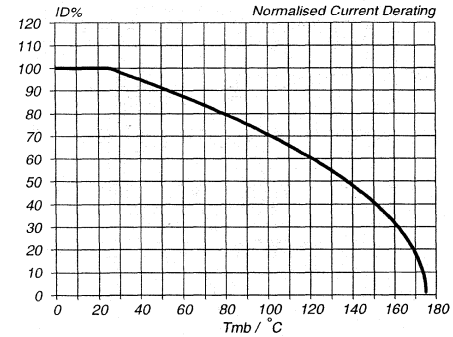


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 5 V

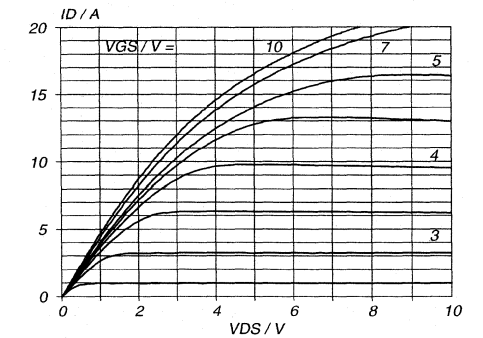


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

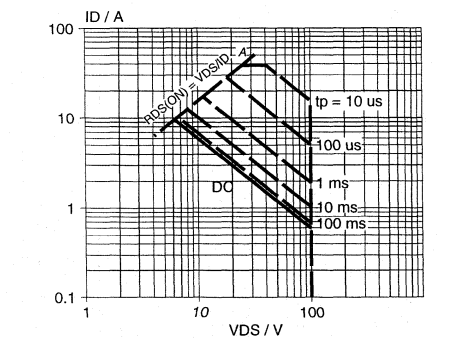


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

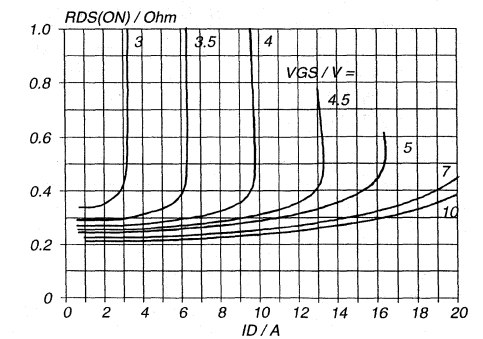


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

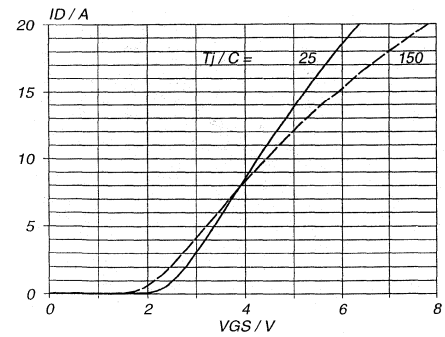


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

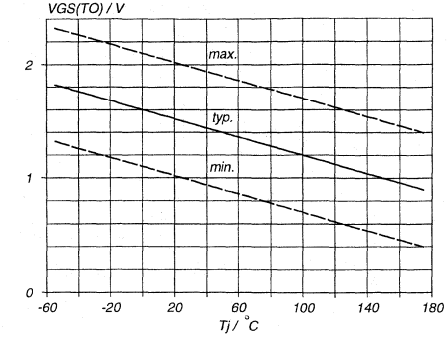


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

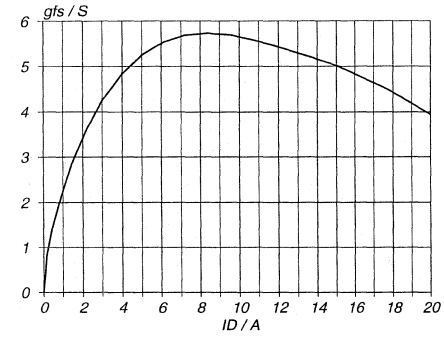


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

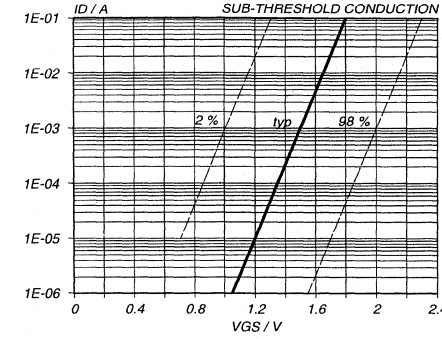


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

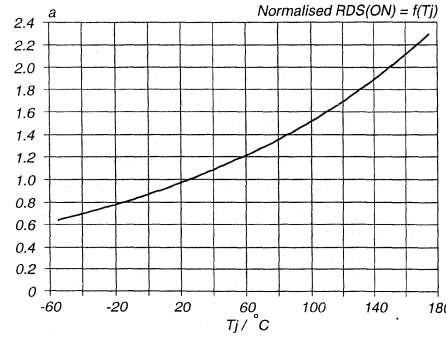


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 5.5 A; V_{GS} = 5 V

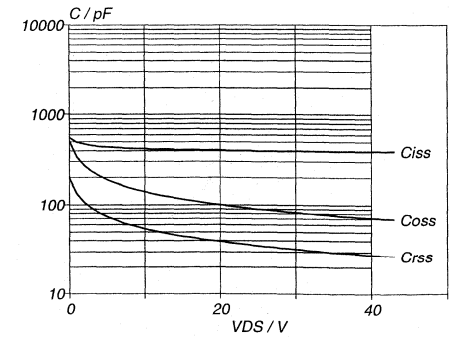


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

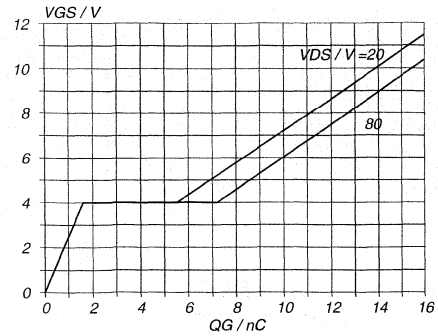


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 10 A; parameter V_{DS}

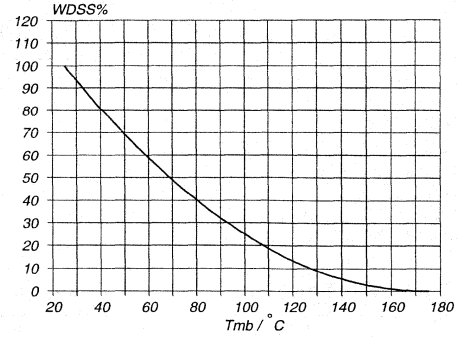


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: I_D = 10 A

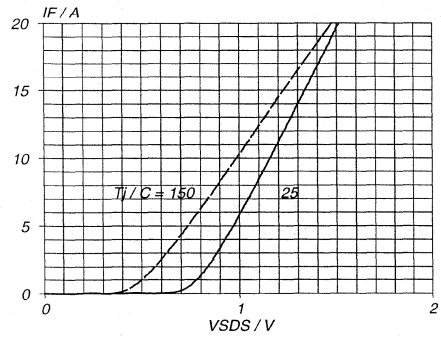


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

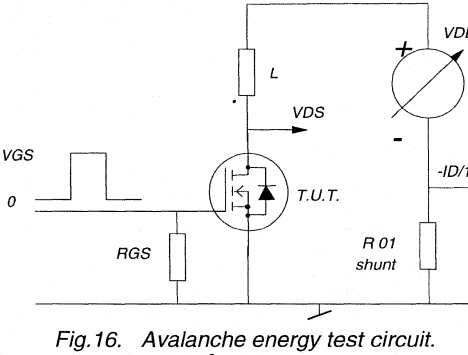


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor Logic level FET

BUK563-100A

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

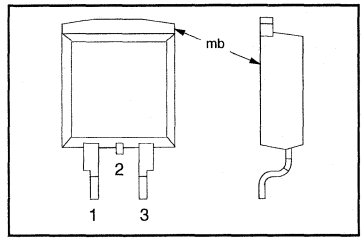
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	13	A
P_{tot}	Total power dissipation	75	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.18	Ω

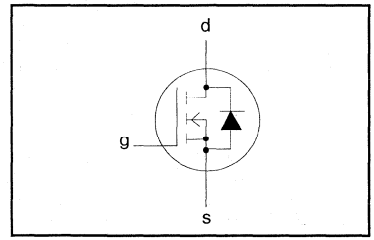
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ μs	-	20	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	13	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	9	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	52	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	75	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 boards (see Fig 18).	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 6.5 A	-	0.17	0.18	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 6.5 A	6.0	8.0	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	620	825	pF
C_{oss}	Output capacitance		-	180	250	pF
C_{rss}	Feedback capacitance		-	90	120	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	10	20	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	45	60	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	90	115	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	13	A
I_{DRM}	Pulsed reverse drain current	-	-	-	52	A
V_{SD}	Diode forward voltage	I_F = 13 A ; V_{GS} = 0 V	-	1.2	1.5	V
t_{rr}	Reverse recovery time	I_F = 13 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.6	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 13 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	70	mJ

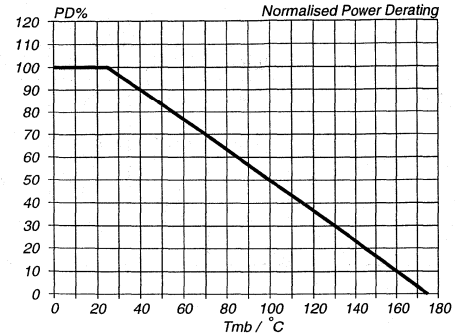


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

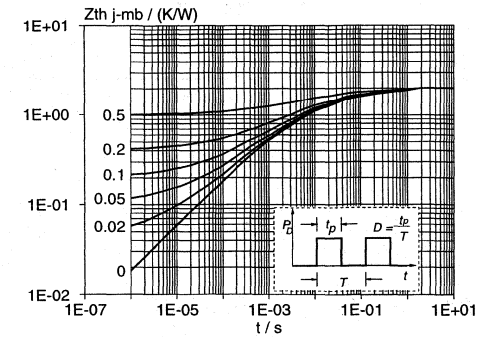


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

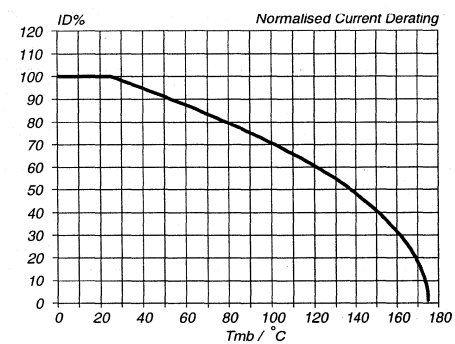


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: V_{GS} ≥ 5 V

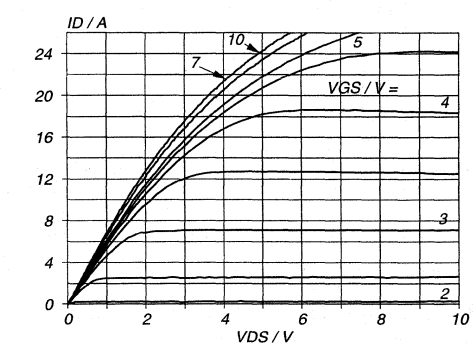


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

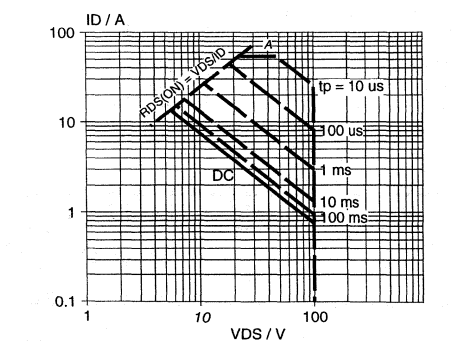


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

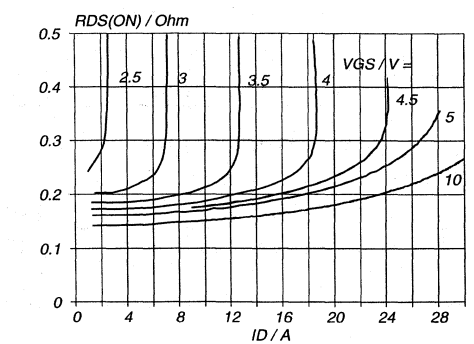


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

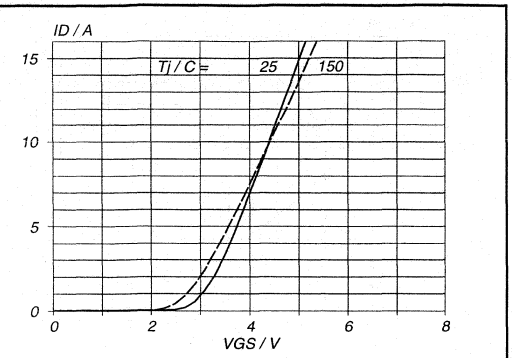


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

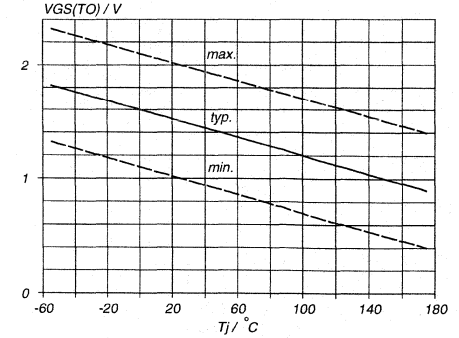


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

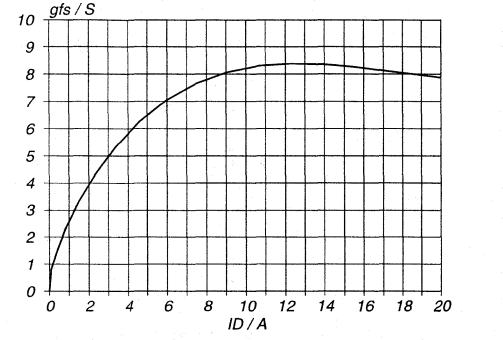


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

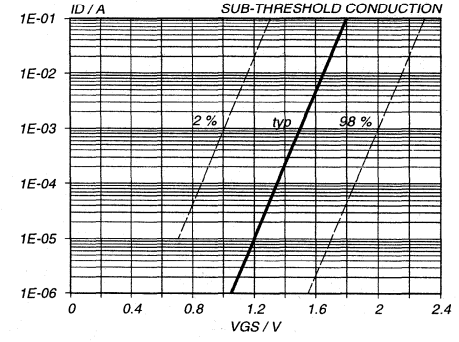


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

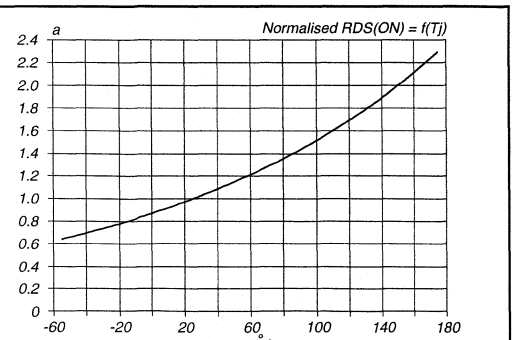


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 6.5 A; V_{GS} = 5 V

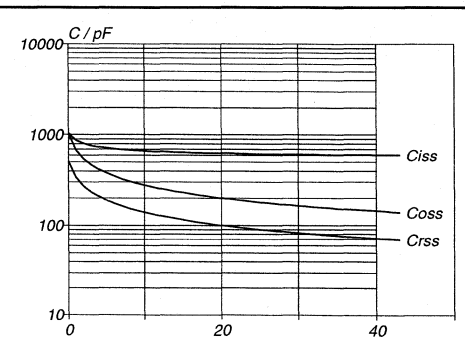


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

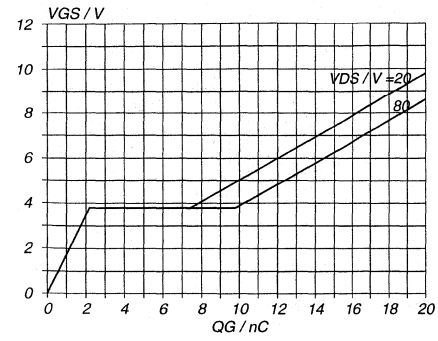


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: I_D = 13 A; parameter V_{DS}

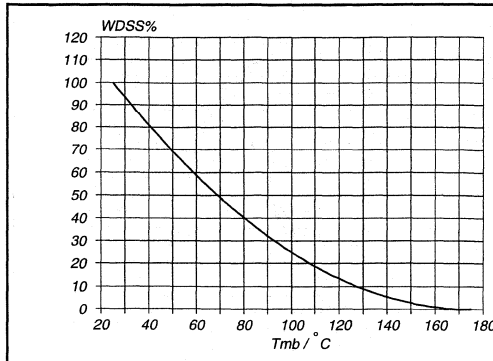


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: I_D = 13 A

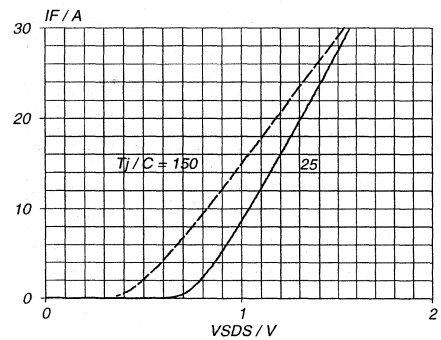


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

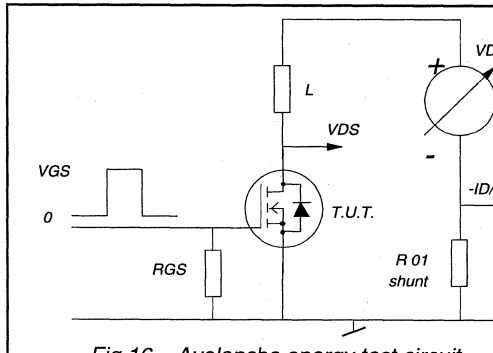


Fig.16. Avalanche energy test circuit.
$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PowerMOS transistor Logic level FET

BUK564-200A

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

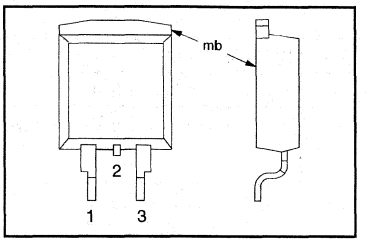
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (DC)	9.2	A
P_{tot}	Total power dissipation	90	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.4	Ω

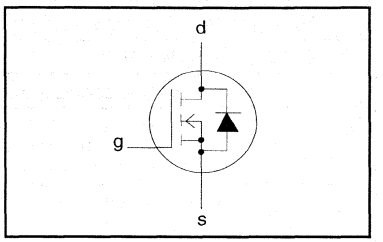
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	200	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	9.2	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	6.5	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	36	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	90	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.67	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board (see Fig. 18).	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 3.5 A	-	0.35	0.4	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 3.5 A	3.5	6.0	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	800	1000	pF
C_{oss}	Output capacitance		-	120	160	pF
C_{rss}	Feedback capacitance		-	65	90	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.9 A;	-	16	30	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	75	110	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	120	180	ns
t_f	Turn-off fall time		-	50	75	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	9.2	A
I_{DRM}	Pulsed reverse drain current	-	-	-	36	A
V_{SD}	Diode forward voltage	I_F = 9.2 A ; V_{GS} = 0 V	-	1.1	1.3	V
t_{rr}	Reverse recovery time	I_F = 9.2 A; -dI_F/dt = 100 A/µs;	-	200	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	0.6	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 9 A ; V_{DD} ≤ 100 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	50	mJ

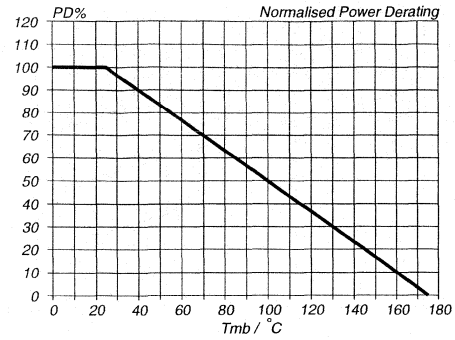


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D / P_{D\,25\,°C} = f(T_{mb})$

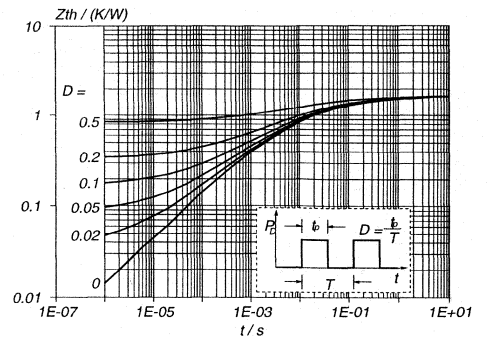


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb} = f(t)$; parameter $D = t_p/T$

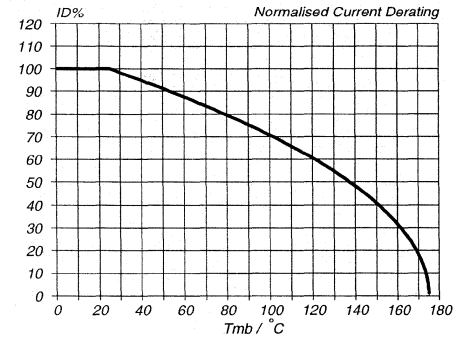


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D / I_{D\,25\,°C} = f(T_{mb})$; conditions: $V_{GS} \geq 5$ V

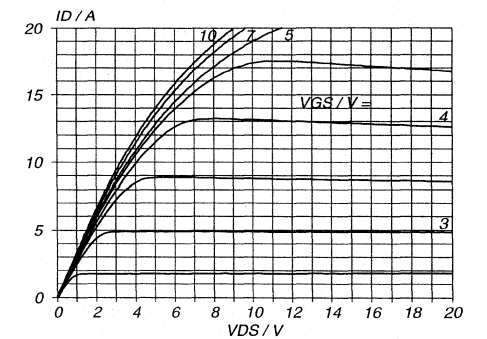


Fig.5. Typical output characteristics, $T_j = 25$ °C.
$I_D = f(V_{DS})$; parameter V_{GS}

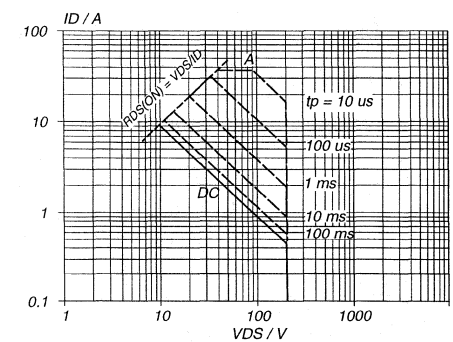


Fig.3. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

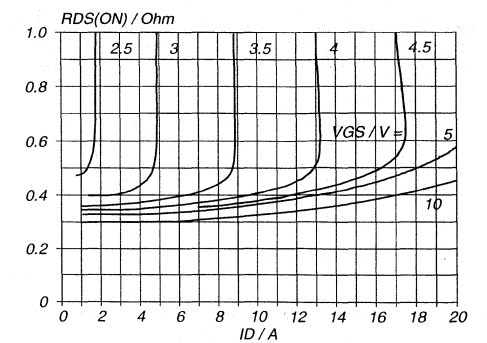


Fig.6. Typical on-state resistance, $T_j = 25$ °C.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

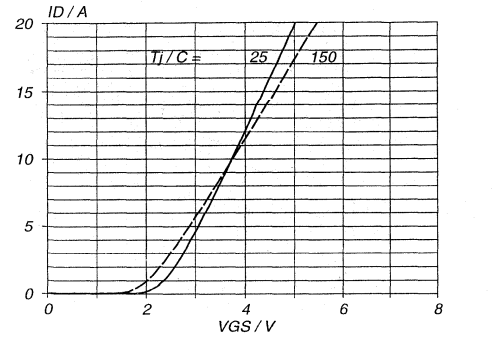


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

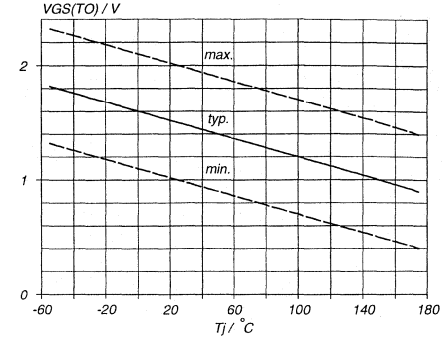


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

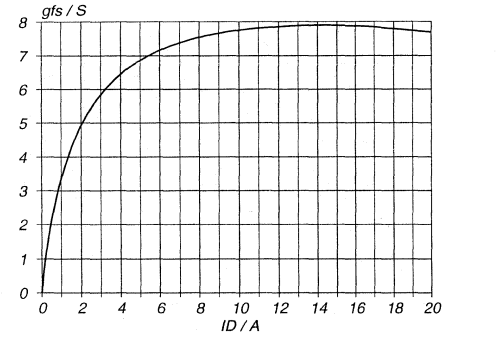


Fig.8. Typical transconductance, $T_j = 25$ °C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

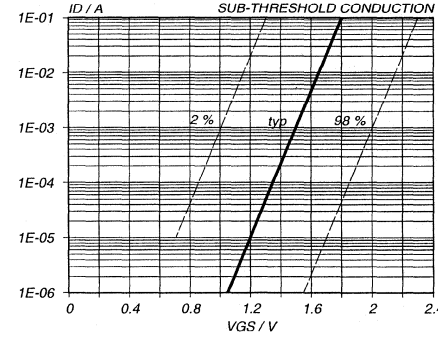


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

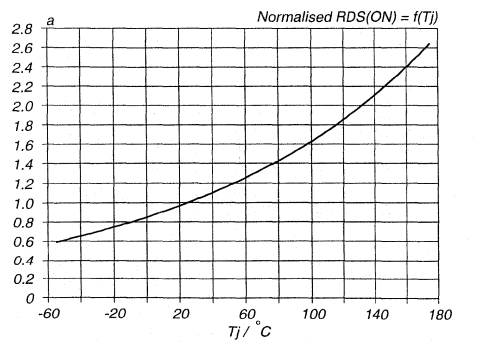


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ °C} = f(T_j)$; $I_D = 3.5$ A; $V_{GS} = 5$ V

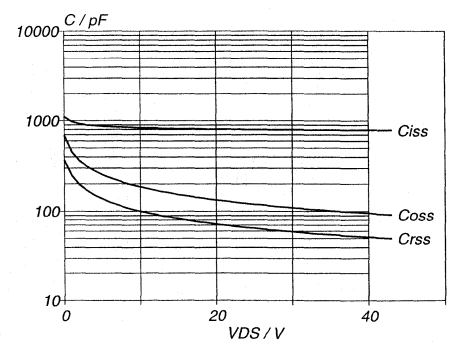


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

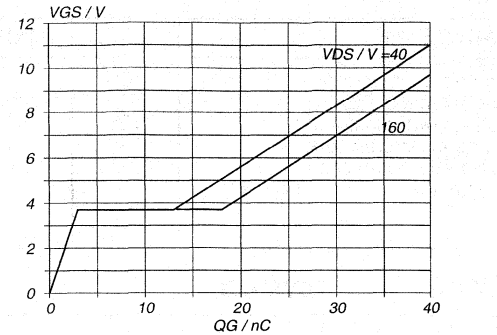


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 9.2$ A; parameter V_{DS}

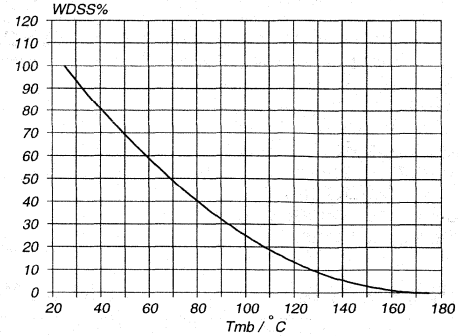


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 9$ A

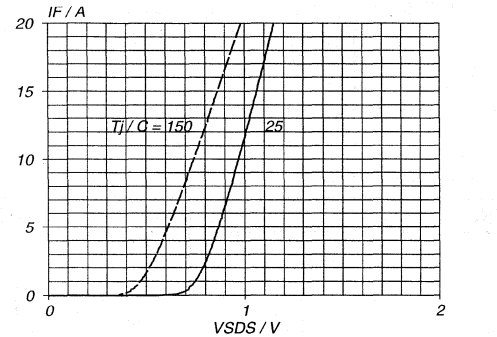


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

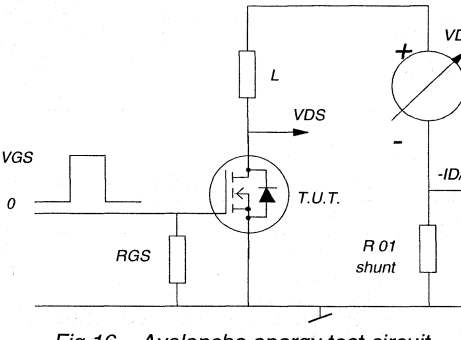


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor Logic level FET

BUK565-100A

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

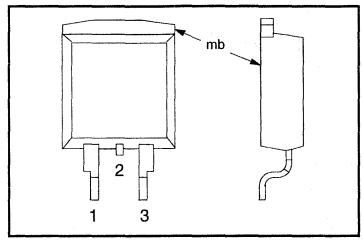
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	25	A
P_{tot}	Total power dissipation	125	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; $V_{GS} = 5$ V	0.085	Ω

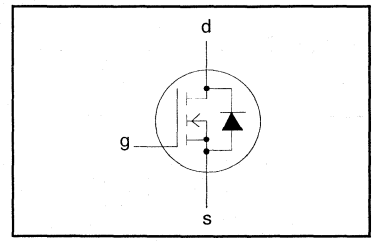
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	25	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	18	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	100	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board (see Fig 18).	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 13 A	-	0.075	0.085	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 13 A	10	13.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1450	1750	pF
C_{oss}	Output capacitance		-	280	350	pF
C_{rss}	Feedback capacitance		-	100	150	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	25	40	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	65	85	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	135	180	ns
t_f	Turn-off fall time		-	80	110	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	25	A
I_{DRM}	Pulsed reverse drain current	-	-	-	100	A
V_{SD}	Diode forward voltage	I_F = 25 A ; V_{GS} = 0 V	-	1.3	1.7	V
t_{rr}	Reverse recovery time	I_F = 25 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.8	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 25 A ; V_{DD} ≤ 50 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	140	mJ

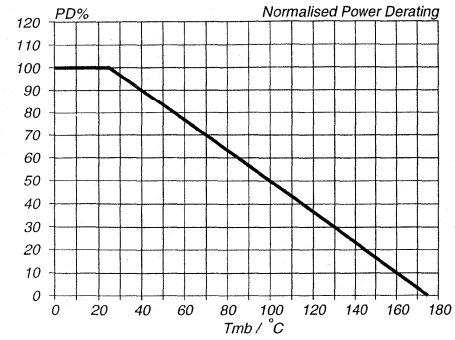


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

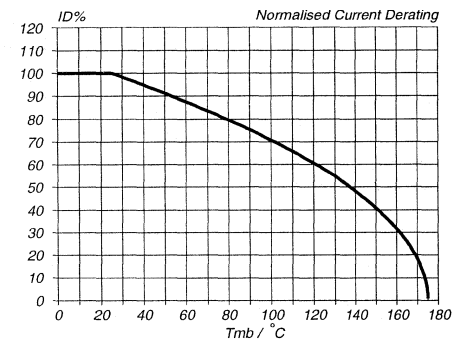


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 5 V

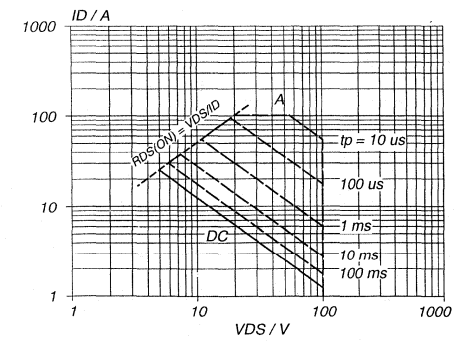


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

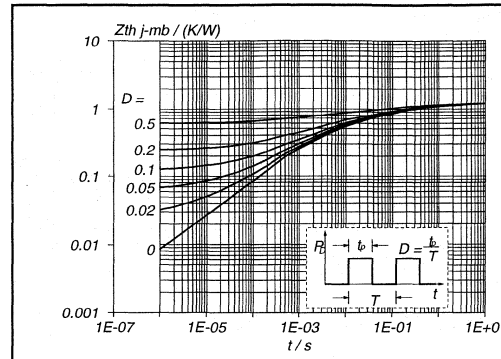


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

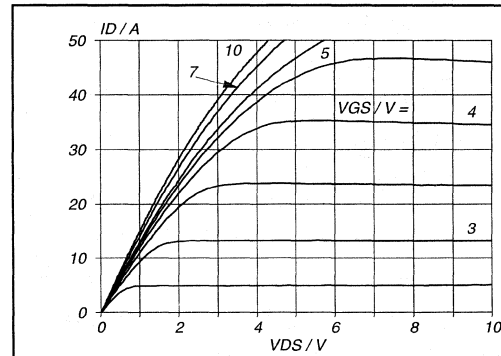


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

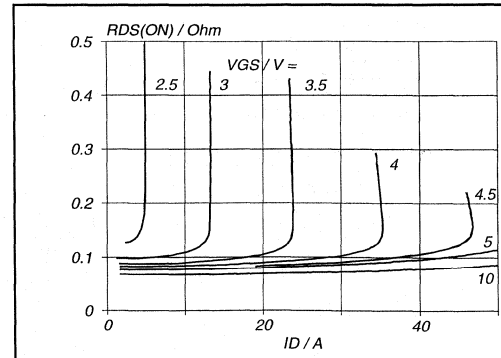


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

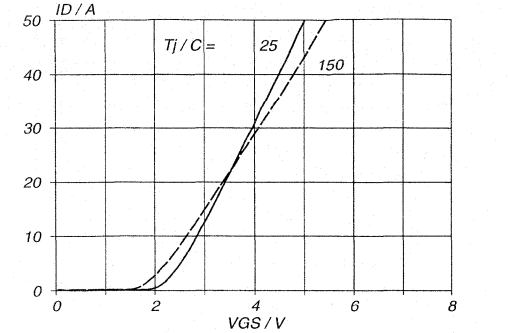


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

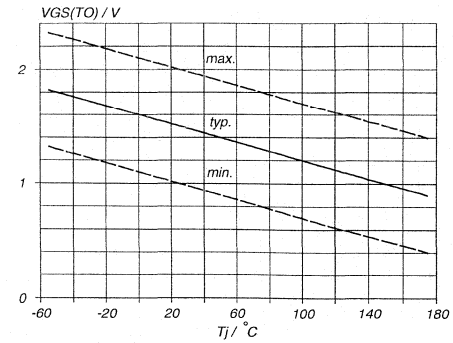


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

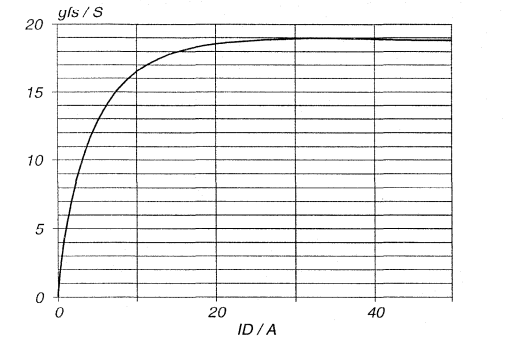


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

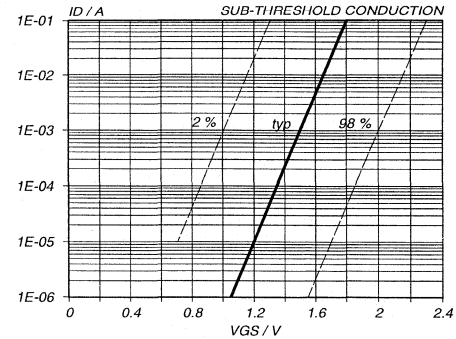


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

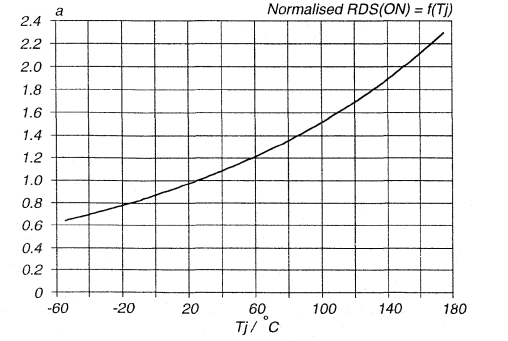


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 13 A; V_{GS} = 5 V

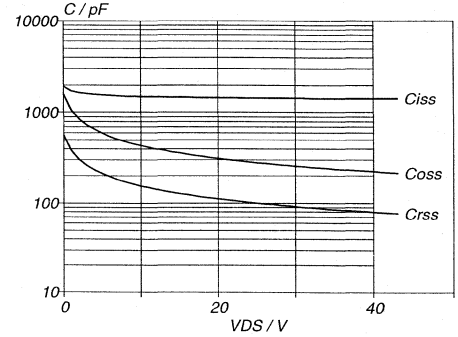


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

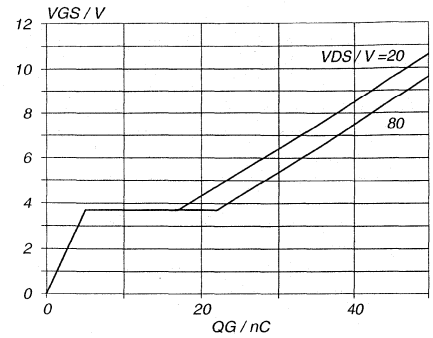


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 25$ A; parameter V_{DS}

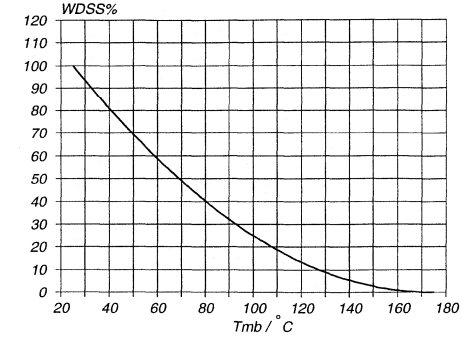


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 25$ A

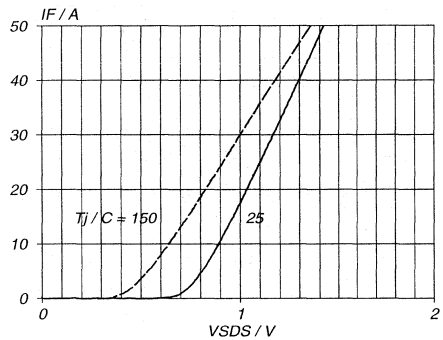


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

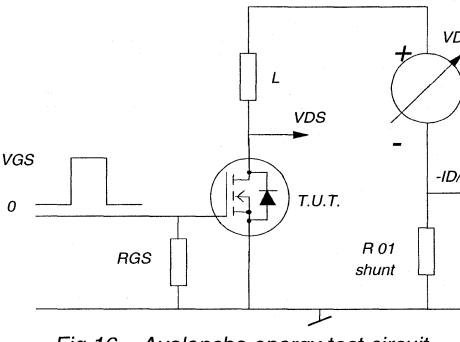


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor Logic level FET

BUK565-200A

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

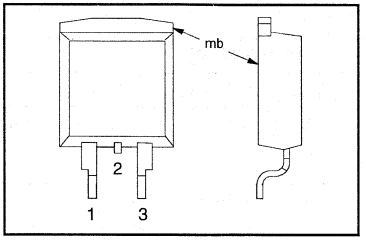
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (DC)	14	A
P_{tot}	Total power dissipation	125	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; $V_{GS} = 5$ V	0.23	Ω

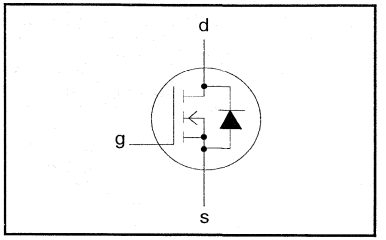
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	200	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	14	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	10	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	56	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 boards (see Fig. 18).	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 7 A	-	0.2	0.23	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 7 A	8.0	15	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1600	2000	pF
C_{oss}	Output capacitance		-	180	250	pF
C_{rss}	Feedback capacitance		-	55	80	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	25	40	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	45	75	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	140	180	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	14	A
I_{DRM}	Pulsed reverse drain current	-	-	-	56	A
V_{SD}	Diode forward voltage	I_F = 14 A ; V_{GS} = 0 V	-	1.0	1.5	V
t_{rr}	Reverse recovery time	I_F = 14 A; -dI_F/dt = 100 A/µs;	-	200	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.25	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 14 A ; $V_{DD} \leq$ 100 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	100	mJ

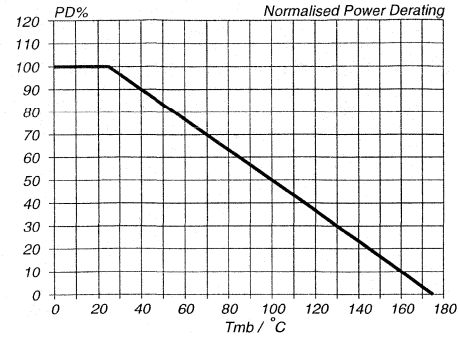


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D / P_{D\,25\,°C} = f(T_{mb})$

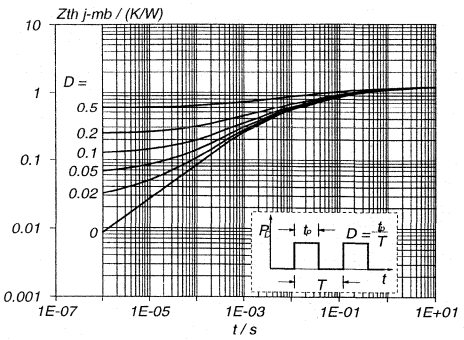


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb} = f(t)$; parameter $D = t_p/T$

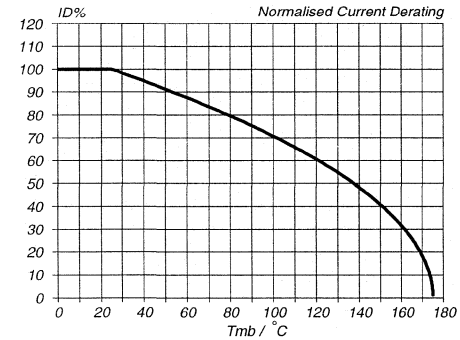


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D / I_{D\,25\,°C} = f(T_{mb})$; conditions: $V_{GS} \geq 5$ V

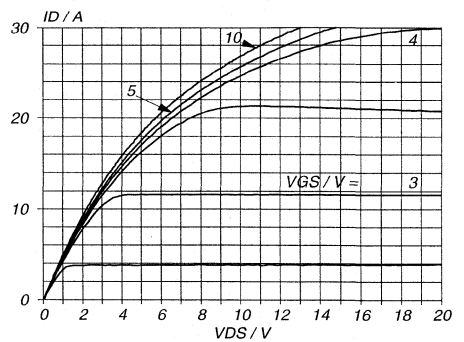


Fig.5. Typical output characteristics, $T_j = 25$ °C.
$I_D = f(V_{DS})$; parameter V_{GS}

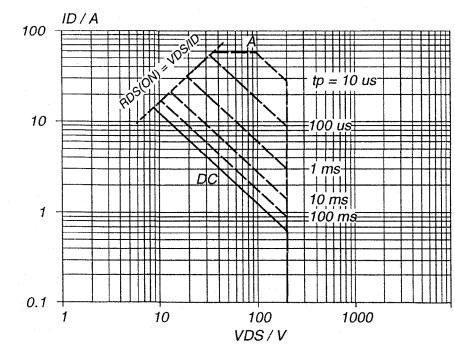


Fig.3. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

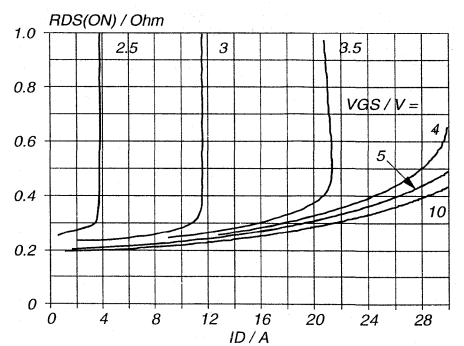


Fig.6. Typical on-state resistance, $T_j = 25$ °C.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

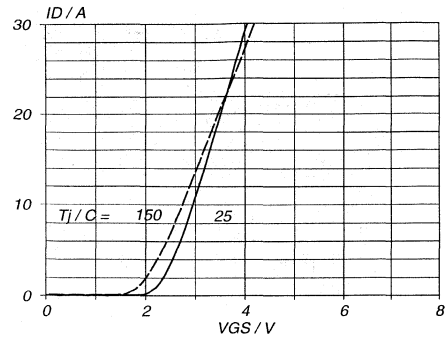


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

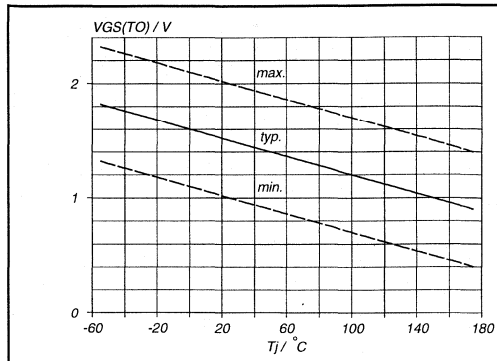


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

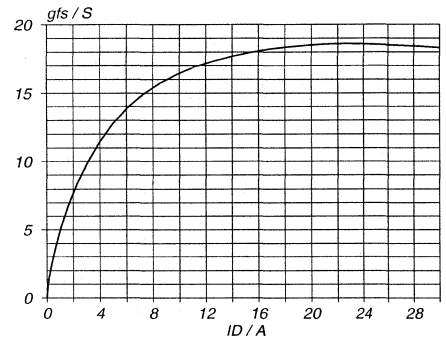


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

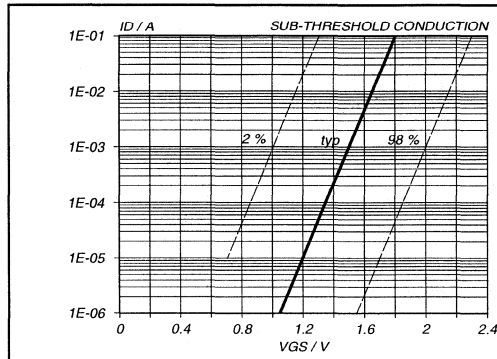


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

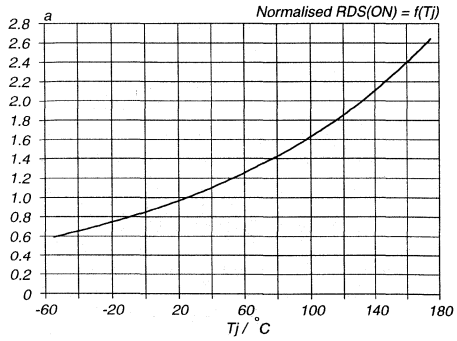


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 7 A; V_{GS} = 5 V

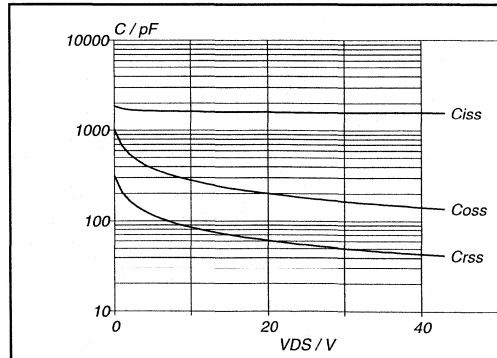


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

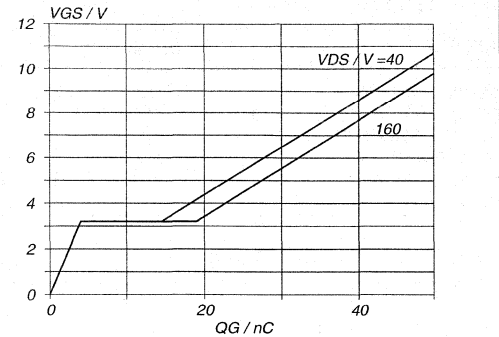


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 14 A; parameter V_{DS}

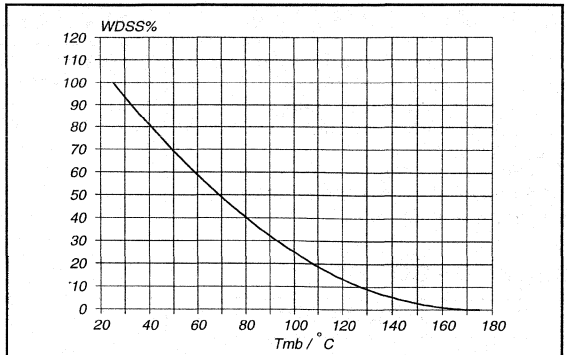


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: I_D = 14 A

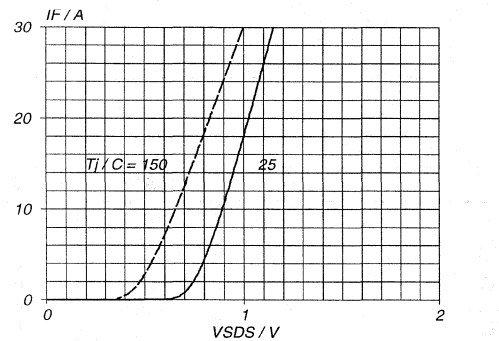


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

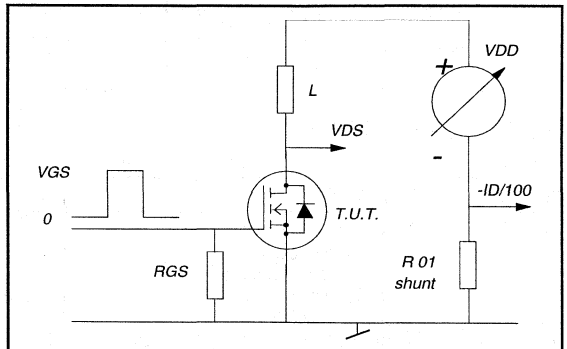


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor Logic level FET

BUK581-100A

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in automotive and general purpose switching applications.

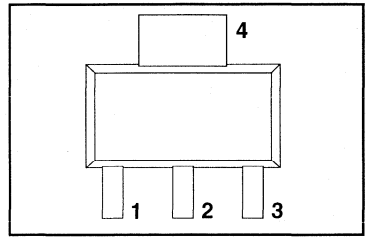
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	0.9	A
P_{tot}	Total power dissipation	1.5	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.90	Ω

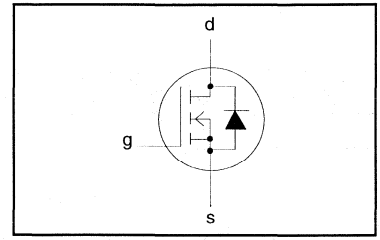
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
I_D	Drain current (DC)	T_{amb} = 25 °C	-	0.9	A
I_D	Drain current (DC)	T_{amb} = 100 °C	-	0.6	A
I_{DM}	Drain current (pulse peak value)	T_{amb} = 25 °C	-	3.6	A
P_{tot}	Total power dissipation	T_{amb} = 25 °C	-	1.5	W
T_{stg}	Storage temperature	-	- 55	150	°C
T_j	Junction Temperature	-	-	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}b}$	From junction to board[1]	Mounted on any PCB	-	50	-	K/W
$R_{th\ j\text{-}amb}$	From junction to ambient	Mounted on PCB of Fig.17	-	-	85	K/W

1 Temperature measured 1-3 mm from tab.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V;	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 0.9 A	-	0.51	0.90	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 0.9 A	1	1.8	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	180	300	pF
C_{oss}	Output capacitance		-	45	60	pF
C_{rss}	Feedback capacitance		-	16	25	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	6	10	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	45	55	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	15	25	ns
t_f	Turn-off fall time		-	20	30	ns

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	0.9	A
I_{DRM}	Pulsed reverse drain current	-	-	-	3.6	A
V_{SD}	Diode forward voltage	I_F = 0.9 A; V_{GS} = 0 V	-	0.85	1.1	V
t_{rr}	Reverse recovery time	I_F = 0.9 A; -dI_F/dt = 100 A/µs;	-	40	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	100	-	nC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 0.9 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{amb} = 25 °C	-	-	10	mJ

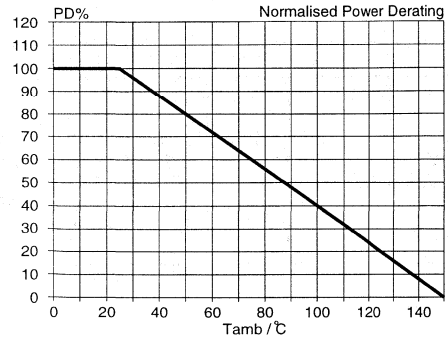


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ ^\circ C}$ = f(T_{amb})

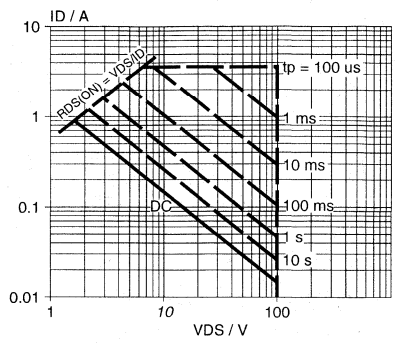


Fig.4. Safe operating area T_{amb} = 25 ˚C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

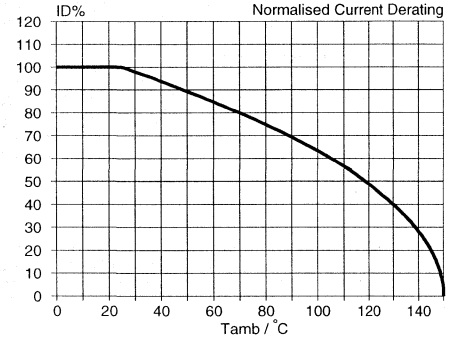


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ ^\circ C}$ = f(T_{amb}); conditions: $V_{GS} \geq 5$ V

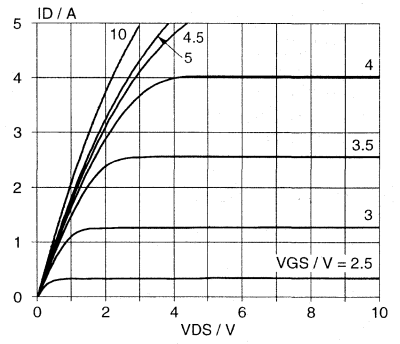


Fig.5. Typical output characteristics, T_j = 25 ˚C.
I_D = f(V_{DS}); parameter V_{GS}

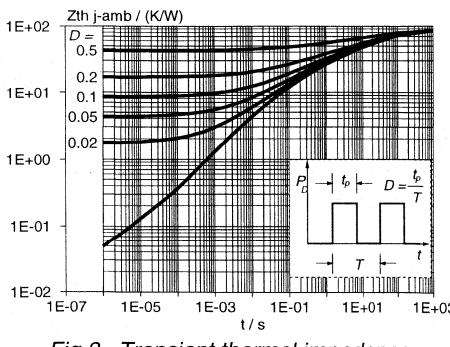


Fig.3. Transient thermal impedance.
$Z_{th\ j\text{-}amb}$ = f(t); parameter D = t_p/T

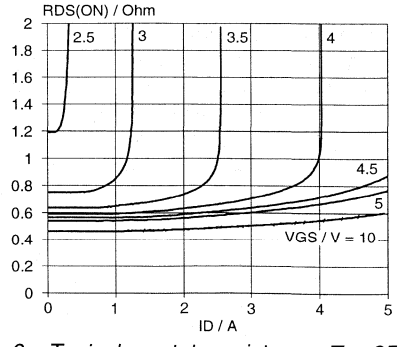


Fig.6. Typical on-state resistance, T_j = 25 ˚C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

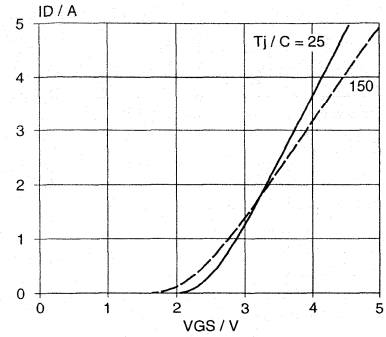


Fig.7. Typical transfer characteristics.
I_D = f(V_{GS}) ; conditions: V_{DS} = 25 V; parameter T_j

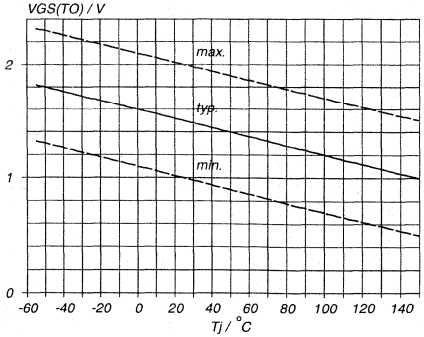


Fig.10. Gate threshold voltage.
$V_{GS(TO)}$ = f(T_j); conditions: I_D = 0.1 mA; V_{DS} = V_{GS}

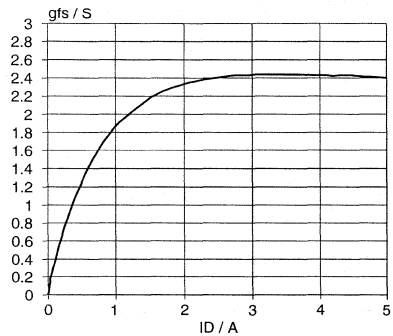


Fig.8. Typical transconductance, T_j = 25 °C.
g_{fs} = f(I_D); conditions: V_{DS} = 25 V

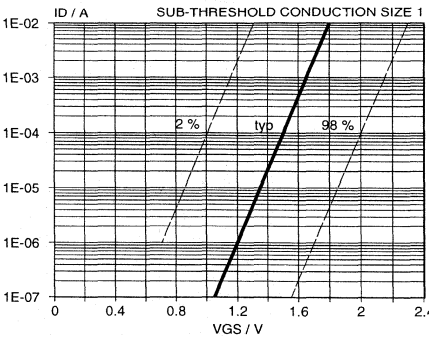


Fig.11. Sub-threshold drain current.
I_D = f(V_{GS}); conditions: T_j = 25 °C; V_{DS} = V_{GS}

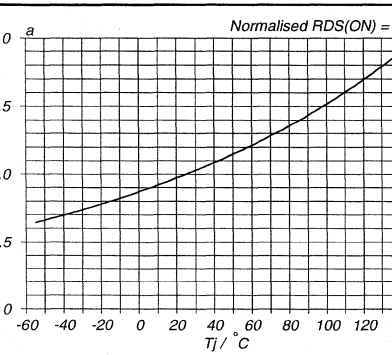


Fig.9. Normalised drain-source on-state resistance.
a = $R_{DS(ON)}$/$R_{DS(ON)25\ °C}$ = f(T_j); I_D = 0.9 A; V_{GS} = 5 V

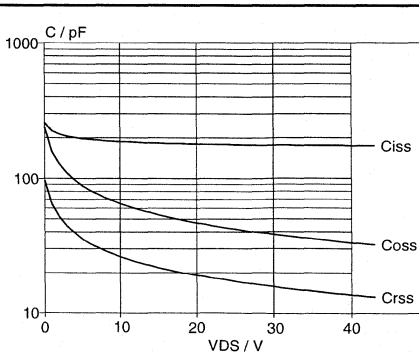


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
C = f(V_{DS}); conditions: V_{GS} = 0 V; f = 1 MHz

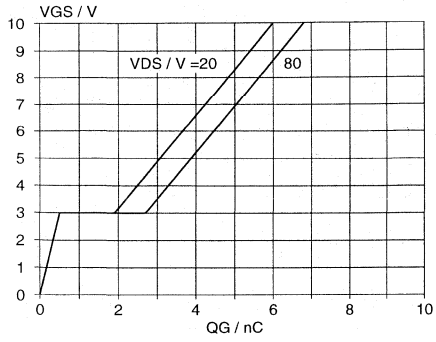


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 0.9$ A; parameter V_{DS}

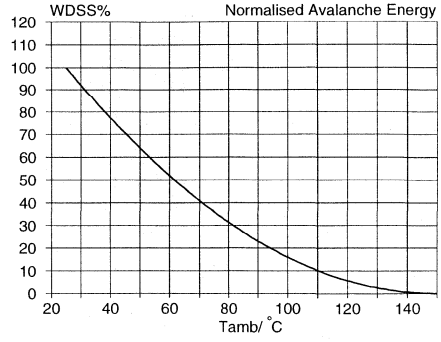


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{amb})$; conditions: $I_D = 0.9$ A

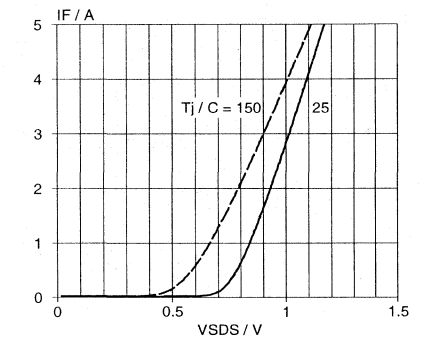


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

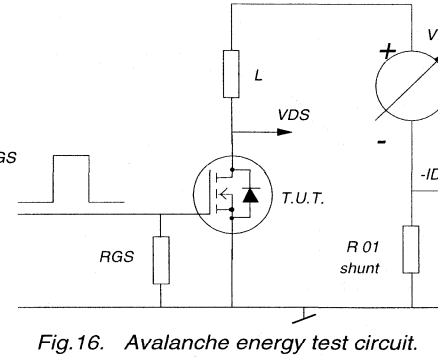


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PRINTED CIRCUIT BOARD

Dimensions in mm.

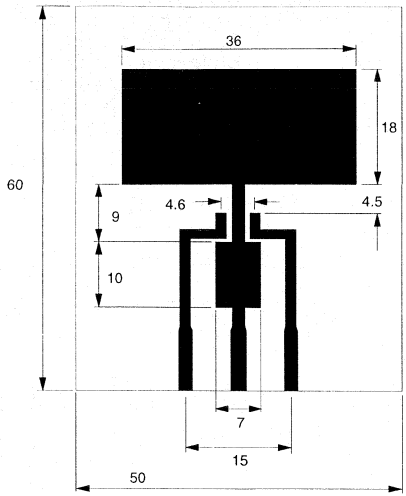


Fig.17. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).

PowerMOS transistor Logic level FET

BUK582-100A

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in automotive and general purpose switching applications.

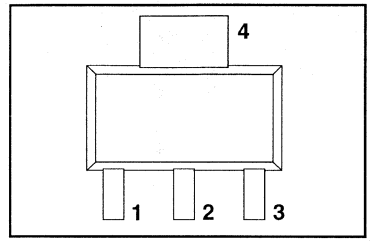
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	1.7	A
P_{tot}	Total power dissipation	1.8	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.31	Ω

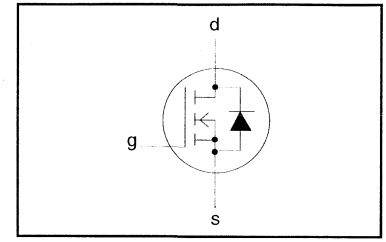
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
I_D	Drain current (DC)	T_{amb} = 25 °C	-	1.7	A
I_D	Drain current (DC)	T_{amb} = 100 °C	-	1.1	A
I_{DM}	Drain current (pulse peak value)	T_{amb} = 25 °C	-	6.8	A
P_{tot}	Total power dissipation	T_{amb} = 25 °C	-	1.8	W
T_{stg}	Storage temperature	-	- 55	150	°C
T_j	Junction Temperature	-	-	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}b}$	From junction to board[1]	Mounted on any PCB	-	40	-	K/W
$R_{th\ j\text{-}amb}$	From junction to ambient	Mounted on PCB of Fig.17	-	-	70	K/W

1 Temperature measured 1-3 mm from tab.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V;	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 1.7 A	-	0.23	0.31	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1.7 A	2	3	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	400	600	pF
C_{oss}	Output capacitance		-	90	120	pF
C_{rss}	Feedback capacitance		-	35	50	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	12	18	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	45	70	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	50	70	ns
t_f	Turn-off fall time		-	30	45	ns

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	1.7	A
I_{DRM}	Pulsed reverse drain current	-	-	-	6.8	A
V_{SD}	Diode forward voltage	I_F = 1.7 A; V_{GS} = 0 V	-	0.85	1.1	V
t_{rr}	Reverse recovery time	I_F = 1.7 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.30	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 1.7 A; V_{DD} ≤ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{amb} = 25 °C	-	-	45	mJ

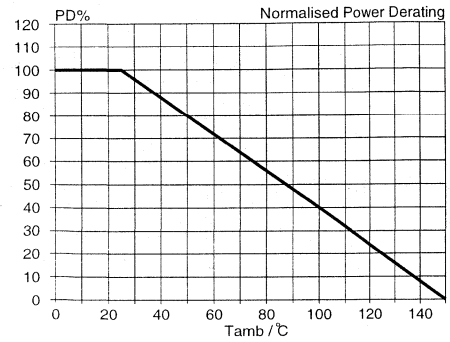


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{amb})

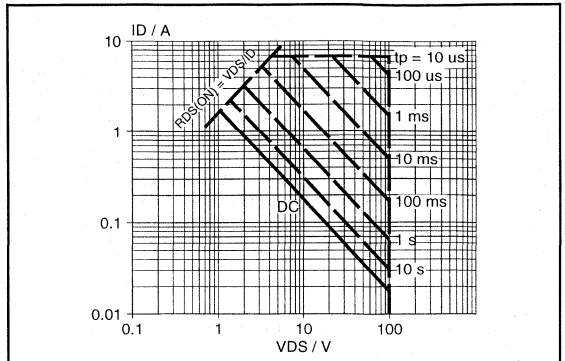


Fig.4. Safe operating area T_{amb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

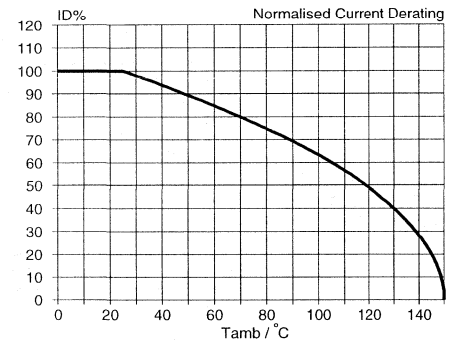


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{amb}); conditions: V_{GS} ≥ 5 V

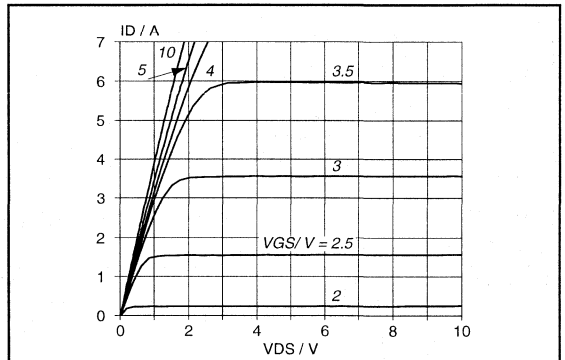


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

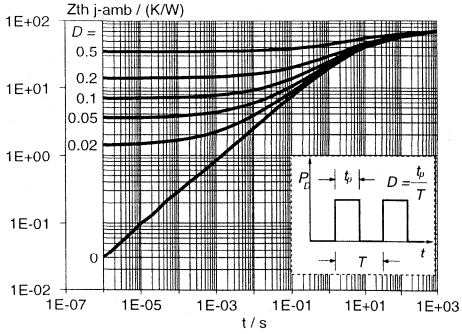


Fig.3. Transient thermal impedance.
$Z_{th\ j\text{-}amb}$ = f(t); parameter D = t_p/T

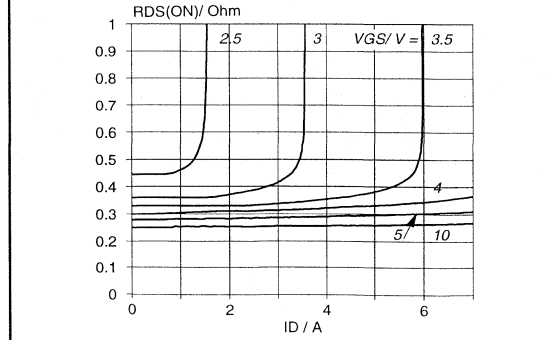


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

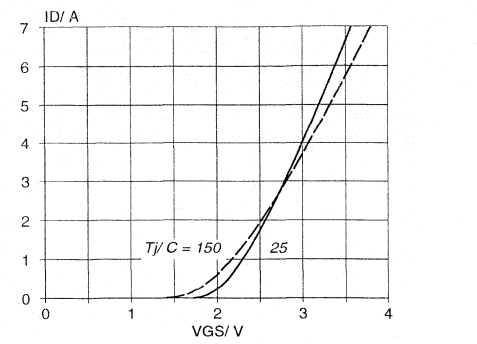


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

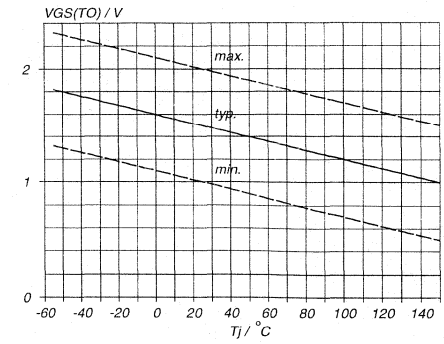


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

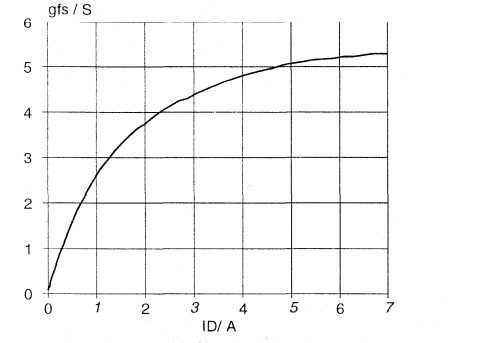


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

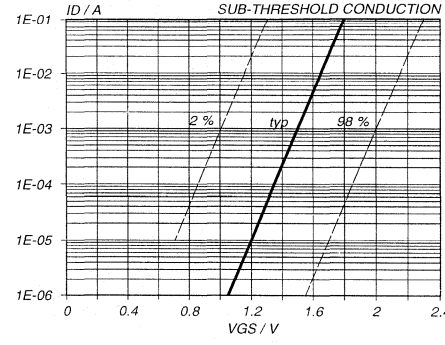


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

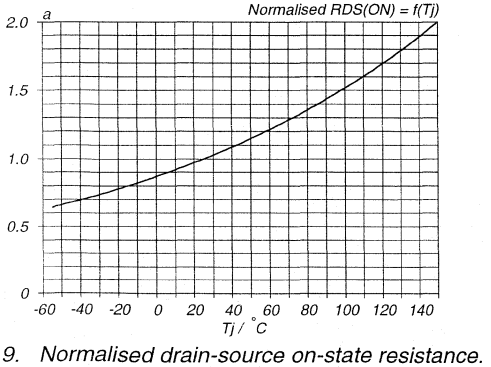


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 1.7 A; V_{GS} = 5 V

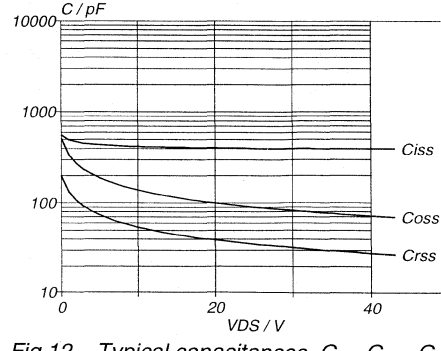


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

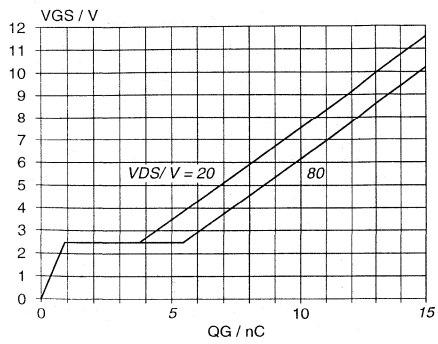


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 1.7$ A; parameter V_{DS}

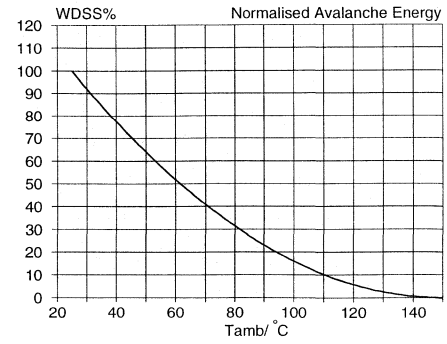


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{amb})$; conditions: $I_D = 1.7$ A

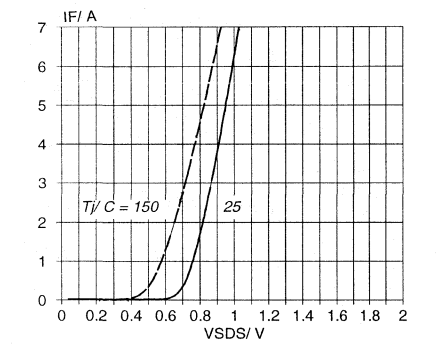


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

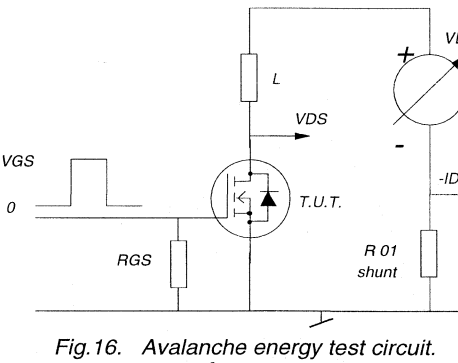


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PRINTED CIRCUIT BOARD

Dimensions in mm.

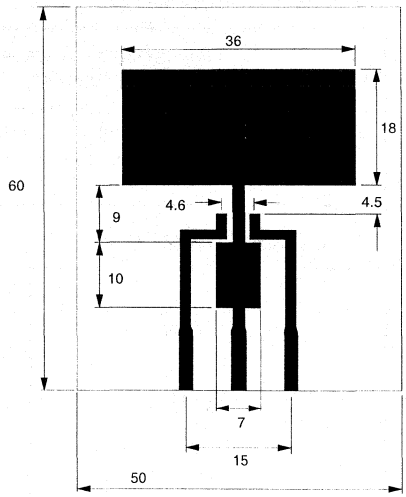


Fig.17. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).

Insulated Gate Bipolar Transistor (IGBT) — BUK854-800A

GENERAL DESCRIPTION

Fast-switching N-channel insulated gate bipolar power transistor in a plastic envelope.
The device is intended for use in motor control, DC/DC and AC/DC converters, and in general purpose high frequency switching applications.

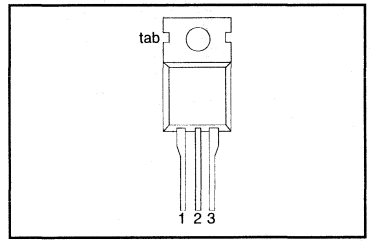
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{CE}	Collector-emitter voltage	800	V
I_C	Collector current (DC)	12	A
P_{tot}	Total power dissipation	85	W
V_{CEsat}	Collector-emitter on-state voltage	3.5	V
E_{off}	Turn-off Energy Loss	0.5	mJ

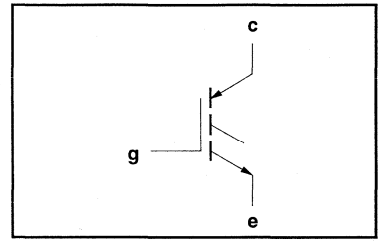
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	collector
3	emitter
tab	collector

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CE}	Collector-emitter voltage	-	-5	800	V
V_{CGR}	Collector-gate voltage	R_{GE} = 20 kΩ	-	800	V
$\pm V_{GE}$	Gate-emitter voltage	-	-	30	V
I_C	Collector current (DC)	T_{mb} = 25 °C	-	12	A
I_C	Collector current (DC)	T_{mb} = 100 °C	-	6	A
I_{CLM}	Collector Current (Clamped Inductive Load)	$T_j \leq T_{jmax.}$ $V_{CL} \leq$ 500 V	-	20	A
I_{CM}	Collector current (pulsed peak value, on-state)	$T_j \leq T_{jmax.}$	-	30	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	85	W
T_{stg}	Storage temperature	-	- 55	150	°C
T_j	Junction Temperature	-	-	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	1.47	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	In free air	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CES}$	Collector-emitter breakdown voltage	V_{GE} = 0 V; I_C = 0.25 mA	800	-	-	V
$V_{GE(TO)}$	Gate threshold voltage	V_{CE} = V_{GE}; I_C = 1 mA	3	4	5.5	V
I_{CES}	Zero gate voltage collector current	V_{CE} = 800 V; V_{GE} = 0 V; T_j = 25 °C	-	10	100	µA
I_{CES}	Zero gate voltage collector current	V_{CE} = 800 V; V_{GE} = 0 V; T_j =125 °C	-	0.1	1	mA
I_{ECS}	Reverse collector current	V_{CE} = -5 V; V_{GE} = 0 V	-	0.1	5	mA
I_{GES}	Gate emitter leakage current	V_{GE} = ±30 V; V_{CE} = 0 V	-	10	100	nA
V_{CEsat}	Collector-emitter saturation voltage	V_{GE} = 15 V; I_C = 6 A	-	2.4	3.5	V
		V_{GE} = 15 V; I_C = 12 A	-	3.1	-	V

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fe}	Forward transconductance	V_{CE} = 15 V; I_C = 3 A	1.5	4	-	S
C_{ies}	Input capacitance	V_{GE} = 0 V; V_{CE} = 25 V; f = 1 MHz	-	400	750	pF
C_{oes}	Output capacitance		-	45	80	pF
C_{res}	Feedback capacitance		-	15	40	pF
$t_{d\,on}$	Turn-on delay time	I_C = 6 A; V_{CC} = 500 V;	-	20	-	ns
t_r	Turn-on rise time	V_{GE} = 15 V; R_G = 25Ω;	-	30	-	ns
E_{on}	Turn-on Energy Loss	T_j = 25°C;	-	0.25	-	mJ
$t_{d\,off}$	Turn-off delay time	Inductive Load	-	170	270	ns
t_f	Turn-off fall time	Energy Losses include all 'tail'	-	200	400	ns
E_{off}	Turn-off Energy Loss	losses	-	0.25	0.5	mJ
$t_{d\,on}$	Turn-on delay time	I_C = 6 A; V_{CC} = 500 V;	-	20	-	ns
t_r	Turn-on rise time	V_{GE} = 15 V; R_G = 25Ω;	-	30	-	ns
E_{on}	Turn-on Energy Loss	T_j = 125°C;	-	0.25	-	mJ
$t_{d\,off}$	Turn-off delay time	Inductive Load	-	200	350	ns
t_f	Turn-off fall time	Energy Losses include all 'tail'	-	400	800	ns
E_{off}	Turn-off Energy Loss	losses	-	0.5	1	mJ

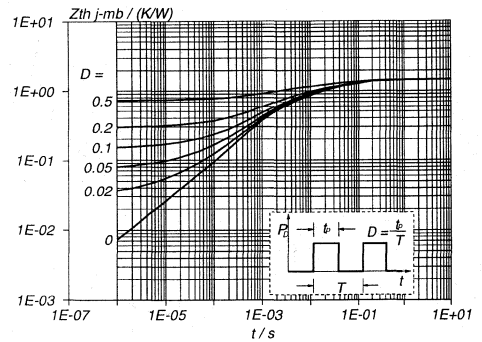


Fig.1. Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$; *parameter* $D = t_p/T$

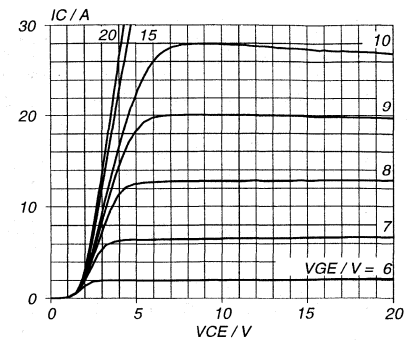


Fig.4. Typical output characteristics, T_j=25 ˚C. $I_C=f(V_{CE})$; *parameter* V_{GE}

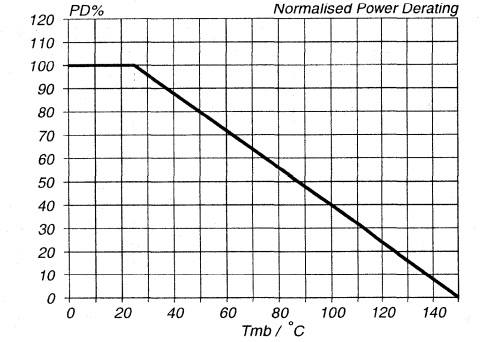


Fig.2. Normalised power dissipation. PD% = 100.$P_D/P_{D\ 25°C}$ = f(T_{mb})

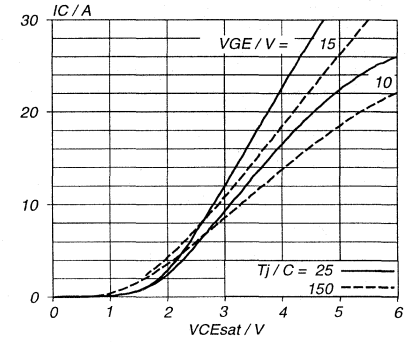


Fig.5. Typical on-state characteristics $I_C=f(V_{CE})$; *parameters* T_j, V_{GE}

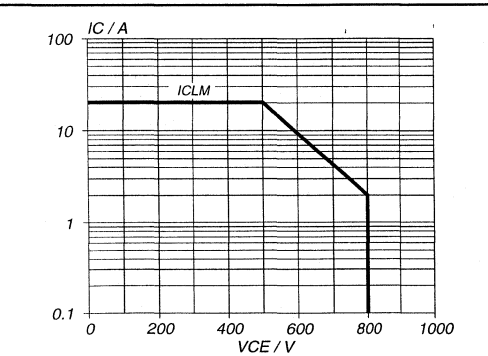


Fig.3. Turn-off Safe Operating Area conditions: $T_j \leq T_{jmax.}$; $R_G = 50\ \Omega$

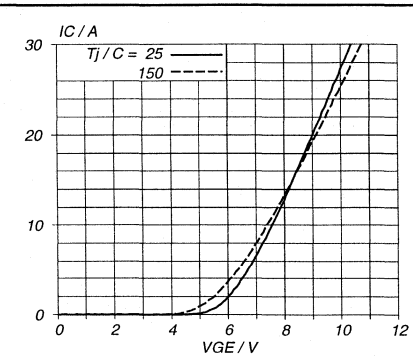


Fig.6. Typical transfer characteristics $I_C=f(V_{GE})$; *conditions:* V_{CE}=15 V; *parameter* T_j

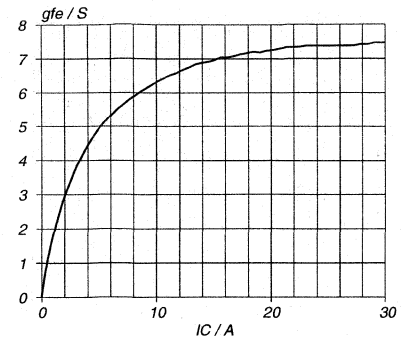


Fig.7. Typical transconductance, T_j = 25 °C. $g_{fe} = f(I_C)$; conditions: V_{CE} = 15 V

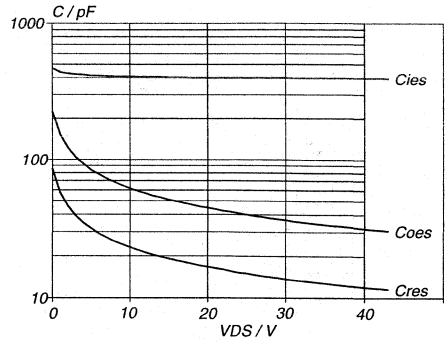


Fig.10. Typical capacitances, C_{ies}, C_{oes}, C_{res}. $C = f(V_{CE})$; conditions: V_{GE} = 0 V; f = 1MHz.

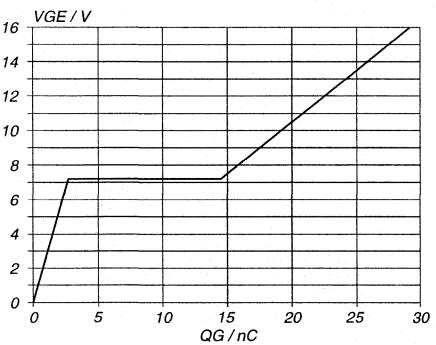


Fig.8. Typical turn-on gate-charge characteristics. $V_{GE} = f(Q_G)$; conditions: I_C = 6 A; V_{CE} = 500 V

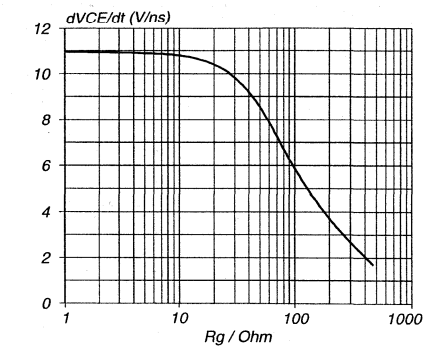


Fig.11. Typical turn-off dV_{CE}/dt vs. R_G conditions: I_C = 6 A; V_{CL} = 500 V; T_j = 125 °C

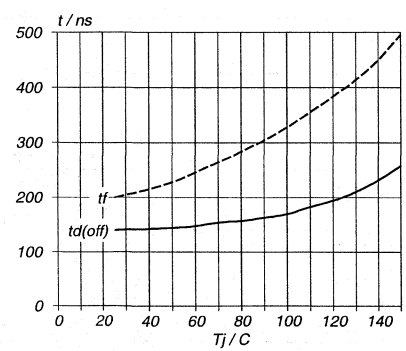


Fig.9. Typical Switching Times vs. T_j conditions: I_C = 6 A; V_{CL} = 500 V; R_G = 25 Ω

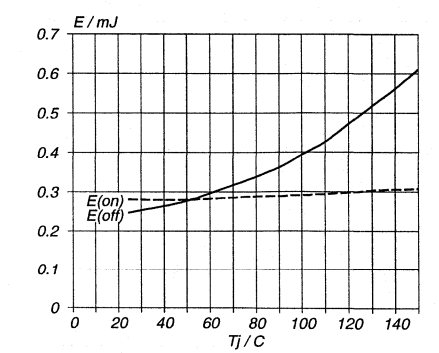


Fig.12. Typical Switching losses vs. T_j conditions: I_C = 6 A; V_{CL} = 500 V; R_G = 25 Ω

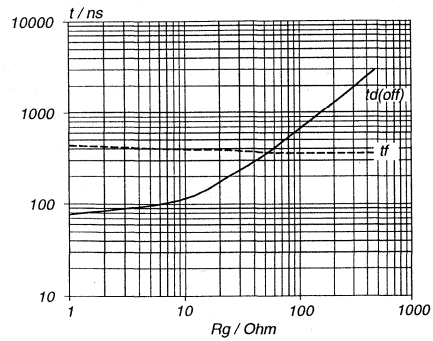


Fig.13. Typical Switching Times vs. R_G conditions: I_C = 6 A; V_{CL} = 500 V; T_j = 125 °C

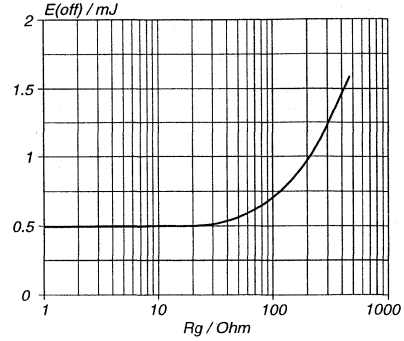


Fig.16. Typical Energy loss at turn-off vs. R_G conditions: I_C = 6 A; V_{CL} = 500 V; T_j = 125 °C

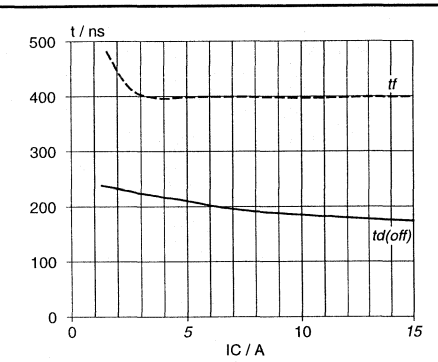


Fig.14. Typical Switching Times vs. I_C conditions: V_{CL} = 500 V; R_G = 25 Ω; T_j = 125°C

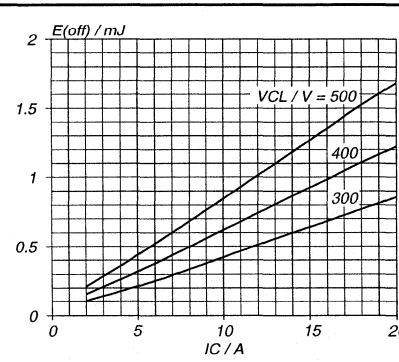


Fig.17. Typical Energy loss at turn-off vs. I_C conditions: V_{CL} = 500 V; R_G = 25 Ω; T_j = 125°C; parameter V_{CL}

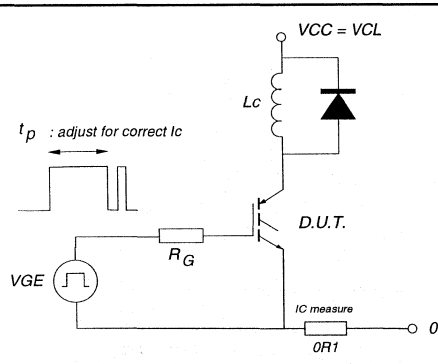


Fig.15. Test circuit for inductive load switching times.

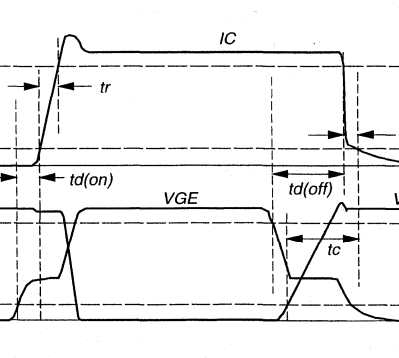


Fig.18. Inductive Load Switching Times definitions.

Insulated Gate Bipolar Transistor Protected Logic-Level IGBT

BUK856-400 IZ

GENERAL DESCRIPTION

Protected N-channel logic-level insulated gate bipolar power transistor in a plastic envelope, intended for automotive ignition applications. The device has built-in zener diodes providing active collector voltage clamping and ESD protection up to 2 kV.

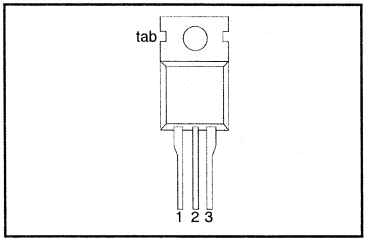
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{(CL)CER}$	Collector-emitter clamp voltage	350	400	500	V
V_{CEsat}	Collector-emitter on-state voltage			2.2	V
I_C	Collector current (DC)			20	A
P_{tot}	Total power dissipation			100	W
E_{CERS}	Clamped energy dissipation			300	mJ

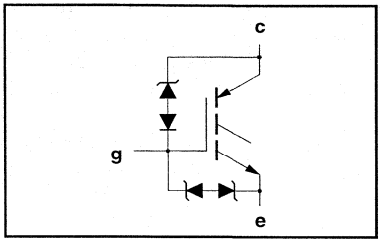
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	collector
3	emitter
tab	collector

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CE}	Collecter-emitter voltage	$t_p \leq 500\ \mu s$	-	500	V
V_{CE}	Collector-emitter voltage	Continuous	-20	50	V
$\pm V_{GE}$	Gate-emitter voltage	-	-	12	V
I_C	Collector current (DC)	$T_{mb} = 100\ ^\circ C$	-	10	A
I_C	Collector current (DC)	$T_{mb} = 25\ ^\circ C$	-	20	A
I_{CM}	Collector current (pulsed peak value, on-state)	$T_{mb} = 25\ ^\circ C$; $t_p \leq 10$ ms; $V_{CE} \leq 15$ V	-	25	A
I_{CLM}	Collector current (clamped inductive load)	$1\ k\Omega \leq R_G \leq 10\ k\Omega$	-	10	A
E_{CERS}	Clamped turn-off energy (non-repetitive)	$T_{mb} = 25\ ^\circ C$; $I_C = 10$ A; $R_G = 1\ k\Omega$; see Figs. 23,24	-	300	mJ
E_{CERR} [1]	Clamped turn-off energy (repetitive)	$T_{mb} = 100\ ^\circ C$; $I_C = 8$ A; $R_G = 1\ k\Omega$; f = 50 Hz	-	125	mJ
E_{ECR} [1]	Reverse avalanche energy (repetitive)	$I_E = 1$ A; f = 50 Hz	-	5	mJ
P_{tot}	Total power dissipation	$T_{mb} = 25\ ^\circ C$	-	125	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Operating Junction Temperature	-	-40	150	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model (100 pF, 1.5 kΩ)	-	2	kV

1 This applies to short-term operation in ignition circuits with open-secondary ignition coil.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Junction to mounting base		-	1.0	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	In free air	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CG}$	Collector-gate zener breakdown voltage	2 mA ≤ $-I_G$ ≤ 5 mA; -40 ≤ T_j ≤150°C	350	400	500	V
$V_{(BR)EC}$	Reverse collector-emitter breakdown voltage	I_E = 10 mA	20	30	50	V
$\pm V_{(BR)GES}$	Gate-emitter breakdown voltage	I_G = ± 1 mA	12	16	20	V
$V_{GE(TO)}$	Gate threshold voltage	V_{CE} = V_{GE}; I_C = 1 mA	1	1.5	2	V
$V_{GE(TO)}$	Gate threshold voltage	V_{CE} = V_{GE}; I_C = 1 mA; -40 ≤ T_j ≤150°C	0.6	-	2.4	V
I_{CES}	Zero gate voltage collector current	V_{CE} = 50 V; V_{GE} = 0 V; T_j = 25 °C	-	0.01	10	µA
I_{CES}	Zero gate voltage collector current	T_j = 125 °C	-	0.01	1	mA
I_{EC}	Reverse collector current	V_{CE} = -20 V	-	0.2	5	mA
I_{EC}	Reverse collector current	V_{CE} = -20 V; T_j = 125°C	-	2	20	mA
I_{GES}	Gate emitter leakage current	V_{GE} = ±6 V	-	0.1	1	µA
		T_j = 150°C	-	5	100	µA
V_{CEsat}	Collector-emitter on-state voltage	V_{GE} = 4.5 V; I_C = 8 A	-	1.2	2.2	V
		V_{GE} = 3.5 V; I_C = 6 A; -40 ≤ T_j ≤150°C	-	1.2	2.2	V

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)CER}$	Collector-emitter clamp voltage (peak value)	R_G = 1 kΩ; I_C = 10 A; -40 ≤ T_j ≤150°C; Inductive load; see Figs. 23,24	350	400	500	V
g_{fe}	Forward transconductance	V_{CE} = 15 V; I_C = 4 A	5.5	15	20	S
C_{ies}	Input capacitance	V_{GE} = 0 V; V_{CE} = 25 V; f = 1 MHz	-	940	1200	pF
C_{oes}	Output capacitance		-	95	130	pF
C_{res}	Feedback capacitance		-	30	50	pF
$t_{d\ off}$	Turn-off delay time	I_C = 8 A; V_{CL} = 300 V; R_G = 1 kΩ;	-	13	18	µs
t_f	Fall time	V_{GE} = 5 V; T_j = 125°C;	-	6	10	µs
t_c	Crossover Time	Inductive load; see Figs. 20,21	-	12	-	µs
E_{off}	Turn-off Energy loss		-	13	-	mJ

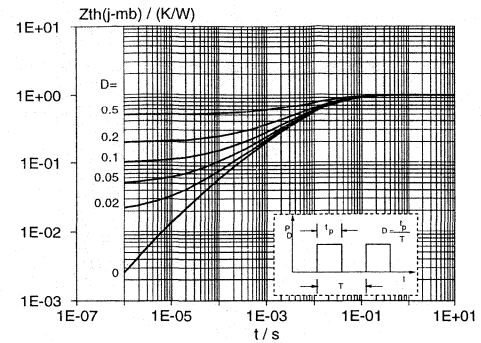


Fig.1. Transient thermal impedance
$Z_{th\ j\text{-}mb} = f(t)$; *parameter* $D = t_p/T$

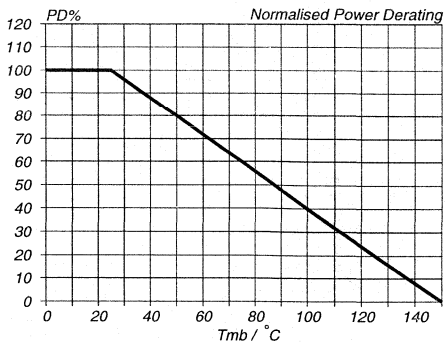


Fig.4. Normalised power dissipation.
$PD\% = 100.P_D/P_{D\ 25°C} = f(T_{mb})$

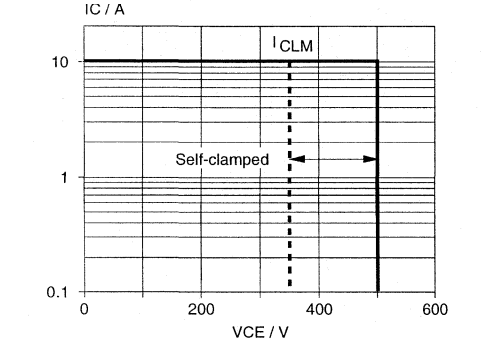


Fig.2. Turn-off Safe Operating Area
conditions: $T_j \leq T_{jmax.}$; $R_G \geq 1\ k\Omega$

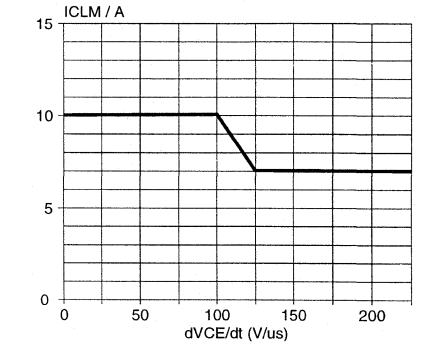


Fig.5. Derating of I_{CLM} *with turn-off* dV_{CE}/dt
conditions: $V_{CE} \leq 500\ V$; $T_j \leq T_{jmax.}$

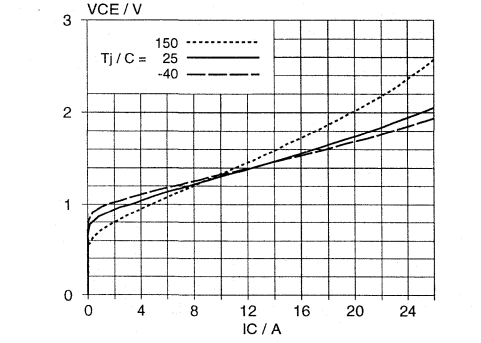


Fig.3. Typical On-state Voltage
$V_{CEsat} = f(I_C)$; *parameter* T_j; *conditions:* $V_{GE} = 3.5\ V$

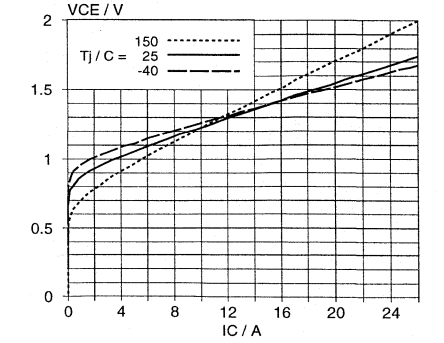


Fig.6. Typical On-state Voltage
$V_{CEsat} = f(I_C)$; *parameter* T_j; *conditions:* $V_{GE} = 5\ V$

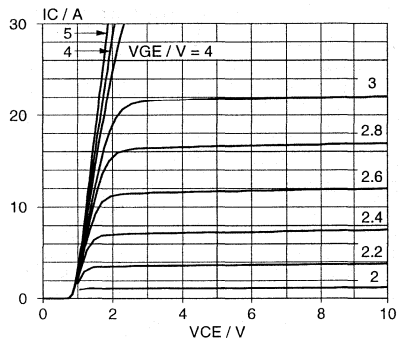


Fig.7. Typical Output Characteristics
$I_C = f(V_{CE})$; parameter V_{GE}; conditions: $T_j = 25°C$

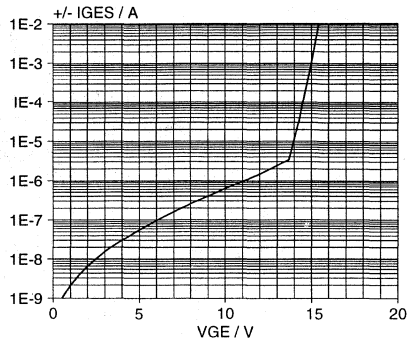


Fig.10. Typical gate-emitter charcteristics
$I_{GES} = f(V_{GE})$; conditions: $V_{CE} = 0$ V; $T_j = 25°C$

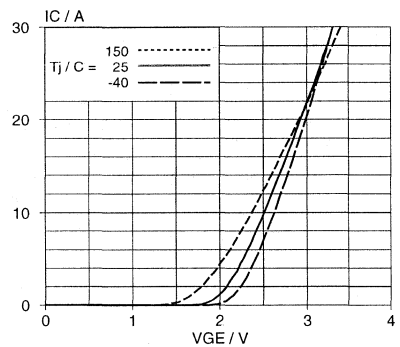


Fig.8. Typical Transfer Characteristics
$I_C = f(V_{GE})$, parameter T_j; conditions: $V_{CE} = 10$ V

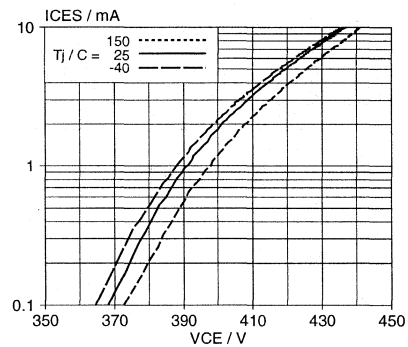


Fig.11. Typical collector clamp characteristics
$I_{CES} = f(V_{CE})$; parameter T_j; conditions: $V_{GE} = 0$ V

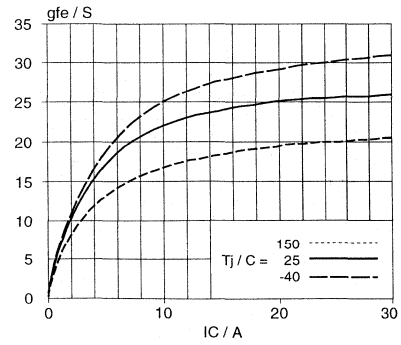


Fig.9. Typical Forward Transconductance
$g_{fe} = f(I_C)$; parameter T_j; conditions: $V_{CE} = 10$ V

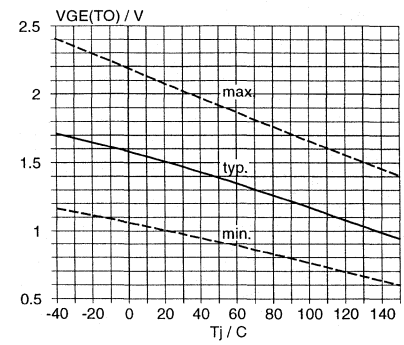


Fig.12. Gate Threshold Voltage
$V_{GE(TO)} = f(T_j)$; conditions: $I_C = 1$ mA; $V_{CE} = V_{GE}$

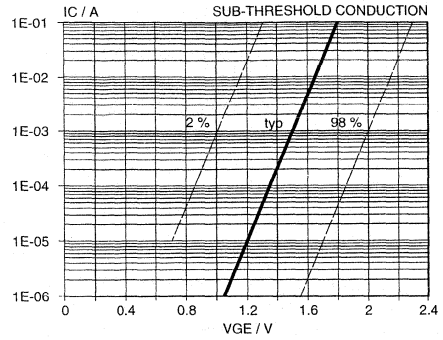


Fig.13. Sub-threshold collector current $I_C = f(V_{GE})$; $T_j = 25°C$; $V_{CE} = V_{GE}$

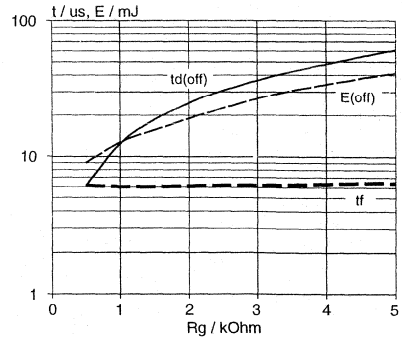


Fig.16. Typical Switching Characteristics vs. R_G conditions: T_j=125 °C; I_C=8 A; V_{CL}=300 V; L_C=5 mH.

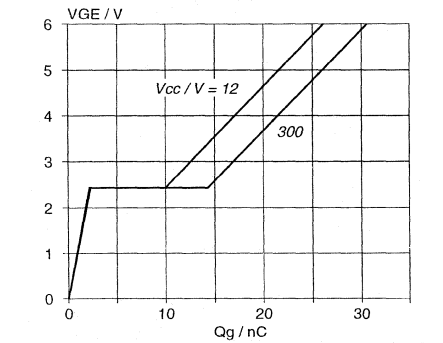


Fig.14. Typical Turn-on Gate Charge Characteristics $V_{GE} = f(Q_G)$; conditions: I_C = 8 A.

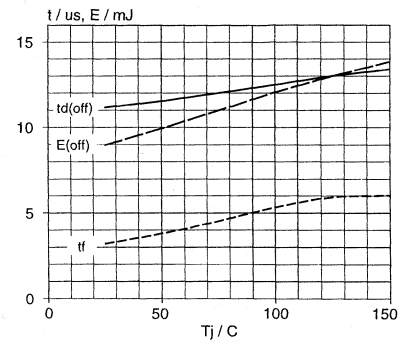


Fig.17. Typical Switching Characteristics vs. T_j conditions: I_C=8 A; V_{CL}=300 V; R_G=1 kΩ; L_C=5 mH.

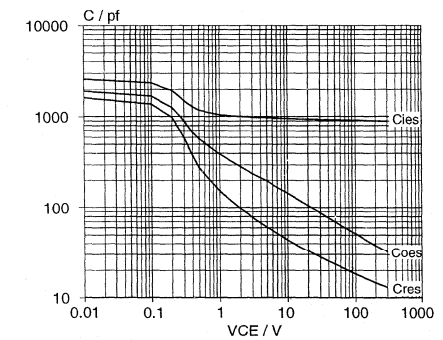


Fig.15. Typical Capacitances C_{ies}, C_{oes}, C_{res} $C = f(V_{CE})$; conditions: V_{GE} = 0 V; f = 1 MHz

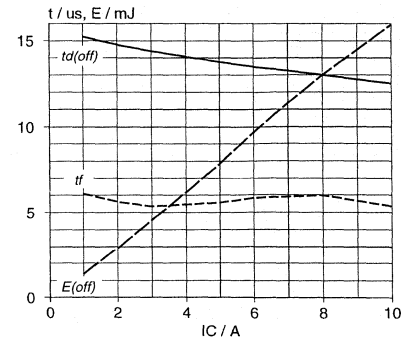


Fig.18. Typical Switching Characteristics vs. I_C conditions: T_j=125 °C V_{CL}=300 V; R_G=1 kΩ; L_C=5 mH.

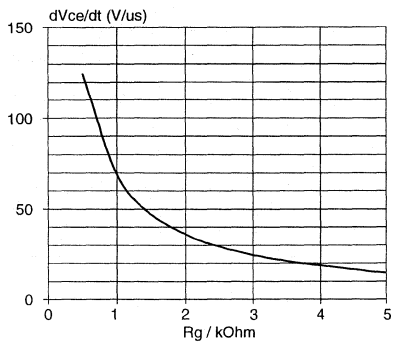


Fig.19. Typical Turn-off dV_{CE}/dt vs. R_G conditions: T_j=125 °C; I_C=8 A; V_{CL}=300 V; L_C=5 mH.

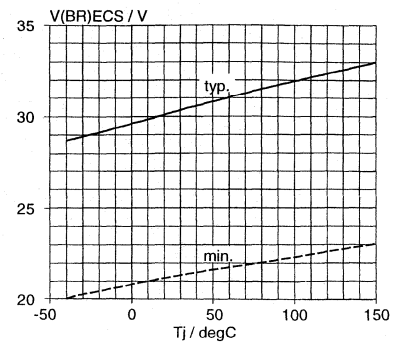


Fig.22. Reverse Breakdown Voltage $V_{(BR)ECS} = f(T_j)$; conditions: I_{EC} = 50 mA

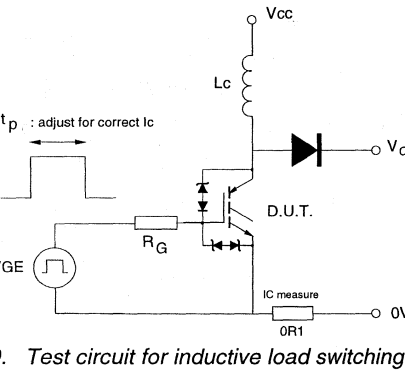


Fig.20. Test circuit for inductive load switching times.

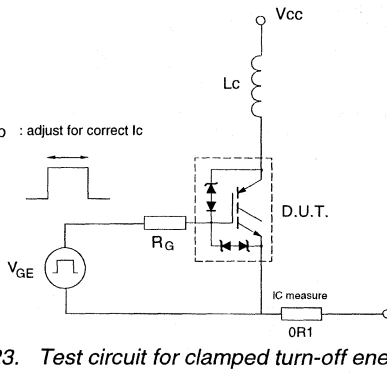


Fig.23. Test circuit for clamped turn-off energy test

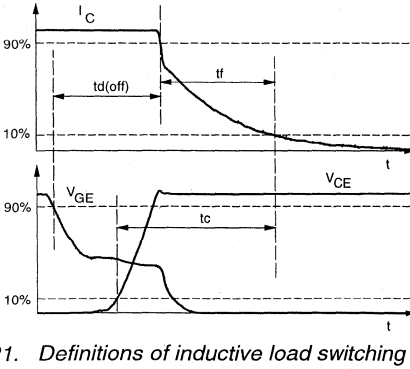


Fig.21. Definitions of inductive load switching times.

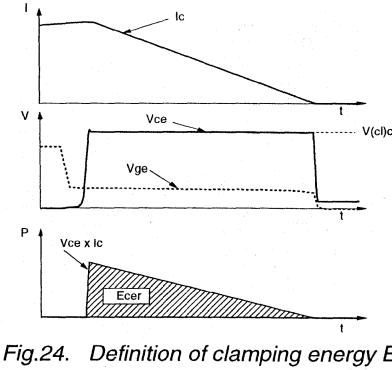


Fig.24. Definition of clamping energy E_{CER}

Insulated Gate Bipolar Transistor (IGBT) — BUK856-800A

GENERAL DESCRIPTION

Fast-switching N-channel insulated gate bipolar power transistor in a plastic envelope.
The device is intended for use in motor control, DC/DC and AC/DC converters, and in general purpose high frequency switching applications.

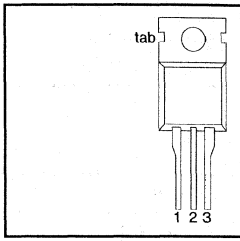
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{CE}	Collector-emitter voltage	800	V
I_C	Collector current (DC)	24	A
P_{tot}	Total power dissipation	125	W
V_{CEsat}	Collector-emitter on-state voltage	3.5	V
E_{off}	Turn-off energy Loss	1.0	mJ

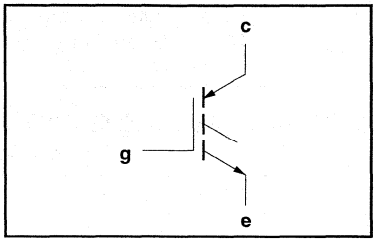
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	collector
3	emitter
tab	collector

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CE}	Collector-emitter voltage	-	-5	800	V
V_{CGR}	Collector-gate voltage	R_{GE} = 20 kΩ	-	800	V
$\pm V_{GE}$	Gate-emitter voltage	-	-	30	V
I_C	Collector current (DC)	T_{mb} = 25 °C	-	24	A
I_C	Collector current (DC)	T_{mb} = 100 °C	-	12	A
I_{CLM}	Collector Current (Clamped Inductive Load)	$T_j \leq T_{jmax.}$ $V_{CL} \leq 500$ V	-	40	A
I_{CM}	Collector current (pulsed peak value, on-state)	$T_j \leq T_{jmax.}$	-	50	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}	Storage temperature	-	- 55	150	°C
T_j	Junction Temperature	-	-	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	1.0	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	In free air	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CES}$	Collector-emitter breakdown voltage	V_{GE} = 0 V; I_C = 0.25 mA	800	-	-	V
$V_{GE(TO)}$	Gate threshold voltage	V_{CE} = V_{GE}; I_C = 1 mA	3	4	5.5	V
I_{CES}	Zero gate voltage collector current	V_{CE} = 800 V; V_{GE} = 0 V; T_j = 25 °C	-	10	200	µA
I_{CES}	Zero gate voltage collector current	V_{CE} = 800 V; V_{GE} = 0 V; T_j =125 °C	-	0.2	1	mA
I_{ECS}	Reverse collector current	V_{CE} = -5 V; V_{GE} = 0 V	-	0.1	5	mA
I_{GES}	Gate emitter leakage current	V_{GE} = ±30 V; V_{CE} = 0 V	-	10	100	nA
V_{CEsat}	Collector-emitter saturation voltage	V_{GE} = 15 V; I_C = 12 A	-	2.4	3.5	V
		V_{GE} = 15 V; I_C = 24 A	-	3.1	-	V

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fe}	Forward transconductance	V_{CE} = 15 V; I_C = 6 A	3	7	-	S
C_{ies}	Input capacitance	V_{GE} = 0 V; V_{CE} = 25 V; f = 1 MHz	-	900	1250	pF
C_{oes}	Output capacitance		-	85	120	pF
C_{res}	Feedback capacitance		-	30	50	pF
$t_{d\,on}$	Turn-on delay time	I_C = 12 A; V_{CC} = 500 V;	-	25	-	ns
t_r	Turn-on rise time	V_{GE} = 15 V; R_G = 25Ω;	-	45	-	ns
E_{on}	Turn-on Energy Loss	T_j = 25°C;	-	0.6	-	mJ
$t_{d\,off}$	Turn-off delay time	Inductive Load	-	230	350	ns
t_f	Turn-off fall time	Energy Losses include all 'tail'	-	200	400	ns
E_{off}	Turn-off Energy Loss	losses	-	0.5	1	mJ
$t_{d\,on}$	Turn-on delay time	I_C = 12 A; V_{CC} = 500 V;	-	25	-	ns
t_r	Turn-on rise time	V_{GE} = 15 V; R_G = 25Ω;	-	45	-	ns
E_{on}	Turn-on Energy Loss	T_j = 125°C;	-	0.6	-	mJ
$t_{d\,off}$	Turn-off delay time	Inductive Load	-	300	450	ns
t_f	Turn-off fall time	Energy Losses include all 'tail'	-	400	800	ns
E_{off}	Turn-off Energy Loss	losses	-	1	2	mJ

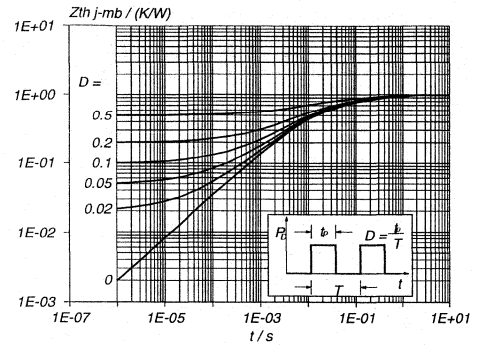


Fig.1. Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

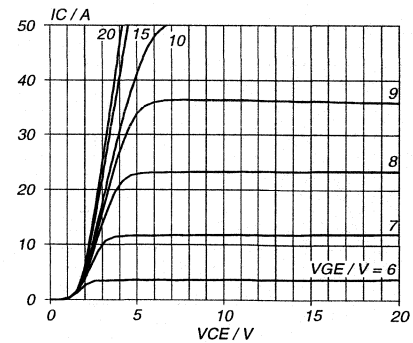


Fig.4. Typical output characteristics, T_j=25 °C. $I_C=f(V_{CE})$; parameter V_{GE}

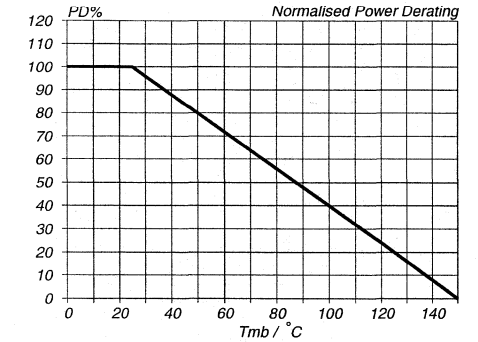


Fig.2. Normalised power dissipation. PD% = 100.$P_D/P_{D\ 25°C}$ = f(T_{mb})

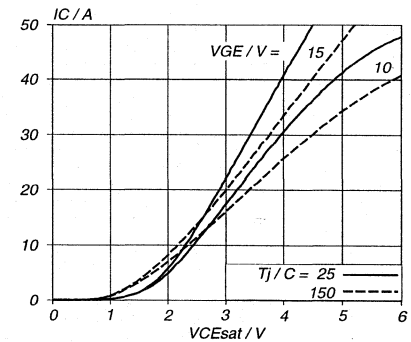


Fig.5. Typical on-state characteristics $I_C=f(V_{CE})$; parameters T_j, V_{GE}

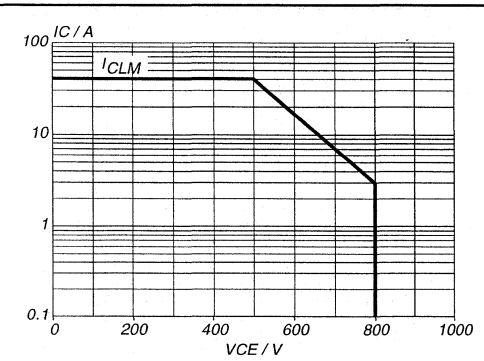


Fig.3. Turn-off Safe Operating Area conditions: $T_j \leq T_{jmax.}$; $R_G = 50\ \Omega$

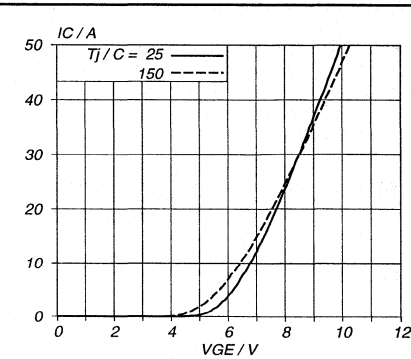


Fig.6. Typical transfer characteristics $I_C=f(V_{GE})$; conditions: V_{CE}=15 V; parameter T_j

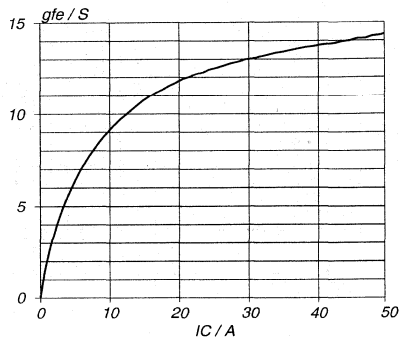


Fig.7. Typical transconductance, T_j = 25 °C. $g_{fe} = f(I_C)$; conditions: V_{CE} = 15 V

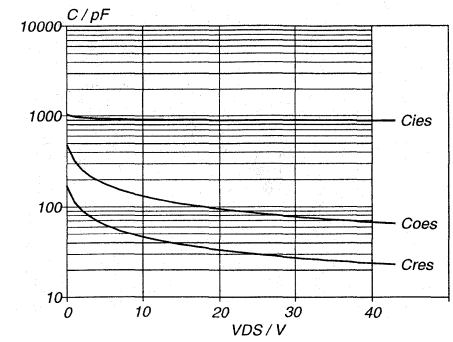


Fig.10. Typical capacitances, C_{ies}, C_{oes}, C_{res}. $C = f(V_{CE})$; conditions: V_{GE} = 0 V; f = 1MHz.

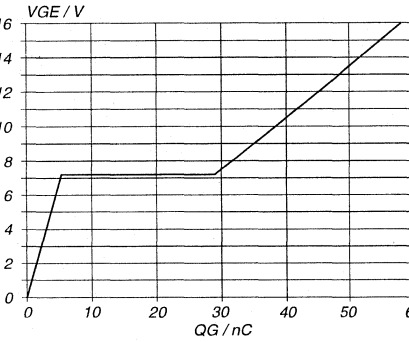


Fig.8. Typical turn-on gate-charge characteristics. $V_{GE} = f(Q_G)$; conditions: I_C = 12 A; parameter V_{CE}

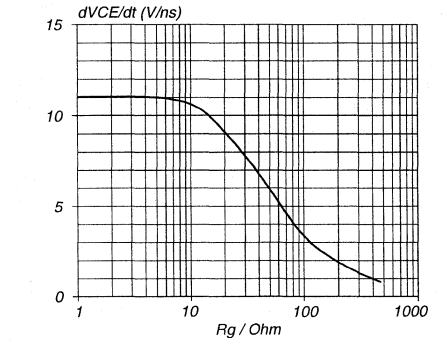


Fig.11. Typical turn-off dV_{CE}/dt vs. R_G conditions: I_C = 12 A; V_{CL} = 500 V; T_j = 125 °C

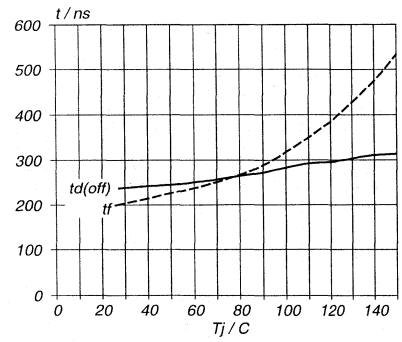


Fig.9. Typical Switching Times vs. T_j conditions: I_C = 12 A; V_{CL} = 500 V; R_G = 25 Ω

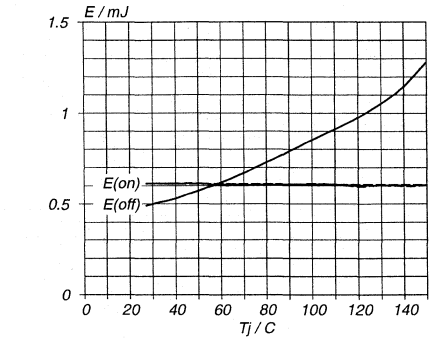


Fig.12. Typical Switching losses vs. T_j conditions: I_C = 12 A; V_{CL} = 500 V; R_G = 25 Ω

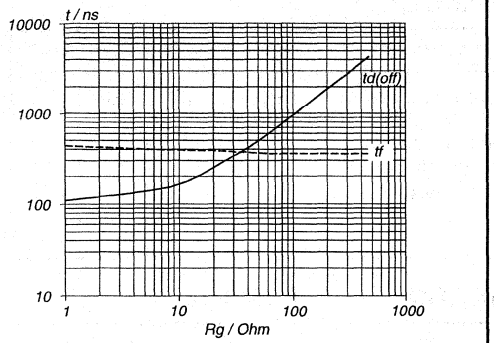


Fig.13. Typical Switching Times vs. R_G conditions: I_C = 12 A; V_{CL} = 500 V; T_j = 125 °C

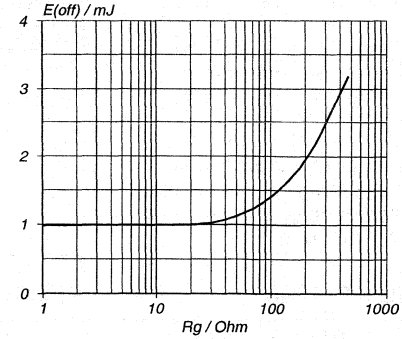


Fig.16. Typical Energy loss at turn-off vs. R_G conditions: I_C = 12 A; V_{CL} = 500 V; T_j = 125 °C

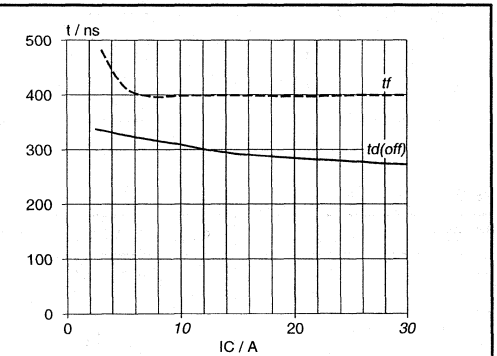


Fig.14. Typical Switching Times vs. I_C conditions: V_{CL} = 500 V; R_G = 25 Ω; T_j = 125°C

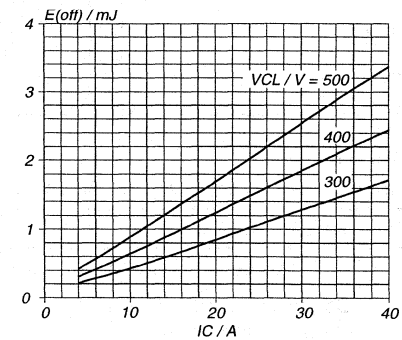


Fig.17. Typical Energy loss at turn-off vs. I_C conditions: V_{CL} = 500 V; R_G = 25 Ω; T_j = 125°C; parameter V_{CL}

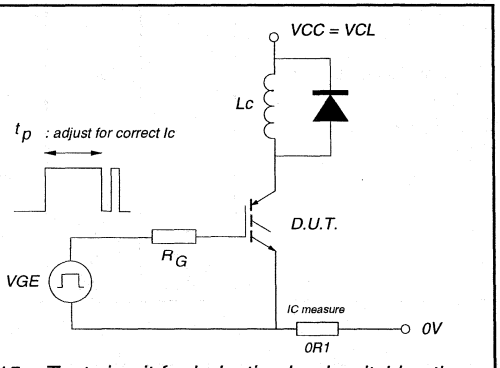


Fig.15. Test circuit for inductive load switching times.

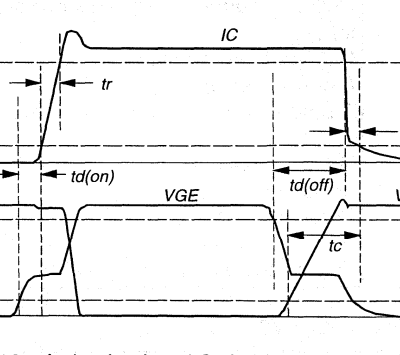


Fig.18. Inductive Load Switching Times definitions.

Insulated Gate Bipolar Transistor Protected Logic-Level IGBT

BUK866-400 IZ

GENERAL DESCRIPTION

Protected N-channel logic-level insulated gate bipolar power transistor in a plastic envelope suitable for surface mount applications. It is intended for automotive ignition applications, and has integral zener diodes providing active collector voltage clamping and ESD protection up to 2 kV.

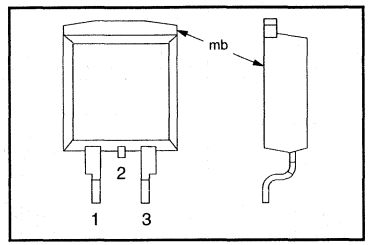
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{(CL)CER}$	Collector-emitter clamp voltage	350	400	500	V
V_{CEsat}	Collector-emitter on-state voltage			2.2	V
I_C	Collector current (DC)			20	A
P_{tot}	Total power dissipation			100	W
E_{CERS}	Clamped energy dissipation			300	mJ

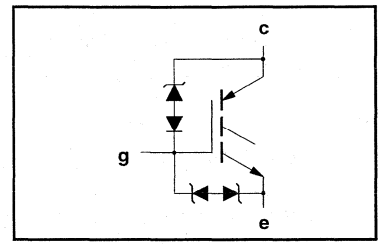
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	collector
3	emitter
tab	collector

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CE}	Collecter-emitter voltage	$t_p \leq 500$ µs	-	500	V
V_{CE}	Collector-emitter voltage	Continuous	-20	50	V
$\pm V_{GE}$	Gate-emitter voltage	-	-	12	V
I_C	Collector current (DC)	T_{mb} = 100 °C	-	10	A
I_C	Collector current (DC)	T_{mb} = 25 °C	-	20	A
I_{CM}	Collector current (pulsed peak value, on-state)	T_{mb} = 25 °C; $t_p \leq 10$ ms; $V_{CE} \leq 15$ V	-	25	A
I_{CLM}	Collector current (clamped inductive load)	1 kΩ ≤ R_G ≤ 10 kΩ	-	10	A
E_{CERS}	Clamped turn-off energy (non-repetitive)	T_{mb} = 25 °C; I_C = 10 A; R_G = 1 kΩ; see Figs. 23,24	-	300	mJ
E_{CERR}	Clamped turn-off energy (repetitive)	T_{mb} = 125 °C; I_C = 8 A; R_G = 1 kΩ; f = 50 Hz; t = 60 min.	-	125	mJ
E_{ECR}	Reverse avalanche energy (repetitive)	I_E = 1 A; f = 50 Hz	-	5	mJ
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Operating Junction Temperature	-	-40	150	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board (see Fig. 26).	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CG}$	Collector-gate zener breakdown voltage	2 mA ≤ $-I_G$ ≤ 5 mA; -40 ≤ T_j ≤150°C	350	400	500	V
$V_{(BR)EC}$	Reverse collector-emitter breakdown voltage	I_E = 10 mA	20	30	50	V
$\pm V_{(BR)GES}$	Gate-emitter breakdown voltage	I_G = ± 1 mA	12	16	20	V
$V_{GE(TO)}$	Gate threshold voltage	V_{CE} = V_{GE}; I_C = 1 mA	1	1.5	2	V
$V_{GE(TO)}$	Gate threshold voltage	V_{CE} = V_{GE}; I_C = 1 mA; -40 ≤ T_j ≤150°C	0.6	-	2.4	V
I_{CES}	Zero gate voltage collector current	V_{CE} = 50 V; V_{GE} = 0 V; T_j = 25 °C	-	0.01	10	µA
I_{CES}	Zero gate voltage collector current	T_j = 125 °C	-	0.01	1	mA
I_{EC}	Reverse collector current	V_{CE} = -20 V	-	0.2	5	mA
I_{EC}	Reverse collector current	V_{CE} = -20 V; T_j = 125°C	-	2	20	mA
I_{GES}	Gate emitter leakage current	V_{GE} = ±6 V	-	0.1	1	µA
		T_j = 150°C	-	5	100	µA
V_{CEsat}	Collector-emitter on-state voltage	V_{GE} = 4.5 V; I_C = 8 A	-	1.2	2.2	V
		V_{GE} = 3.5 V; I_C = 6 A; -40 ≤ T_j ≤150°C	-	1.2	2.2	V

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)CER}$	Collector-emitter clamp voltage (peak value)	R_G = 1 kΩ; I_C = 10 A; -40 ≤ T_j ≤150°C; Inductive load; see Figs. 23,24	350	400	500	V
g_{fe}	Forward transconductance	V_{CE} = 15 V; I_C = 4 A	5.5	15	20	S
C_{ies}	Input capacitance	V_{GE} = 0 V; V_{CE} = 25 V; f = 1 MHz	-	940	1200	pF
C_{oes}	Output capacitance		-	95	130	pF
C_{res}	Feedback capacitance		-	30	50	pF
$t_{d\ off}$	Turn-off delay time	I_C = 8 A; V_{CL} = 300 V; R_G = 1 kΩ;	-	13	18	µs
t_f	Fall time	V_{GE} = 5 V; T_j = 125°C;	-	6	10	µs
t_c	Crossover Time	Inductive load; see Figs. 20,21	-	12	-	µs
E_{off}	Turn-off Energy loss		-	13	-	mJ

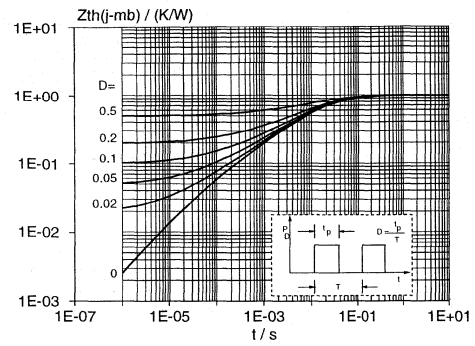


Fig.1. Transient thermal impedance
$Z_{th\ j\text{-}mb} = f(t)$; *parameter* $D = t_p/T$

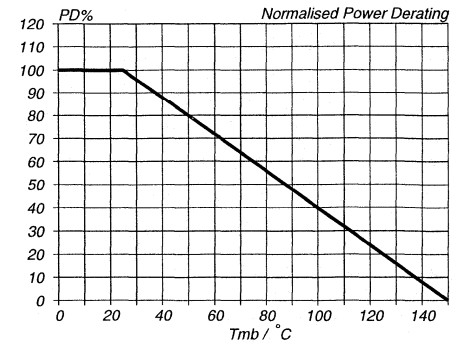


Fig.4. Normalised power dissipation.
$PD\% = 100.P_D/P_{D\ 25°C} = f(T_{mb})$

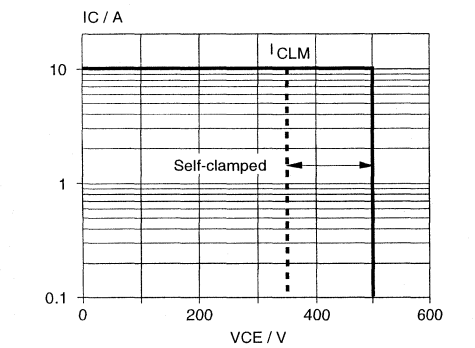


Fig.2. Turn-off Safe Operating Area
conditions: $T_j \leq T_{jmax.}$; $R_G \geq 1\ k\Omega$

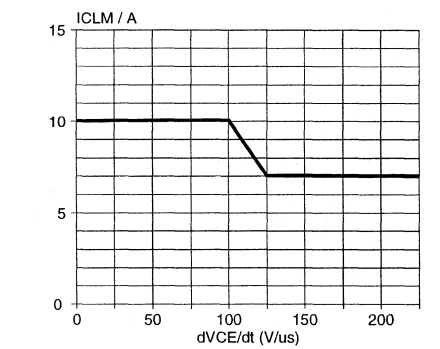


Fig.5. Derating of I_{CLM} *with turn-off* dV_{CE}/dt
conditions: $V_{CE} \leq 500\ V$; $T_j \leq T_{jmax.}$

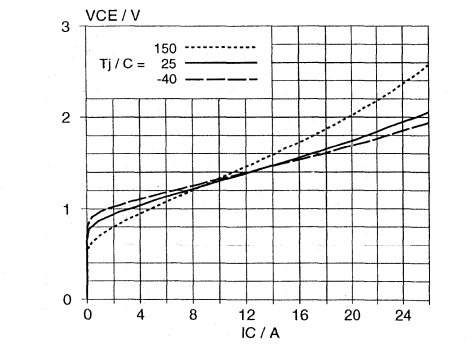


Fig.3. Typical On-state Voltage
$V_{CEsat} = f(I_C)$; *parameter* T_j; *conditions:* $V_{GE} = 3.5\ V$

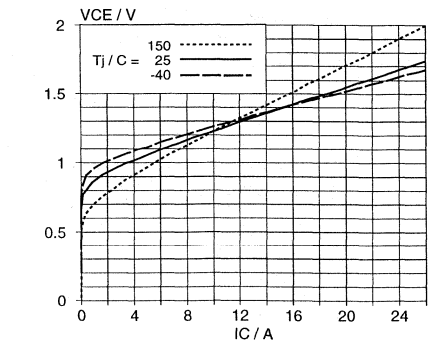


Fig.6. Typical On-state Voltage
$V_{CEsat} = f(I_C)$; *parameter* T_j; *conditions:* $V_{GE} = 5\ V$

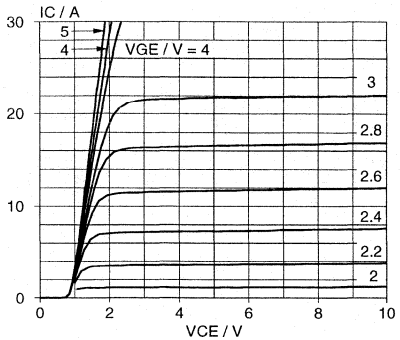


Fig.7. Typical Output Characteristics
$I_C = f(V_{CE})$; parameter V_{GE}; conditions: $T_j = 25^\circ C$

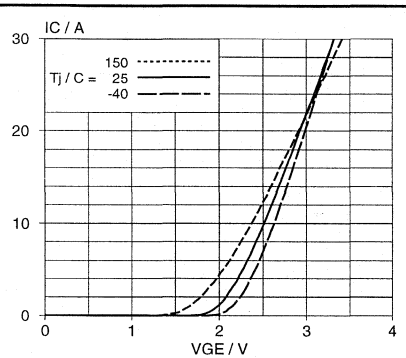


Fig.8. Typical Transfer Characteristics
$I_C = f(V_{GE})$, parameter T_j; conditions: $V_{CE} = 10$ V

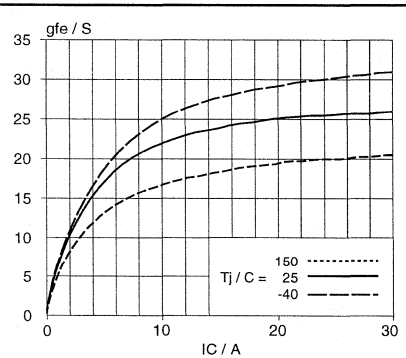


Fig.9. Typical Forward Transconductance
$g_{fe} = f(I_C)$; parameter T_j; conditions: $V_{CE} = 10$ V

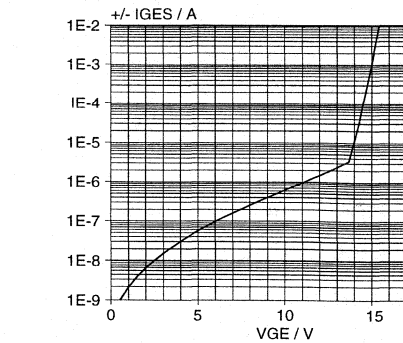


Fig.10. Typical gate-emitter charcteristics
$I_{GES} = f(V_{GE})$; conditions: $V_{CE} = 0$ V; $T_j = 25^\circ C$

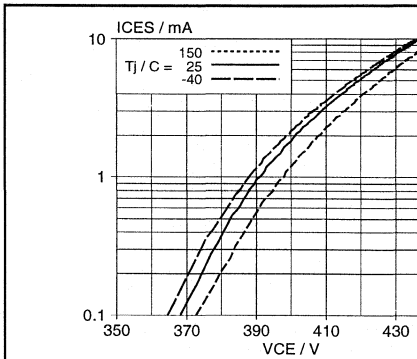


Fig.11. Typical collector clamp characteristics
$I_{CES} = f(V_{CE})$; parameter T_j; conditions: $V_{GE} = 0$ V

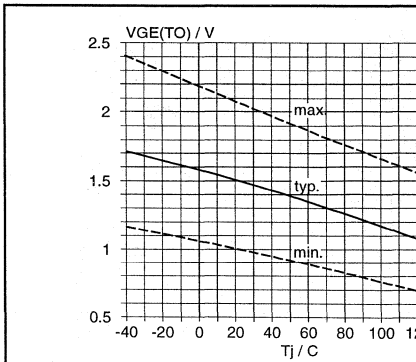


Fig.12. Gate Threshold Voltage
$V_{GE(TO)} = f(T_j)$; conditions: $I_C = 1$ mA; $V_{CE} = V_{GE}$

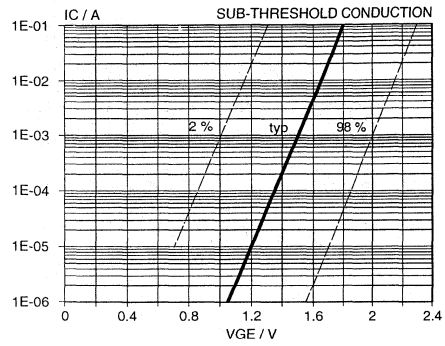


Fig.13. Sub-threshold collector current $I_C = f(V_{GE})$; $T_j = 25°C$; $V_{CE} = V_{GE}$

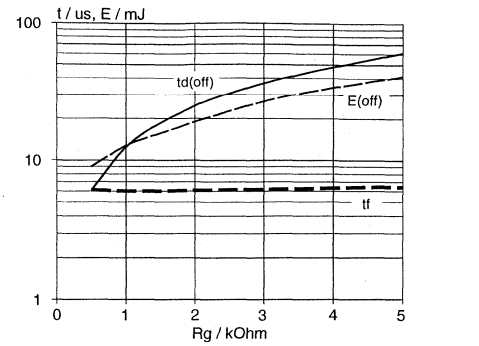


Fig.16. Typical Switching Characteristics vs. R_G conditions: T_j=125 °C; I_C=8 A; V_{CL}=300 V; L_C=5 mH.

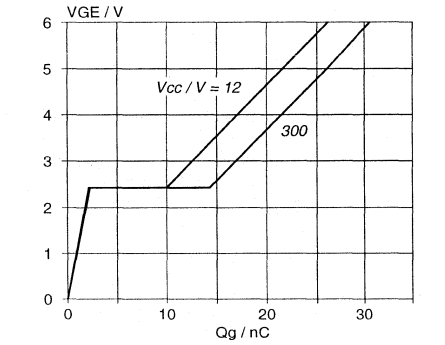


Fig.14. Typical Turn-on Gate Charge Characteristics $V_{GE} = f(Q_G)$; conditions: I_C = 8 A.

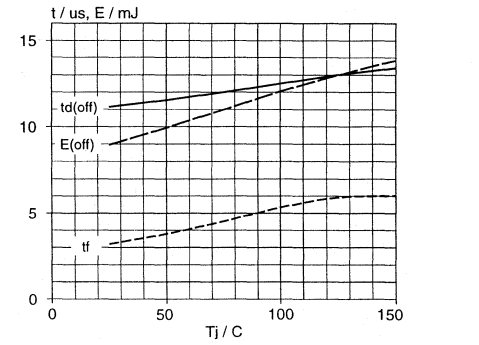


Fig.17. Typical Switching Characteristics vs. T_j conditions: I_C=8 A; V_{CL}=300 V; R_G=1 kΩ; L_C=5 mH.

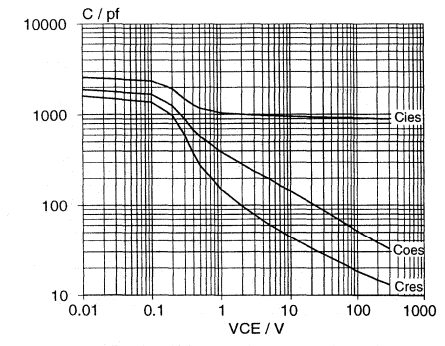


Fig.15. Typical Capacitances C_{ies}, C_{oes}, C_{res} $C = f(V_{CE})$; conditions: V_{GE} = 0 V; f = 1 MHz

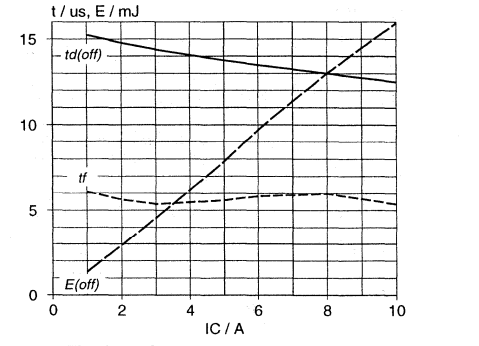


Fig.18. Typical Switching Characteristics vs. I_C conditions: T_j=125 °C V_{CL}=300 V; R_G=1 kΩ; L_C=5 mH.

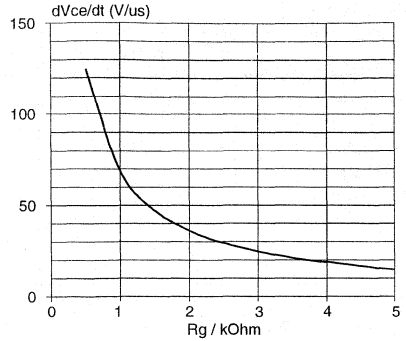


Fig.19. Typical Turn-off dV_{CE}/dt vs. R_G conditions: T_j=125 °C; I_C=8 A; V_{CL}=300 V; L_C=5 mH.

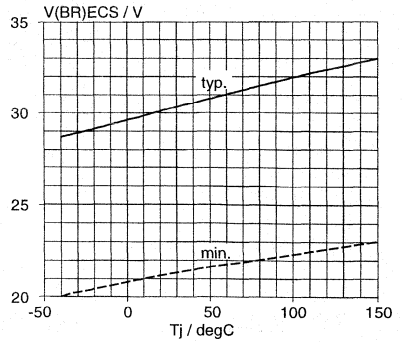


Fig.22. Reverse Breakdown Voltage $V_{(BR)ECS} = f(T_j)$; conditions: I_{EC} = 50 mA

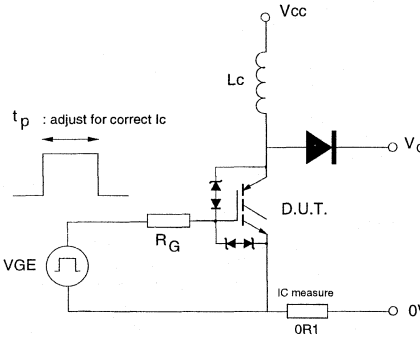


Fig.20. Test circuit for inductive load switching times.

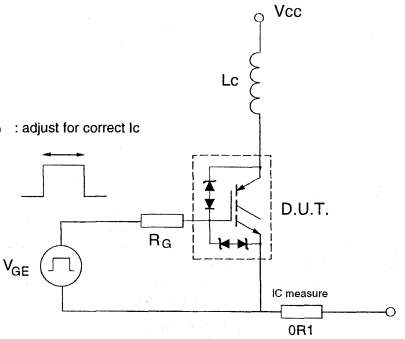


Fig.23. Test circuit for clamped turn-off energy test

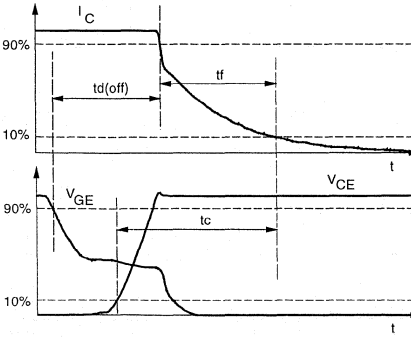


Fig.21. Definitions of inductive load switching times.

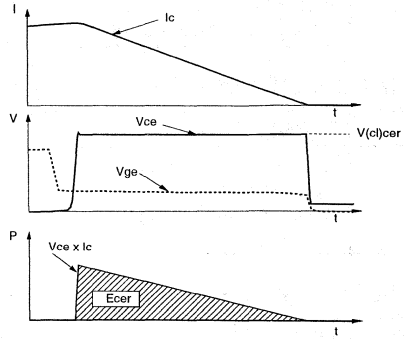


Fig.24. Definition of clamping energy E_{CER}

TrenchMOS™ transistor Standard level FET

BUK7506-30

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope using '**trench**' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

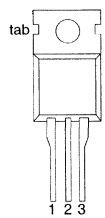
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	30	V
I_D	Drain current (DC)	75	A
P_{tot}	Total power dissipation	188	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	6	mΩ

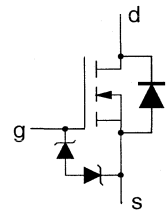
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	30	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	30	V
$\pm V_{GS}$	Gate-source voltage	-	-	16	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	75	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	53	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	240	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	188	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	0.8	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	30	-	-	V
		T_j = -55˚C	27	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.0	3.0	4.0	V
		T_j = 175˚C	1.0	-	-	V
		T_j = -55˚C	-	-	4.4	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 30 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	20	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A	-	5	6	mΩ
		T_j = 175˚C	-	-	11	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	12	25	-	S
$Q_{g(tot)}$	Total gate charge	I_D = 75 A; V_{DD} = 24 V; V_{GS} = 10 V	-	84	-	nC
Q_{gs}	Gate-source charge		-	14	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	28	-	nC
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	4000	-	pF
C_{oss}	Output capacitance		-	1150	-	pF
C_{rss}	Feedback capacitance		-	450	-	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 15 V; I_D = 25 A;	-	40	50	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 5 Ω	-	70	105	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	100	140	ns
t_f	Turn-off fall time		-	50	70	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	75	A
I_{DRM}	Pulsed reverse drain current		-	-	240	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.85	1.2	V
		I_F = 75 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 75 A; -dI_F/dt = 100 A/µs;	-	100	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 25 V	-	0.2	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 75 A; $V_{DD} \leq$ 15 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 ˚C	-	-	500	mJ

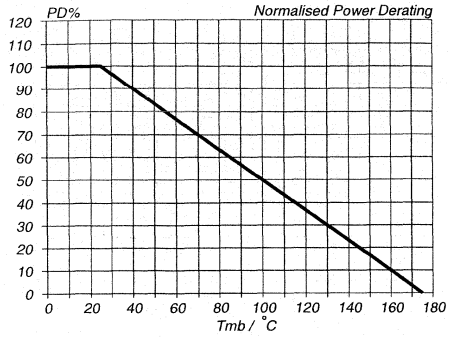


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

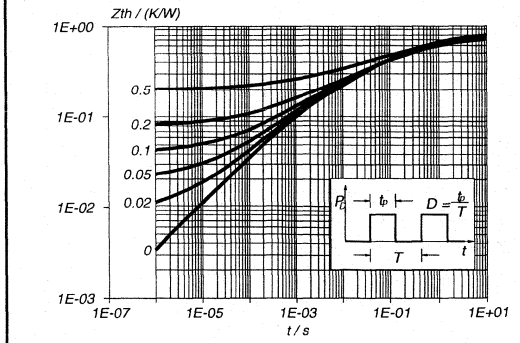


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

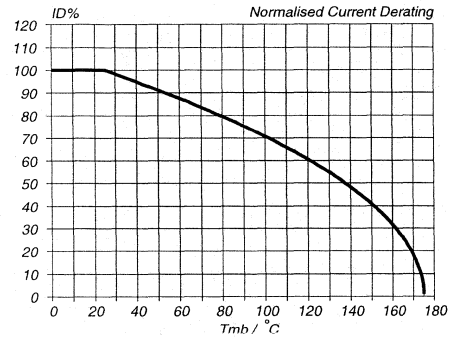


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

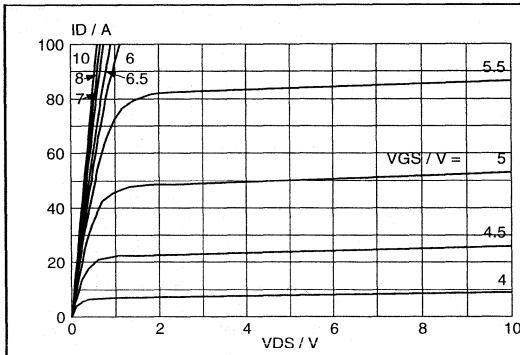


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

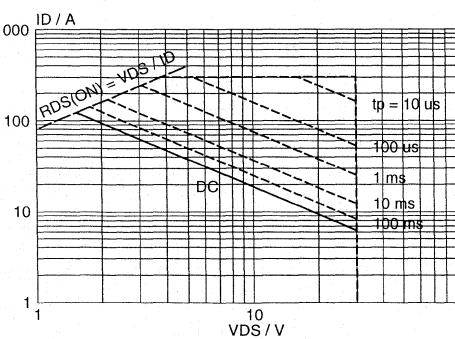


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

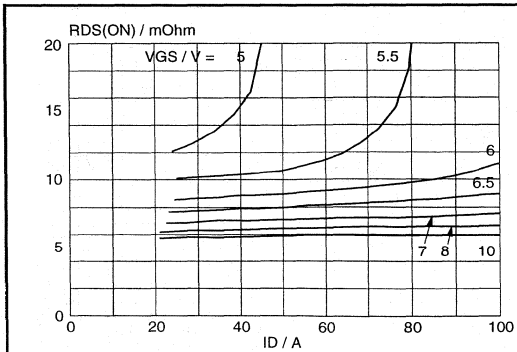


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

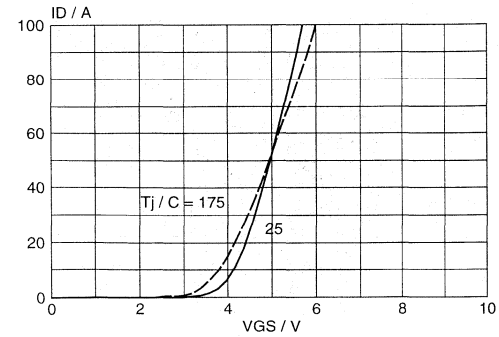


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

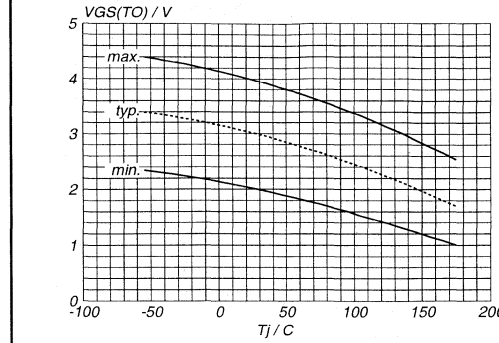


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

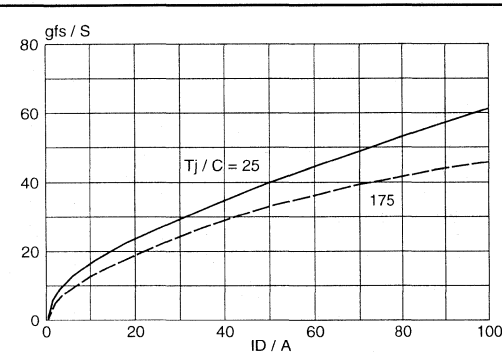


Fig.8. Typical transconductance, T_j = 25 ˚C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

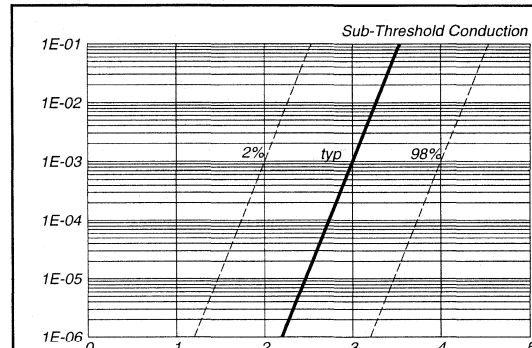


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

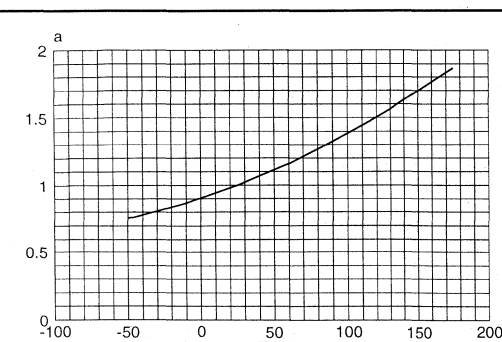


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ ^{\circ}C} = f(T_j)$; I_D = 25 A; V_{GS} = 10 V

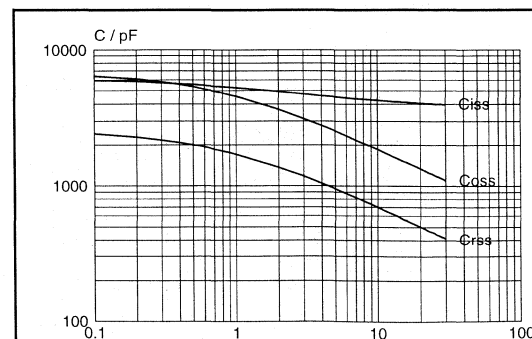


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

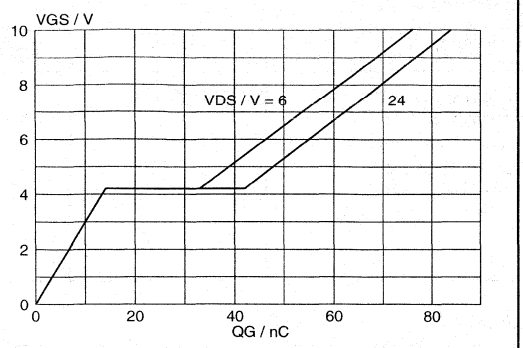


Fig.13. Typical turn-on gate-charge characteristics.
V_{GS} = f(Q_G); conditions: I_D = 75 A; parameter V_{DS}

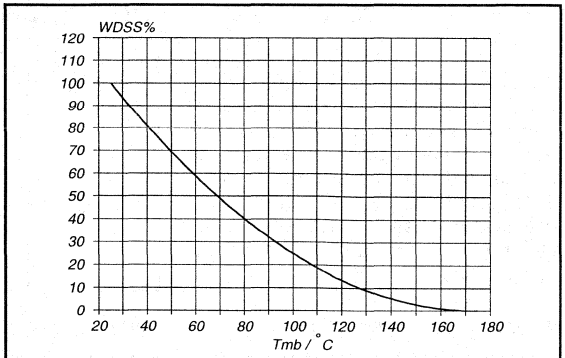


Fig.15. Normalised avalanche energy rating.
W_{DSS}% = f(T_{mb}); conditions: I_D = 75 A

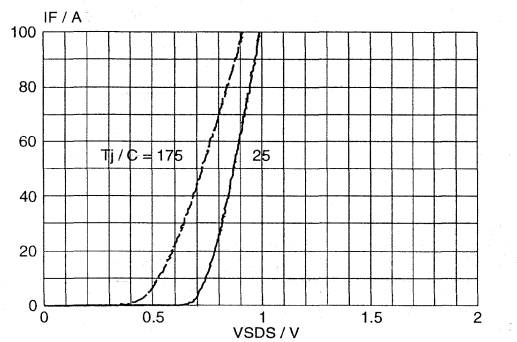


Fig.14. Typical reverse diode current.
I_F = f(V_{SDS}); conditions: V_{GS} = 0 V; parameter T_j

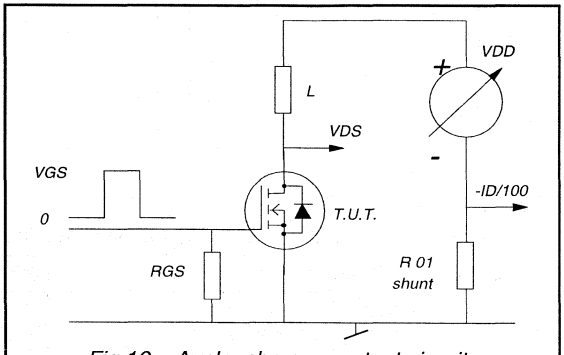


Fig.16. Avalanche energy test circuit.
$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

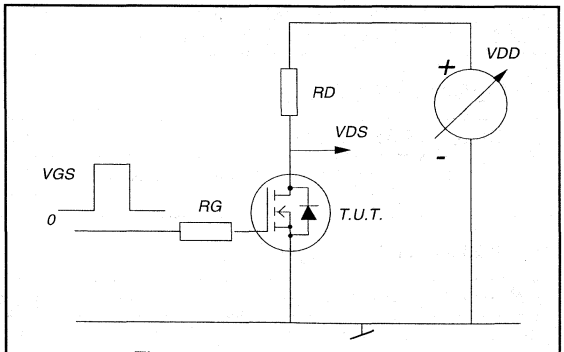


Fig.17. Switching test circuit.

TrenchMOS™ transistor Standard level FET

BUK7508-55

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope using '**trench**' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

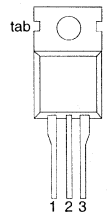
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	75	A
P_{tot}	Total power dissipation	187	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	8	mΩ

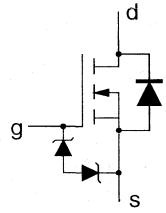
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	16	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	75	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	65	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	240	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	187	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	0.8	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2	3.0	4.0	V
		T_j = 175˚C	1	-	-	V
		T_j = -55˚C	-	-	4.4	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	20	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A	-	6.5	8	mΩ
		T_j = 175˚C	-	-	17	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	10	45	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	3600	4500	pF
C_{oss}	Output capacitance		-	830	1000	pF
C_{rss}	Feedback capacitance		-	320	440	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	27	40	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 10 Ω	-	70	105	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	100	140	ns
t_f	Turn-off fall time		-	50	70	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	75	A
I_{DRM}	Pulsed reverse drain current		-	-	240	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.85	1.2	V
		I_F = 75 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 75 A; -dI_F/dt = 100 A/µs;	-	65	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.18	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 75 A; $V_{DD} \leq$ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	500	mJ

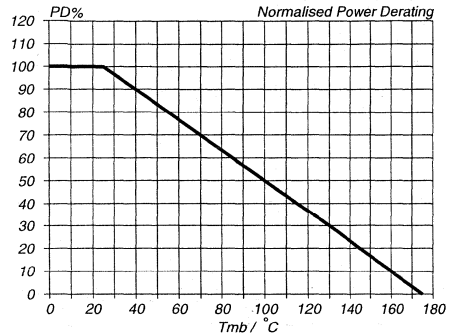


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

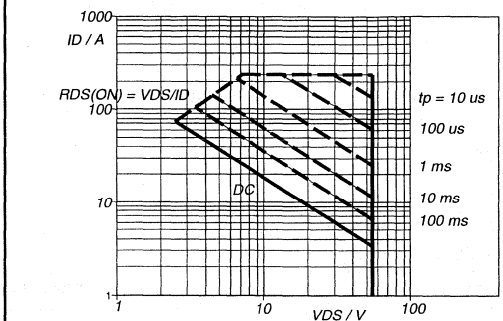


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

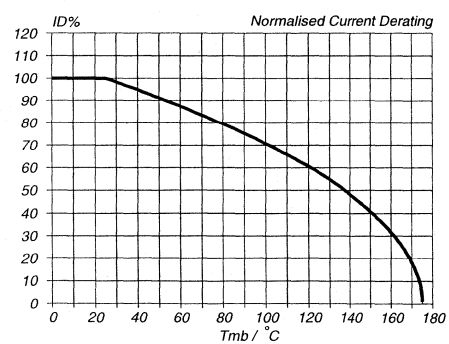


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

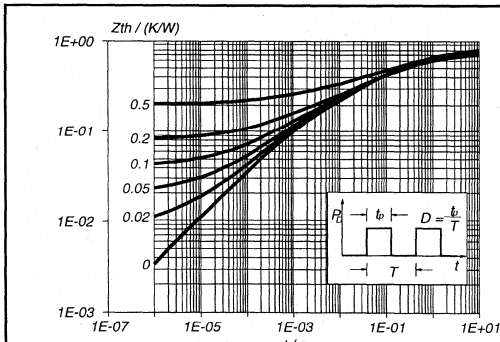


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

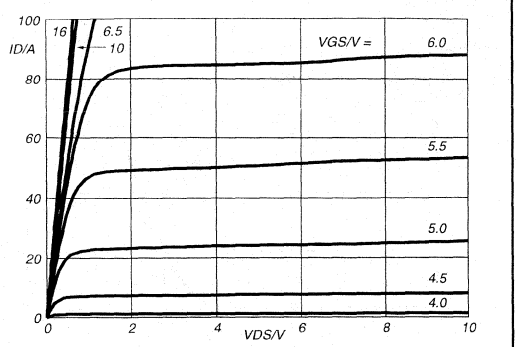


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

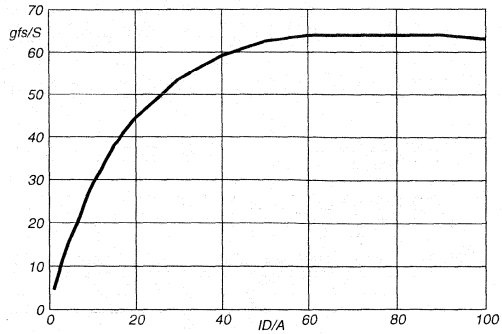


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

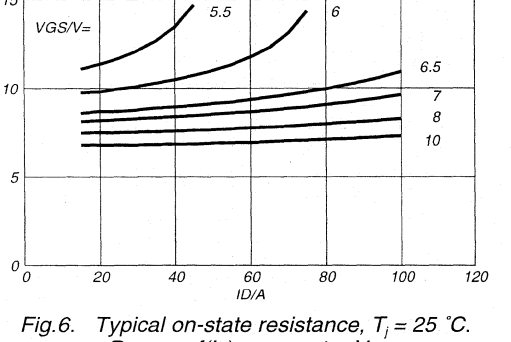


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

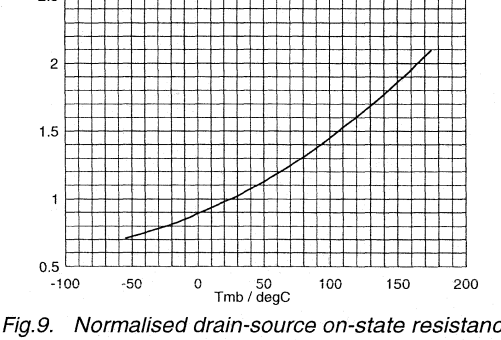


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\ ^\circ C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

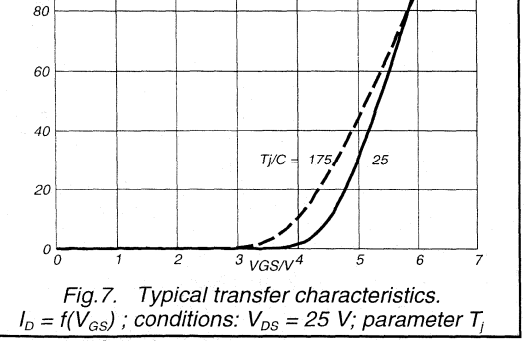


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

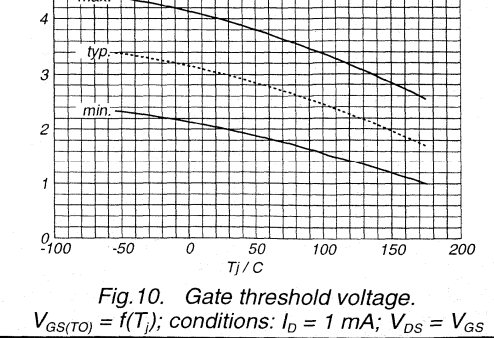


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

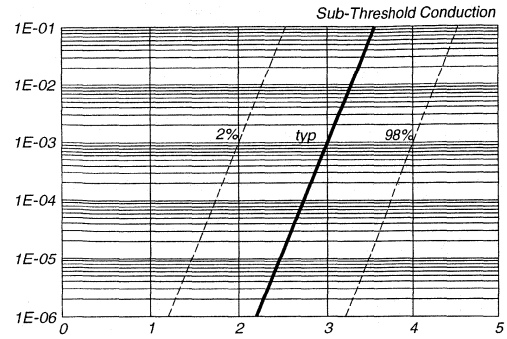


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

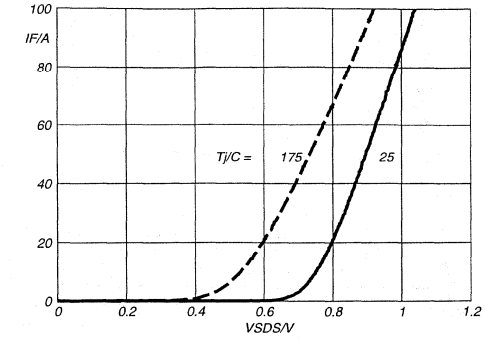


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

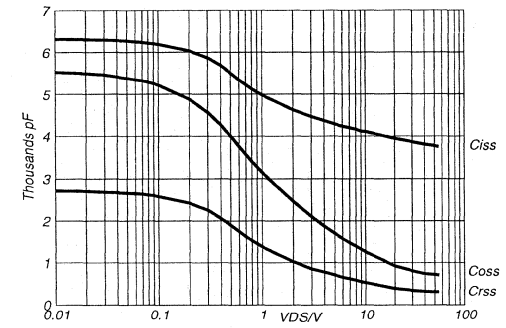


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

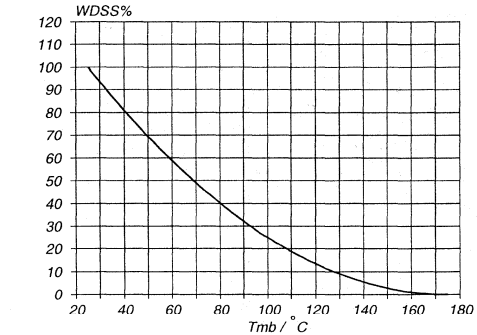


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 75$ A

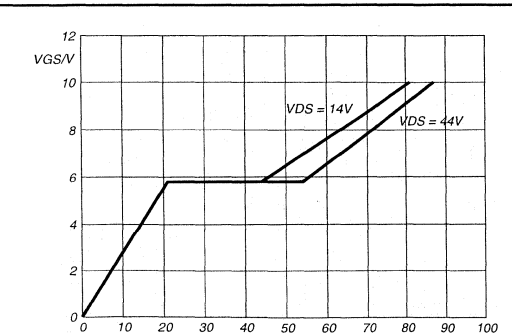


Fig.13. Typical turn-on gate-characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 50$ A; parameter V_{DS}

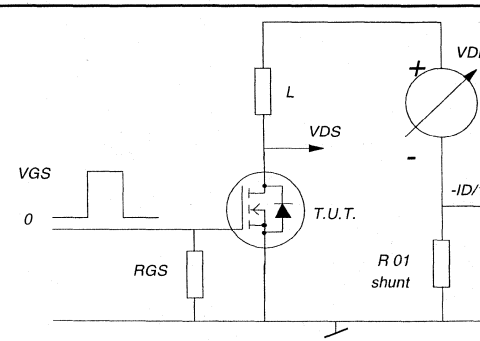


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

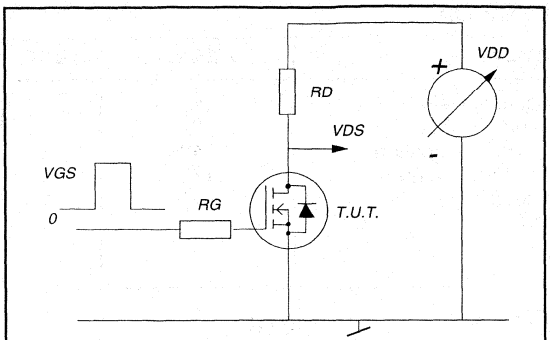


Fig.17. Switching test circuit.

TrenchMOS™ transistor Standard level FET

BUK7510-30

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope using '**trench**' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

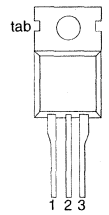
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	30	V
I_D	Drain current (DC)	75	A
P_{tot}	Total power dissipation	142	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	10.5	mΩ

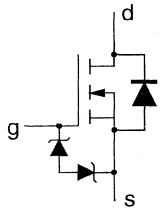
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	30	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	30	V
$\pm V_{GS}$	Gate-source voltage	-	-	16	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	75	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	53	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	240	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	142	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.05	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	30	-	-	V
		T_j = -55˚C	27	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2	3.0	4.0	V
		T_j = 175˚C	1	-	-	V
		T_j = -55˚C	-	-	4.4	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 30 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	20	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A	-	9	10.5	mΩ
		T_j = 175˚C	-	-	19.5	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	9	18	-	S
$Q_{g(tot)}$	Total gate charge	I_D = 75 A; V_{DD} = 24 V; V_{GS} = 10 V	-	51	-	nC
Q_{gs}	Gate-source charge		-	9	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	20	-	nC
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	2000	-	pF
C_{oss}	Output capacitance		-	700	-	pF
C_{rss}	Feedback capacitance		-	300	-	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 25 V; I_D = 25 A;	-	26	30	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 5 Ω	-	35	85	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	50	60	ns
t_f	Turn-off fall time		-	30	45	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	75	A
I_{DRM}	Pulsed reverse drain current		-	-	240	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 75 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 75 A; -dI_F/dt = 100 A/µs;	-	95	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 25 V	-	0.15	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 45 A; $V_{DD} \leq$ 15 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	200	mJ

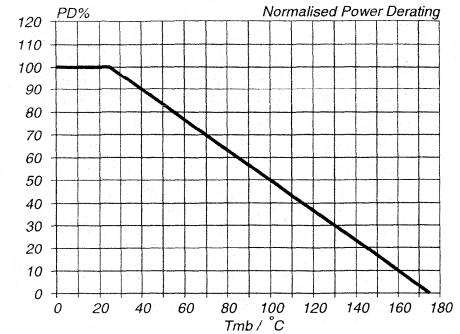


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

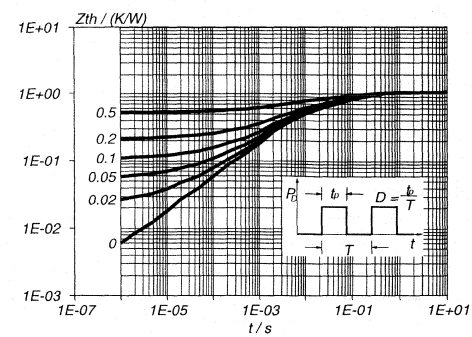


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

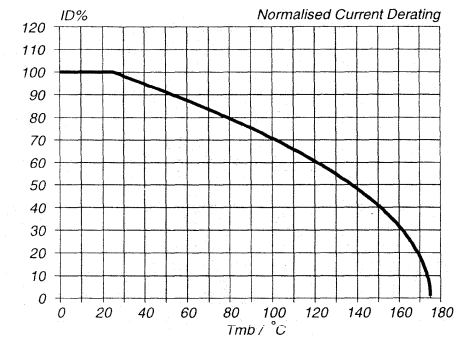


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

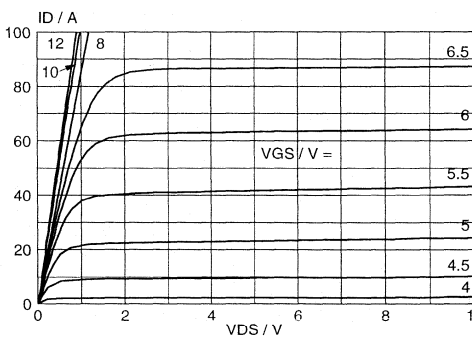


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

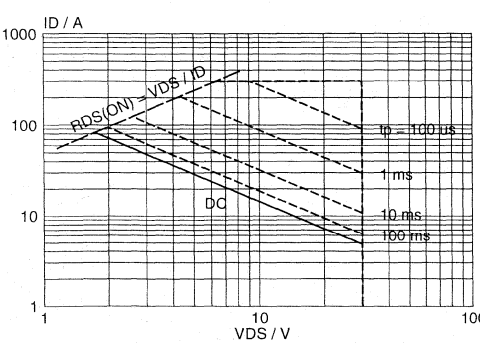


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

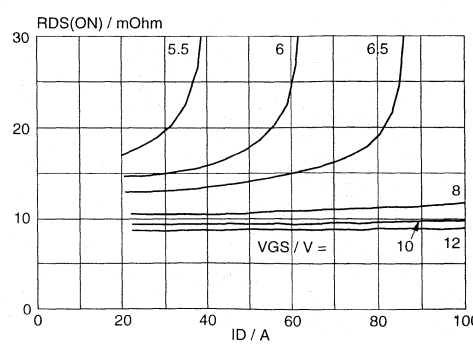


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

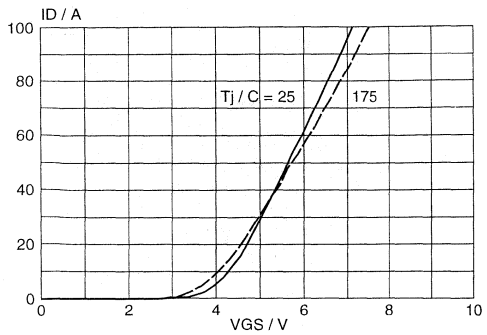


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

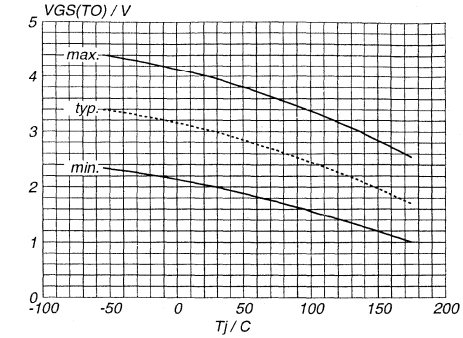


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

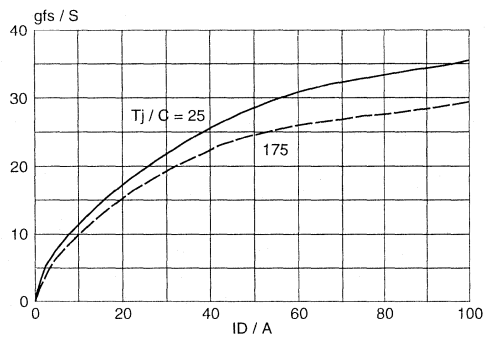


Fig.8. Typical transconductance, T_j = 25 ˚C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

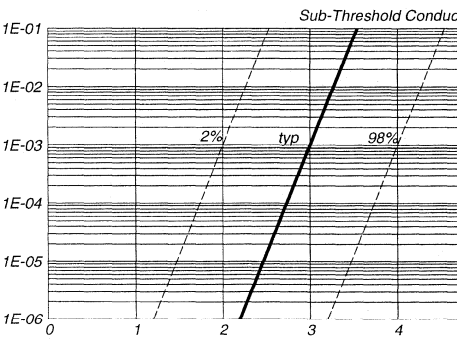


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

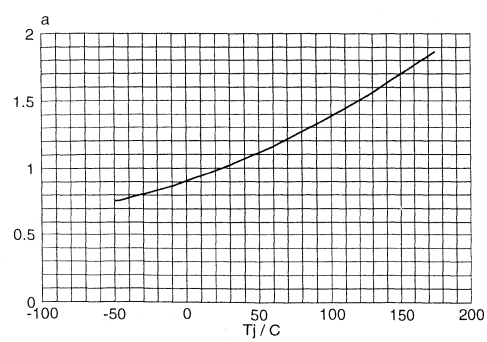


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ ˚C} = f(T_j)$; I_D = 25 A; V_{GS} = 10 V

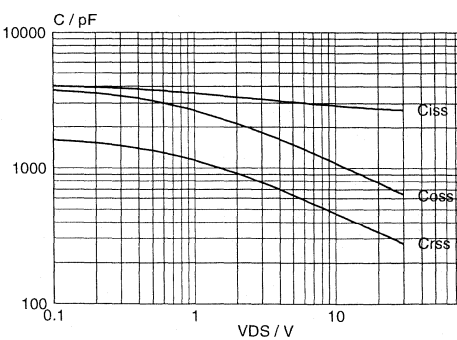


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

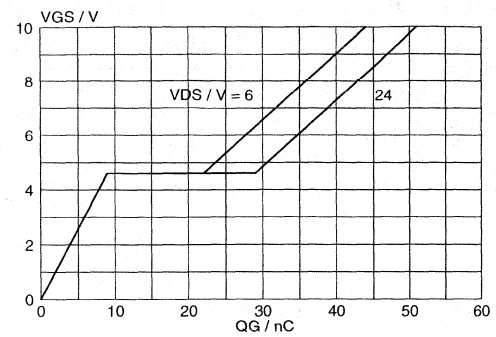


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 75 A; parameter V_{DS}

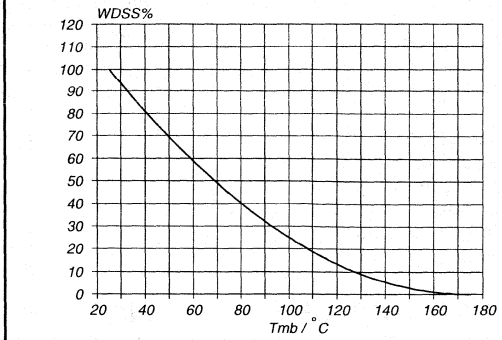


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: I_D = 45 A

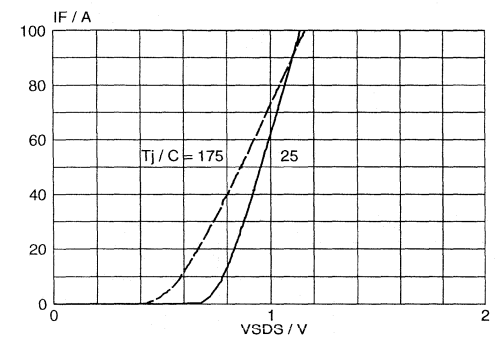


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

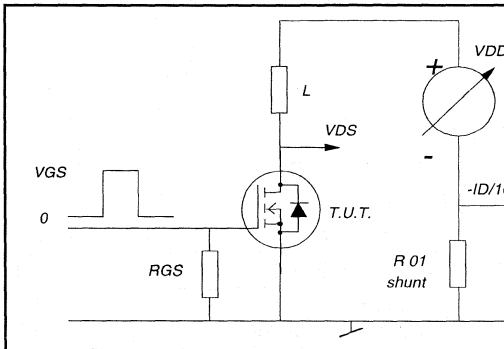


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

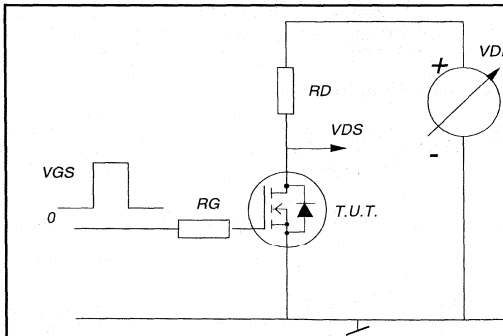


Fig.17. Switching test circuit.

TrenchMOS™ transistor Standard level FET

BUK7514-30

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope using '**trench**' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

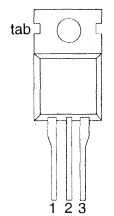
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	30	V
I_D	Drain current (DC)	69	A
P_{tot}	Total power dissipation	125	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	14	mΩ

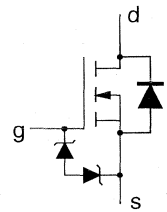
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	30	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	30	V
$\pm V_{GS}$	Gate-source voltage	-	-	16	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	69	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	48	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	240	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	30	-	-	V
		T_j = -55˚C	27	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.0	3.0	4.0	V
		T_j = 175˚C	1.0	-	-	V
		T_j = -55˚C	-	-	4.4	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 30 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	20	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A	-	12	14	mΩ
		T_j = 175˚C	-	-	26	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	9	18	-	S
$Q_{g(tot)}$	Total gate charge	I_D = 69 A; V_{DD} = 24 V; V_{GS} = 10 V	-	38	-	nC
Q_{gs}	Gate-source charge		-	7	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	14	-	nC
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1500	-	pF
C_{oss}	Output capacitance		-	480	-	pF
C_{rss}	Feedback capacitance		-	220	-	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 25 V; I_D = 25 A;	-	22	35	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 5 Ω	-	30	60	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	40	50	ns
t_f	Turn-off fall time		-	25	38	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	69	A
I_{DRM}	Pulsed reverse drain current		-	-	240	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 69 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 69 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 25 V	-	0.1	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 36 A; $V_{DD} \leq$ 15 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 ˚C	-	-	125	mJ

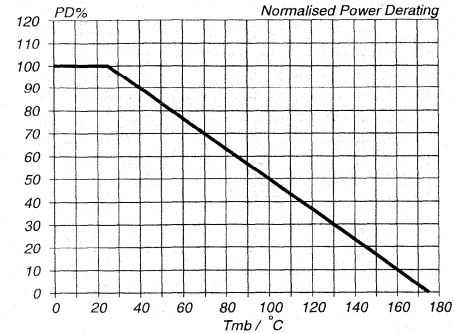


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

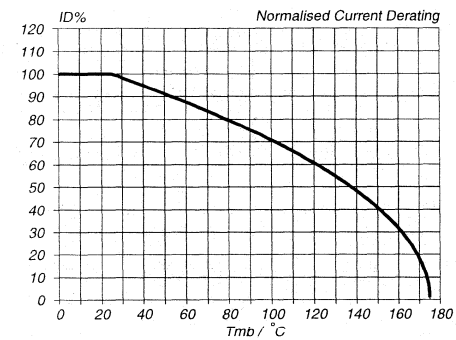


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

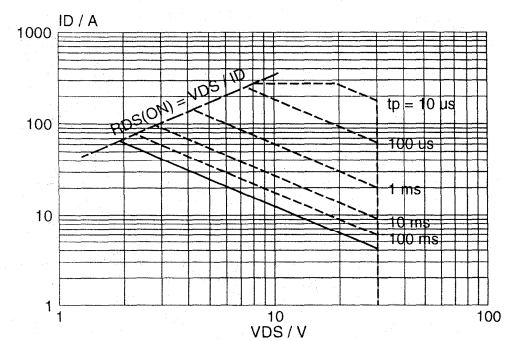


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

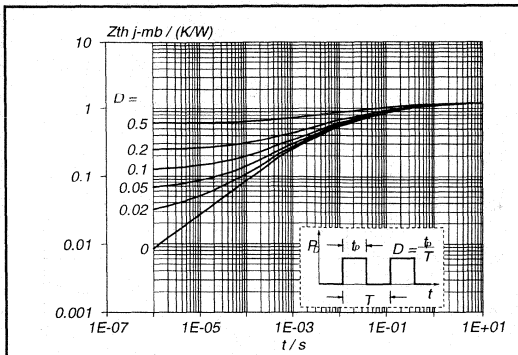


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

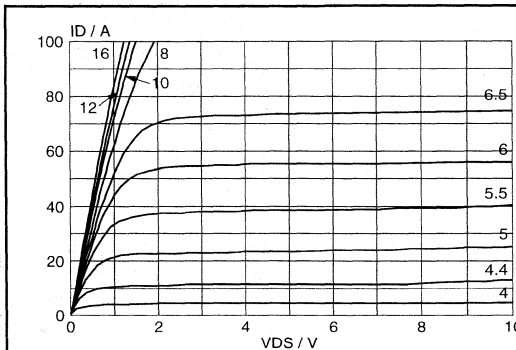


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

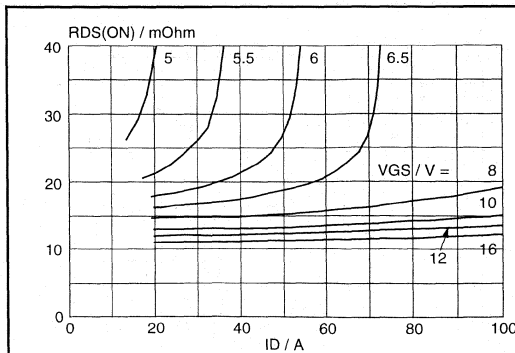


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

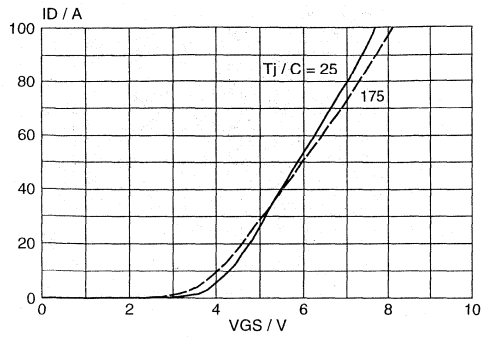


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

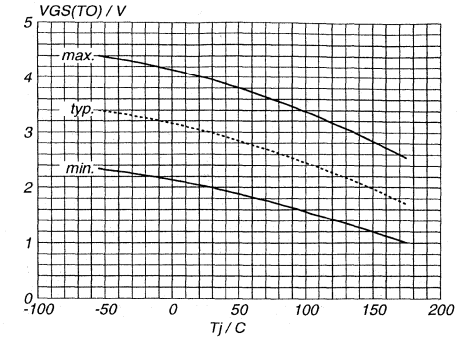


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

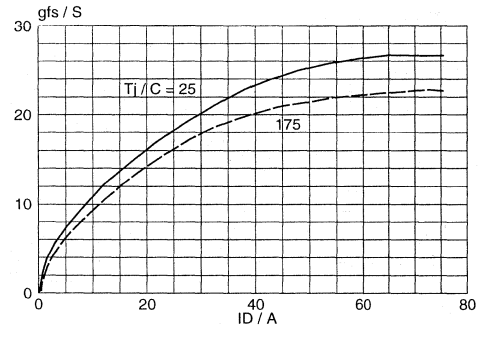


Fig.8. Typical transconductance, T_j = 25 ˚C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

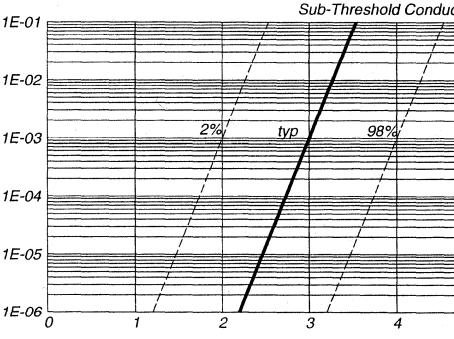


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

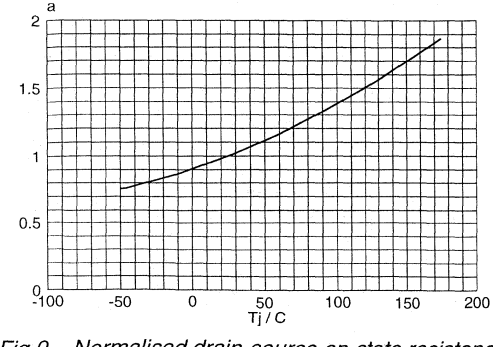


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ ^{\circ}C} = f(T_j)$; I_D = 25 A; V_{GS} = 10 V

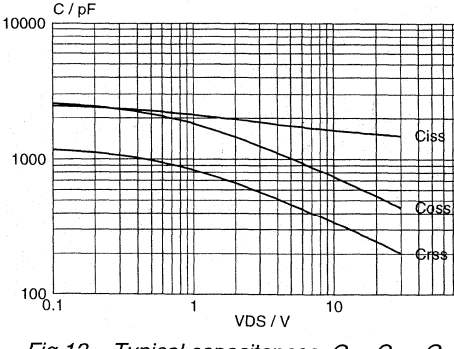


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

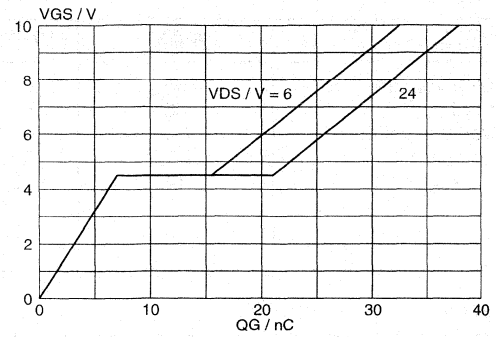


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: I_D = 69 A; parameter V_{DS}

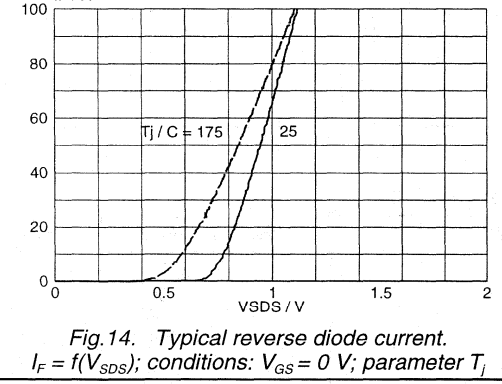


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

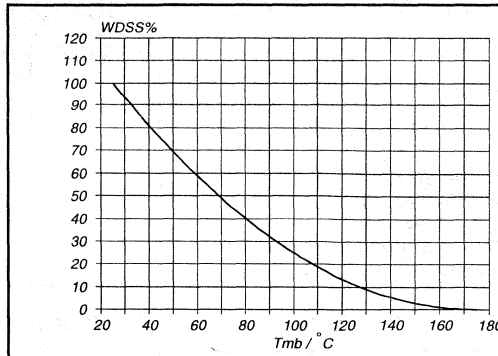


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: I_D = 35 A

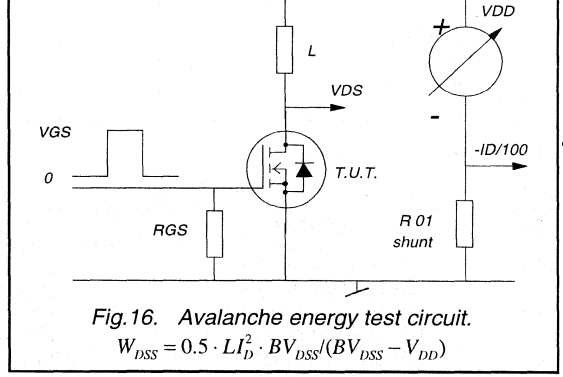


Fig.16. Avalanche energy test circuit.
$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

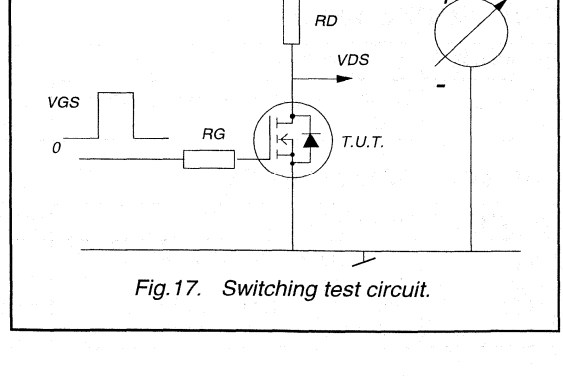


Fig.17. Switching test circuit.

TrenchMOS™ transistor Standard level FET

BUK7514-55

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope using '**trench**' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

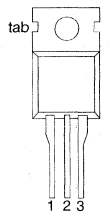
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	68	A
P_{tot}	Total power dissipation	142	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	14	mΩ

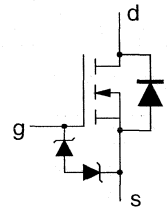
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	16	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	68	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	48	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	240	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	142	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.05	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2	3.0	4.0	V
		T_j = 175˚C	1	-	-	V
		T_j = -55˚C	-	-	4.4	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	20	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A	-	12	14	mΩ
		T_j = 175˚C	-	-	30	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	8	39	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	2200	2900	pF
C_{oss}	Output capacitance		-	500	600	pF
C_{rss}	Feedback capacitance		-	200	270	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	18	26	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 10 Ω	-	35	85	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	45	60	ns
t_f	Turn-off fall time		-	30	45	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	68	A
I_{DRM}	Pulsed reverse drain current		-	-	240	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 65 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 65 A; -dI_F/dt = 100 A/µs;	-	57	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.14	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 65 A; $V_{DD} \leq$ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	200	mJ

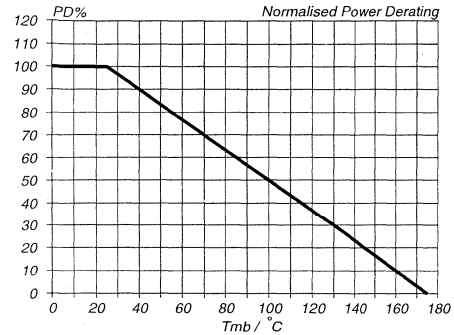


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

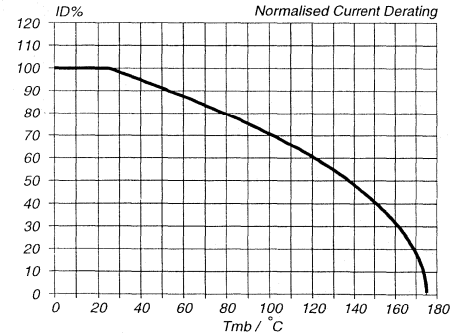


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

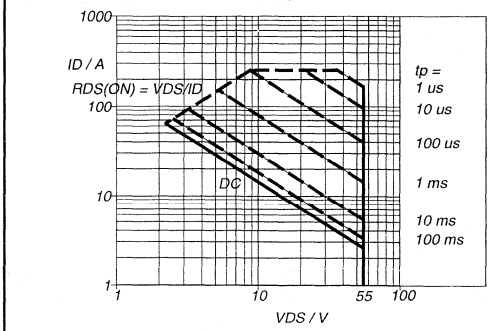


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

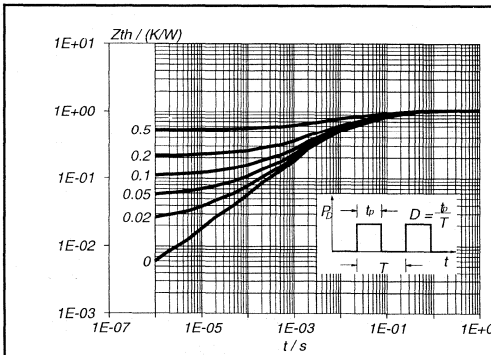


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

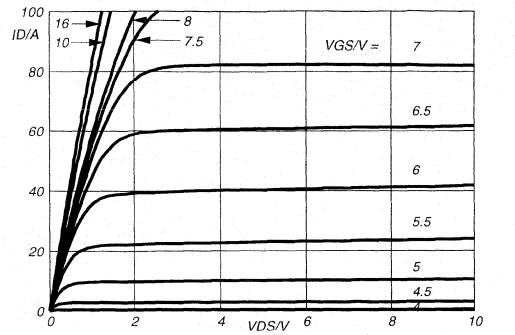


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

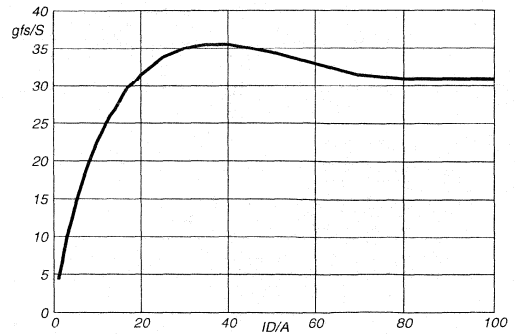


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

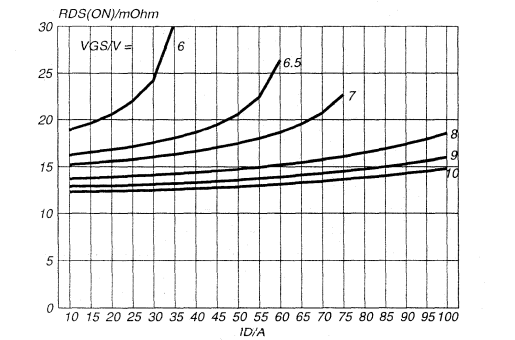


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

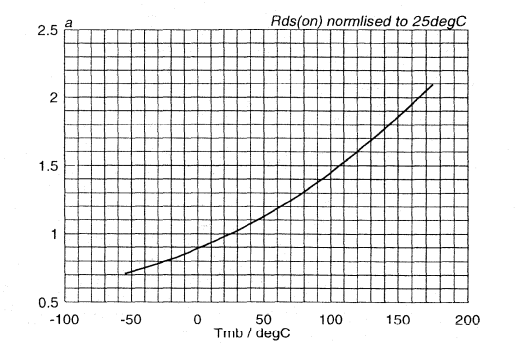


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

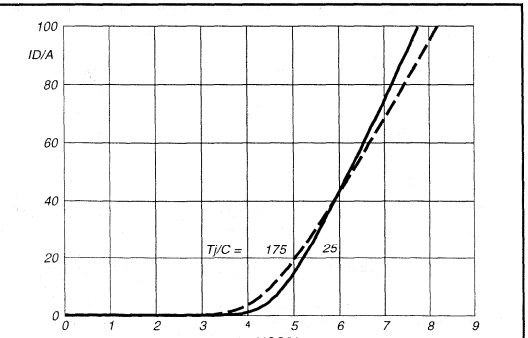


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

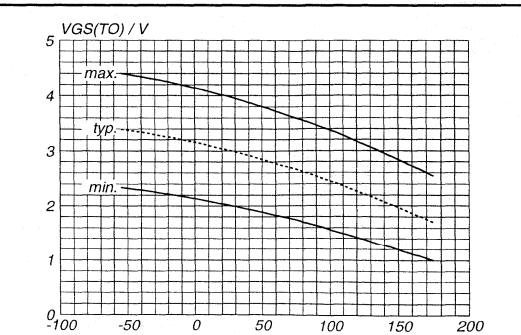


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

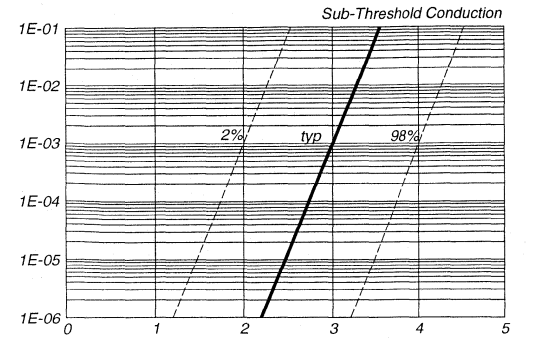


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

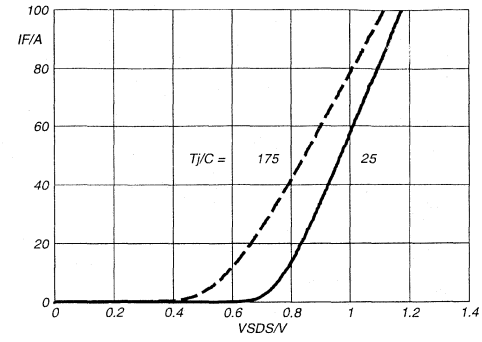


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

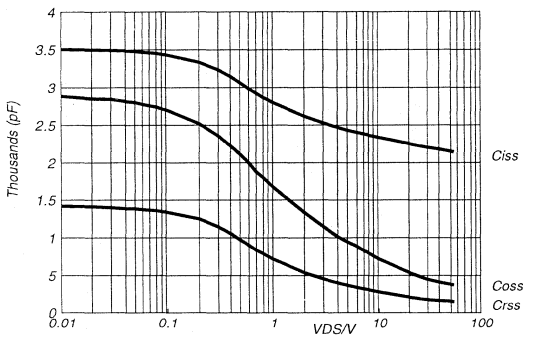


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

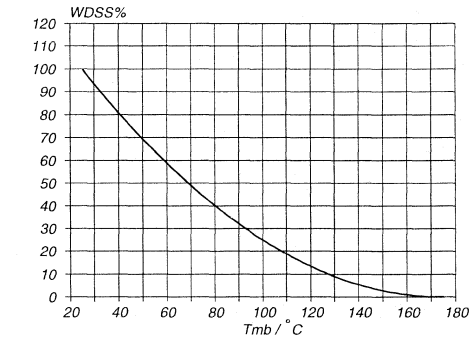


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 75$ A

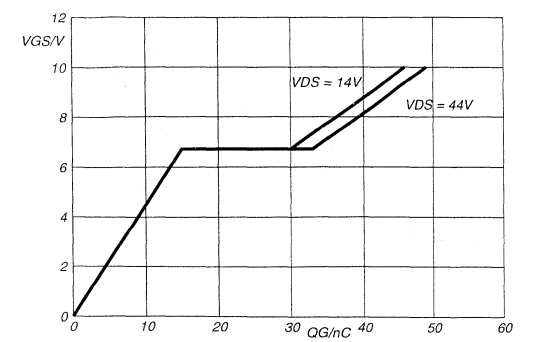


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 50$ A; parameter V_{DS}

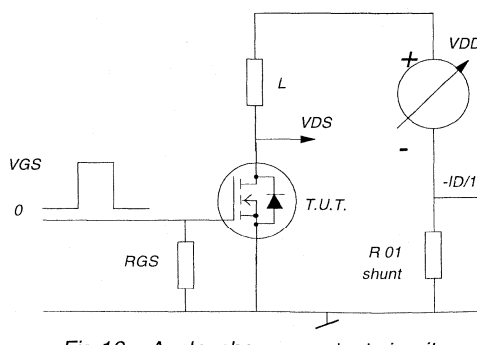


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

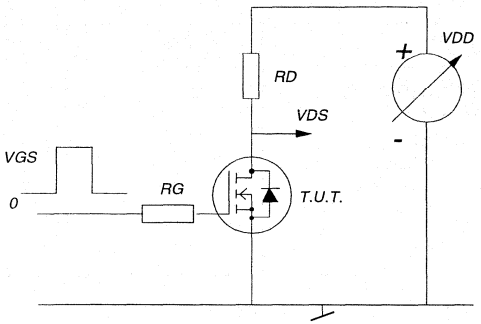


Fig.17. Switching test circuit.

TrenchMOS™ transistor
Standard level FET

BUK7518-30

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope using '**trench**' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

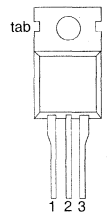
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	30	V
I_D	Drain current (DC)	55	A
P_{tot}	Total power dissipation	103	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	18	mΩ

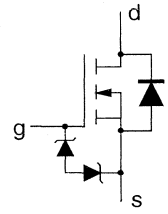
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	30	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	30	V
$\pm V_{GS}$	Gate-source voltage	-	-	16	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	55	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	38	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	220	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	103	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.45	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

STATIC CHARACTERISTICS

T_j = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	30	-	-	V
		T_j = -55°C	27	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.0	3.0	4.0	V
		T_j = 175°C	1.0	-	-	V
		T_j = -55°C	-	-	4.4	
I_{DSS}	Zero gate voltage drain current	V_{DS} = 30 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175°C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175°C	-	-	20	µA
$±V_{(BR)GSS}$	Gate source breakdown voltage	I_G = ±1 mA;	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A	-	15	18	mΩ
		T_j = 175°C	-	-	33.5	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	7	15	-	S
$Q_{g(tot)}$	Total gate charge	I_D = 55 A; V_{DD} = 24 V; V_{GS} = 10 V	-	29.5	-	nC
Q_{gs}	Gate-source charge		-	4.5	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	14	-	nC
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1000	-	pF
C_{oss}	Output capacitance		-	390	-	pF
C_{rss}	Feedback capacitance		-	180	-	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 15 V; I_D = 25 A;	-	15	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 5 Ω	-	22	35	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	30	45	ns
t_f	Turn-off fall time		-	18	25	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	55	A
I_{DRM}	Pulsed reverse drain current		-	-	220	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 55 A; V_{GS} = 0 V	-	1.0	-	
t_{rr}	Reverse recovery time	I_F = 55 A; -dI_F/dt = 100 A/µs;	-	70	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 25 V	-	0.1	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 28 A; $V_{DD} \leq$ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	80	mJ

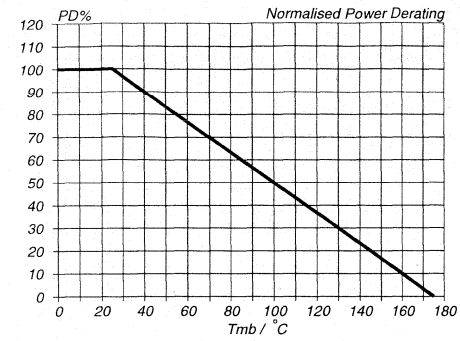


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

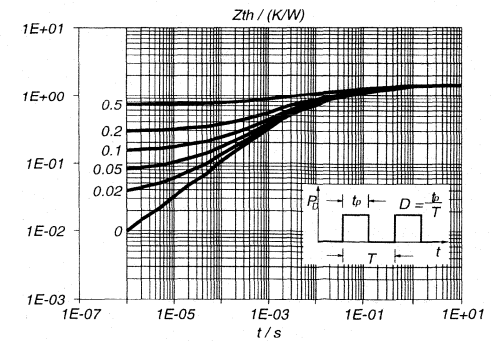


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

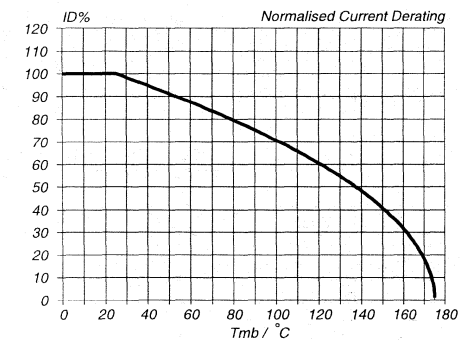


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

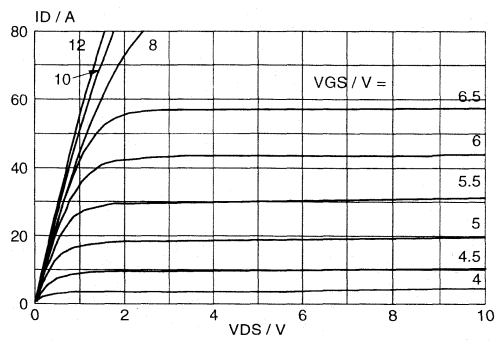


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

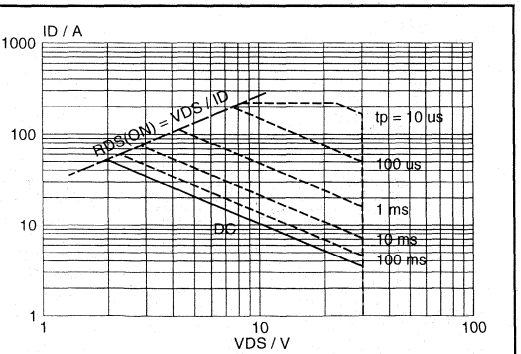


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

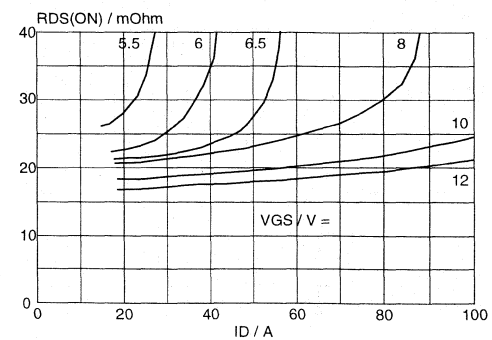


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

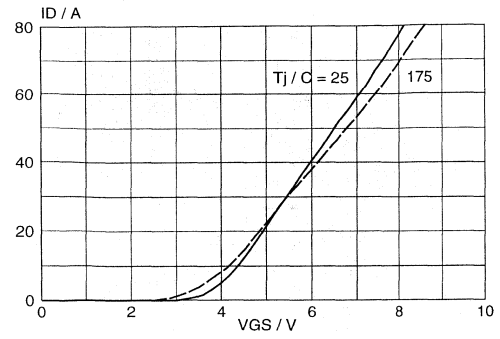


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

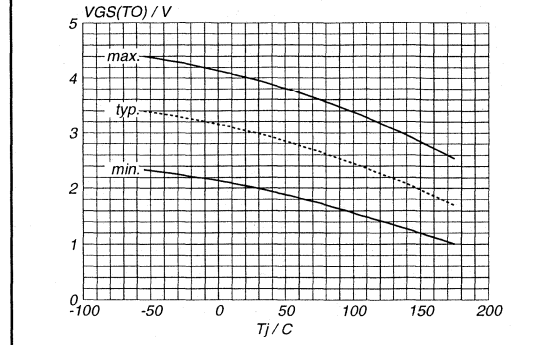


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

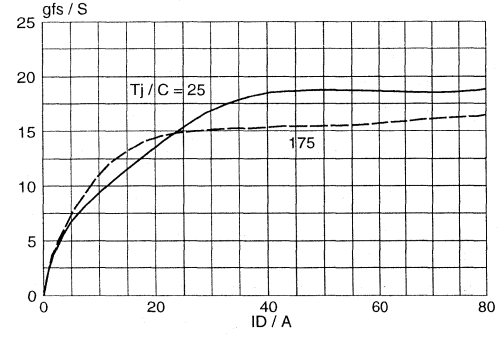


Fig.8. Typical transconductance, T_j = 25 ˚C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

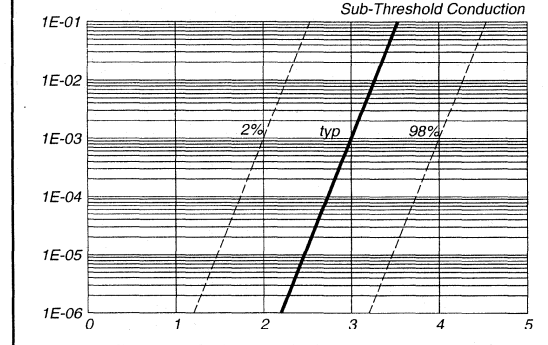


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

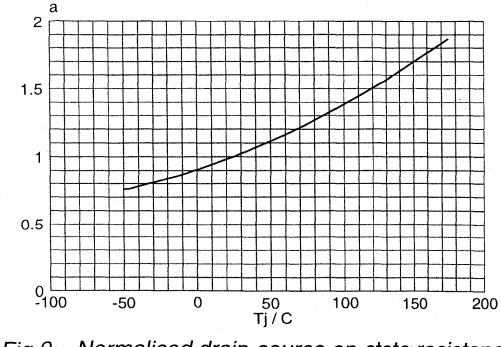


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ ^\circ C} = f(T_j)$; I_D = 25 A; V_{GS} = 10 V

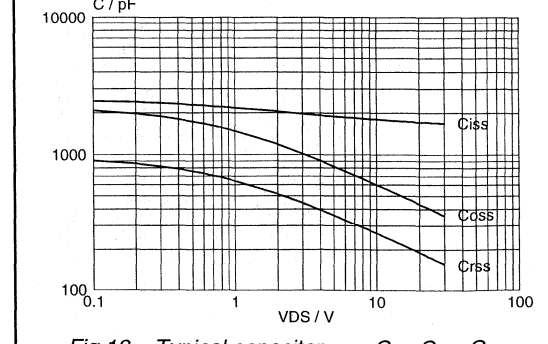


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

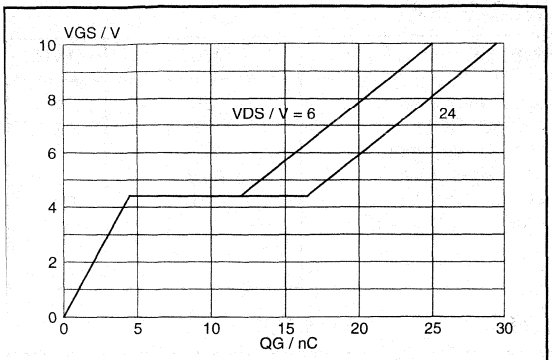


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 55 A; parameter V_{DS}

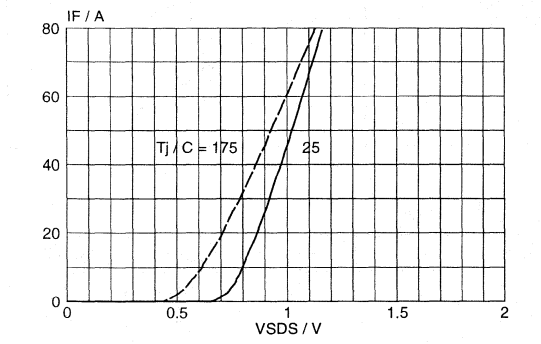


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

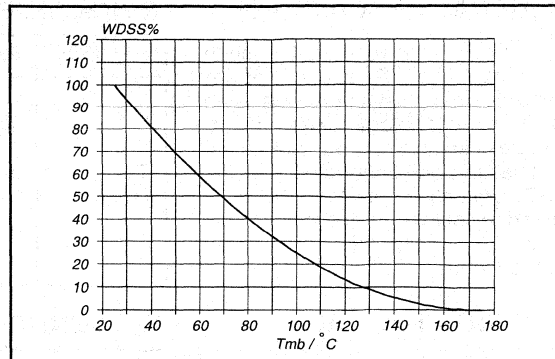


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: I_D = 28 A

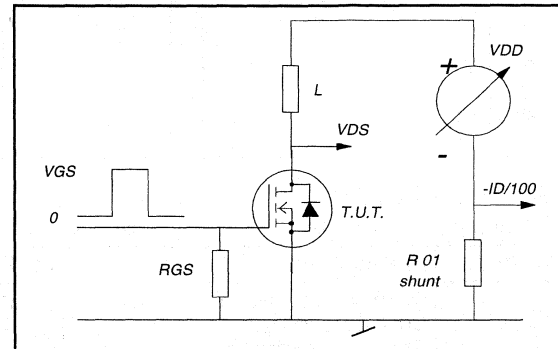


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

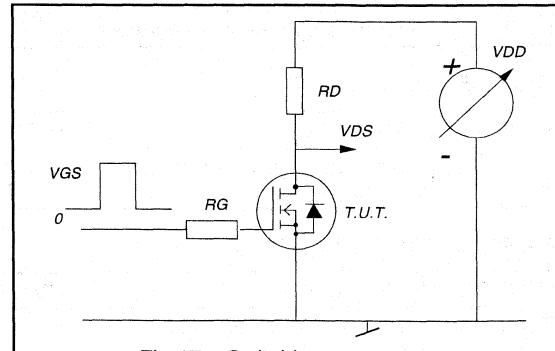


Fig.17. Switching test circuit.

TrenchMOS™ transistor
Standard level FET

BUK7518-55

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope using '**trench**' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

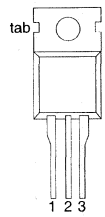
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	57	A
P_{tot}	Total power dissipation	125	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	18	mΩ

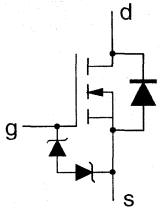
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	16	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	57	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	40	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	228	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55°C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.0	3.0	4.0	V
		T_j = 175°C	1.0	-	-	V
		T_j = -55°C	-	-	4.4	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175°C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175°C	-	-	20	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A	-	15	18	mΩ
		T_j = 175°C	-	-	38	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	6	30	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1500	2000	pF
C_{oss}	Output capacitance		-	370	470	pF
C_{rss}	Feedback capacitance		-	170	250	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	15	22	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 10 Ω	-	30	60	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	35	50	ns
t_f	Turn-off fall time		-	25	38	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	57	A
I_{DRM}	Pulsed reverse drain current		-	-	200	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 50 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 50 A; -dI_F/dt = 100 A/µs;	-	48	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.1	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 50 A; $V_{DD} \leq$ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	125	mJ

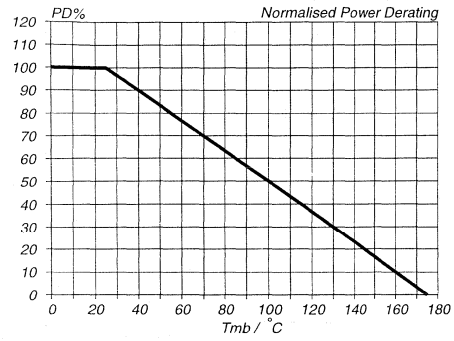


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

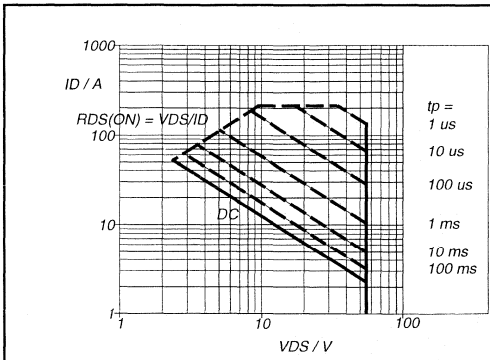


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

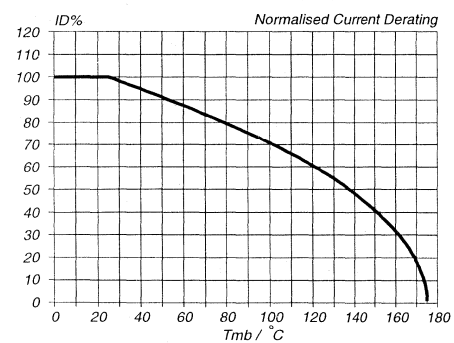


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

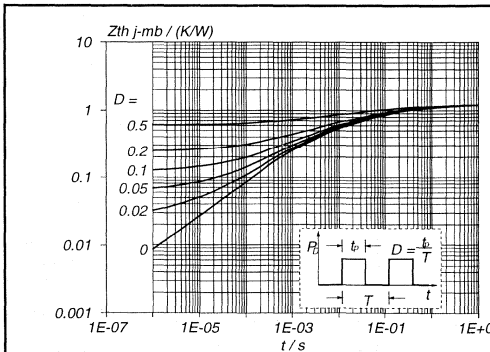


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

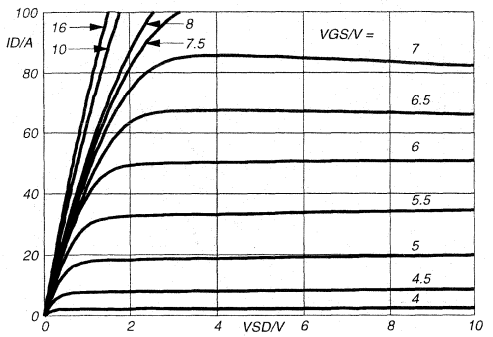


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

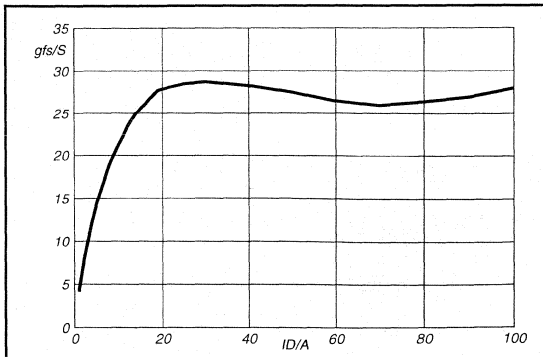


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

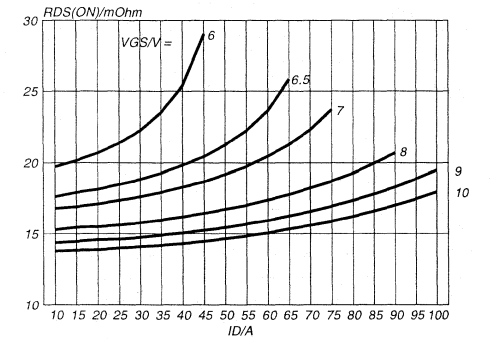


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

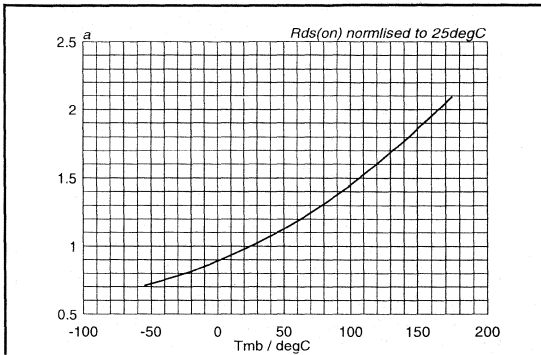


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\ ˚C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

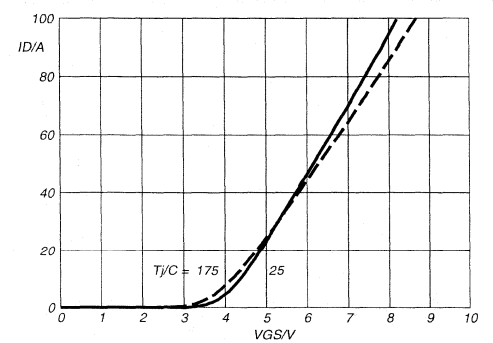


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

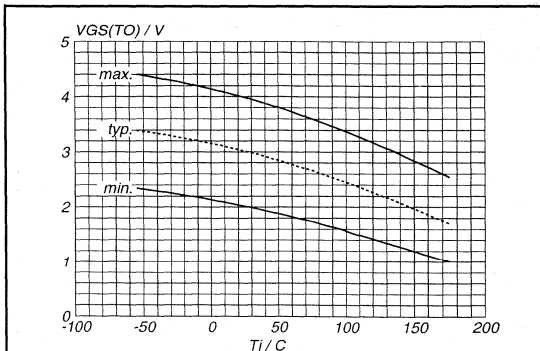


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

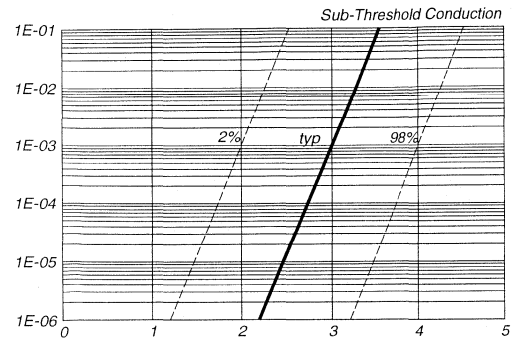


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

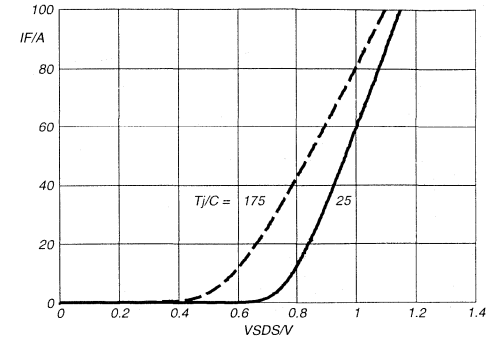


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

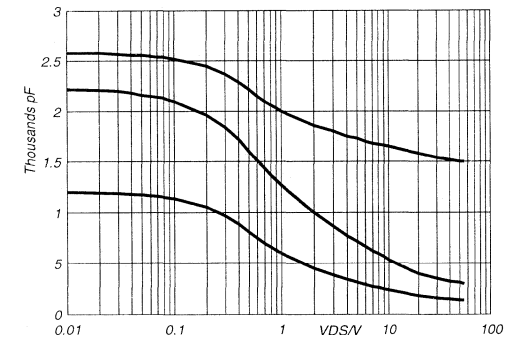


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

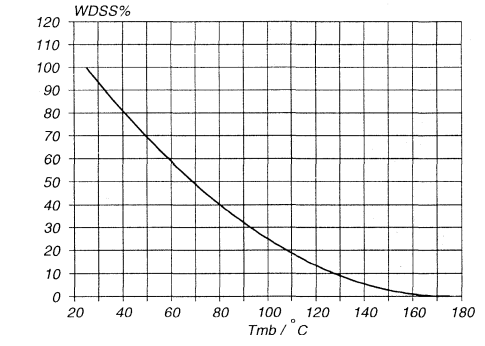


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: I_D = 75 A

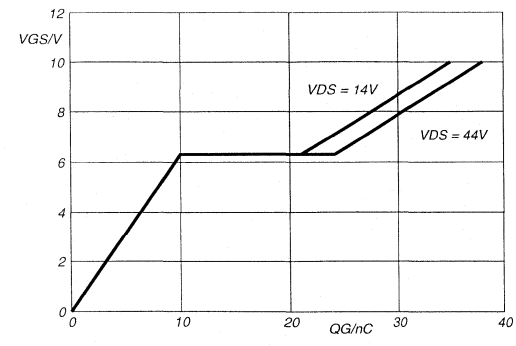


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 50 A; parameter V_{DS}

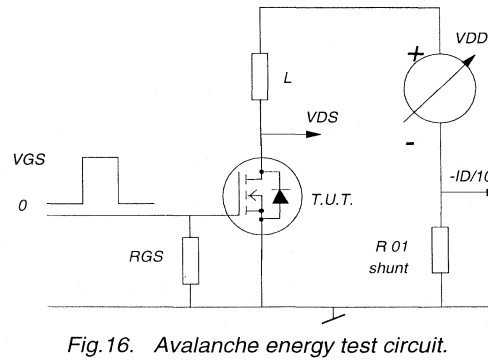


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

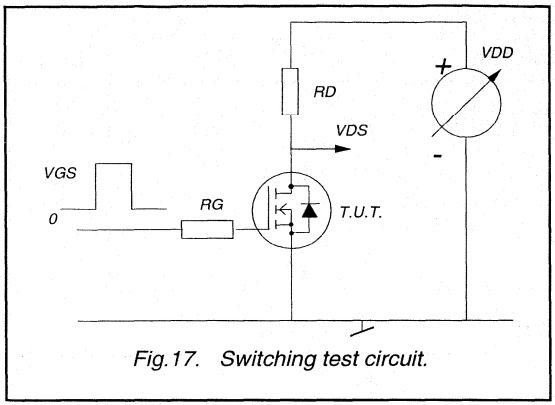


Fig.17. Switching test circuit.

TrenchMOS™ transistor Standard level FET

BUK7520-55

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope using '**trench**' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

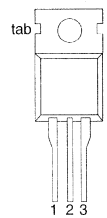
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	52	A
P_{tot}	Total power dissipation	116	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	20	mΩ

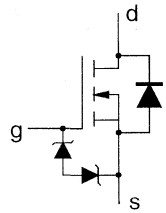
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	16	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	52	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	37	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	208	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	116	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.29	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55°C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.0	3.0	4.0	V
		T_j = 175°C	1.0	-	-	V
		T_j = -55°C	-	-	4.4	
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175°C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	0.04	1	µA
		T_j = 175°C	-	-	20	µA
$\pm V_{(BR)GSS}$	Gate source breakdown voltage	I_G = ±1 mA;	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A	-	15	20	mΩ
		T_j = 175°C	-	-	42	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	6	-	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1350	1800	pF
C_{oss}	Output capacitance		-	330	400	pF
C_{rss}	Feedback capacitance		-	155	215	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	18	26	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 10 Ω	-	50	75	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	40	50	ns
t_f	Turn-off fall time		-	30	40	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	52	A
I_{DRM}	Pulsed reverse drain current		-	-	208	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 40 A; V_{GS} = 0 V	-	1.0	-	
t_{rr}	Reverse recovery time	I_F = 40 A; -dI_F/dt = 100 A/µs;	-	47	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.15	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 45 A; $V_{DD} \leq$ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	110	mJ

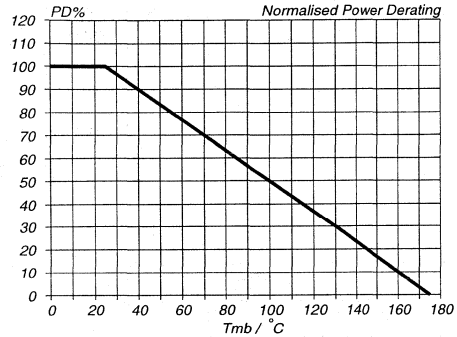


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

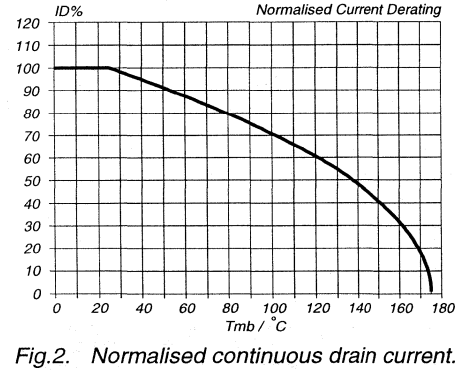


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 10 V

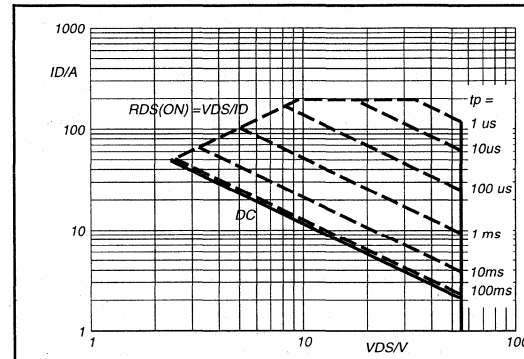


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

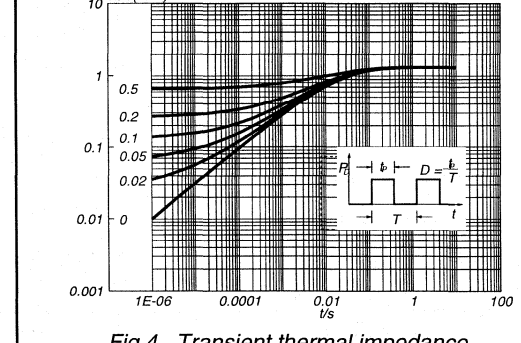


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

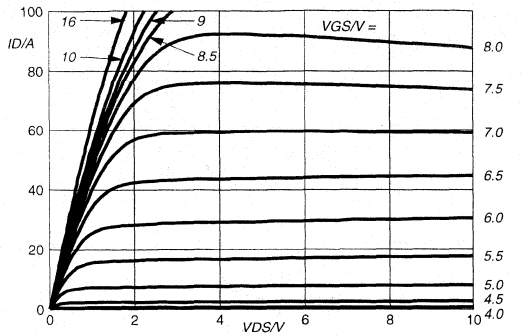


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

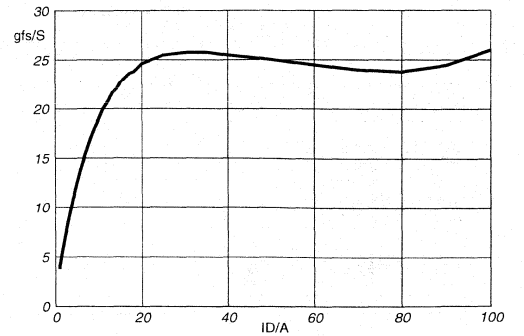


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

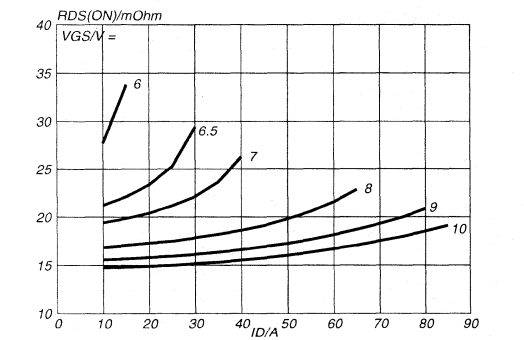


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

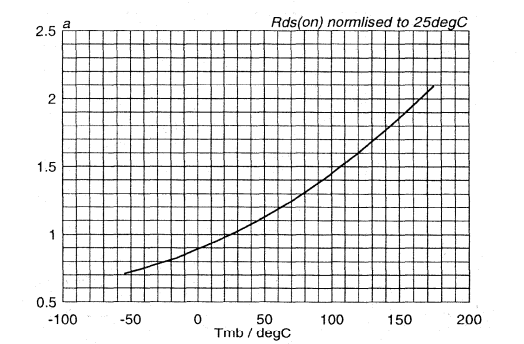


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\ ˚C} = f(T_j)$; I_D = 25 A; V_{GS} = 10 V

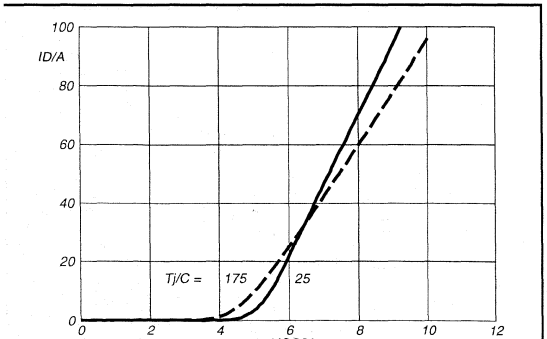


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

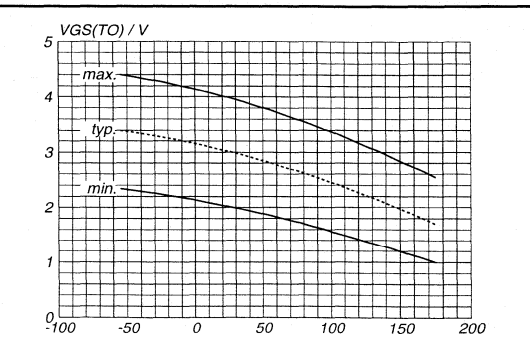


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

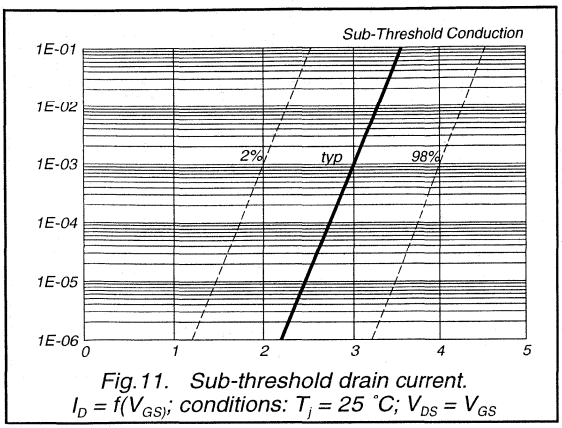


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

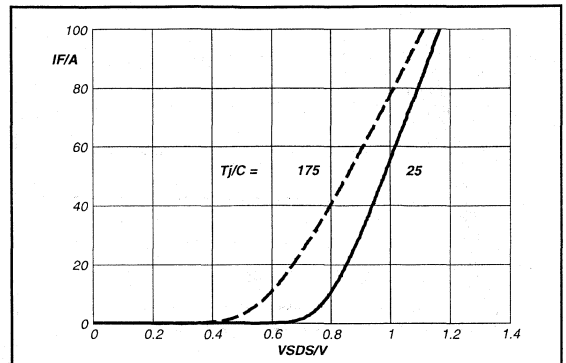


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

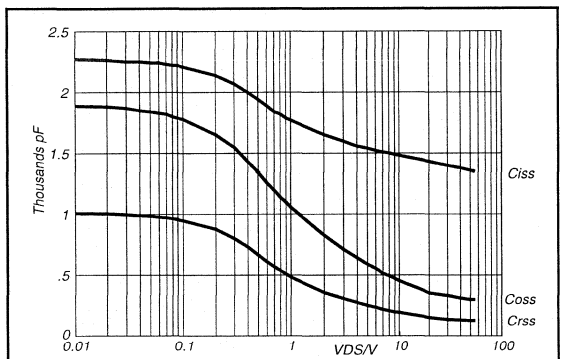


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

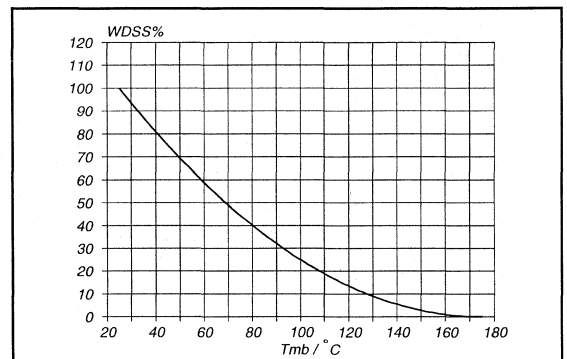


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 49$ A

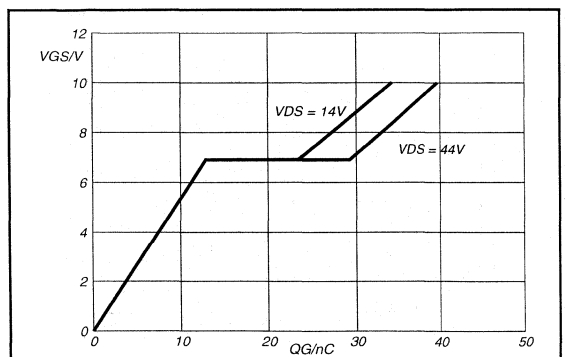


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 50$ A; parameter V_{DS}

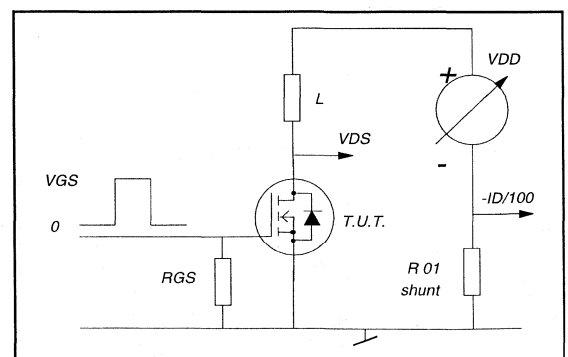


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

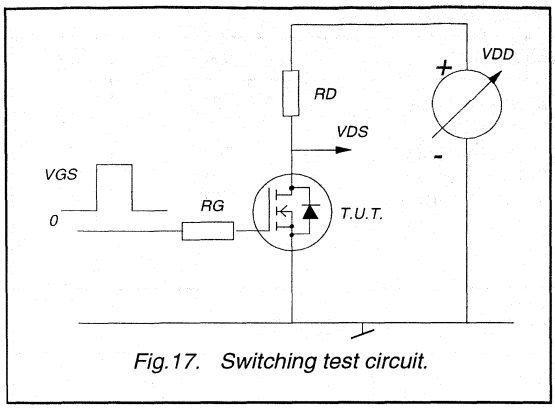


Fig.17. Switching test circuit.

TrenchMOS™ transistor
Standard level FET

BUK7524-55

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope using '**trench**' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

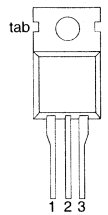
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	45	A
P_{tot}	Total power dissipation	103	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	24	mΩ

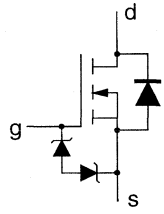
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	16	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	45	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	31	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	180	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	103	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.45	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55°C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.0	3.0	4.0	V
		T_j = 175°C	1.0	-	-	V
		T_j = -55°C	-	-	4.4	
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175°C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175°C	-	-	20	µA
$\pm V_{(BR)GSS}$	Gate source breakdown voltage	I_G = ±1 mA;	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A	-	19	24	mΩ
		T_j = 175°C	-	-	50	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	4	11	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1100	1500	pF
C_{oss}	Output capacitance		-	280	340	pF
C_{rss}	Feedback capacitance		-	130	180	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	12	18	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 10 Ω	-	19	35	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	25	35	ns
t_f	Turn-off fall time		-	18	25	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	45	A
I_{DRM}	Pulsed reverse drain current		-	-	160	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 40 A; V_{GS} = 0 V	-	1.0	-	
t_{rr}	Reverse recovery time	I_F = 40 A; -dI_F/dt = 100 A/µs;	-	40	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.07	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 40 A; $V_{DD} \leq$ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	80	mJ

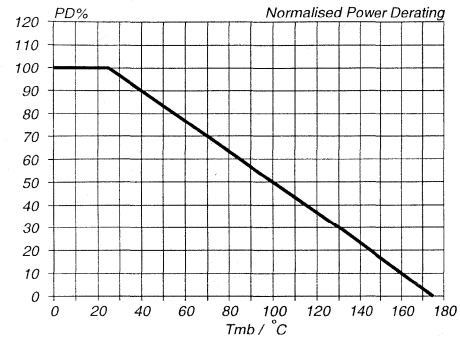


Fig.1. Normalised power dissipation. PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

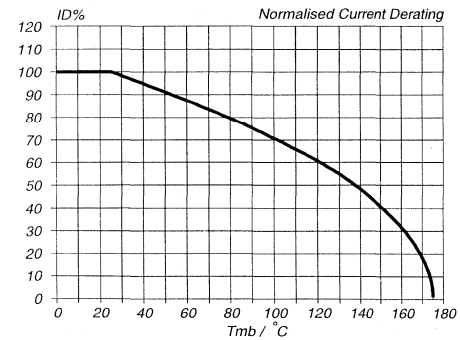


Fig.2. Normalised continuous drain current. ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

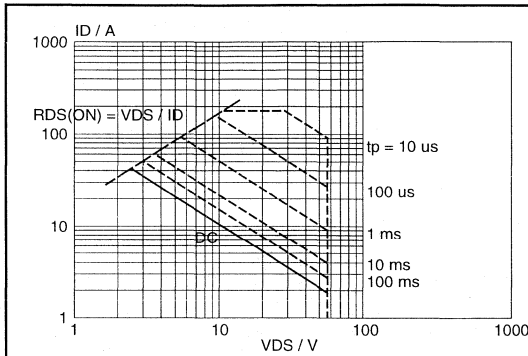


Fig.3. Safe operating area. T_{mb} = 25 °C I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

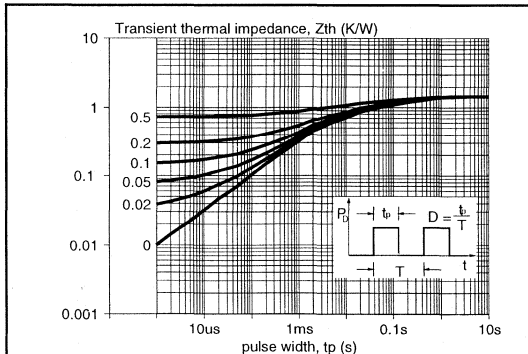


Fig.4. Transient thermal impedance. $Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

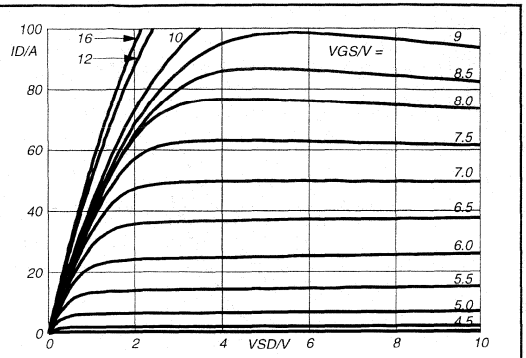


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

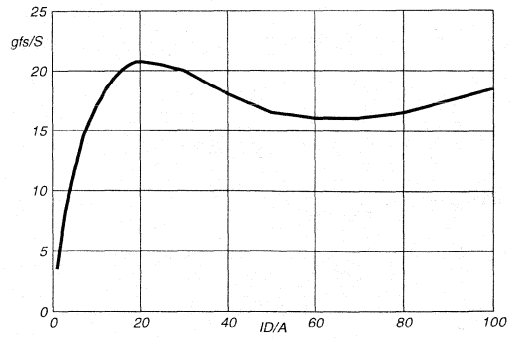


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

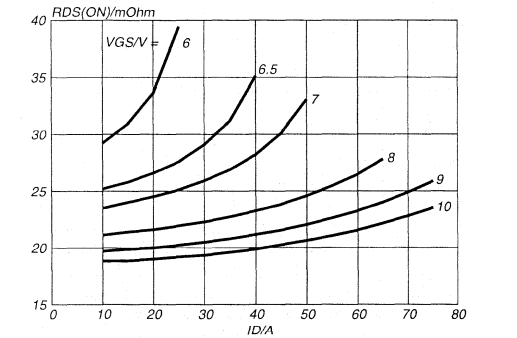


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

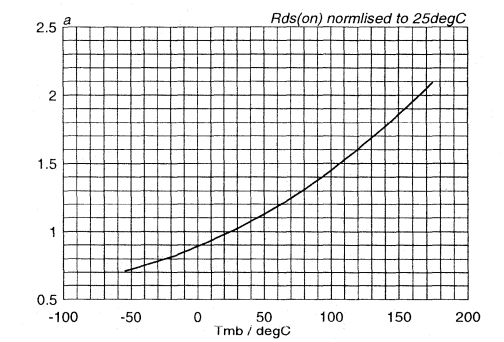


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\ ^{\circ}C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

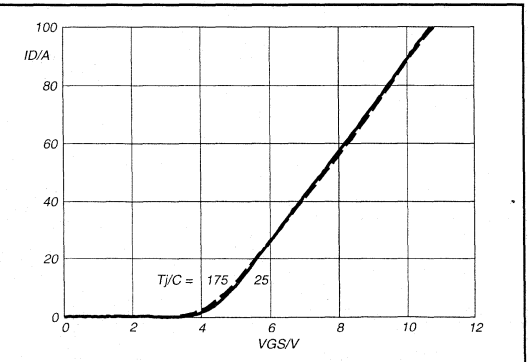


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

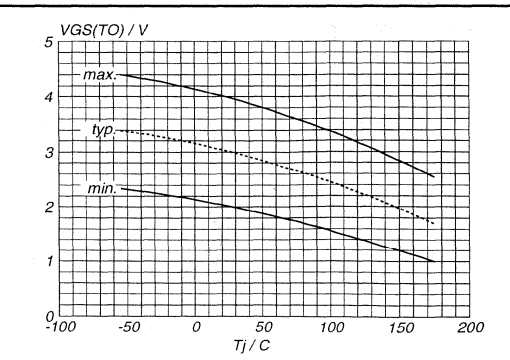


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

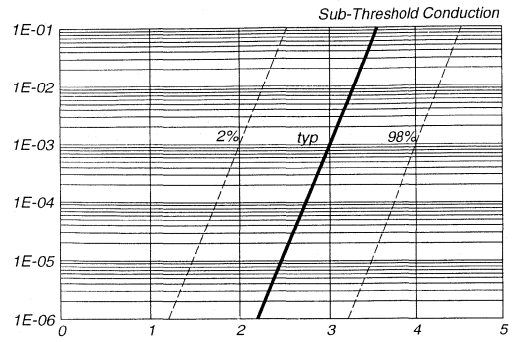


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

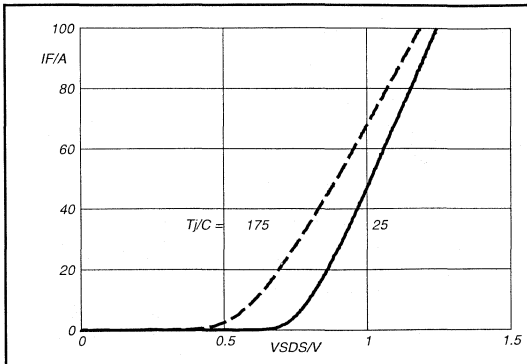


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

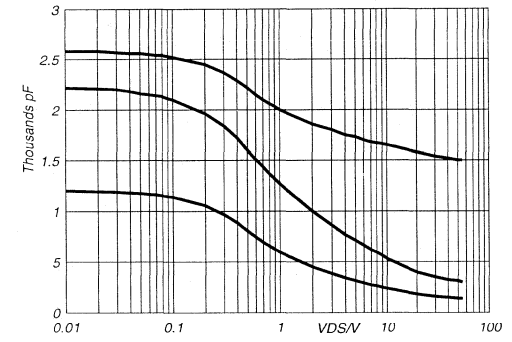


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

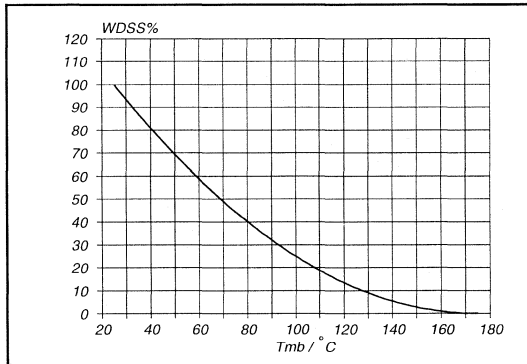


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: I_D = 75 A

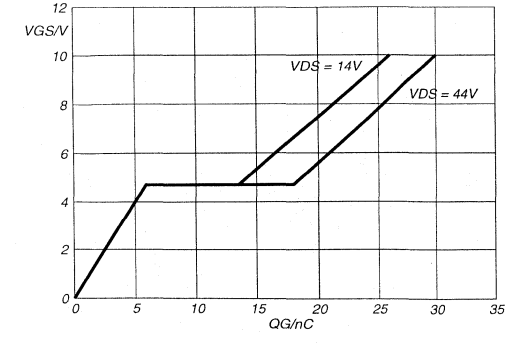


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 50 A; parameter V_{DS}

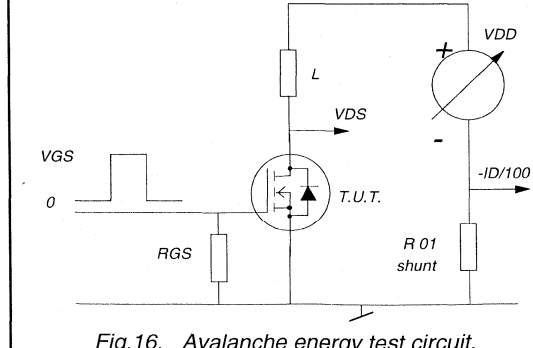


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

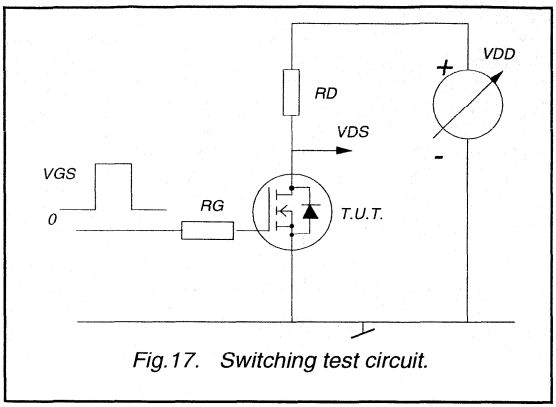


Fig.17. Switching test circuit.

TrenchMOS™ transistor Standard level FET

BUK7528-55

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope using '**trench**' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

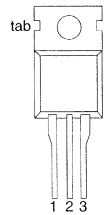
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	40	A
P_{tot}	Total power dissipation	96	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	28	mΩ

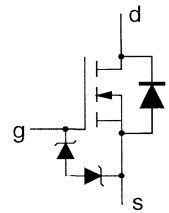
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	16	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	40	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	28	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	160	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	96	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.56	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55°C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.0	3.0	4.0	V
		T_j = 175°C	1.0	-	-	V
		T_j = -55°C	-	-	4.4	
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175°C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	0.04	1	µA
		T_j = 175°C	-	-	20	µA
$\pm V_{(BR)GSS}$	Gate source breakdown voltage	I_G = ±1 mA;	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 20 A	-	22	28	mΩ
		T_j = 175°C	-	-	59	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	4	-	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1000	1300	pF
C_{oss}	Output capacitance		-	240	300	pF
C_{rss}	Feedback capacitance		-	115	160	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	13	19	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 10 Ω	-	50	75	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	27	35	ns
t_f	Turn-off fall time		-	20	27	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	40	A
I_{DRM}	Pulsed reverse drain current		-	-	160	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 40 A; V_{GS} = 0 V	-	1.0	-	
t_{rr}	Reverse recovery time	I_F = 40 A; -dI_F/dt = 100 A/µs;	-	41	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.16	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 35 A; $V_{DD} \leq$ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	70	mJ

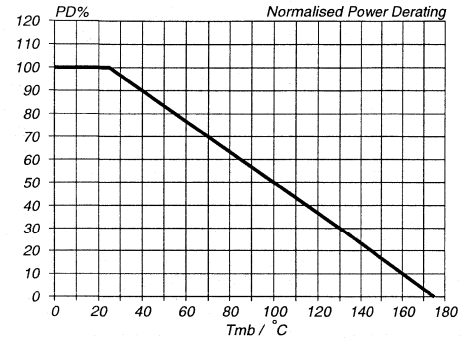


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

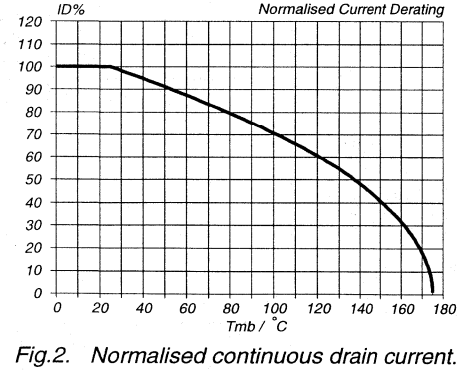


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 10 V

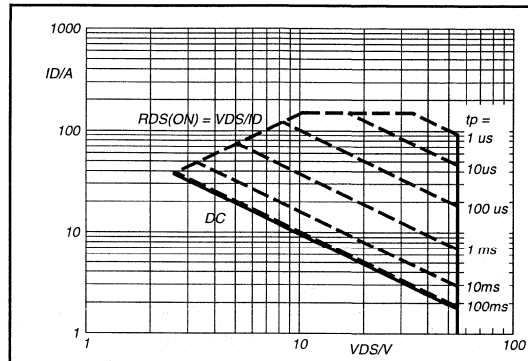


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

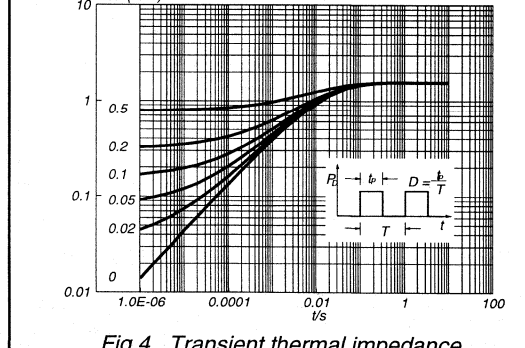


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

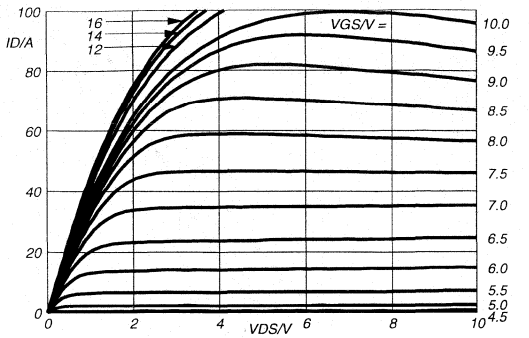


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

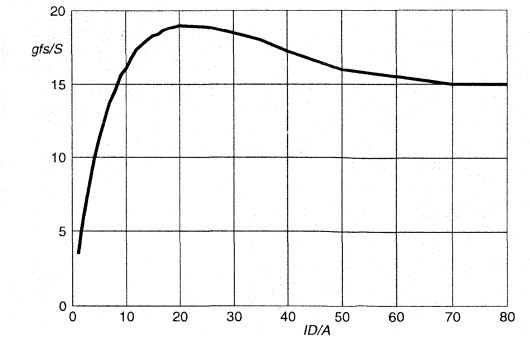


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

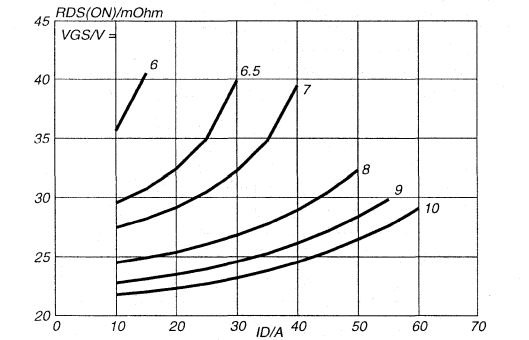


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

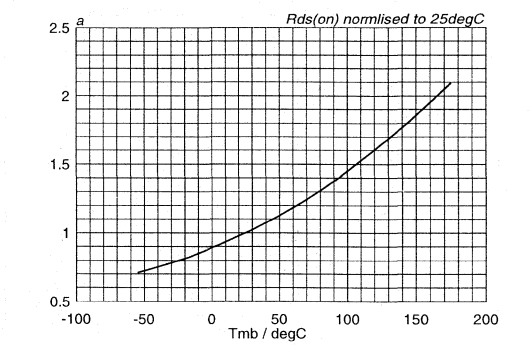


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\ ^\circ C} = f(T_j)$; I_D = 20 A; V_{GS} = 10 V

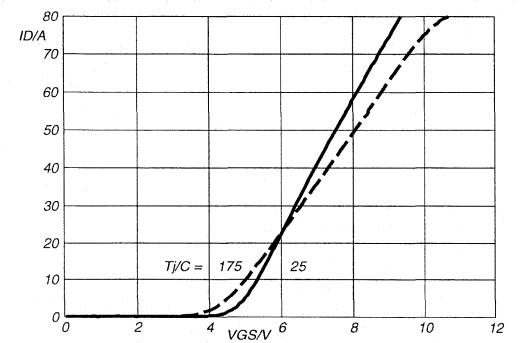


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

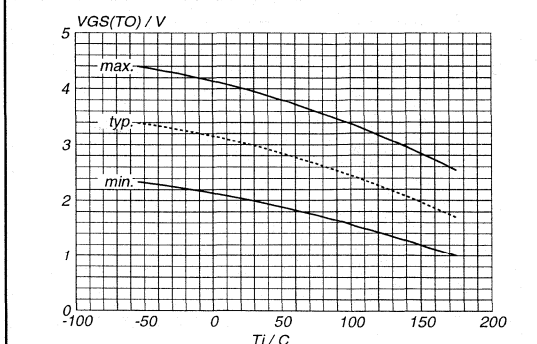


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

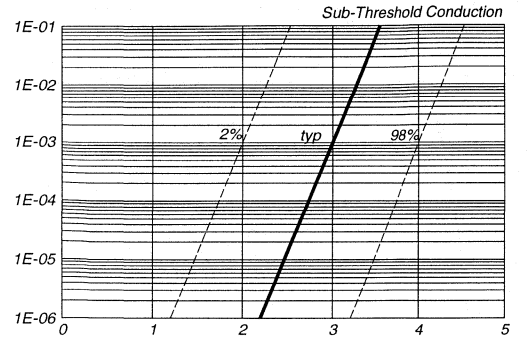


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

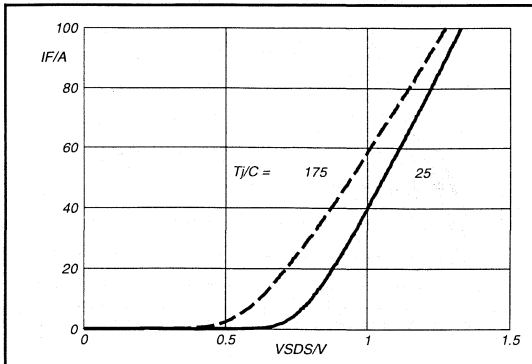


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

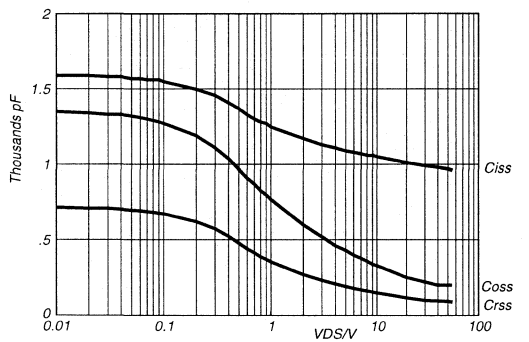


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

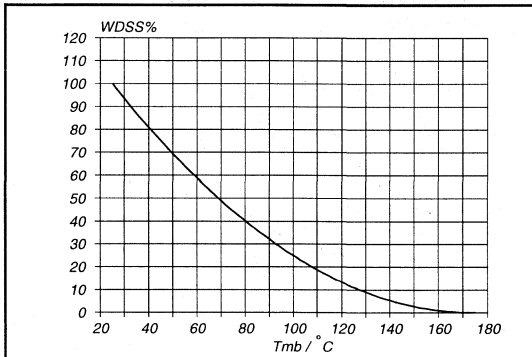


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 40$ A

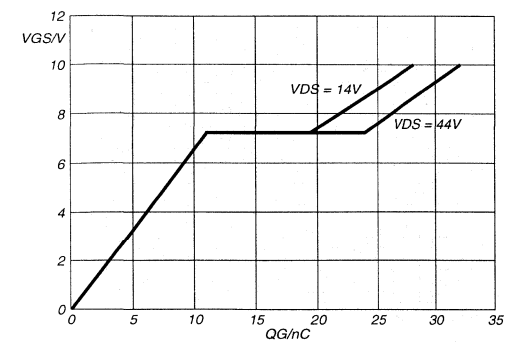


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 40$ A; parameter V_{DS}

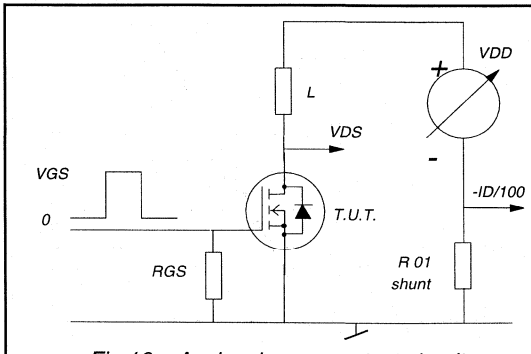


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

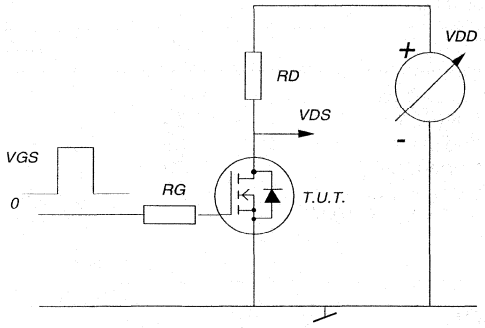


Fig.17. Switching test circuit.

TrenchMOS™ transistor Standard level FET

BUK7535-55

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope using '**trench**' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

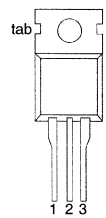
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	34	A
P_{tot}	Total power dissipation	85	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	35	mΩ

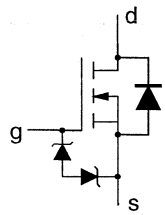
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	16	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	34	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	24	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	136	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	85	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.75	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.0	3.0	4.0	V
		T_j = 175˚C	1.0	-	-	V
		T_j = -55˚C	-	-	4.4	
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	0.04	1	µA
		T_j = 175˚C	-	-	20	µA
$\pm V_{(BR)GSS}$	Gate source breakdown voltage	I_G = ±1 mA;	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 17 A	-	28	35	mΩ
		T_j = 175˚C	-	-	74	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 15 A	4	-	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	700	880	pF
C_{oss}	Output capacitance		-	200	240	pF
C_{rss}	Feedback capacitance		-	100	140	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 15 A;	-	11	16	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 10 Ω	-	35	50	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	25	35	ns
t_f	Turn-off fall time		-	22	29	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	34	A
I_{DRM}	Pulsed reverse drain current		-	-	136	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 34 A; V_{GS} = 0 V	-	1.0	-	
t_{rr}	Reverse recovery time	I_F = 34 A; -dI_F/dt = 100 A/µs;	-	40	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.16	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 20 A; $V_{DD} \leq$ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	45	mJ

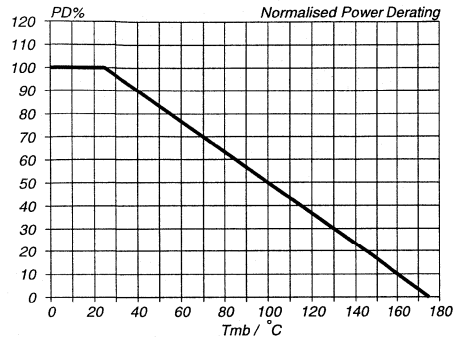


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

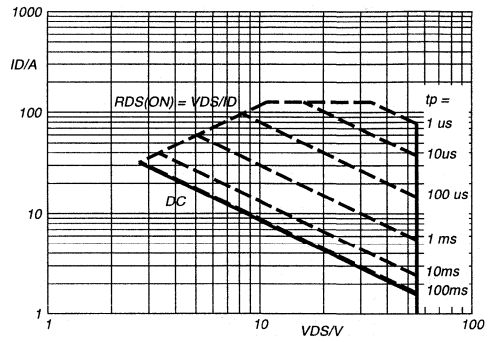


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

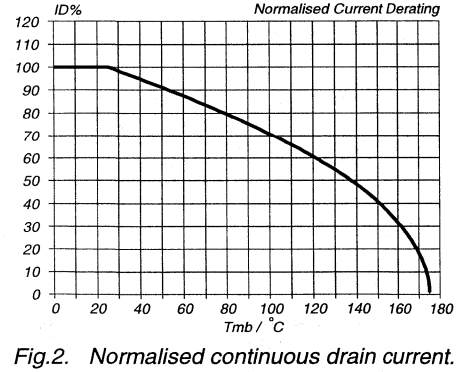


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 10 V

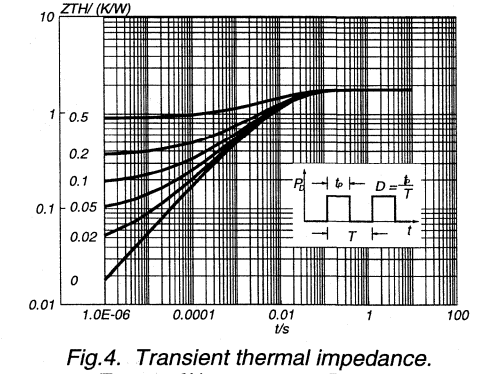


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

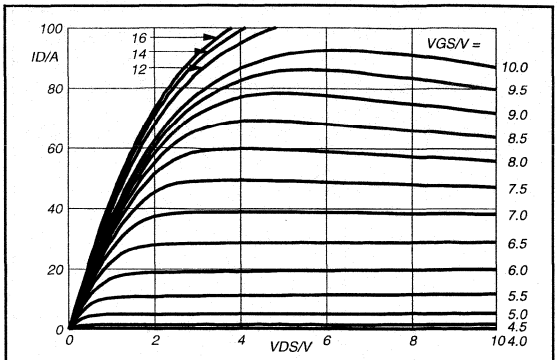


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

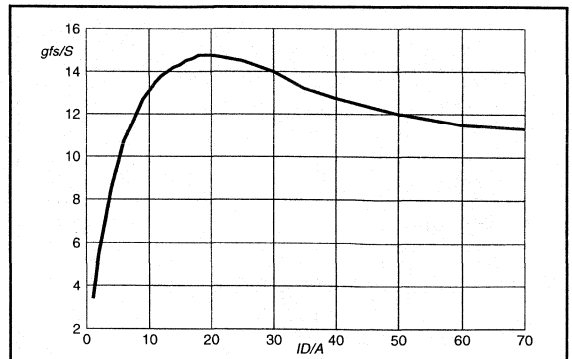


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

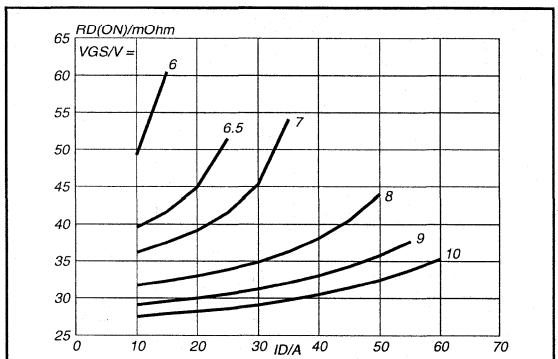


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

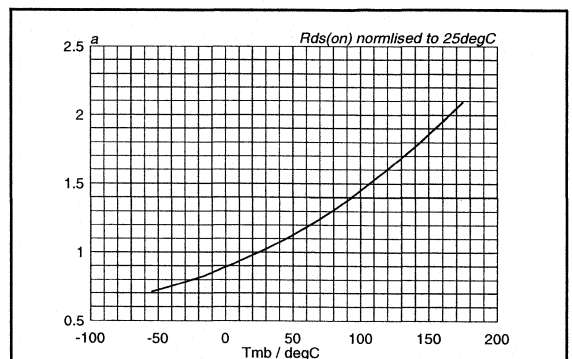


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,˚C} = f(T_j)$; I_D = 17 A; V_{GS} = 10 V

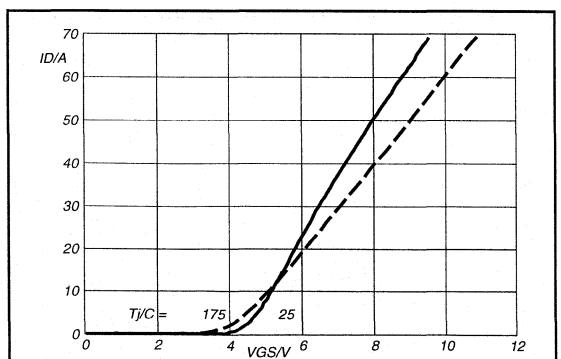


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

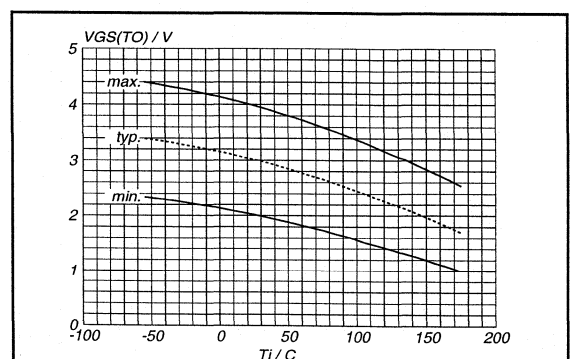


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

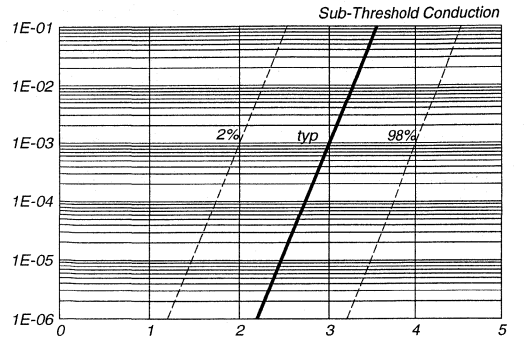


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

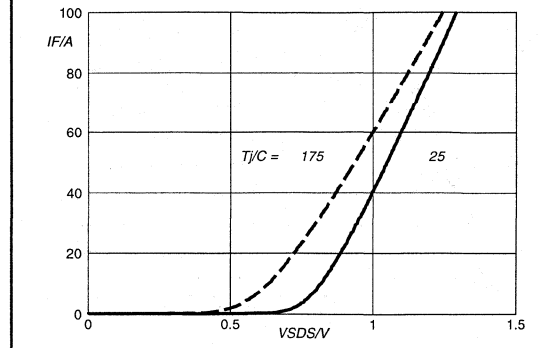


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

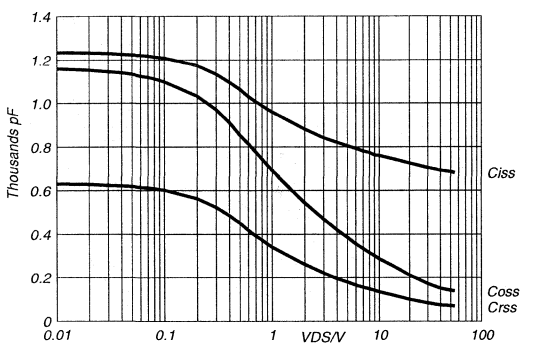


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

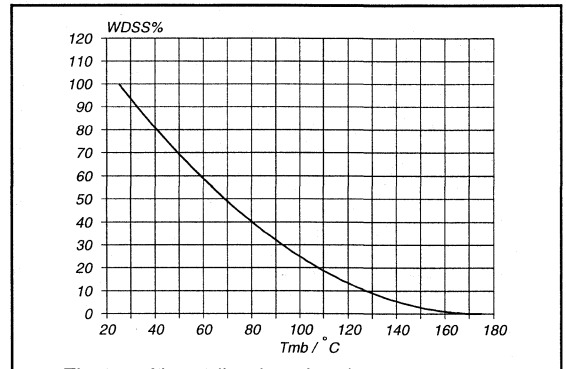


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: I_D = 32 A

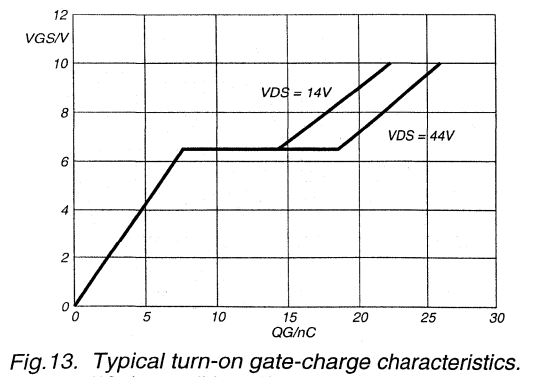


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 30 A; parameter V_{DS}

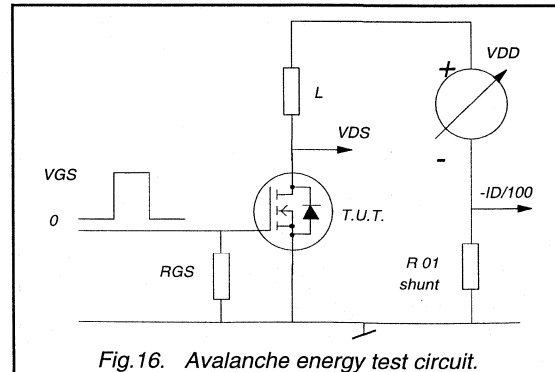


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

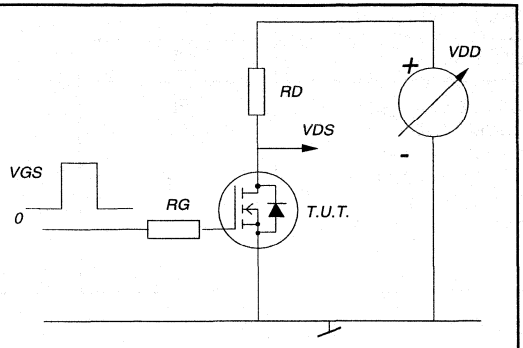


Fig.17. Switching test circuit.

TrenchMOS™ transistor Standard level FET

BUK7575-55

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope using '**trench**' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

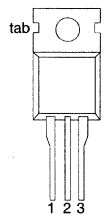
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	19.7	A
P_{tot}	Total power dissipation	61	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	75	mΩ

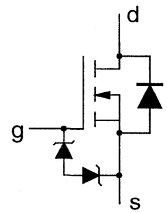
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	16	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	19.7	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	13.9	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	79	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	61	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	2.46	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;		55	-	-	V
			T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA		2.0	3.0	4.0	V
			T_j = 175˚C	1.0	-	-	V
			T_j = -55˚C	-	-	4.4	
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;		-	0.05	10	µA
			T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V		-	0.04	1	µA
			T_j = 175˚C	-	-	20	µA
$\pm V_{(BR)GSS}$	Gate source breakdown voltage	I_G = ±1 mA;		16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 10 A		-	60	75	mΩ
			T_j = 175˚C	-	-	157	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 10 A	1	-	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	365	500	pF
C_{oss}	Output capacitance		-	110	135	pF
C_{rss}	Feedback capacitance		-	60	85	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 10 A;	-	9	14	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 10 Ω	-	16	21	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	14	25	ns
t_f	Turn-off fall time		-	13	20	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	19.7	A
I_{DRM}	Pulsed reverse drain current		-	-	79	A
V_{SD}	Diode forward voltage	I_F = 19.7 A; V_{GS} = 0 V	-	0.95	1.2	V
t_{rr}	Reverse recovery time	I_F = 19.7 A; -dI_F/dt = 100 A/µs;	-	32	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.12	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 10 A; $V_{DD} \leq$ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	30	mJ

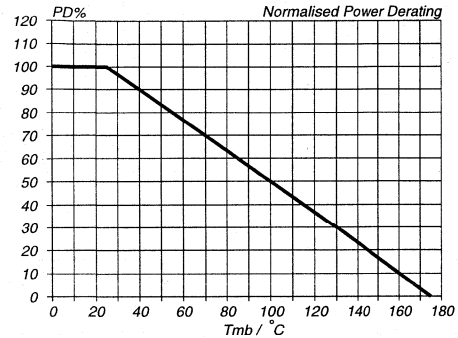


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

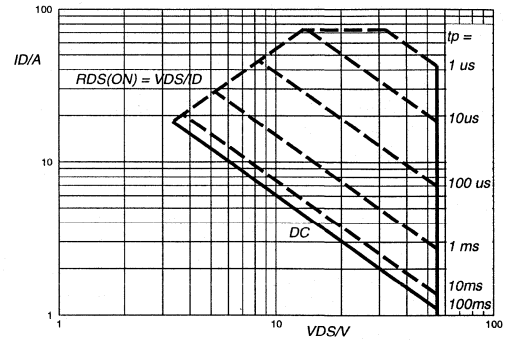


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

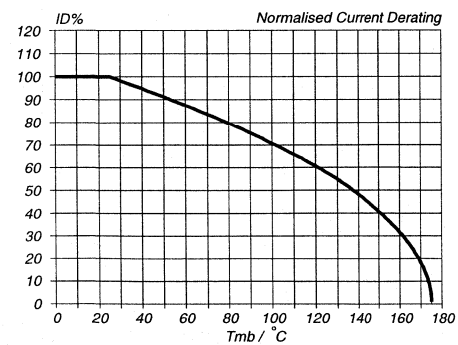


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 10 V

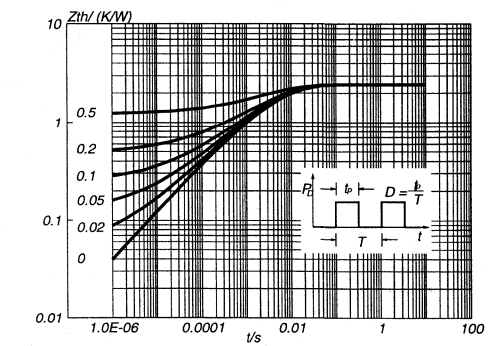


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

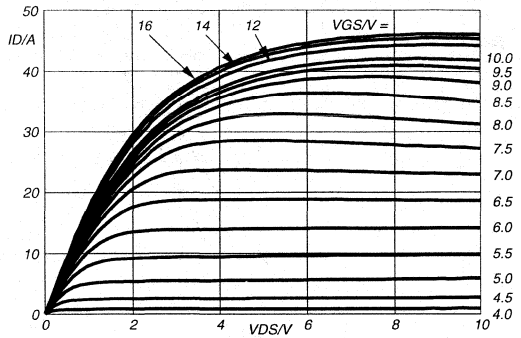


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

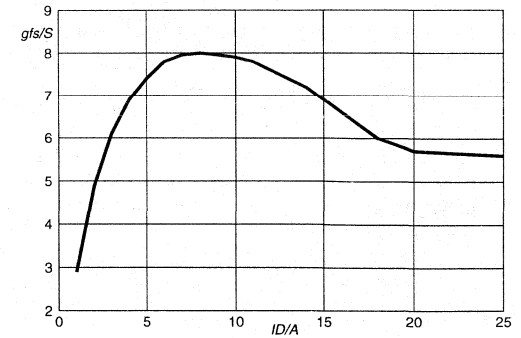


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

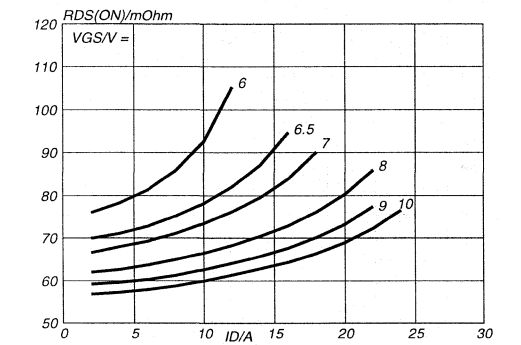


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

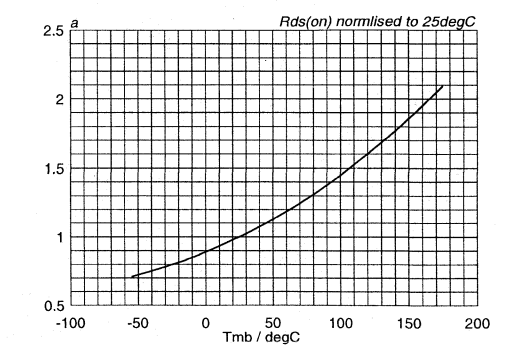


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 10 A; V_{GS} = 10 V

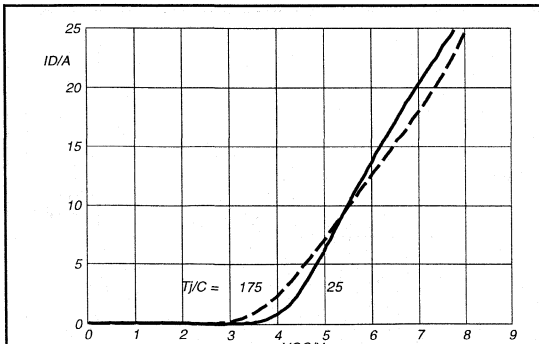


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

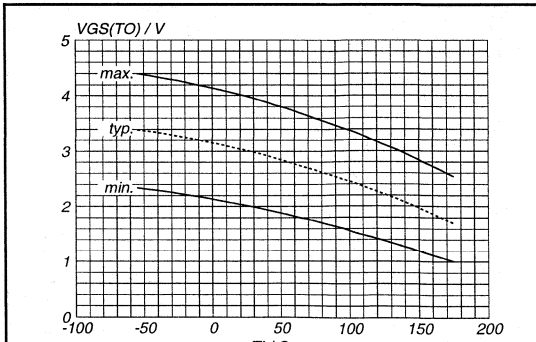


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

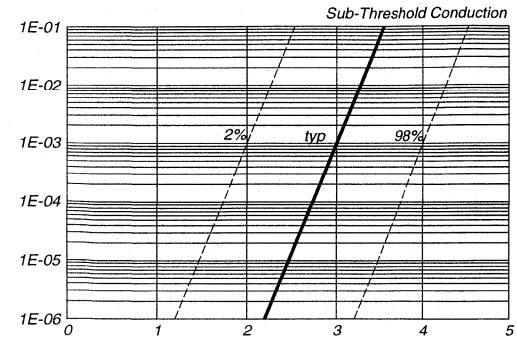


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

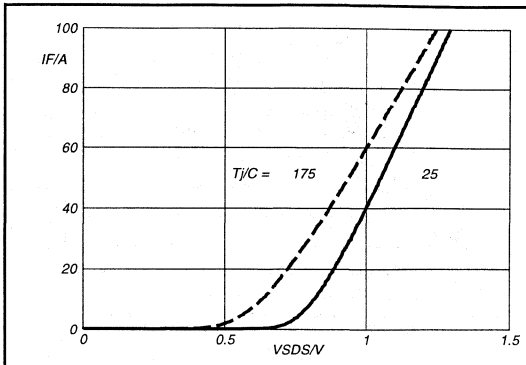


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

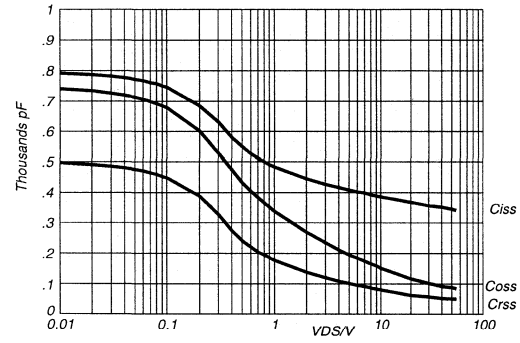


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

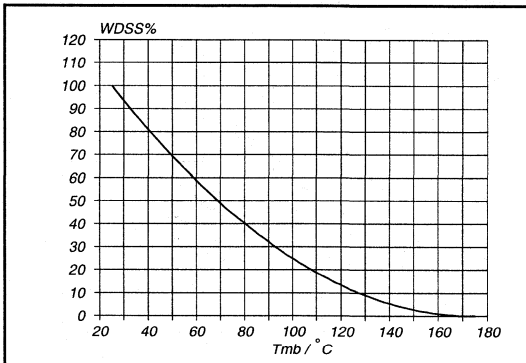


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 17$ A

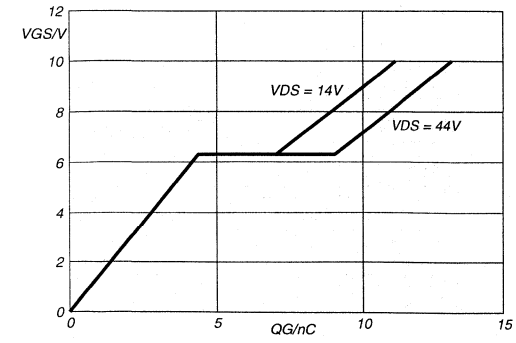


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 20$ A; parameter V_{DS}

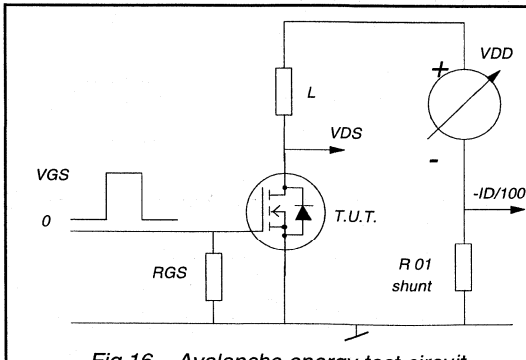


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

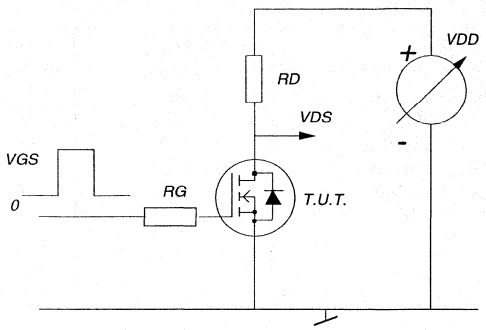


Fig.17. Switching test circuit.

TrenchMOS™ transistor
Standard level FET

BUK7606-30

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope suitable for surface mounting using **'trench'** technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

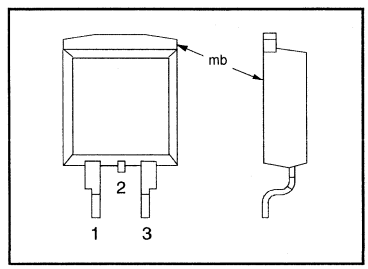
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	30	V
I_D	Drain current (DC)	75	A
P_{tot}	Total power dissipation	188	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	6	mΩ

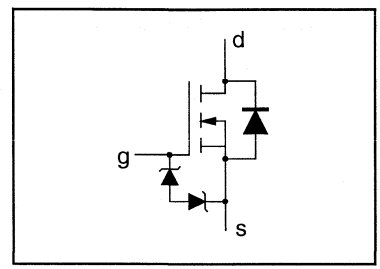
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	30	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	30	V
$\pm V_{GS}$	Gate-source voltage	-	-	20	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	75	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	53	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	240	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	188	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	0.8	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board	50	-	K/W

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	30	-	-	V
		T_j = -55˚C	27	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.0	3.0	4.0	V
		T_j = 175˚C	1.0	-	-	V
		T_j = -55˚C	-	-	4.4	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 30 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	20	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A	-	5	6	mΩ
		T_j = 175˚C	-	-	11	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	12	25	-	S
$Q_{g(tot)}$	Total gate charge	I_D = 75 A; V_{DD} = 24 V; V_{GS} = 10 V	-	84	-	nC
Q_{gs}	Gate-source charge		-	14	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	28	-	nC
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	4000	-	pF
C_{oss}	Output capacitance		-	1150	-	pF
C_{rss}	Feedback capacitance		-	450	-	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 15 V; I_D = 25 A;	-	40	50	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 5 Ω	-	70	105	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	100	140	ns
t_f	Turn-off fall time		-	50	70	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead solder point to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead solder point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	75	A
I_{DRM}	Pulsed reverse drain current		-	-	240	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.85	1.2	V
		I_F = 75 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 75 A; -dI_F/dt = 100 A/µs;	-	100	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 25 V	-	0.2	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 75 A; $V_{DD} \leq$ 15 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	500	mJ

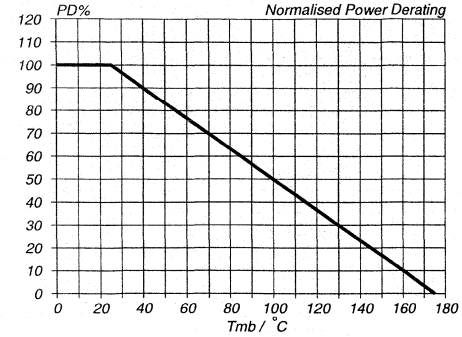


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

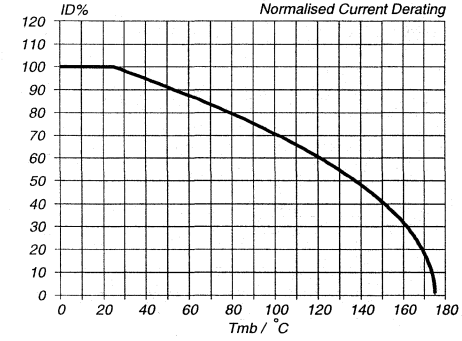


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

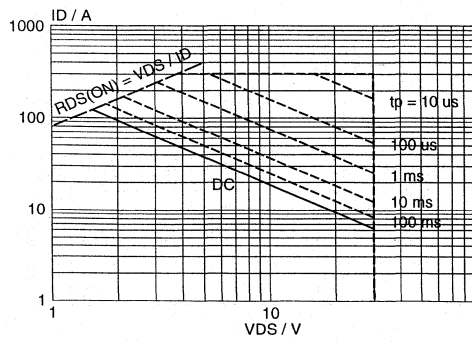


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

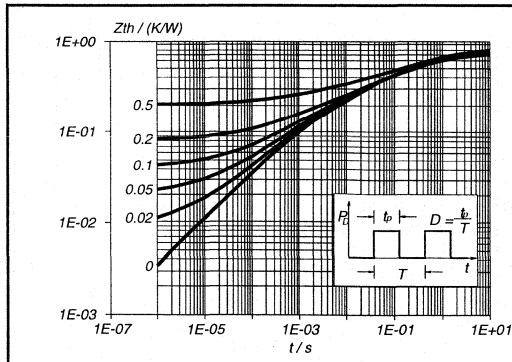


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

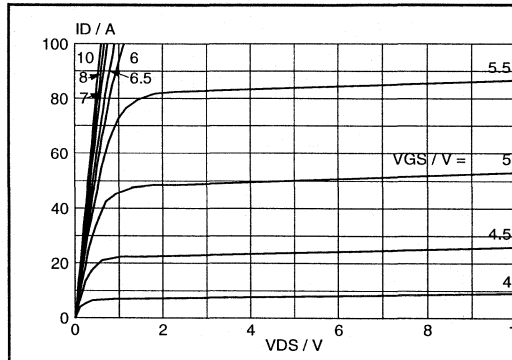


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

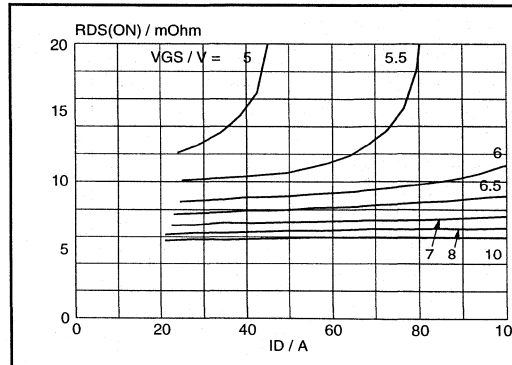


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

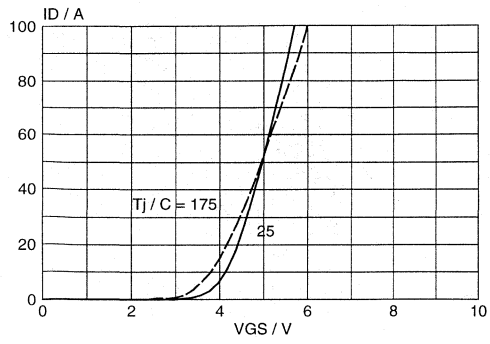


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

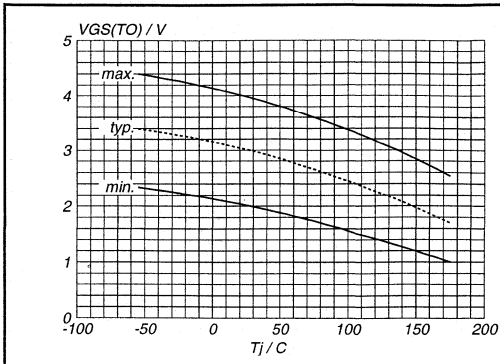


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

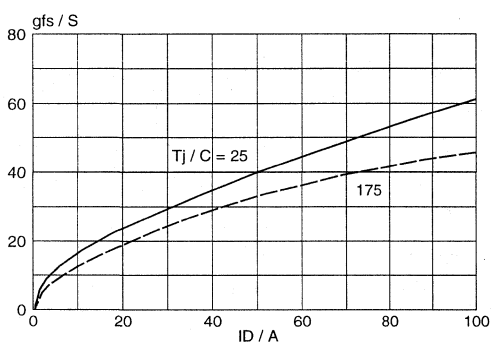


Fig.8. Typical transconductance, T_j = 25 ˚C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

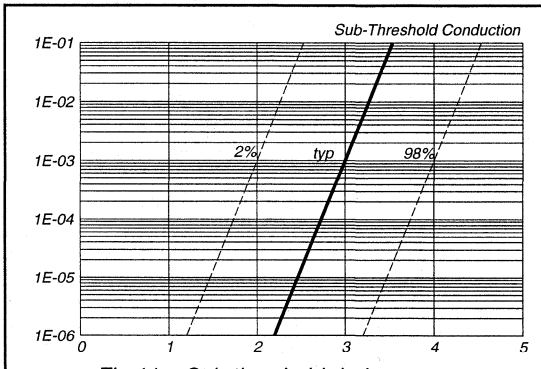


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

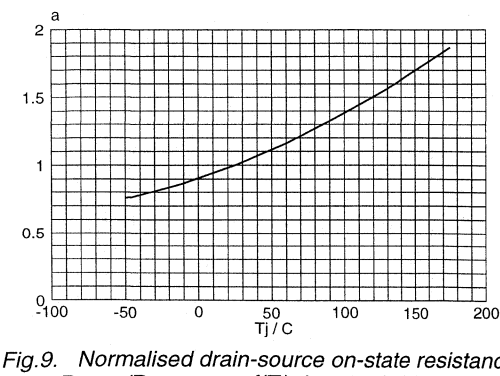


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ ^{\circ}C} = f(T_j)$; I_D = 25 A; V_{GS} = 10 V

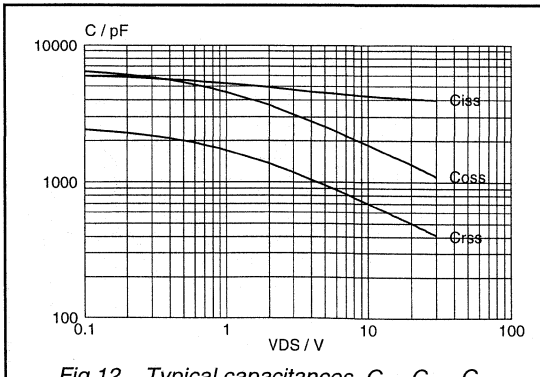


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

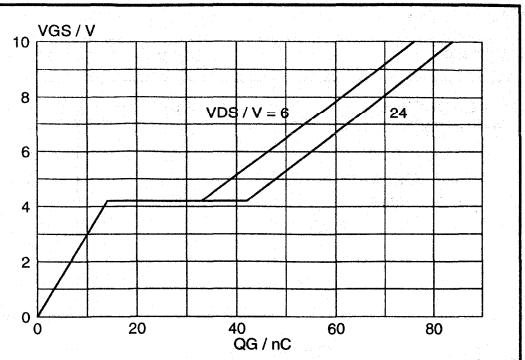


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 75$ A; parameter V_{DS}

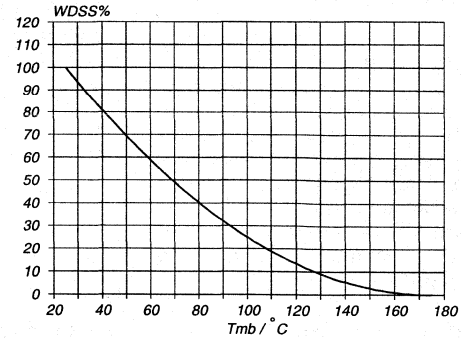


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 75$ A

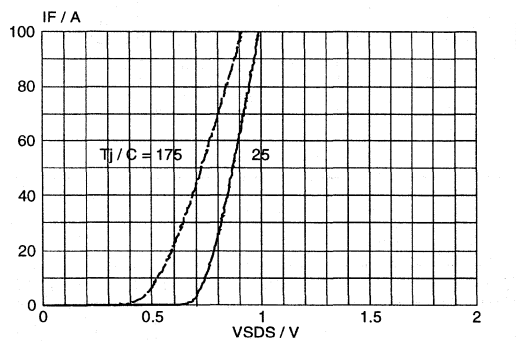


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

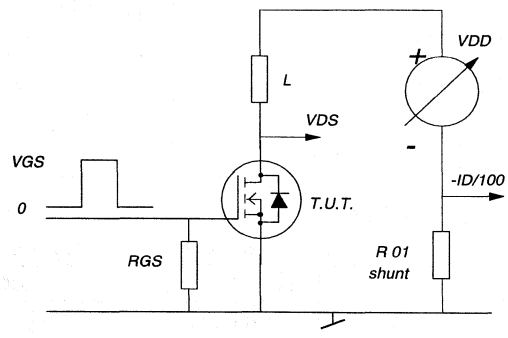


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

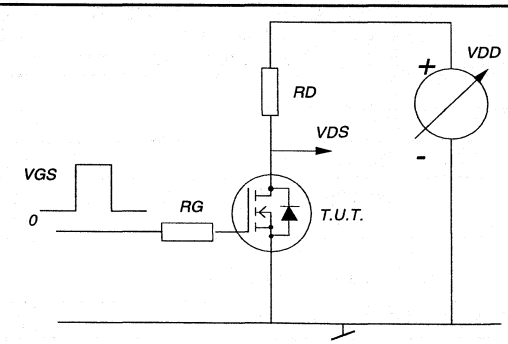


Fig.17. Switching test circuit.

TrenchMOS™ transistor
Standard level FET

BUK7608-55

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope suitable for surface mounting. Using **'trench'** technology the device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

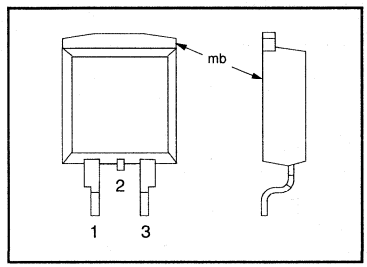
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	75	A
P_{tot}	Total power dissipation	187	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	8	mΩ

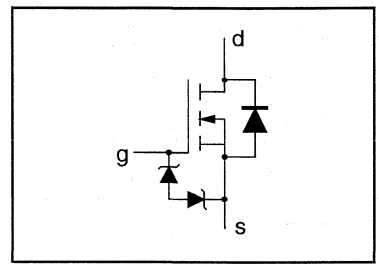
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	16	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	75	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	65	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	240	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	187	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	0.8	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	Minimum footprint, FR4 board	50	-	K/W

STATIC CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2	3.0	4.0	V
		T_j = 175˚C	1	-	-	V
		T_j = -55˚C	-	-	4.4	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	20	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A	-	6.5	8	mΩ
		T_j = 175˚C	-	-	17	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	10	45	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	3600	4500	pF
C_{oss}	Output capacitance		-	830	1000	pF
C_{rss}	Feedback capacitance		-	320	440	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	27	40	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 10 Ω	-	70	105	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	100	140	ns
t_f	Turn-off fall time		-	50	70	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	75	A
I_{DRM}	Pulsed reverse drain current		-	-	240	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.85	1.2	V
		I_F = 75 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 75 A; -dI_F/dt = 100 A/µs;	-	65	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.18	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 75 A; $V_{DD} \leq$ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	500	mJ

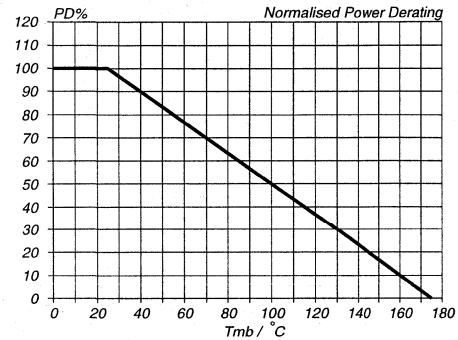


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

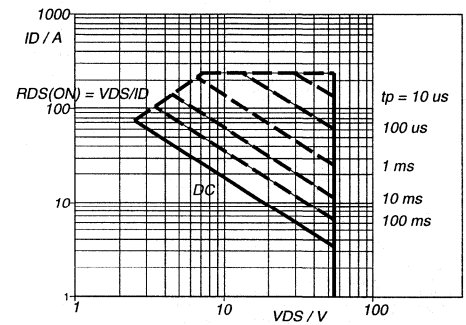


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

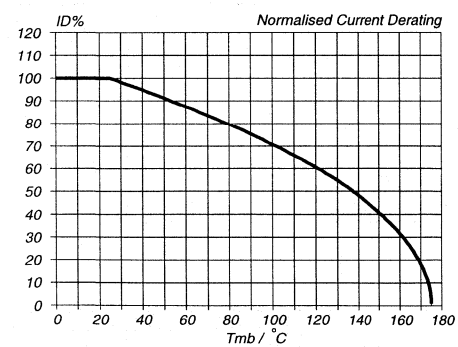


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

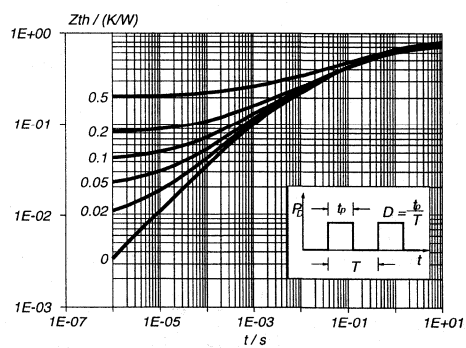


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

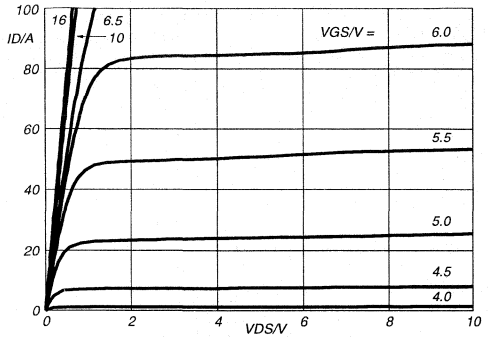


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

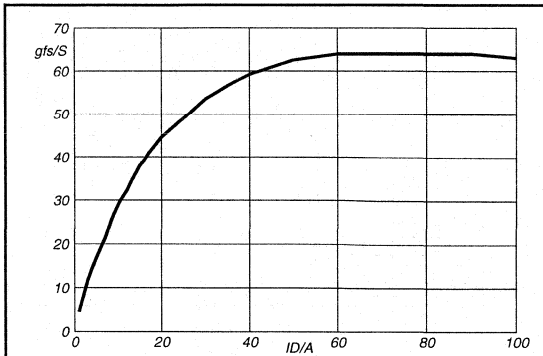


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

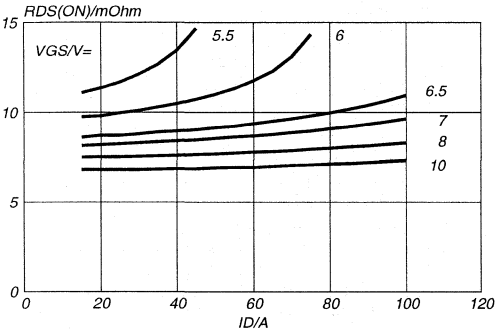


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

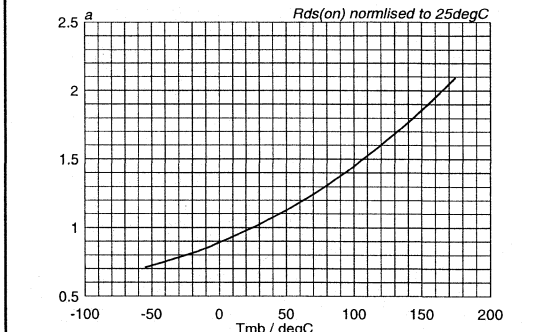


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\ ˚C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

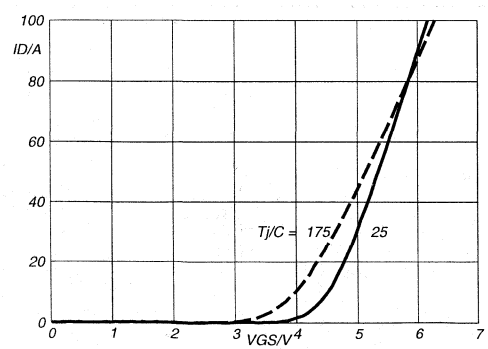


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

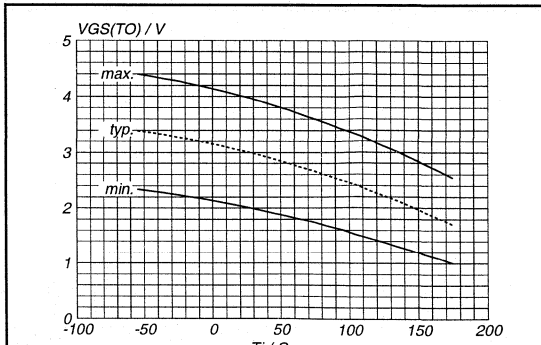


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

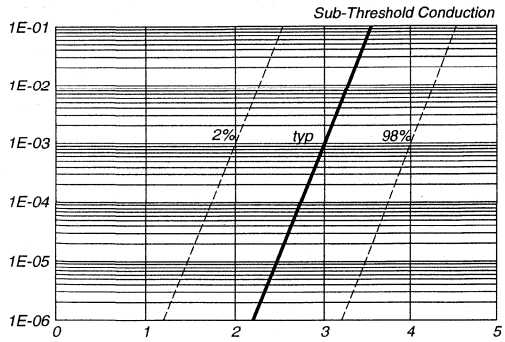


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

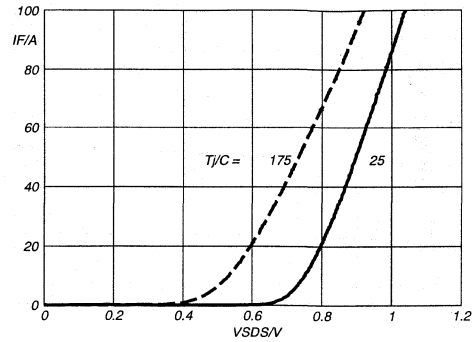


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

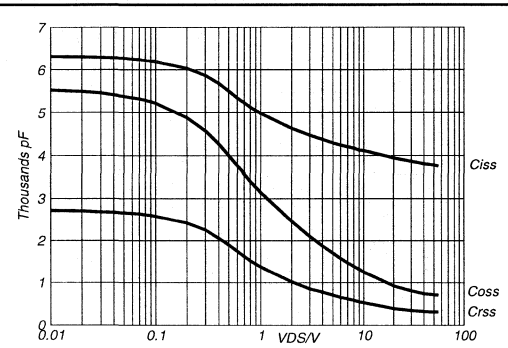


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

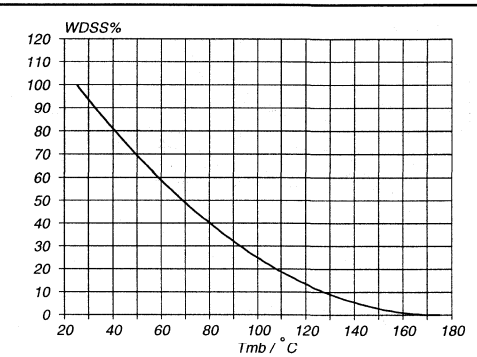


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 75$ A

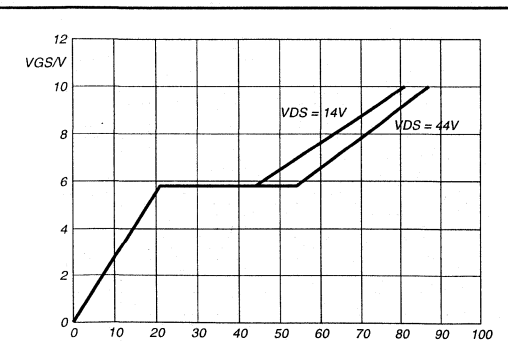


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 50$ A; parameter V_{DS}

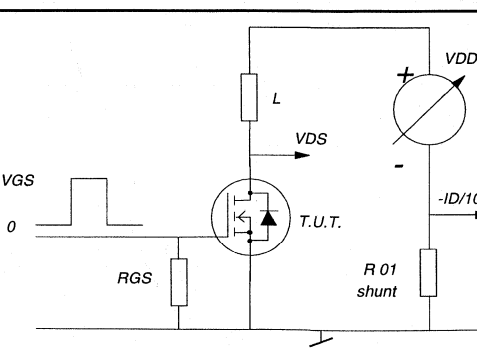


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

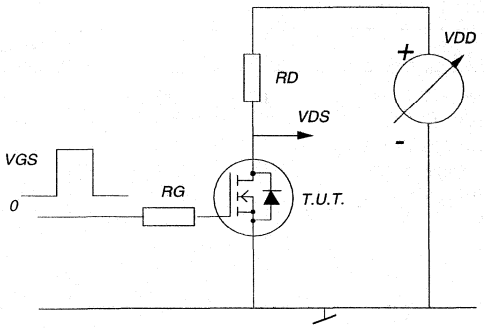


Fig.17. Switching test circuit.

TrenchMOS™ transistor
Standard level FET

BUK7610-30

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope suitable for surface mounting using '**trench**' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

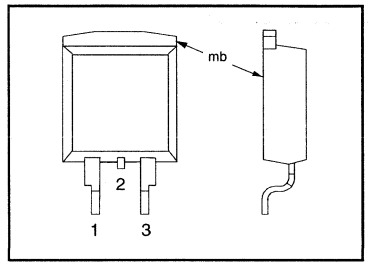
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	30	V
I_D	Drain current (DC)	75	A
P_{tot}	Total power dissipation	142	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	10.5	mΩ

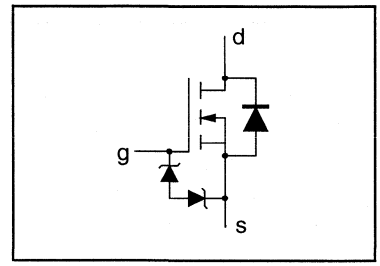
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	30	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	30	V
$\pm V_{GS}$	Gate-source voltage	-	-	20	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	75	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	53	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	240	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	142	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.05	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board	50	-	K/W

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	30	-	-	V
		T_j = -55˚C	27	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2	3.0	4.0	V
		T_j = 175˚C	1	-	-	V
		T_j = -55˚C	-	-	4.4	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 30 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	20	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A	-	9	10.5	mΩ
		T_j = 175˚C	-	-	19.5	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	9	18	-	S
$Q_{g(tot)}$	Total gate charge	I_D = 75 A; V_{DD} = 24 V; V_{GS} = 10 V	-	51	-	nC
Q_{gs}	Gate-source charge		-	9	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	20	-	nC
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	2000	-	pF
C_{oss}	Output capacitance		-	700	-	pF
C_{rss}	Feedback capacitance		-	300	-	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 25 V; I_D = 25 A;	-	26	30	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 5 Ω	-	35	85	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	50	60	ns
t_f	Turn-off fall time		-	30	45	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead solder point to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead solder point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	75	A
I_{DRM}	Pulsed reverse drain current		-	-	240	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 75 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 75 A; -dI_F/dt = 100 A/µs;	-	95	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 25 V	-	0.15	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 45 A; $V_{DD} \leq$ 15 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	200	mJ

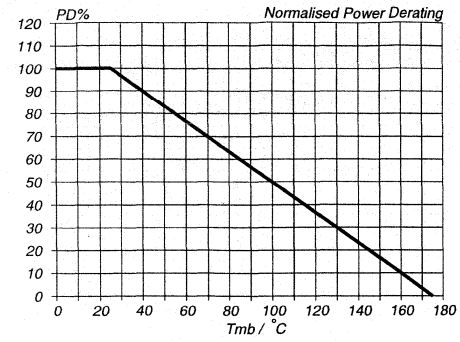


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

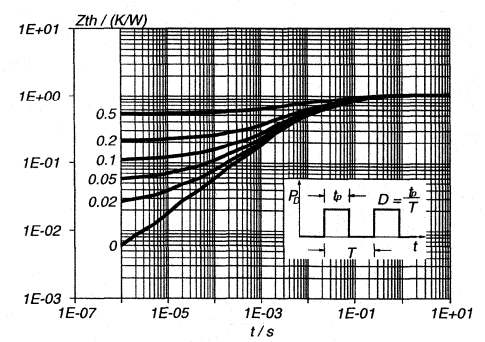


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

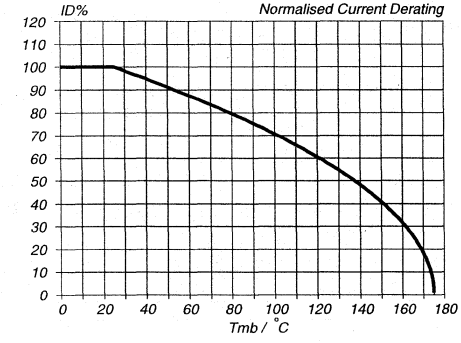


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

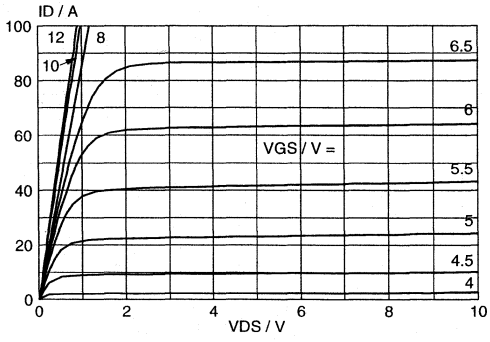


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

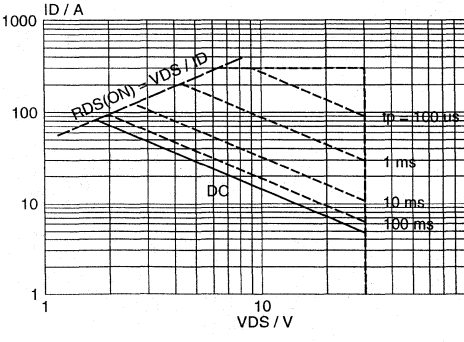


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

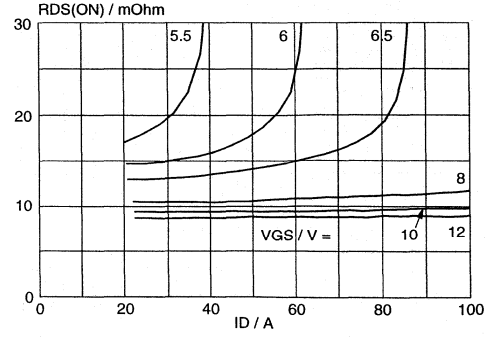


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

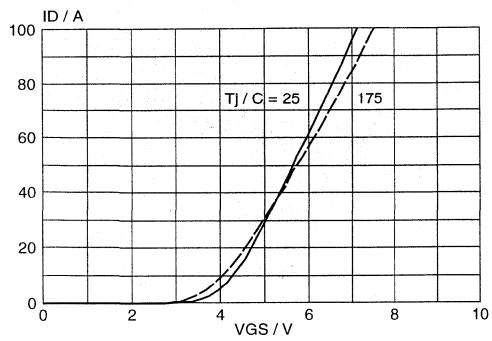


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

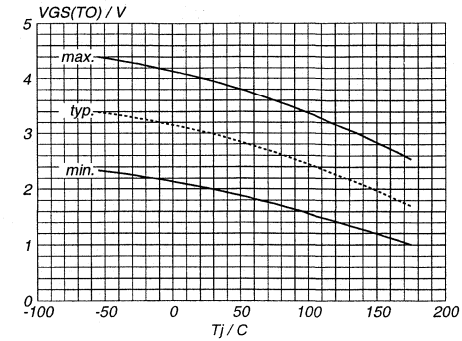


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

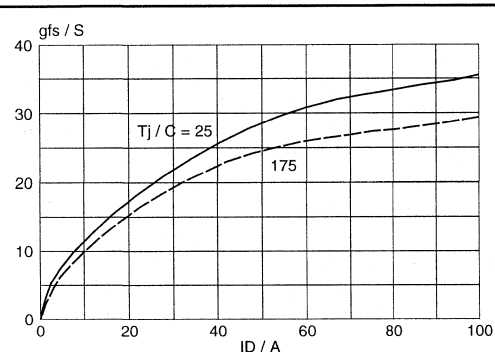


Fig.8. Typical transconductance, T_j = 25 ˚C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

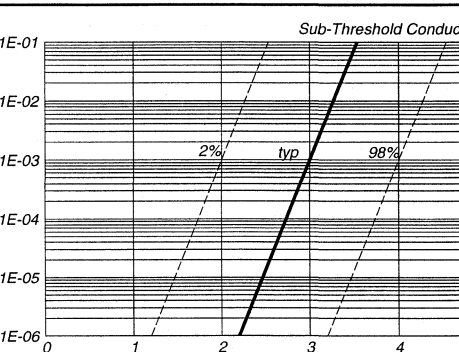


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

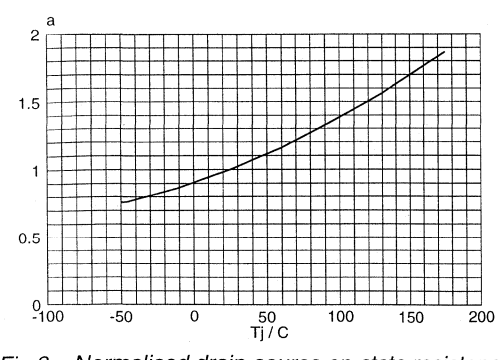


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,˚C} = f(T_j)$; I_D = 25 A; V_{GS} = 10 V

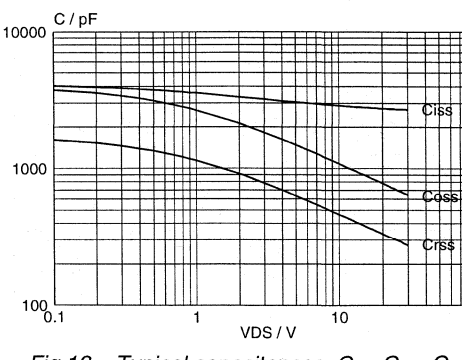


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

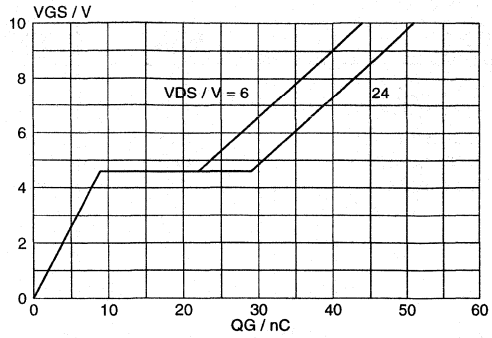


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 75$ A; parameter V_{DS}

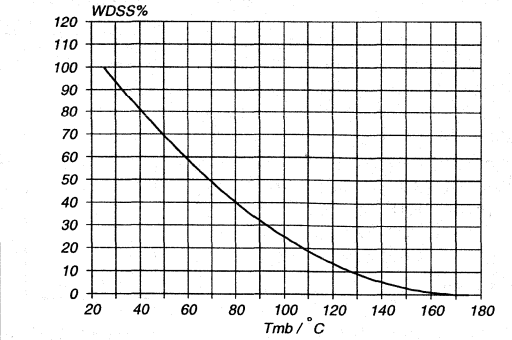


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 45$ A

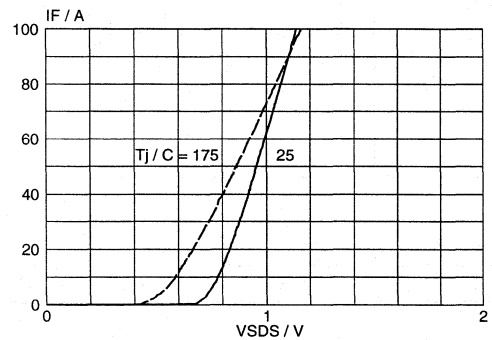


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

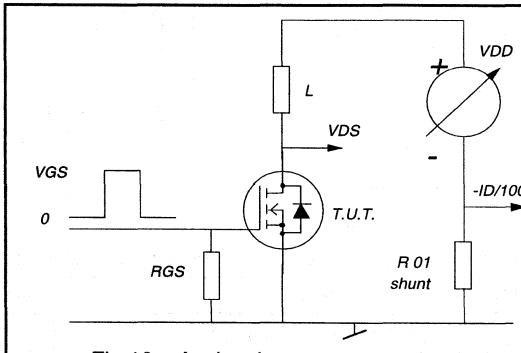


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

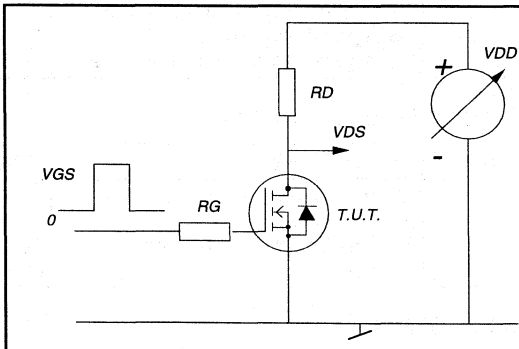


Fig.17. Switching test circuit.

TrenchMOS™ transistor Standard level FET

BUK7614-30

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope suitable for surface mounting using '**trench**' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

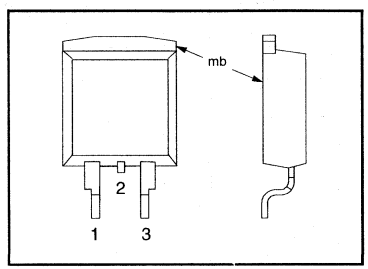
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	30	V
I_D	Drain current (DC)	69	A
P_{tot}	Total power dissipation	125	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	14	mΩ

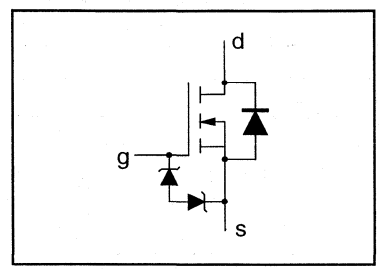
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	30	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	30	V
$\pm V_{GS}$	Gate-source voltage	-	-	20	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	69	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	48	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	240	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board	50	-	K/W

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

STATIC CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;		30	-	-	V
			T_j = -55˚C	27	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA		2.0	3.0	4.0	V
			T_j = 175˚C	1.0	-	-	V
			T_j = -55˚C	-	-	4.4	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 30 V; V_{GS} = 0 V;		-	0.05	10	µA
			T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V		-	0.02	1	µA
			T_j = 175˚C	-	-	20	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;		16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A		-	12	14	mΩ
			T_j = 175˚C	-	-	26	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	9	18	-	S
$Q_{g(tot)}$	Total gate charge	I_D = 69 A; V_{DD} = 24 V; V_{GS} = 10 V	-	38	-	nC
Q_{gs}	Gate-source charge		-	7	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	14	-	nC
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1500	-	pF
C_{oss}	Output capacitance		-	480	-	pF
C_{rss}	Feedback capacitance		-	220	-	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 25 V; I_D = 25 A;	-	22	35	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 5 Ω	-	30	60	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	40	50	ns
t_f	Turn-off fall time		-	25	38	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead solder point to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead solder point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	69	A
I_{DRM}	Pulsed reverse drain current		-	-	240	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 69 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 69 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 25 V	-	0.1	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 36 A; $V_{DD} \leq$ 15 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	125	mJ

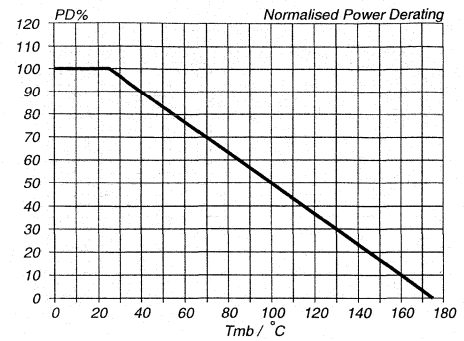


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

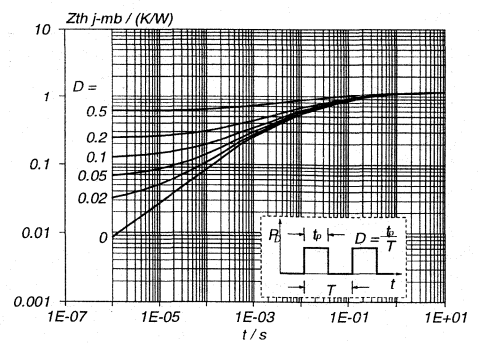


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

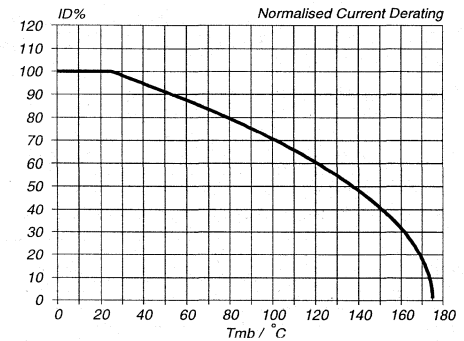


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

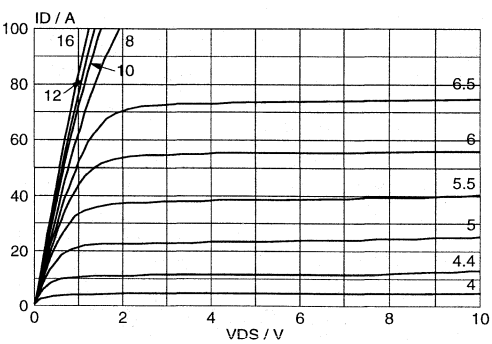


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

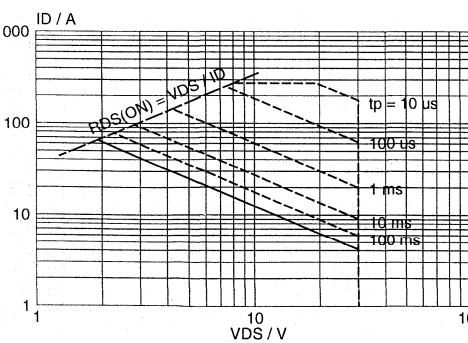


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

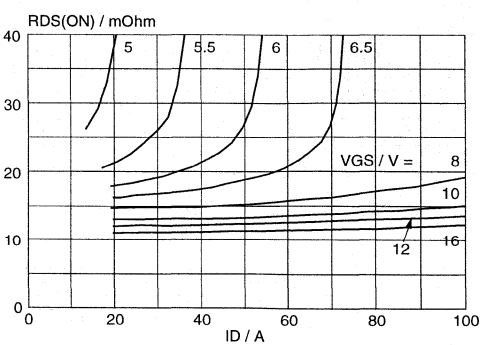


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

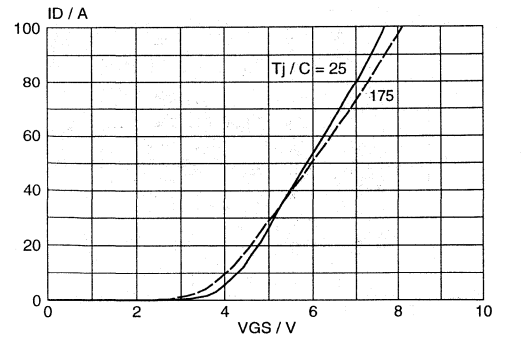


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

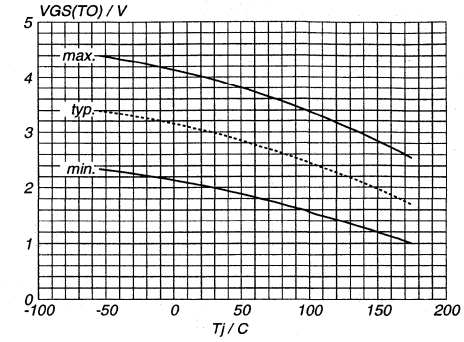


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

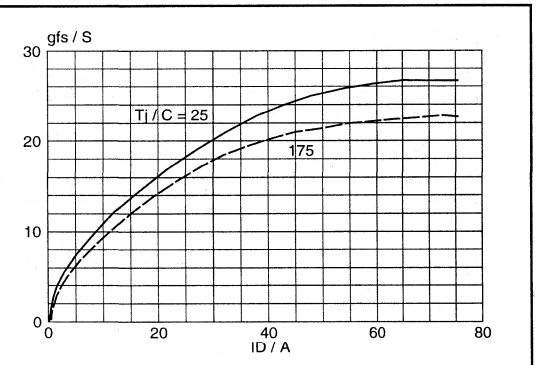


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

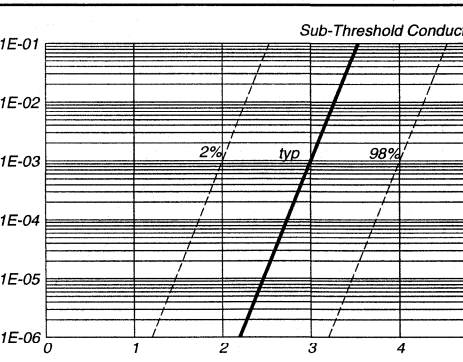


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

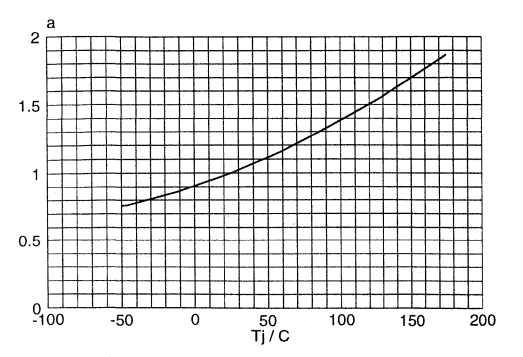


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ °C} = f(T_j)$; I_D = 25 A; V_{GS} = 10 V

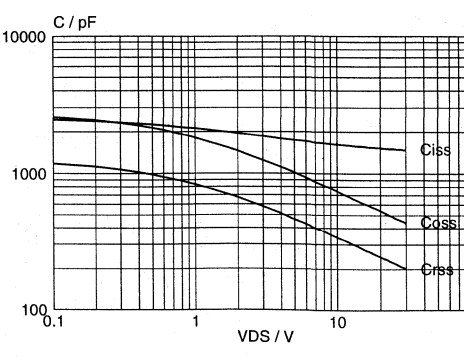


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

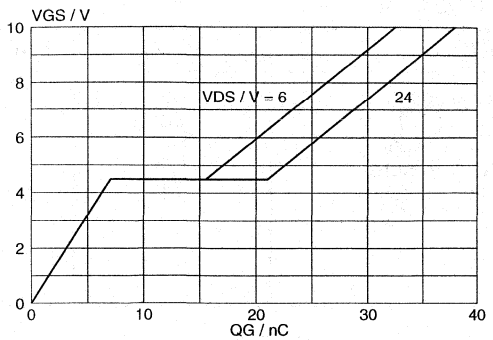


Fig.13. Typical turn-on gate-charge characteristics.
V_{GS} = f(Q_G); conditions: I_D = 69 A; parameter V_{DS}

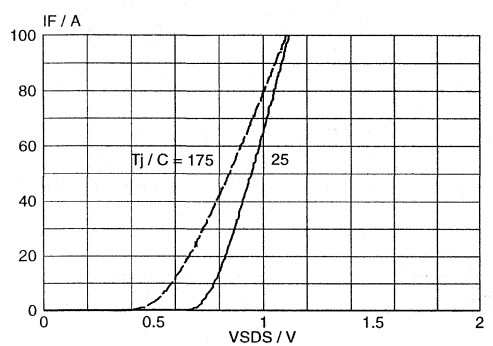


Fig.14. Typical reverse diode current.
I_F = f(V_{SDS}); conditions: V_{GS} = 0 V; parameter T_j

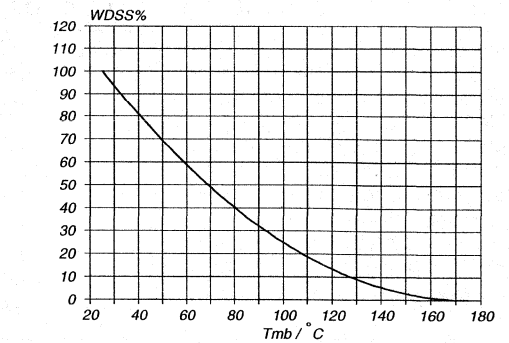


Fig.15. Normalised avalanche energy rating.
W_{DSS}% = f(T_{mb}); conditions: I_D = 35 A

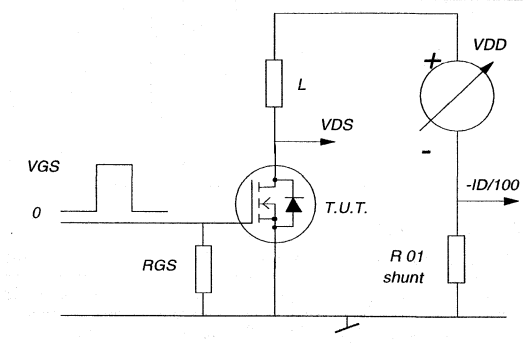


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

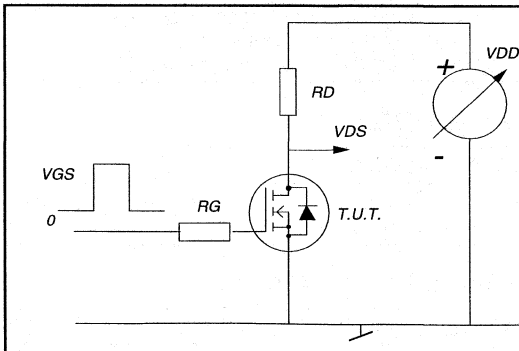


Fig.17. Switching test circuit.

TrenchMOS™ transistor Standard level FET

BUK7614-55

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope suitable for surface mounting. Using '**trench**' technology the device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

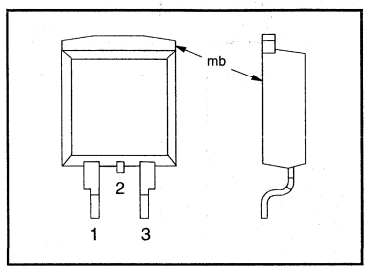
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	68	A
P_{tot}	Total power dissipation	142	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	14	mΩ

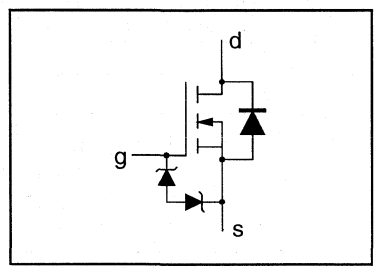
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	16	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	68	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	48	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	240	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	142	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.05	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	Minimum footprint, FR4 board	50	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2	3.0	4.0	V
		T_j = 175˚C	1	-	-	V
		T_j = -55˚C	-	-	4.4	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	20	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A	-	12	14	mΩ
		T_j = 175˚C	-	-	30	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	8	39	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	2200	2900	pF
C_{oss}	Output capacitance		-	500	600	pF
C_{rss}	Feedback capacitance		-	200	270	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	18	26	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 10 Ω	-	35	85	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	45	60	ns
t_f	Turn-off fall time		-	30	45	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	68	A
I_{DRM}	Pulsed reverse drain current		-	-	240	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 65 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 65 A; -dI_F/dt = 100 A/µs;	-	57	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.14	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 65 A; $V_{DD} \leq$ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	200	mJ

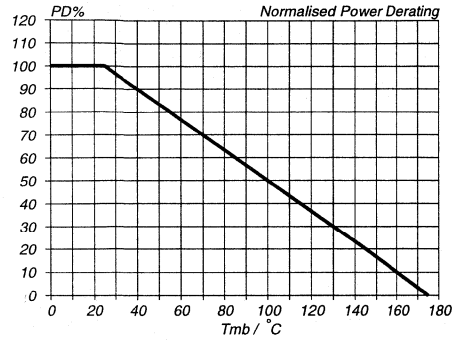


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

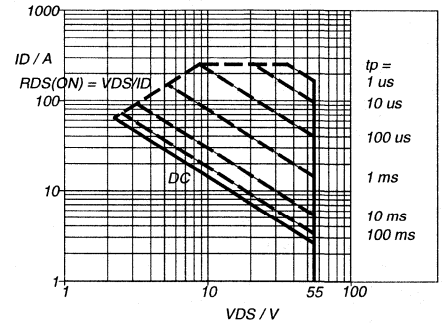


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

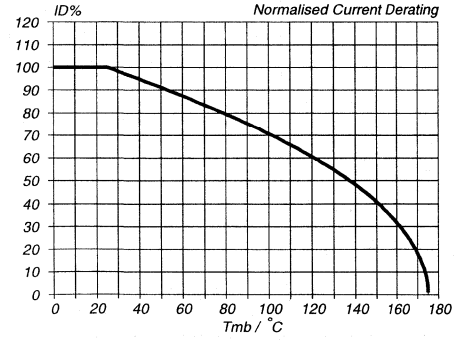


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

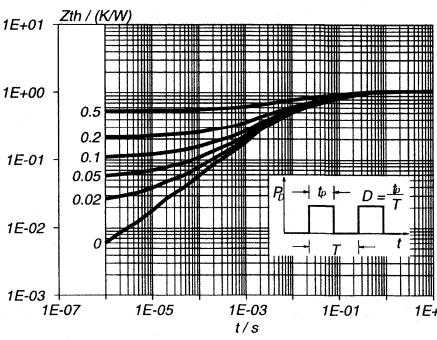


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

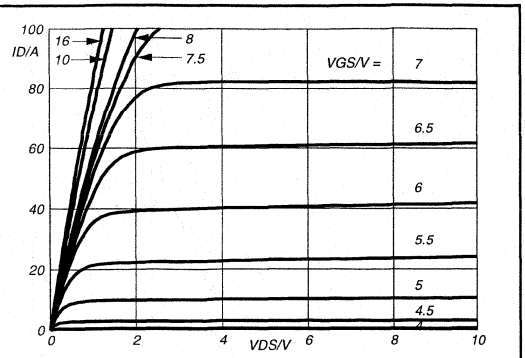


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

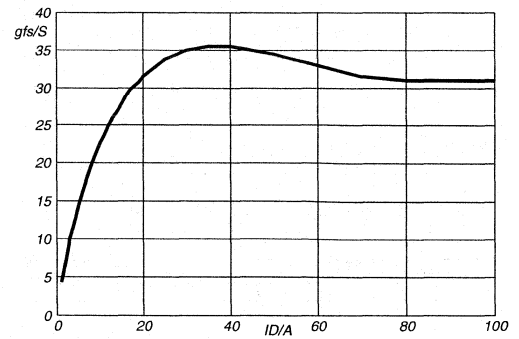


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

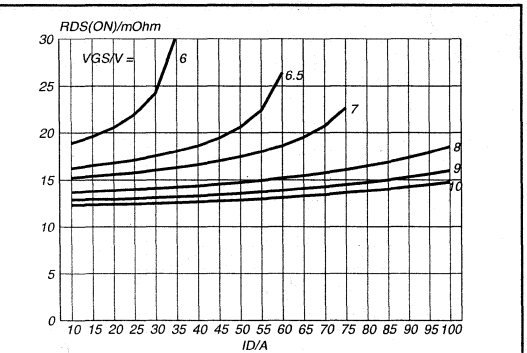


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

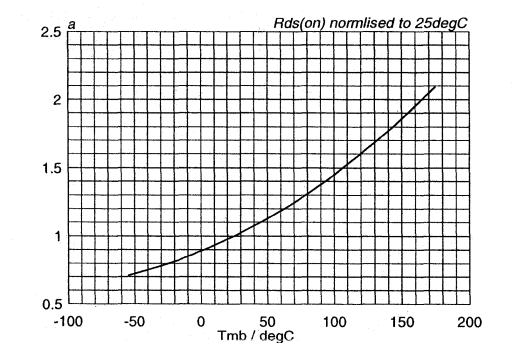


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,˚C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

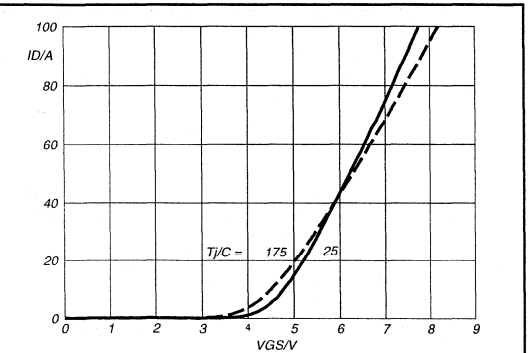


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

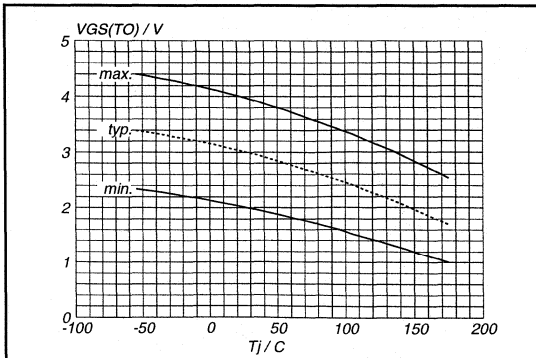


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

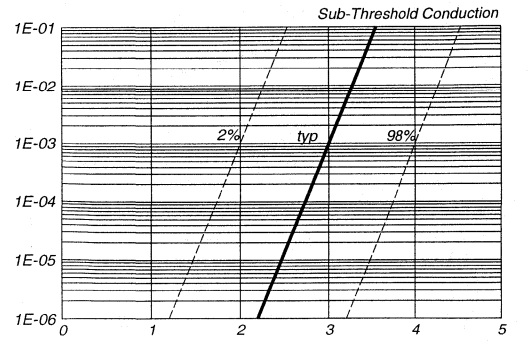


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

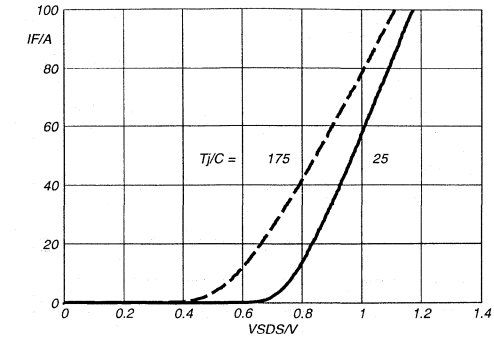


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

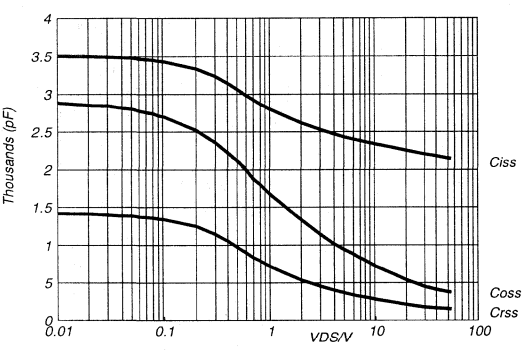


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

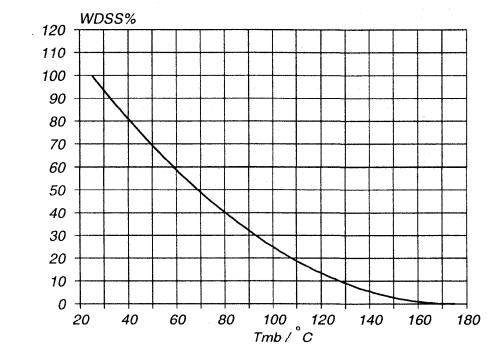


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 75$ A

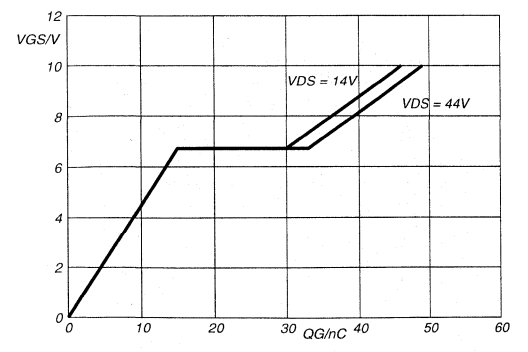


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 50$ A; parameter V_{DS}

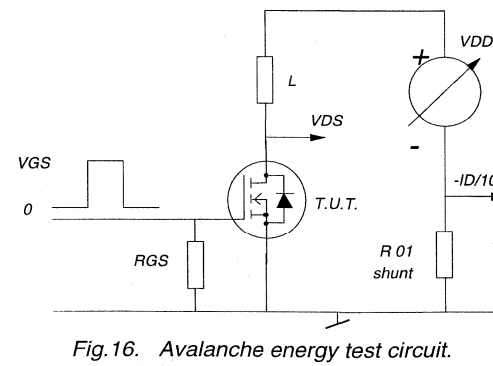


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

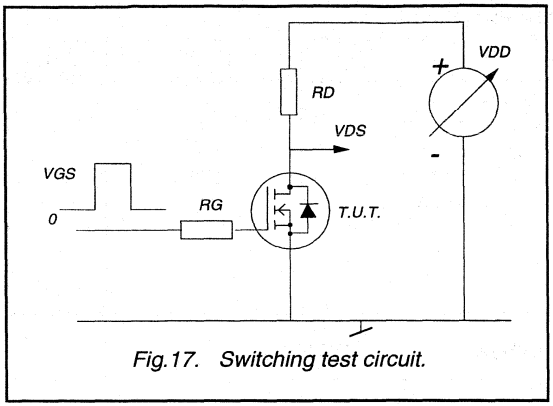


Fig.17. Switching test circuit.

TrenchMOS™ transistor
Standard level FET

BUK7618-30

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope suitable for surface mounting using **'trench'** technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

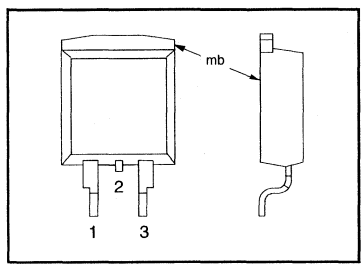
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	30	V
I_D	Drain current (DC)	55	A
P_{tot}	Total power dissipation	103	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	18	mΩ

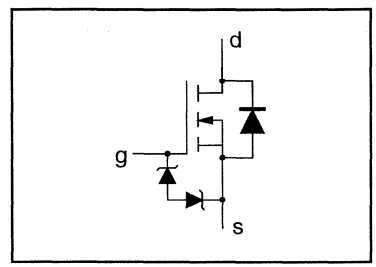
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	30	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	30	V
$\pm V_{GS}$	Gate-source voltage	-	-	20	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	55	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	38	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	220	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	103	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.45	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board	50	-	K/W

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	30	-	-	V
		T_j = -55˚C	27	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.0	3.0	4.0	V
		T_j = 175˚C	1.0	-	-	V
		T_j = -55˚C	-	-	4.4	
I_{DSS}	Zero gate voltage drain current	V_{DS} = 30 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	20	µA
$\pm V_{(BR)GSS}$	Gate source breakdown voltage	I_G = ±1 mA;	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A	-	15	18	mΩ
		T_j = 175˚C	-	-	33.5	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	7	15	-	S
$Q_{g(tot)}$	Total gate charge	I_D = 55 A; V_{DD} = 24 V; V_{GS} = 10 V	-	29.5	-	nC
Q_{gs}	Gate-source charge		-	4.5	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	14	-	nC
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1000	-	pF
C_{oss}	Output capacitance		-	390	-	pF
C_{rss}	Feedback capacitance		-	180	-	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 15 V; I_D = 25 A;	-	15	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 5 Ω	-	22	35	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	30	45	ns
t_f	Turn-off fall time		-	18	25	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead solder point to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead solder point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	55	A
I_{DRM}	Pulsed reverse drain current		-	-	220	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 55 A; V_{GS} = 0 V	-	1.0	-	
t_{rr}	Reverse recovery time	I_F = 55 A; -dI_F/dt = 100 A/µs;	-	70	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 25 V	-	0.1	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 28 A; $V_{DD} \leq$ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	80	mJ

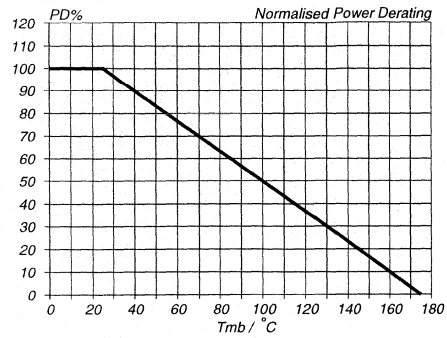


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

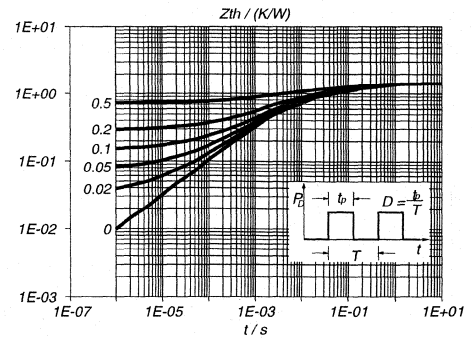


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

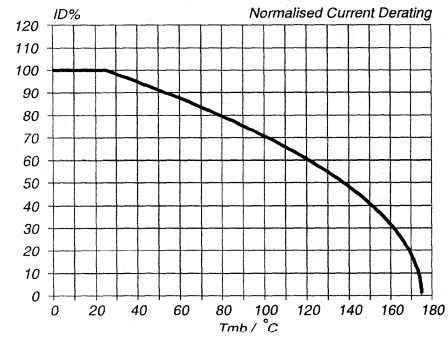


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

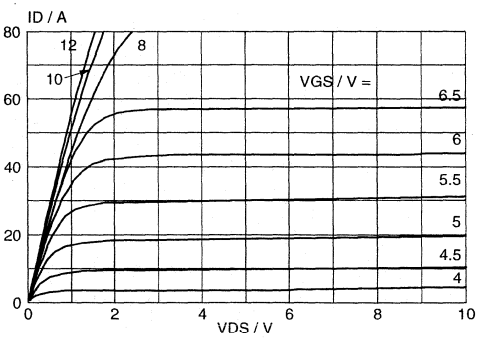


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

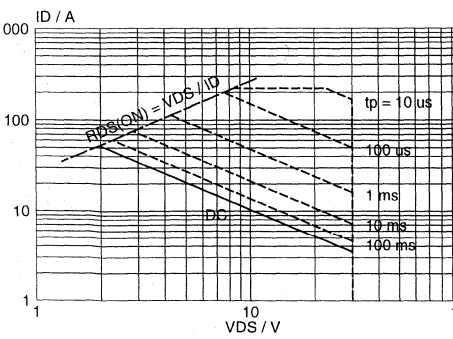


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

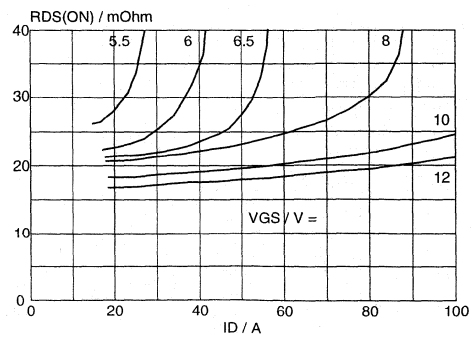


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

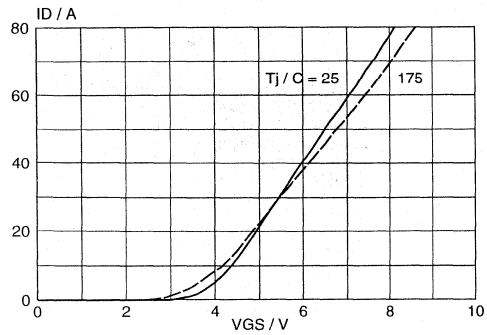


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

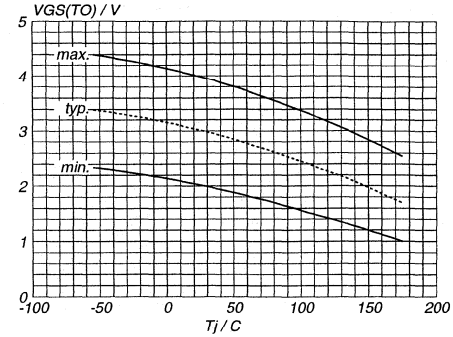


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

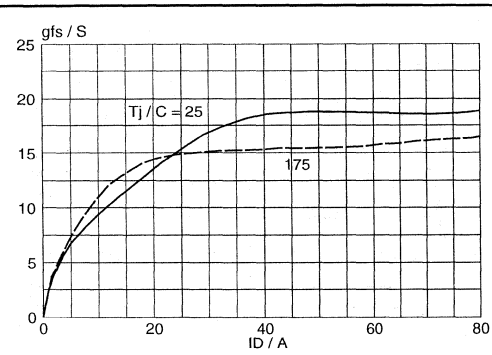


Fig.8. Typical transconductance, $T_j = 25$ °C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

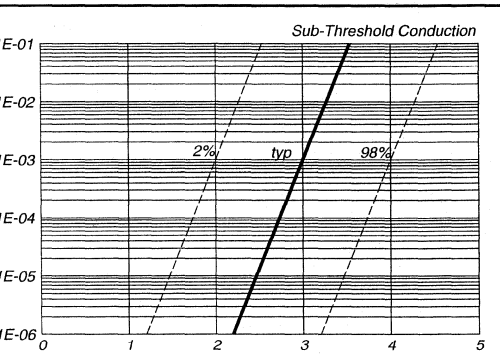


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

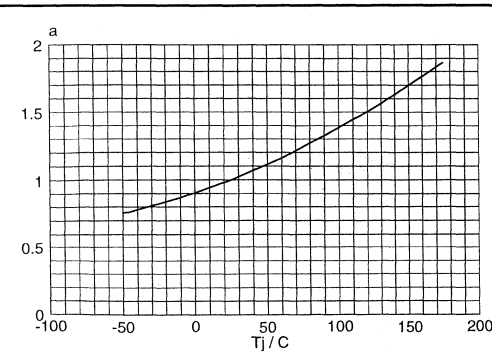


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 25$ A; $V_{GS} = 10$ V

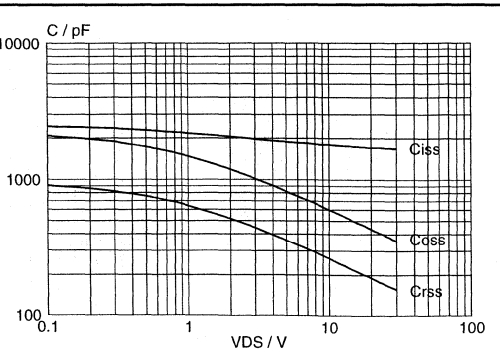


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

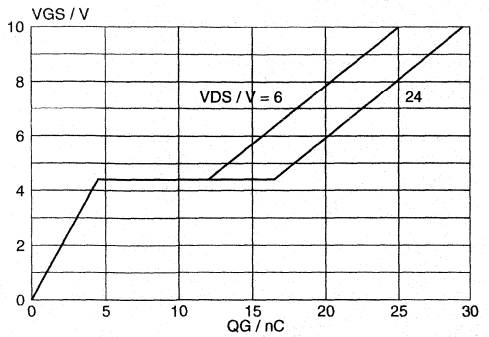


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 55$ A; parameter V_{DS}

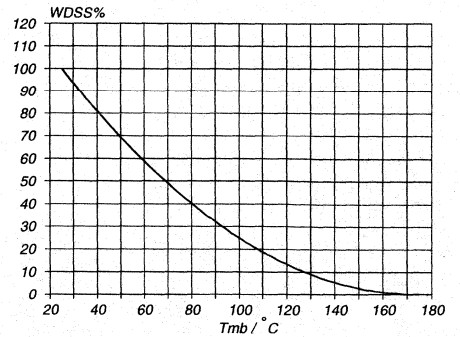


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 28$ A

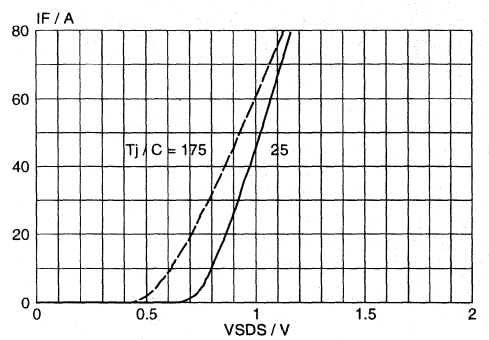


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

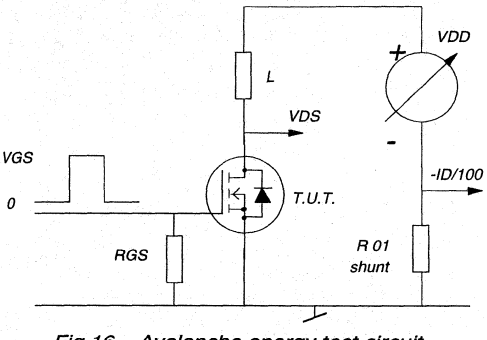


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

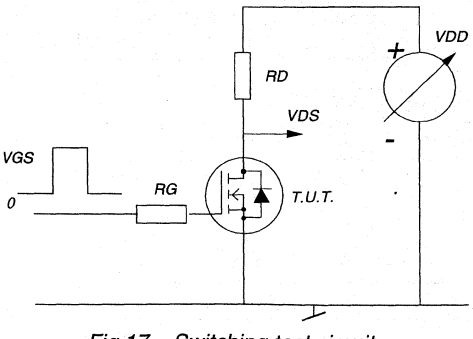


Fig.17. Switching test circuit.

TrenchMOS™ transistor Standard level FET

BUK7618-55

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope suitable for surface mounting. Using **'trench'** technology the device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

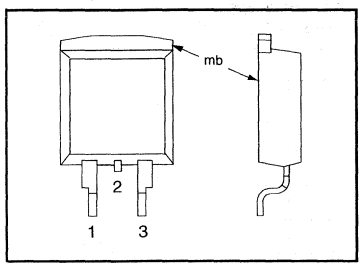
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	57	A
P_{tot}	Total power dissipation	125	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	18	mΩ

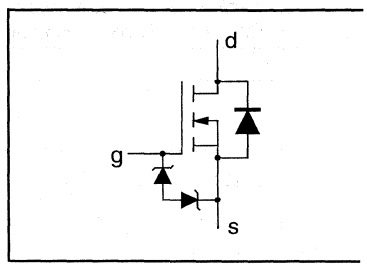
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	16	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	57	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	40	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	228	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	Minimum footprint, FR4 board	50	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.0	3.0	4.0	V
		T_j = 175˚C	1.0	-	-	V
		T_j = -55˚C	-	-	4.4	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	20	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A	-	15	18	mΩ
		T_j = 175˚C	-	-	38	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	6	30	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1500	2000	pF
C_{oss}	Output capacitance		-	370	470	pF
C_{rss}	Feedback capacitance		-	170	250	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	15	22	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 10 Ω	-	30	60	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	35	50	ns
t_f	Turn-off fall time		-	25	38	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	57	A
I_{DRM}	Pulsed reverse drain current		-	-	200	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 50 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 50 A; -dI_F/dt = 100 A/µs;	-	48	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.1	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 50 A; $V_{DD} \leq$ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	125	mJ

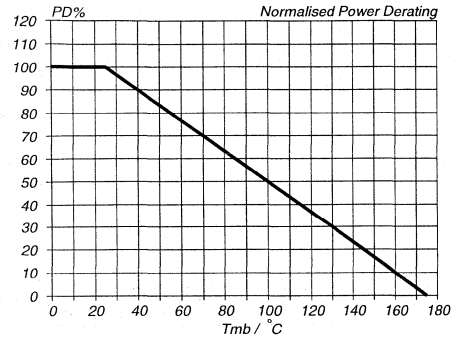


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

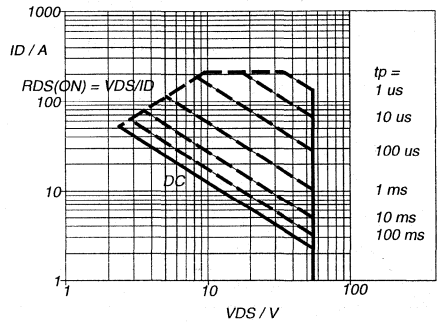


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

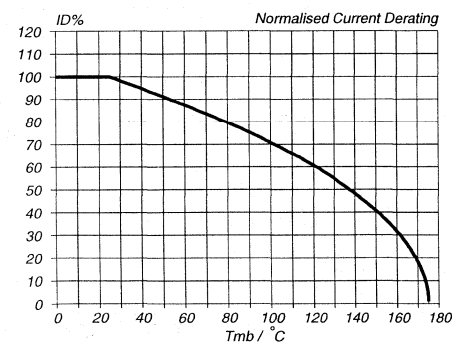


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

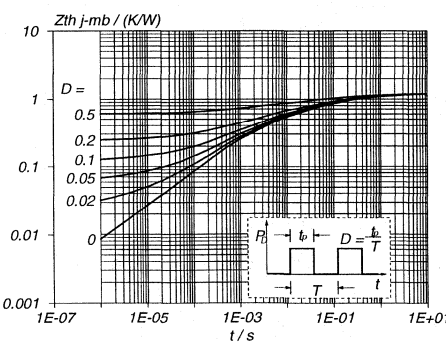


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

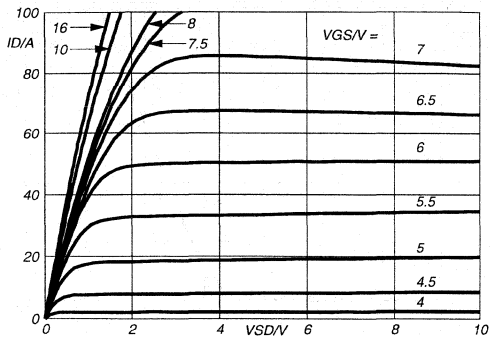


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

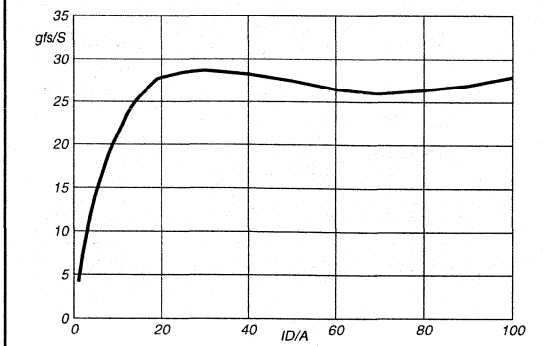


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

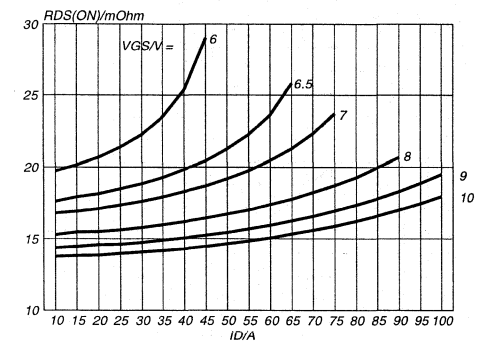


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

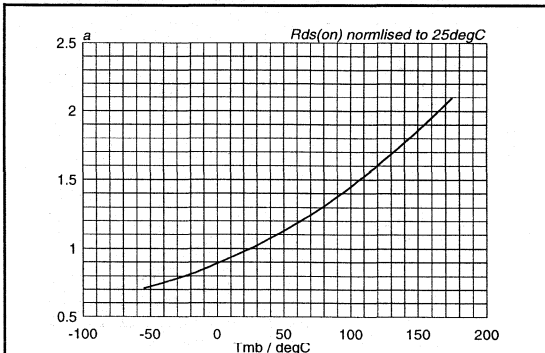


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,˚C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

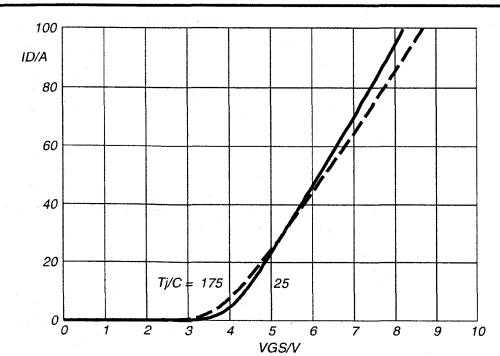


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

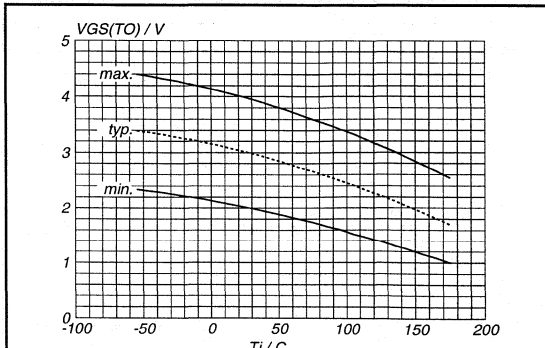


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

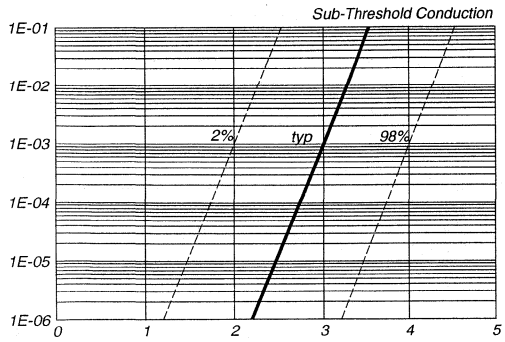


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

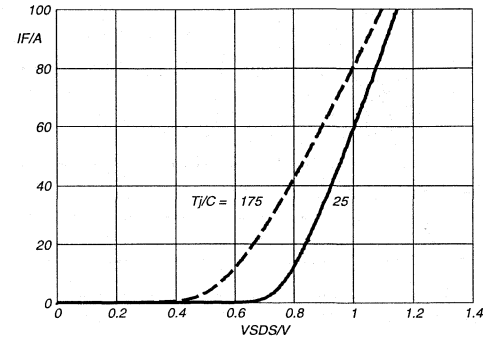


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

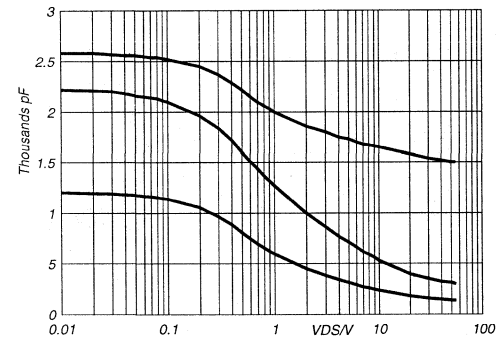


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

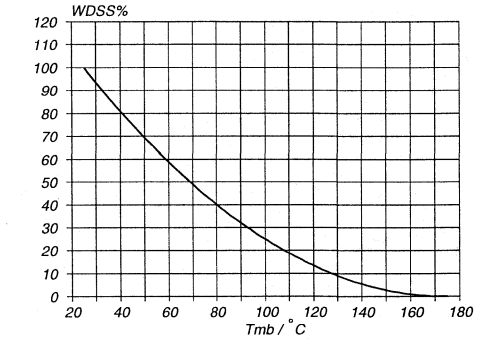


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: I_D = 75 A

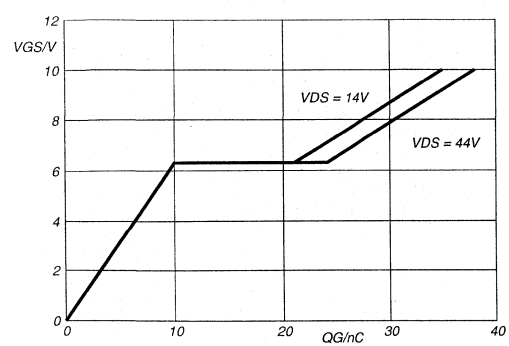


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 50 A; parameter V_{DS}

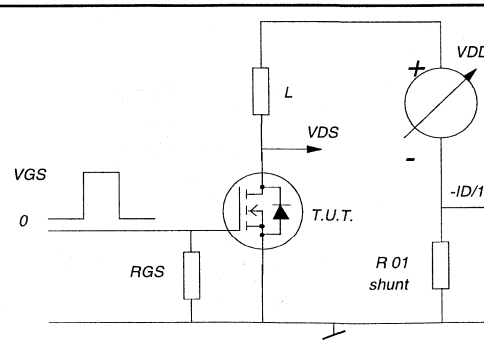


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

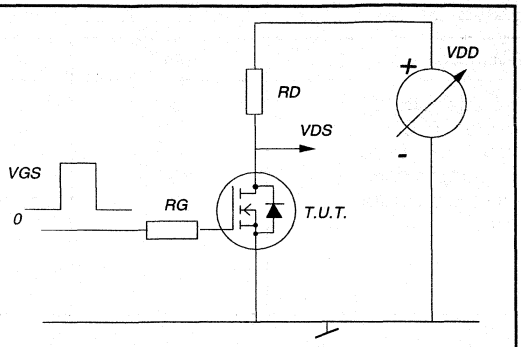


Fig.17. Switching test circuit.

TrenchMOS™ transistor Standard level FET

BUK7620-55

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope suitable for surface mounting. Using '**trench**' technology the device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

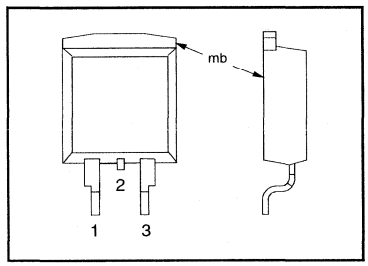
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	52	A
P_{tot}	Total power dissipation	116	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	20	mΩ

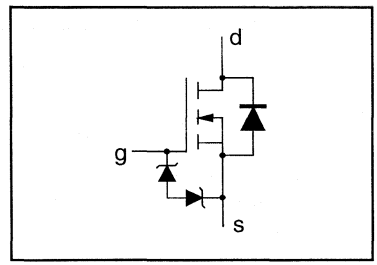
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	16	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	52	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	37	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	208	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	116	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.29	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	Minimum footprint, FR4 board	50	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.0	3.0	4.0	V
		T_j = 175˚C	1.0	-	-	V
		T_j = -55˚C	-	-	4.4	
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	0.04	1	µA
		T_j = 175˚C	-	-	20	µA
$\pm V_{(BR)GSS}$	Gate source breakdown voltage	I_G = ±1 mA;	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A	-	15	20	mΩ
		T_j = 175˚C	-	-	42	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	6	-	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1350	1800	pF
C_{oss}	Output capacitance		-	330	400	pF
C_{rss}	Feedback capacitance		-	155	215	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	18	26	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 10 Ω	-	50	75	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	40	50	ns
t_f	Turn-off fall time		-	30	40	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	52	A
I_{DRM}	Pulsed reverse drain current		-	-	208	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 40 A; V_{GS} = 0 V	-	1.0	-	
t_{rr}	Reverse recovery time	I_F = 40 A; -dI_F/dt = 100 A/µs;	-	47	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.15	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 45 A; $V_{DD} \leq$ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	110	mJ

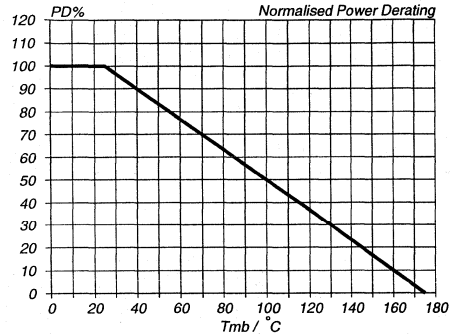


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

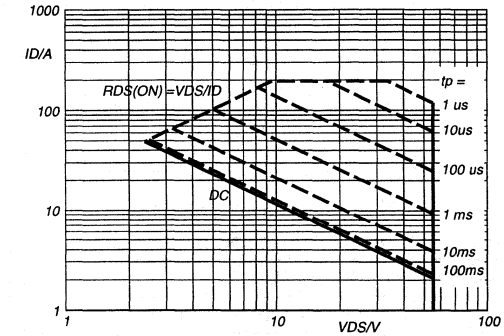


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

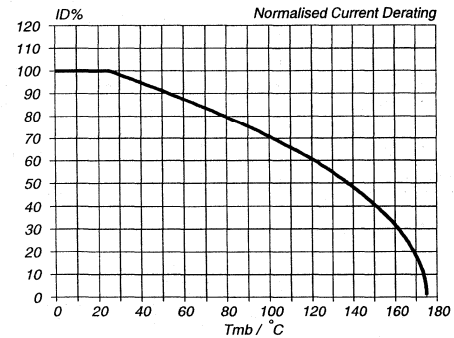


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 10 V

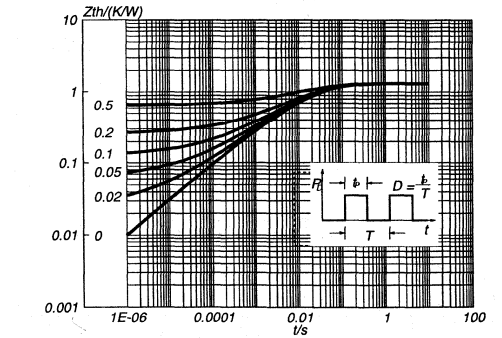


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

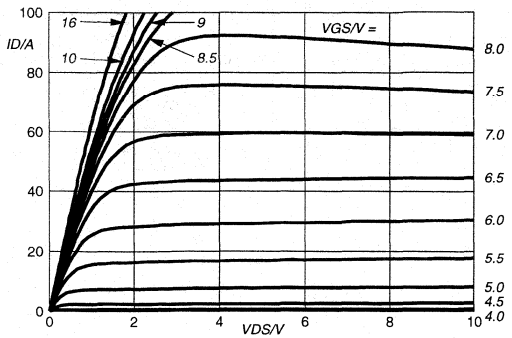


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

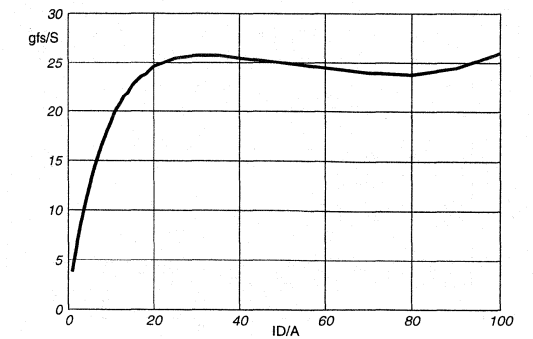


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

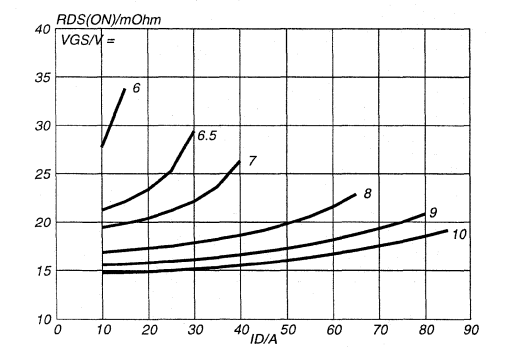


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

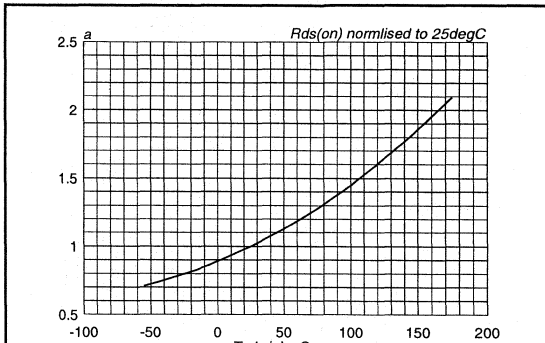


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\ ˚C} = f(T_j)$; I_D = 25 A; V_{GS} = 10 V

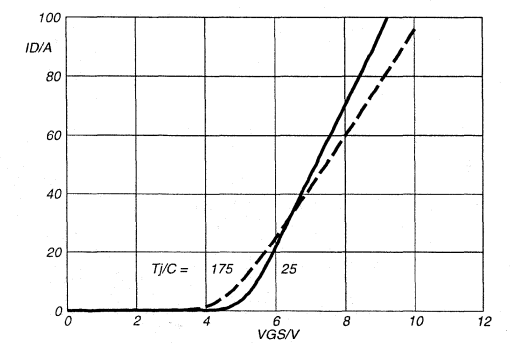


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

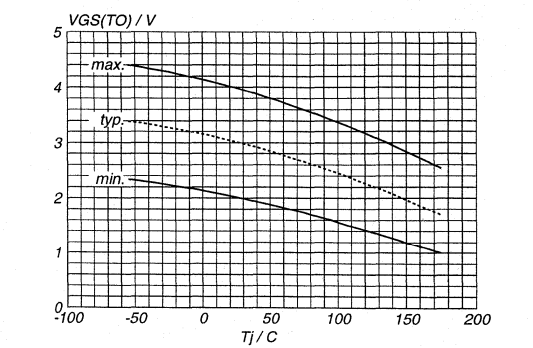


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

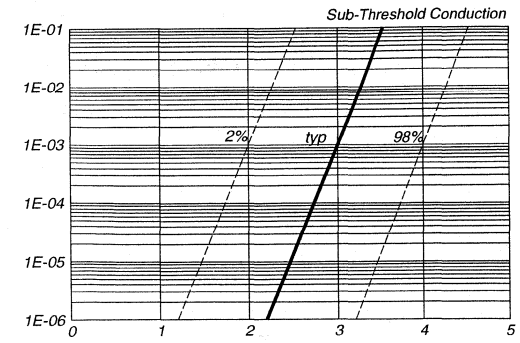


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

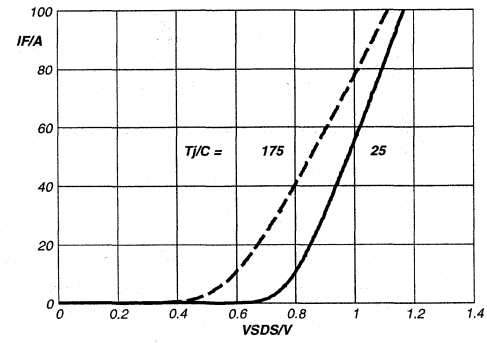


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

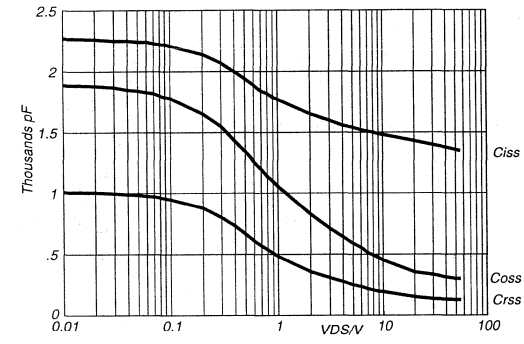


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

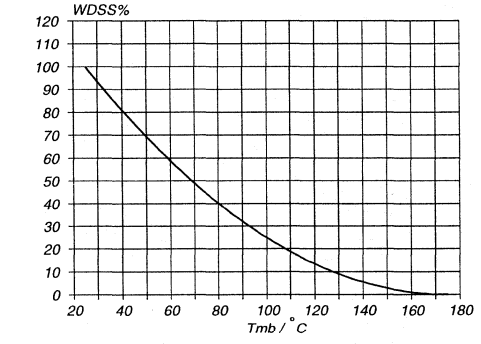


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: I_D = 49 A

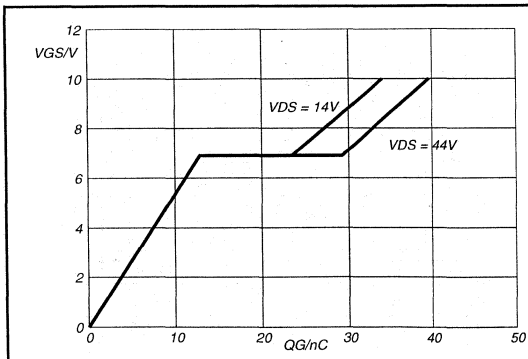


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 50 A; parameter V_{DS}

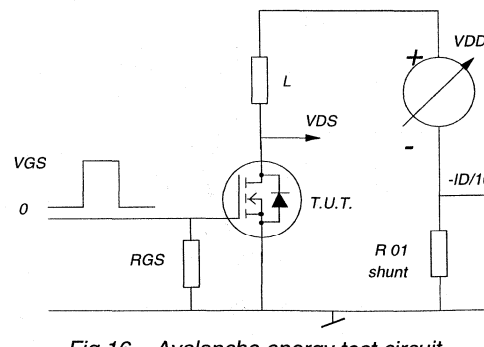


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

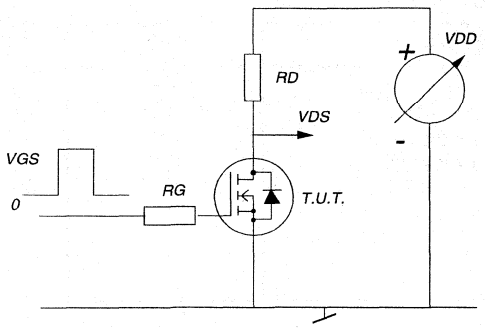


Fig.17. Switching test circuit.

TrenchMOS™ transistor Standard level FET

BUK7624-5

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope suitable for surface mounting. Using '**trench**' technology the device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

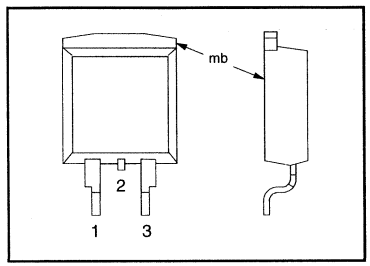
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	45	A
P_{tot}	Total power dissipation	103	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	24	mΩ

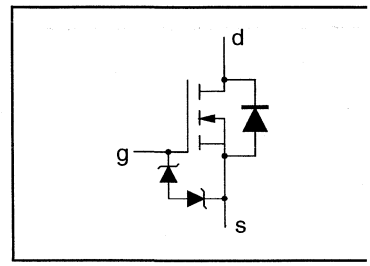
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	16	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	45	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	31	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	180	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	103	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.45	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	Minimum footprint, FR4 board	50	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.0	3.0	4.0	V
		T_j = 175˚C	1.0	-	-	V
		T_j = -55˚C	-	-	4.4	
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	20	µA
$\pm V_{(BR)GSS}$	Gate source breakdown voltage	I_G = ±1 mA;	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A	-	19	24	mΩ
		T_j = 175˚C	-	-	50	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	4	11	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1100	1500	pF
C_{oss}	Output capacitance		-	280	340	pF
C_{rss}	Feedback capacitance		-	130	180	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	12	18	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 10 Ω	-	19	35	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	25	35	ns
t_f	Turn-off fall time		-	18	25	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	45	A
I_{DRM}	Pulsed reverse drain current		-	-	160	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 40 A; V_{GS} = 0 V	-	1.0	-	
t_{rr}	Reverse recovery time	I_F = 40 A; -dI_F/dt = 100 A/µs;	-	40	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.07	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 40 A; $V_{DD} \leq$ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	80	mJ

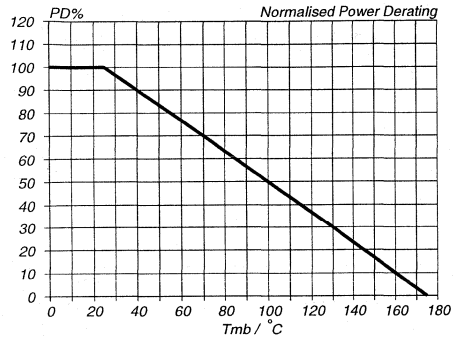


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

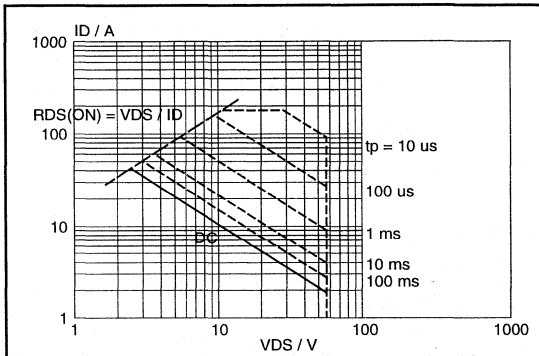


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

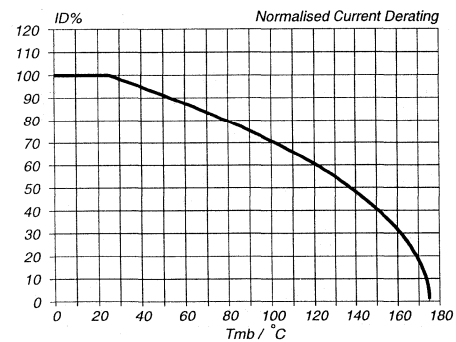


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

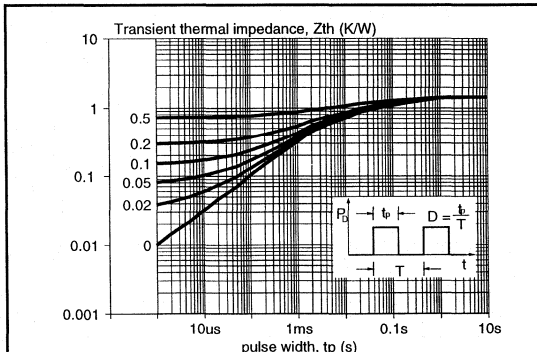


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

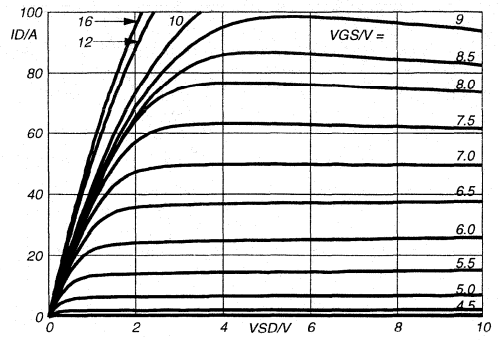


Fig.5. Typical output characteristics, T_j = 25 °C. $I_D = f(V_{DS})$; parameter V_{GS}

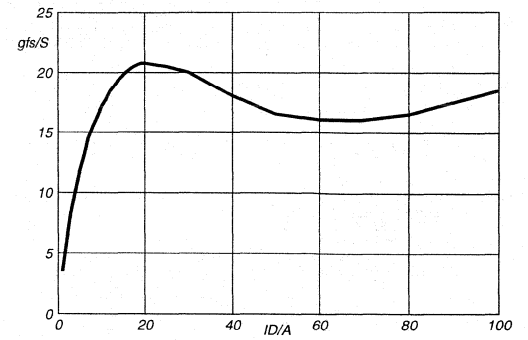


Fig.8. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

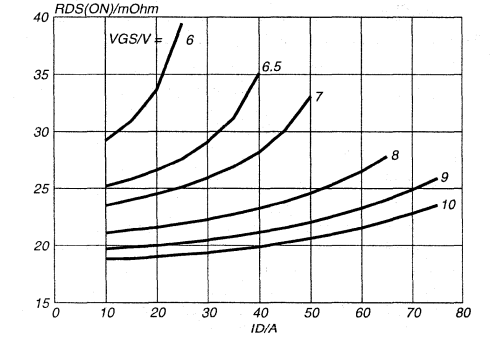


Fig.6. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

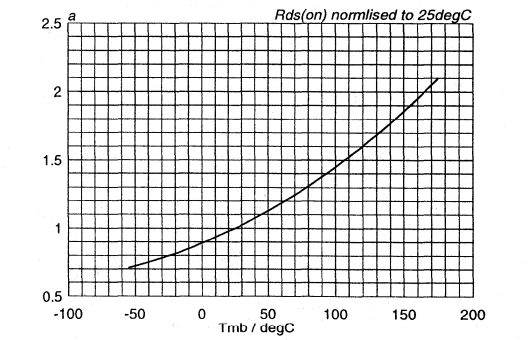


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

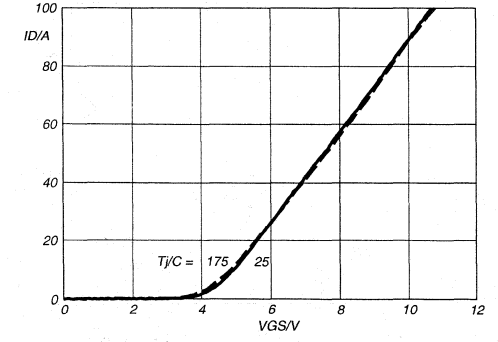


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

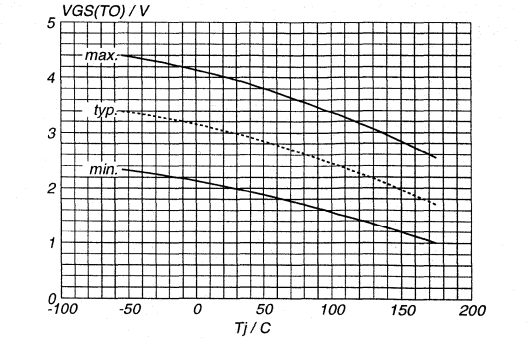


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

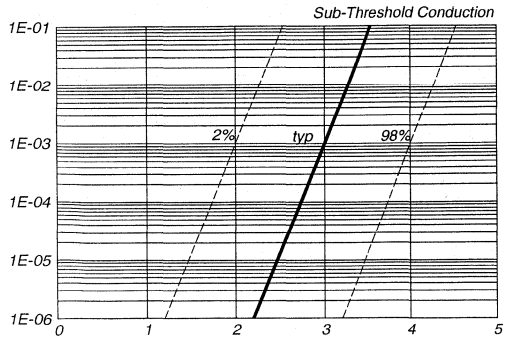


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; *conditions:* $T_j = 25$ °C; $V_{DS} = V_{GS}$

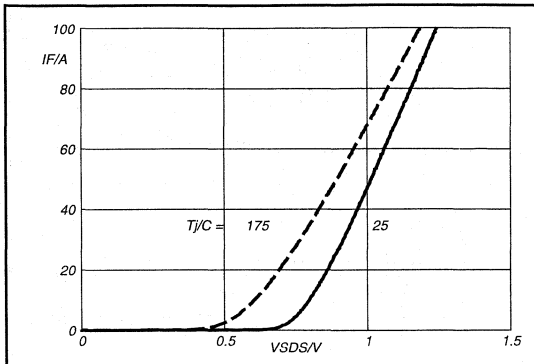


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; *conditions:* $V_{GS} = 0$ V; *parameter* T_j

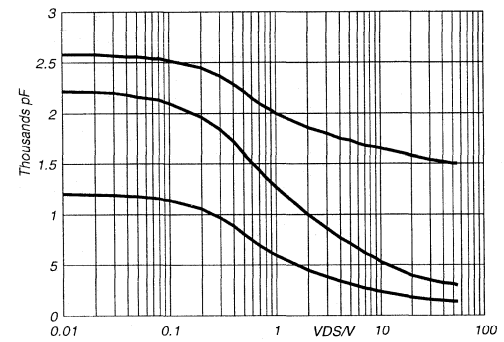


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; *conditions:* $V_{GS} = 0$ V; $f = 1$ MHz

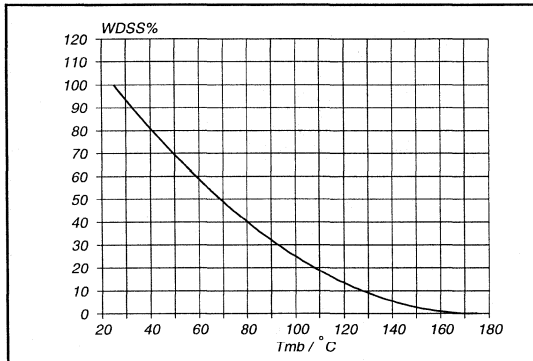


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; *conditions:* $I_D = 75$ A

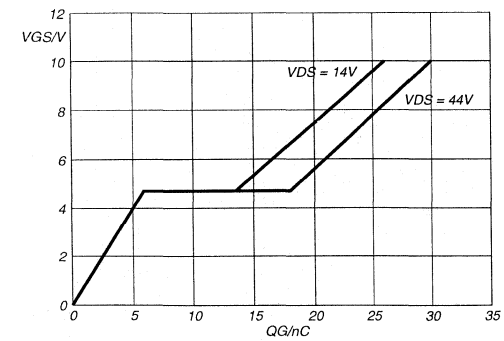


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; *conditions:* $I_D = 50$ A; *parameter* V_{DS}

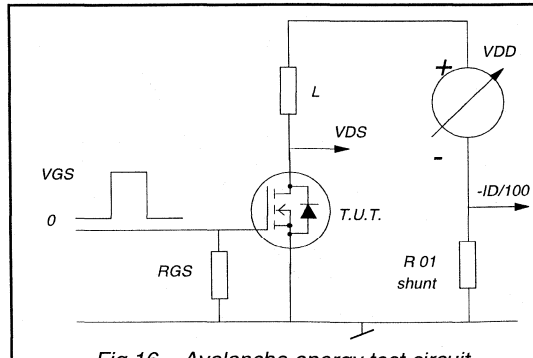


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

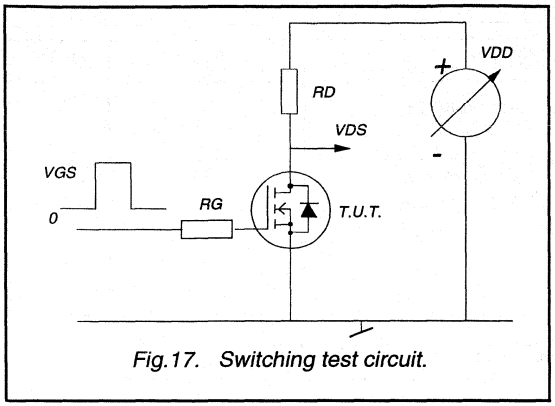


Fig.17. Switching test circuit.

TrenchMOS™ transistor
Standard level FET

BUK7628-55

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope suitable for surface mounting. Using **'trench'** technology the device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

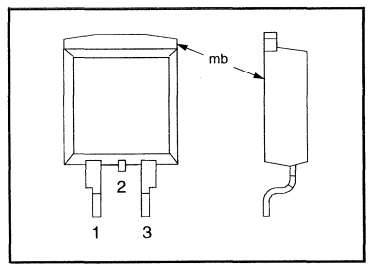
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	40	A
P_{tot}	Total power dissipation	96	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	28	mΩ

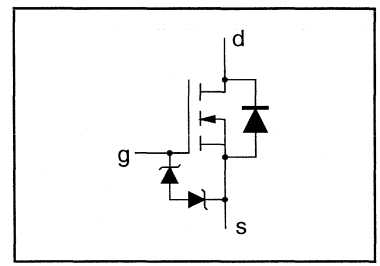
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	16	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	40	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	28	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	160	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	96	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.56	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	Minimum footprint, FR4 board	50	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.0	3.0	4.0	V
		T_j = 175˚C	1.0	-	-	V
		T_j = -55˚C	-	-	4.4	
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	0.04	1	µA
		T_j = 175˚C	-	-	20	µA
$\pm V_{(BR)GSS}$	Gate source breakdown voltage	I_G = ±1 mA;	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 20 A	-	22	28	mΩ
		T_j = 175˚C	-	-	59	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	4	-	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1000	1300	pF
C_{oss}	Output capacitance		-	240	300	pF
C_{rss}	Feedback capacitance		-	115	160	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	13	19	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 10 Ω	-	50	75	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	27	35	ns
t_f	Turn-off fall time		-	20	27	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	40	A
I_{DRM}	Pulsed reverse drain current		-	-	160	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 40 A; V_{GS} = 0 V	-	1.0	-	
t_{rr}	Reverse recovery time	I_F = 40 A; -dI_F/dt = 100 A/µs;	-	41	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.16	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 35 A; $V_{DD} \leq$ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	70	mJ

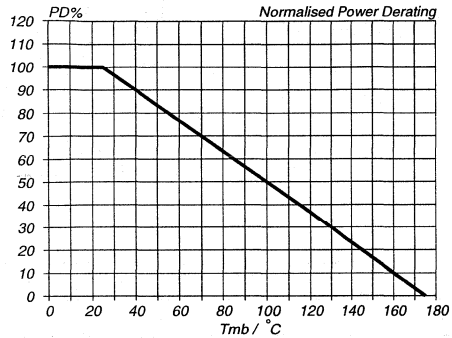


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

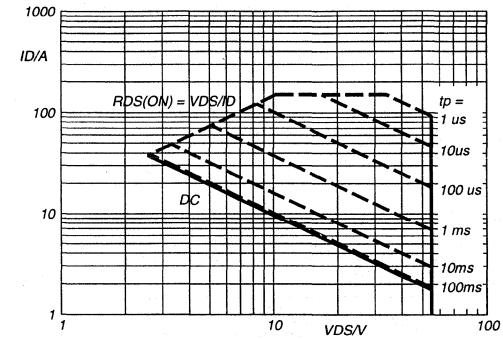


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

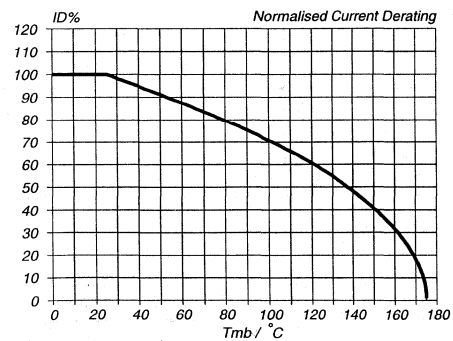


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 10 V

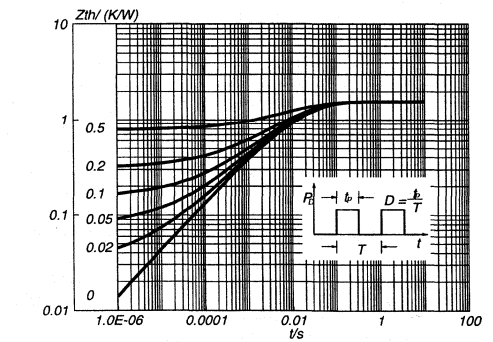


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

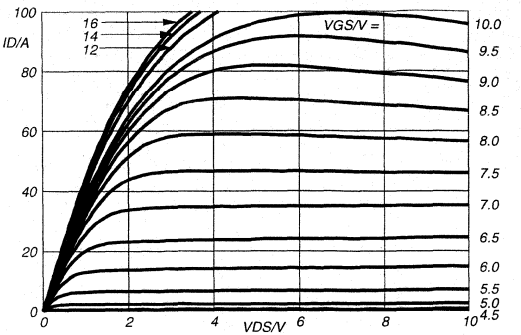


Fig.5. Typical output characteristics, T_j = 25 °C. $I_D = f(V_{DS})$; parameter V_{GS}

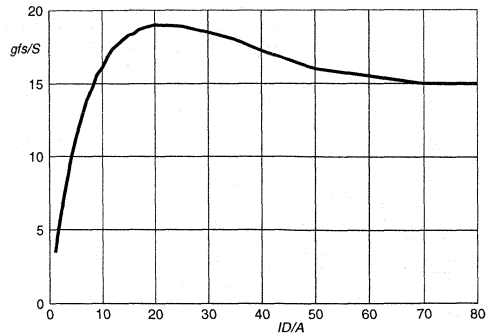


Fig.8. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

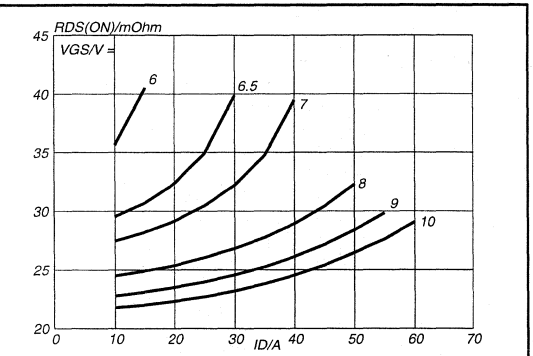


Fig.6. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

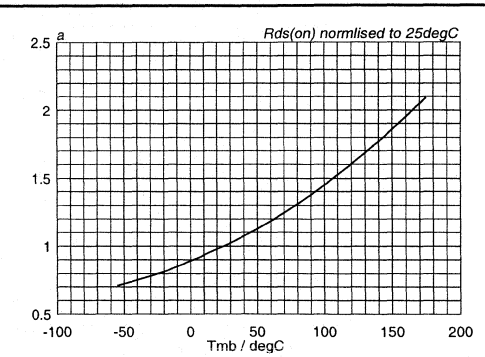


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 20 A; V_{GS} = 10 V

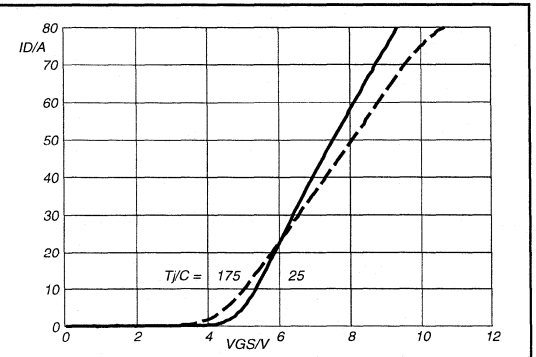


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

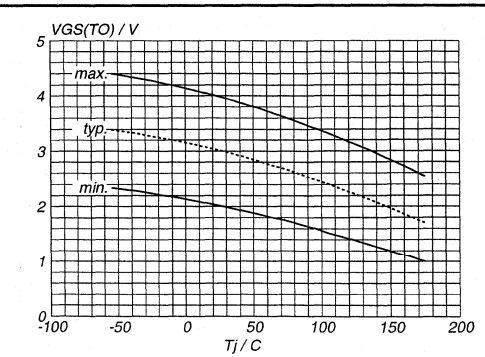


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

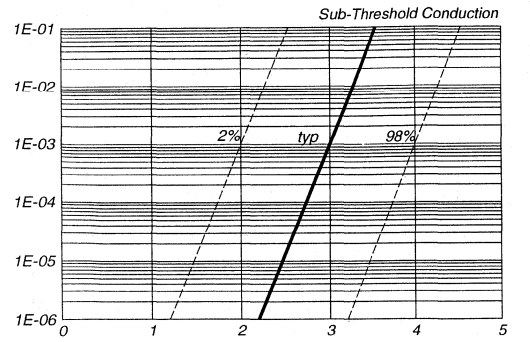


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; *conditions:* $T_j = 25$ °C; $V_{DS} = V_{GS}$

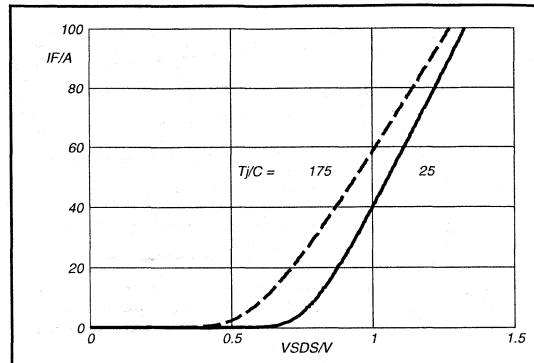


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; *conditions:* $V_{GS} = 0$ V; *parameter* T_j

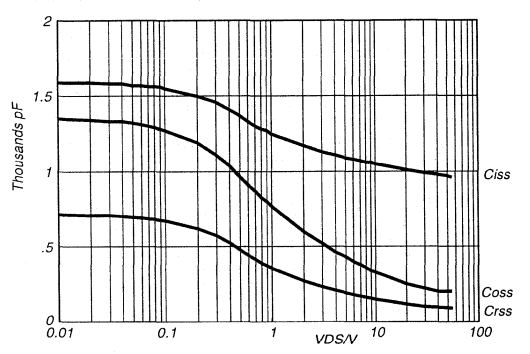


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; *conditions:* $V_{GS} = 0$ V; $f = 1$ MHz

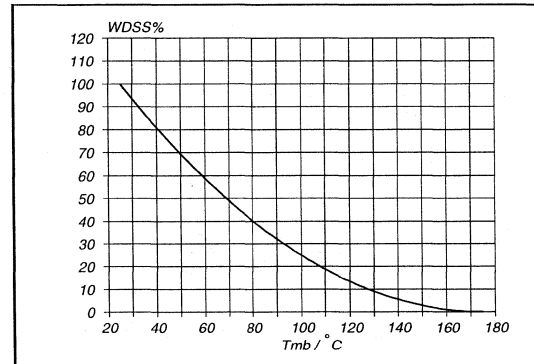


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; *conditions:* $I_D = 40$ A

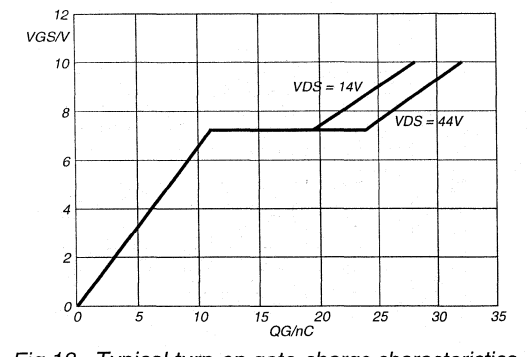


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; *conditions:* $I_D = 40$ A; *parameter* V_{DS}

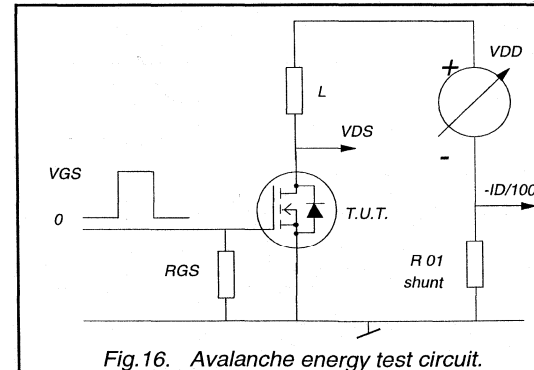


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

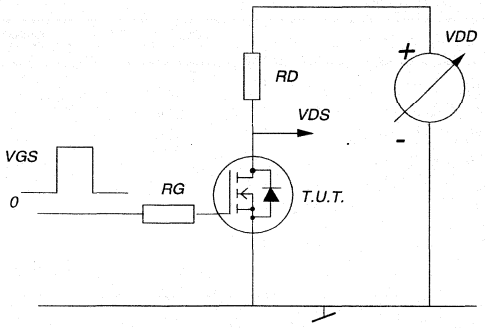


Fig.17. Switching test circuit.

TrenchMOS™ transistor
Standard level FET

BUK7635-55

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope suitable for surface mounting. Using '**trench**' technology the device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

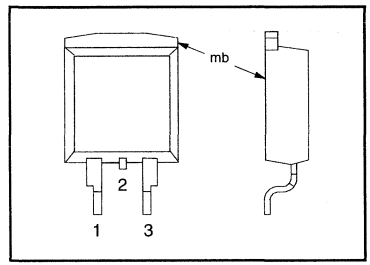
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	34	A
P_{tot}	Total power dissipation	85	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	35	mΩ

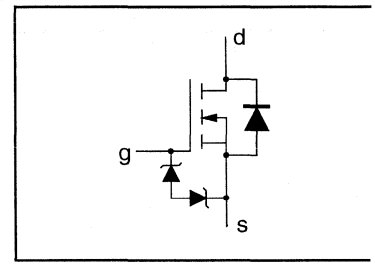
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	16	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	34	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	24	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	136	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	85	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.75	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	Minimum footprint, FR4 board	50	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;		55	-	-	V
			T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA		2.0	3.0	4.0	V
			T_j = 175˚C	1.0	-	-	V
			T_j = -55˚C	-	-	4.4	
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;		-	0.05	10	µA
			T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V		-	0.04	1	µA
			T_j = 175˚C	-	-	20	µA
$\pm V_{(BR)GSS}$	Gate source breakdown voltage	I_G = ±1 mA;		16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 17 A		-	28	35	mΩ
			T_j = 175˚C	-	-	74	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 15 A	4	-	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	700	880	pF
C_{oss}	Output capacitance		-	200	40	pF
C_{rss}	Feedback capacitance		-	100	140	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 15 A;	-	11	16	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 10 Ω	-	35	50	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	25	35	ns
t_f	Turn-off fall time		-	22	29	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	34	A
I_{DRM}	Pulsed reverse drain current		-	-	136	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 34 A; V_{GS} = 0 V	-	1.0	-	
t_{rr}	Reverse recovery time	I_F = 34 A; -dI_F/dt = 100 A/µs;	-	40	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.16	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 20 A; $V_{DD} \leq$ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	45	mJ

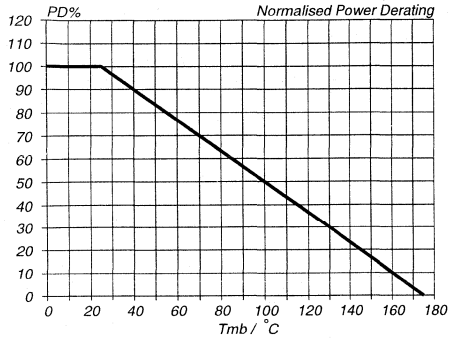


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

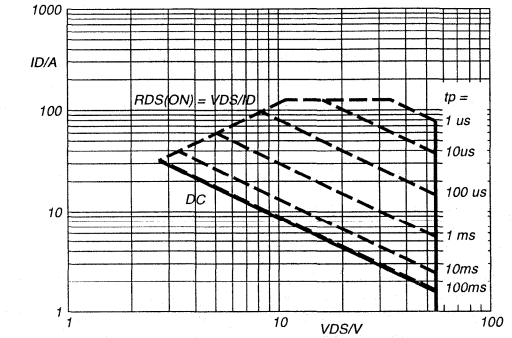


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

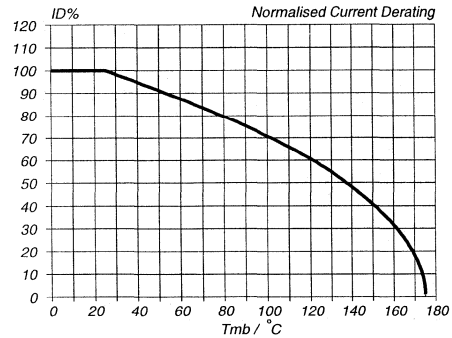


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 10 V

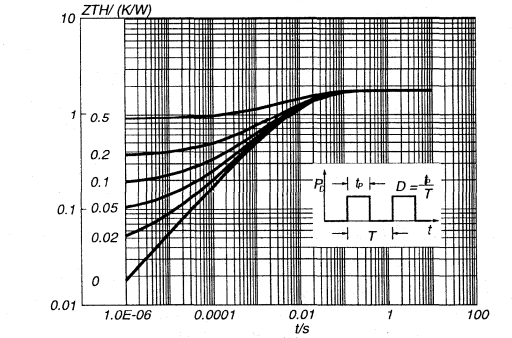


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

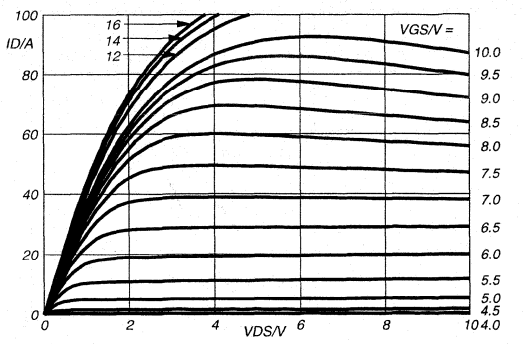


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

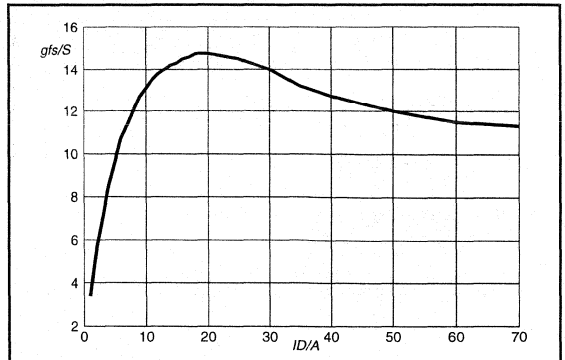


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

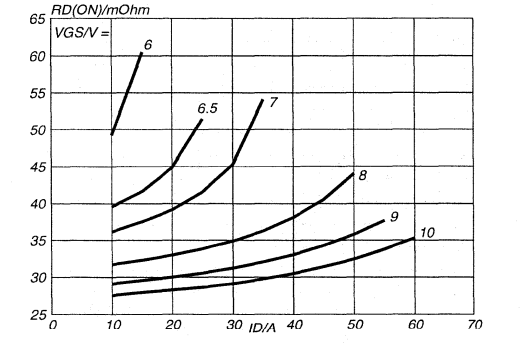


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

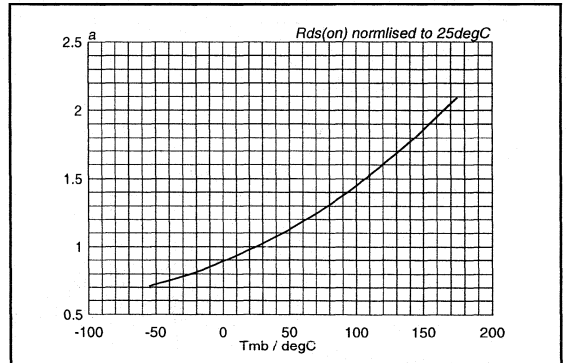


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,^{\circ}C} = f(T_j)$; I_D = 17 A; V_{GS} = 10 V

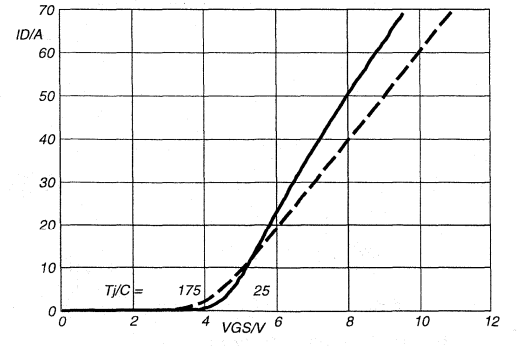


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

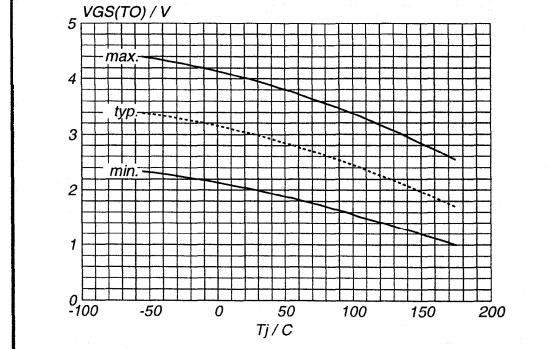


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

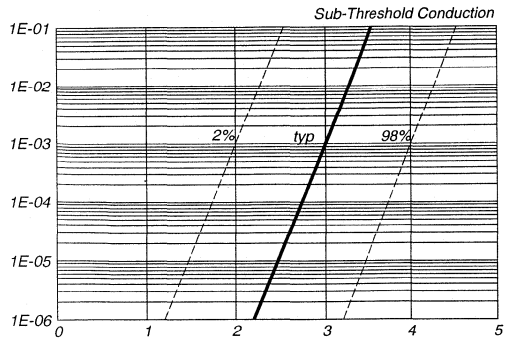


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

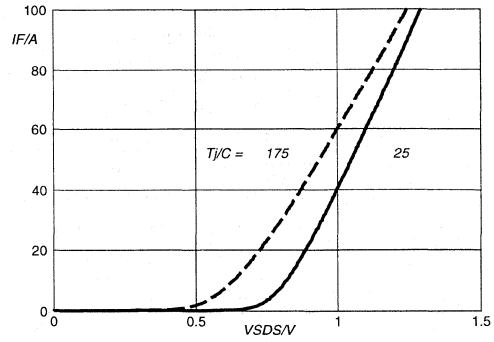


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

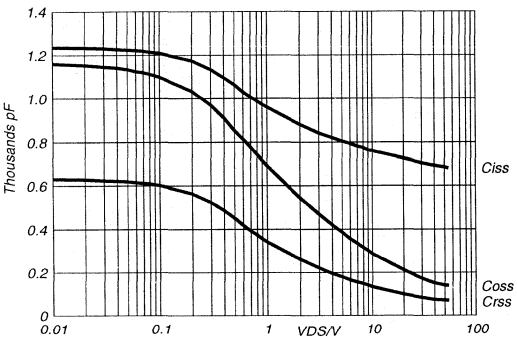


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

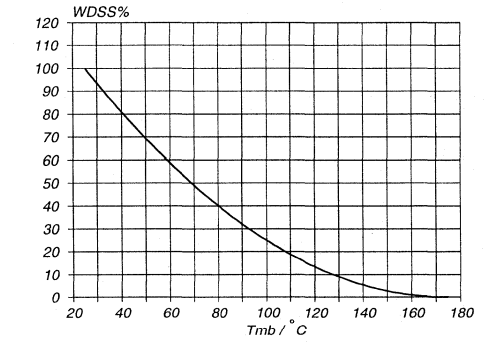


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: I_D = 32 A

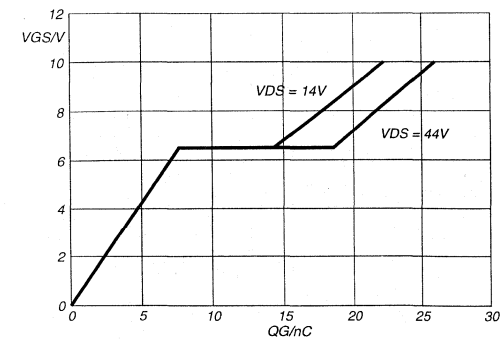


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 30 A; parameter V_{DS}

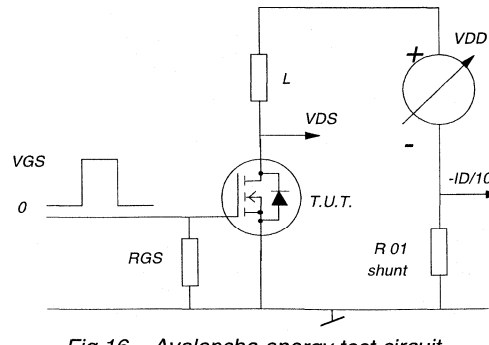


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

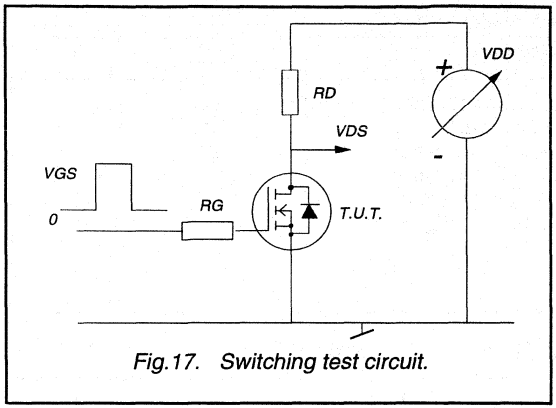


Fig.17. Switching test circuit.

TrenchMOS™ transistor Standard level FET

BUK7675-55

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope suitable for surface mounting. Using '**trench**' technology the device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

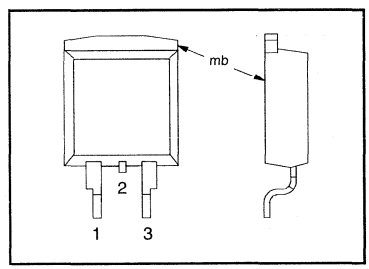
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	19.7	A
P_{tot}	Total power dissipation	61	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	75	mΩ

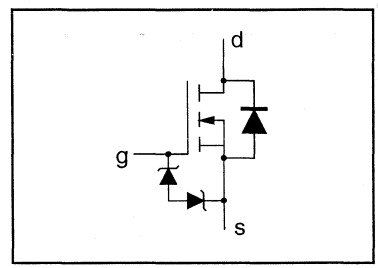
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	16	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	19.7	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	13.9	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	79	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	61	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	2.46	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	Minimum footprint, FR4 board	50	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.0	3.0	4.0	V
		T_j = 175˚C	1.0	-	-	V
		T_j = -55˚C	-	-	4.4	
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	0.04	1	µA
		T_j = 175˚C	-	-	20	µA
$\pm V_{(BR)GSS}$	Gate source breakdown voltage	I_G = ±1 mA;	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 10 A	-	60	75	mΩ
		T_j = 175˚C	-	-	157	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 10 A	1	-	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	365	500	pF
C_{oss}	Output capacitance		-	110	135	pF
C_{rss}	Feedback capacitance		-	60	85	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 10 A;	-	9	14	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 10 Ω	-	16	21	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	14	25	ns
t_f	Turn-off fall time		-	13	20	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	19.7	A
I_{DRM}	Pulsed reverse drain current		-	-	79	A
V_{SD}	Diode forward voltage	I_F = 19.7 A; V_{GS} = 0 V	-	0.95	1.2	V
t_{rr}	Reverse recovery time	I_F = 19.7 A; -dI_F/dt = 100 A/µs;	-	32	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.12	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 10 A; $V_{DD} \leq$ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	30	mJ

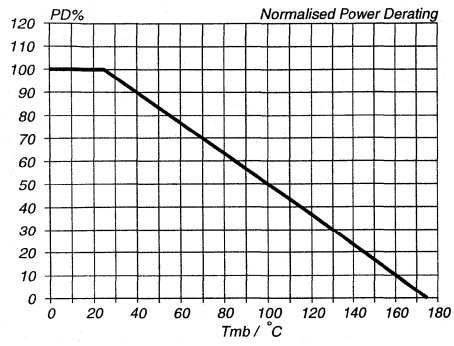


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

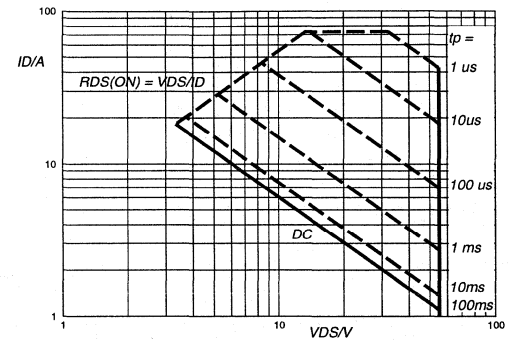


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

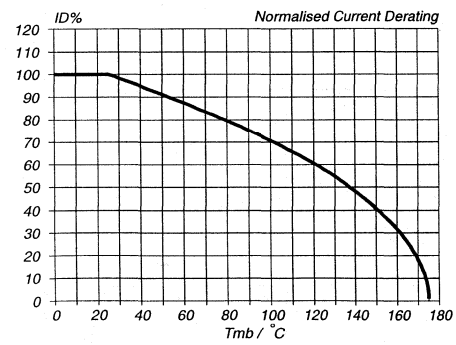


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 10 V

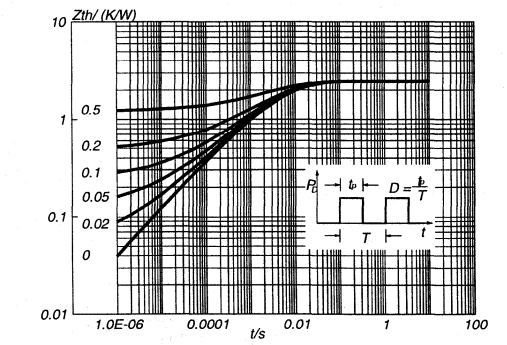


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

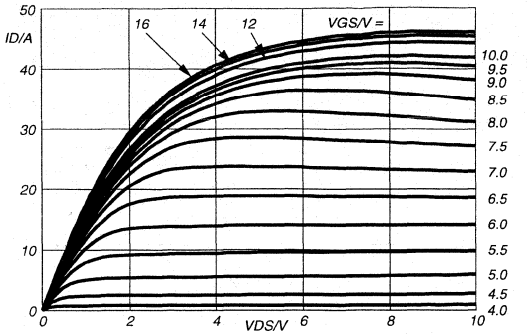


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

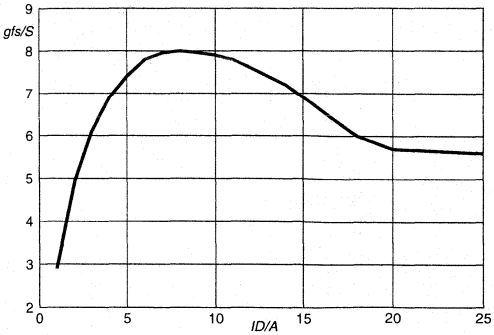


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

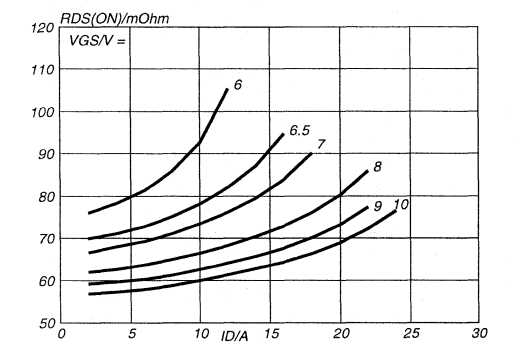


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

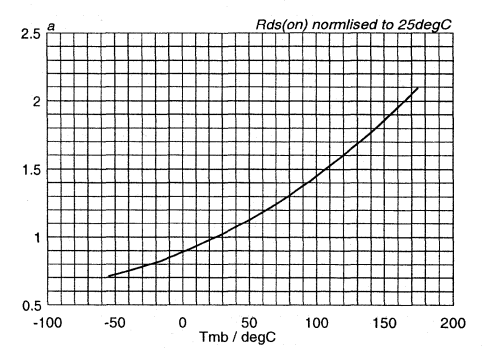


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\ ˚C} = f(T_j)$; I_D = 10 A; V_{GS} = 10 V

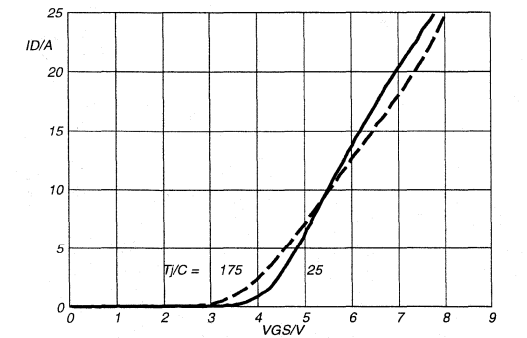


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

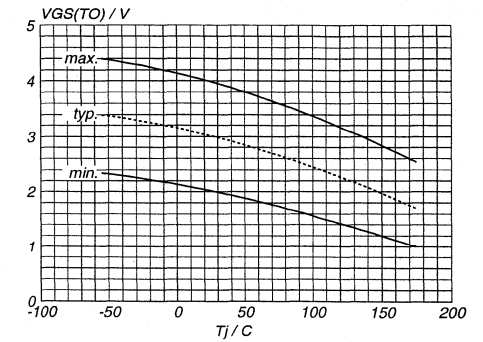


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

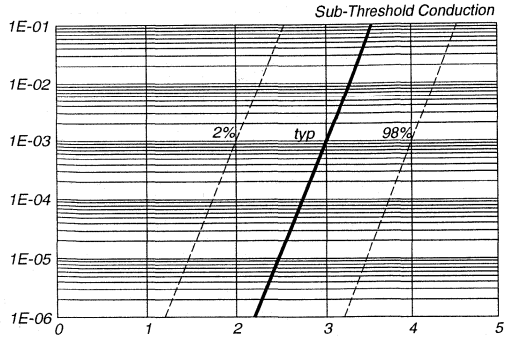


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

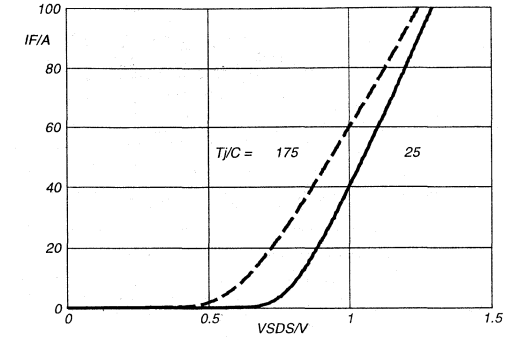


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

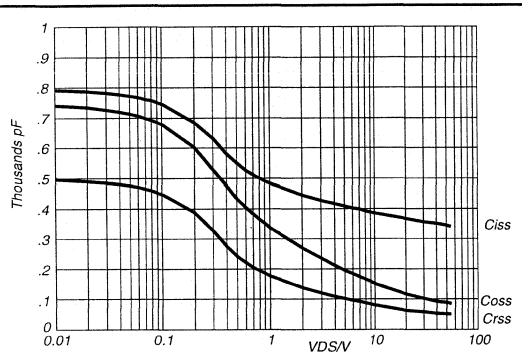


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

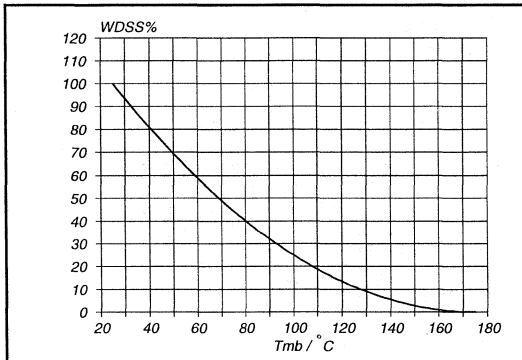


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: I_D = 17 A

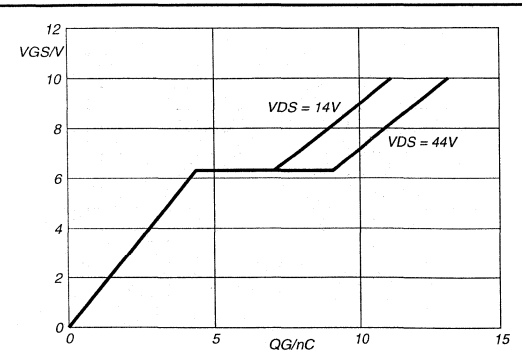


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 20 A; parameter V_{DS}

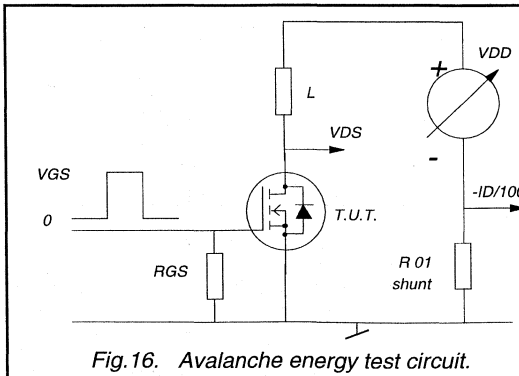


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

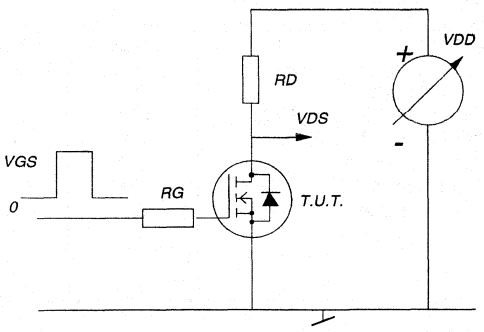


Fig.17. Switching test circuit.

TrenchMOS™ transistor Standard level FET

BUK7830-3

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope suitable for surface mounting. Using '**trench**' technology, the device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

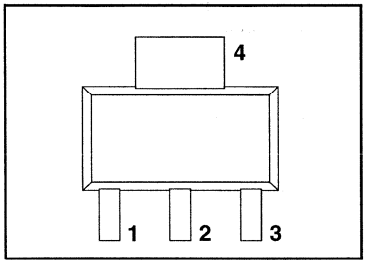
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	30	V
I_D	Drain current (DC) T_{sp} = 25 °C	12.8	A
	Drain current (DC) T_{amb} = 25 °C	5.9	A
P_{tot}	Total power dissipation	8.3	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	30	mΩ

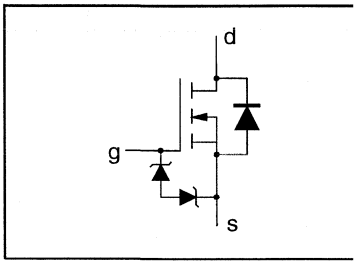
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	30	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	30	V
$\pm V_{GS}$	Gate-source voltage	-	-	16	V
I_D	Drain current (DC)	T_{sp} = 25 °C	-	12.8	A
		T_{amb} = 25 °C	-	5.9	A
I_D	Drain current (DC)	T_{sp} = 100 °C	-	9	A
		T_{amb} = 100 °C	-	4.1	A
I_{DM}	Drain current (pulse peak value)	T_{sp} = 25 °C	-	51.2	A
		T_{amb} = 25 °C	-	23.6	A
P_{tot}	Total power dissipation	T_{sp} = 25 °C	-	8.3	W
		T_{amb} = 25 °C	-	1.8	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}sp}$	Thermal resistance junction to solder point	Mounted on any PCB	12	15	K/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction to ambient	Mounted on PCB of Fig.19	-	70	K/W

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	30	-	-	V
		T_j = -55˚C	27	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.0	3.0	4.0	V
		T_j = 150˚C	1.0	-	-	V
		T_j = -55˚C	-	-	4.4	
I_{DSS}	Zero gate voltage drain current	V_{DS} = 30 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 150˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 150˚C	-	-	20	µA
$\pm V_{(BR)GSS}$	Gate source breakdown voltage	I_G = ±1 mA;	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 3.2 A	-	24	30	mΩ
		T_j = 150˚C	-	-	51	mΩ

DYNAMIC CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5.9 A	5	10	-	S
$Q_{g(tot)}$	Total gate charge	I_D = 5.9 A; V_{DD} = 24 V; V_{GS} = 10 V	-	22.5	-	nC
Q_{gs}	Gate-source charge		-	4.5	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	9	-	nC
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	740	-	pF
C_{oss}	Output capacitance		-	270	-	pF
C_{rss}	Feedback capacitance		-	130	-	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 15 V; I_D = 5.9 A;	-	16	22	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 5 Ω	-	30	60	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	35	50	ns
t_f	Turn-off fall time		-	25	38	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	6.2	A
I_{DRM}	Pulsed reverse drain current		-	-	24.8	A
V_{SD}	Diode forward voltage	I_F = 3.2 A; V_{GS} = 0 V	-	0.75	1.2	V
		I_F = 5.9 A; V_{GS} = 0 V	-	0.85	-	
t_{rr}	Reverse recovery time	I_F = 5.9 A; -dI_F/dt = 100 A/µs;	-	115	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 25 V	-	0.3	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 5.9 A; $V_{DD} \leq$ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{sp} = 25 ˚C	-	-	60	mJ

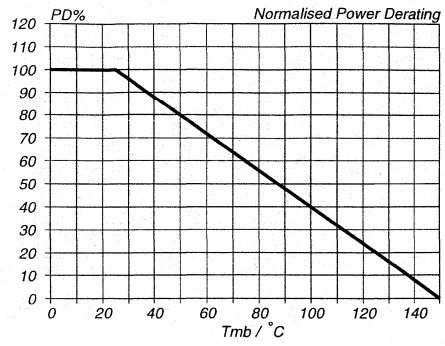


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

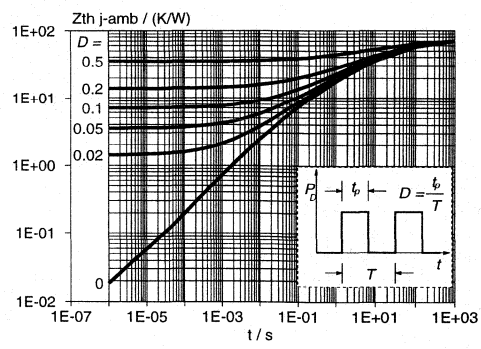


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

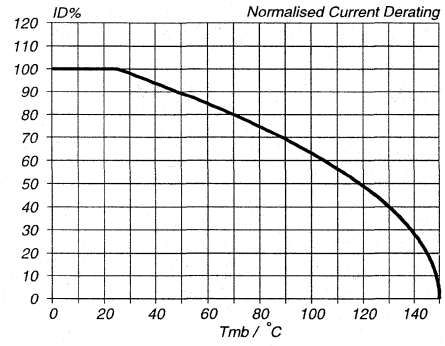


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

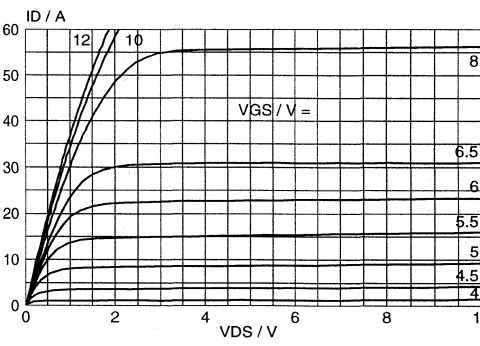


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

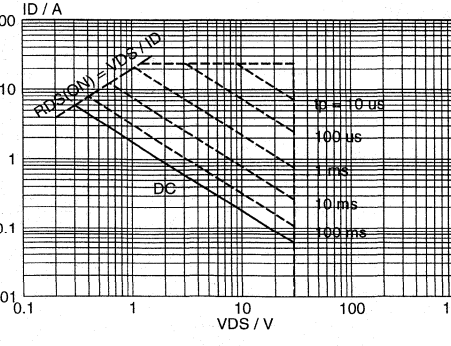


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

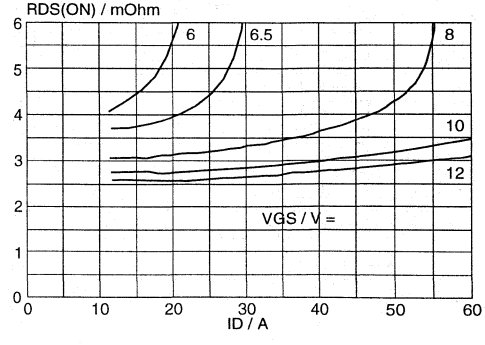


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

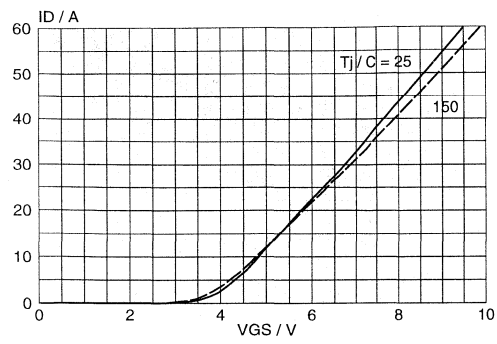


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

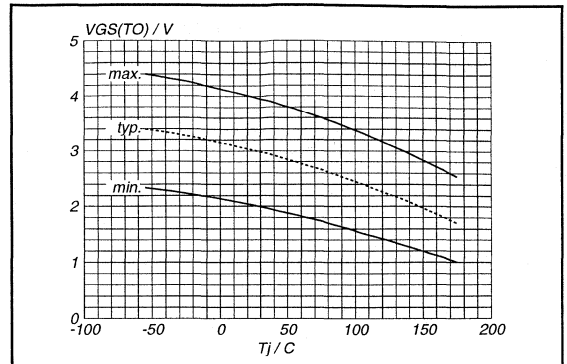


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

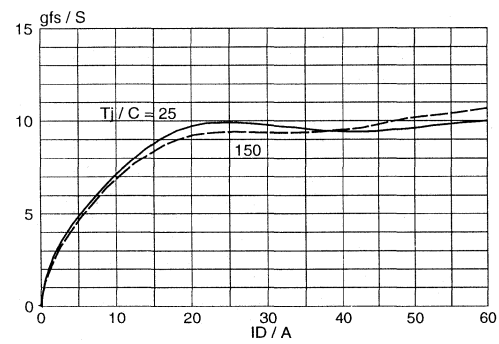


Fig.8. Typical transconductance, T_j = 25 ˚C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

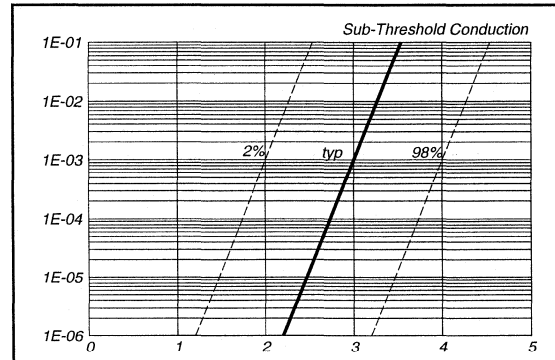


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

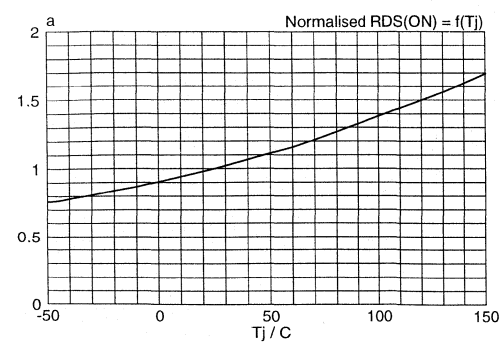


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,^{\circ}C} = f(T_j)$; I_D = 3.2 A; V_{GS} = 10 V

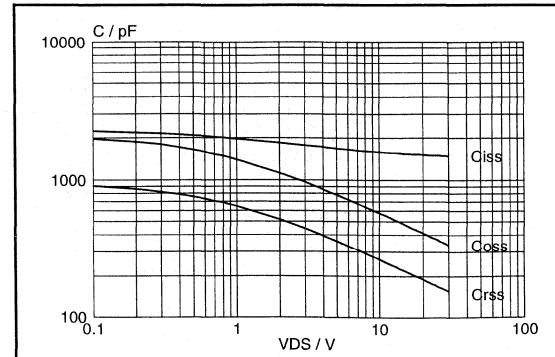


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

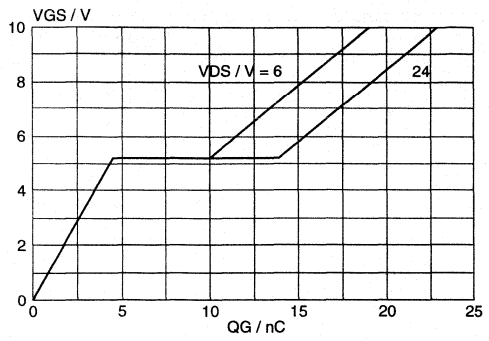


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 5.9$ A; parameter V_{DS}

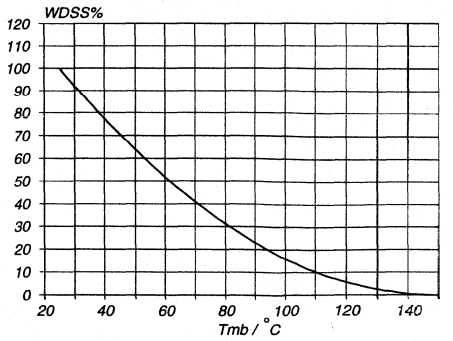


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 5.9$ A

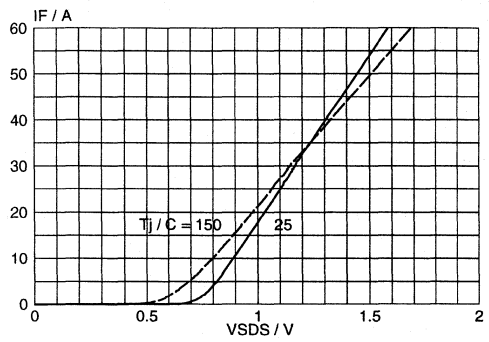


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

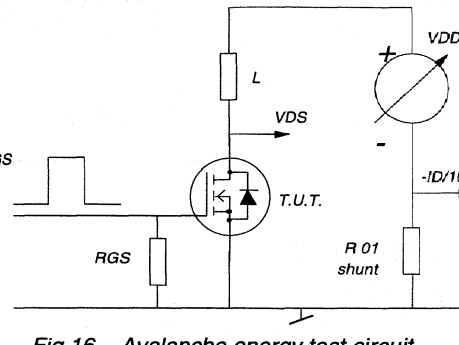


Fig.16. Avalanche energy test circuit.
$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

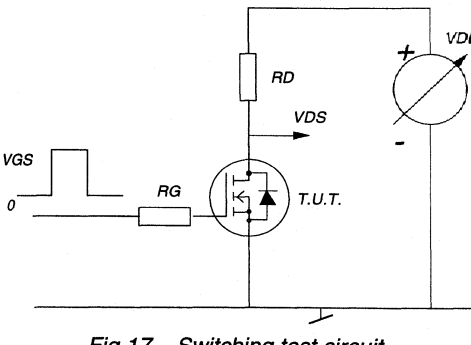


Fig.17. Switching test circuit.

MOUNTING INSTRUCTIONS

Dimensions in mm.

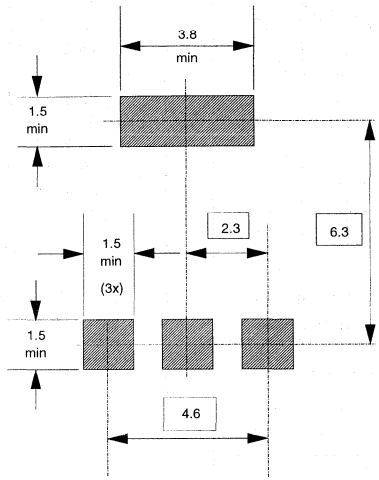


Fig.18. soldering pattern for surface mounting SOT223.

PRINTED CIRCUIT BOARD

Dimensions in mm.

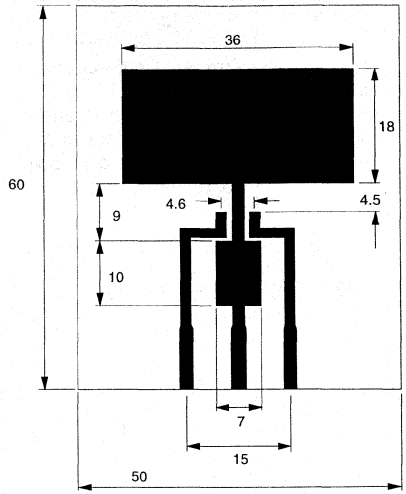


Fig.19. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).

TrenchMOS™ transistor Standard level FET

BUK7840-5

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting. Using **'trench'** technology the device features very low on-state resistance and has integral zener diodes giving ESD protection. It is intended for use in automotive and general purpose switching applications.

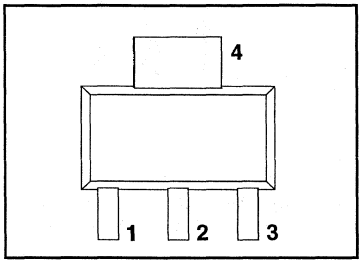
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current	10.7	A
P_{tot}	Total power dissipation	1.8	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	40	mΩ

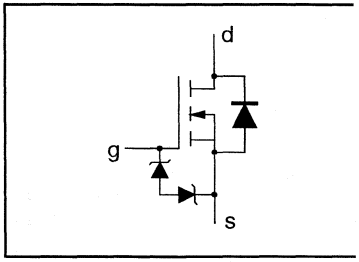
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	16	V
I_D	Drain current (DC)	T_{sp} = 25 °C	-	10.7	A
I_D	Drain current (DC)	On PCB in Fig.19 T_{amb} = 25 °C	-	5	A
I_D	Drain current (DC)	On PCB in Fig.19 T_{amb} = 100 °C	-	3.1	A
I_{DM}	Drain current (pulse peak value)	T_{sp} = 25 °C	-	40	A
P_{tot}	Total power dissipation	T_{sp} = 25 °C	-	10.7	W
P_{tot}	Total power dissipation	On PCB in Fig.19 T_{amb} = 25 °C	-	1.8	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	150	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model (100 pF, 1.5 kΩ)	-	2	kV

HERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}sp}$	From junction to solder point	Mounted on any PCB	12	15	K/W
$R_{th\ j\text{-}amb}$	From junction to ambient	Mounted on PCB of Fig.18	-	70	K/W

TATIC CHARACTERISTICS

= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.0	3.0	4.0	V
		T_j = 150˚C	1.2	-	-	V
		T_j = -55˚C	-	-	4.4	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 150˚C	-	-	100	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V	-	0.04	1	µA
		T_j = 150˚C	-	-	10	µA
$±V_{(BR)GSS}$	Gate source breakdown voltage	I_G = ±1 mA	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A	-	30	40	mΩ
		T_j = 150˚C	-	-	74	mΩ

ʏNAMIC CHARACTERISTICS

$_{mb}$ = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5 A; T_j = 25˚C	3	12	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	700	880	pF
C_{oss}	Output capacitance		-	200	240	pF
C_{rss}	Feedback capacitance		-	100	140	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 9 A;	-	15	23	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_g = 10 Ω	-	50	75	ns
$t_{d\ off}$	Turn-off delay time		-	33	50	ns
t_f	Turn-off fall time	T_j = 25˚C	-	20	30	ns

ɪEVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

$_j$ = -55 to 175˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{sp} = 25˚C	-	-	10.7	A
I_{DRM}	Pulsed reverse drain current	T_{sp} = 25˚C	-	-	40	A
V_{SD}	Diode forward voltage	I_F = 5 A; V_{GS} = 0 V	-	0.85	1.1	V
t_{rr}	Reverse recovery time	I_F = 5 A; -dI_F/dt = 100 A/µs;	-	45	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.3	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 3.6 A; $V_{DD} \leq$ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{sp} = 25 ˚C	-	-	60	mJ

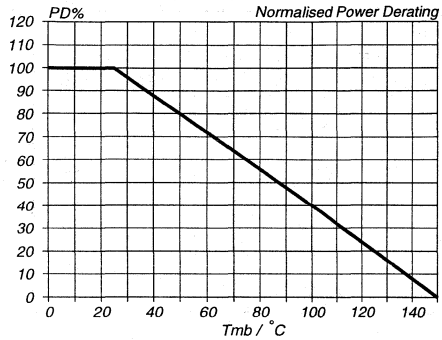


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ ˚C}$ = f(T_{sp})

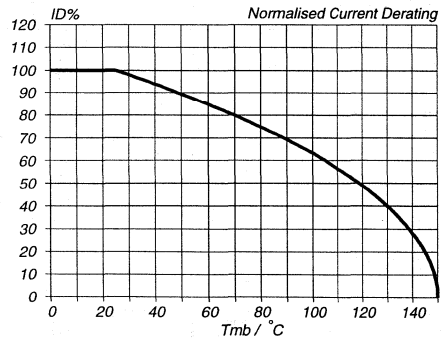


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ ˚C}$ = f(T_{sp}); conditions: $V_{GS} \geq$ 10 V

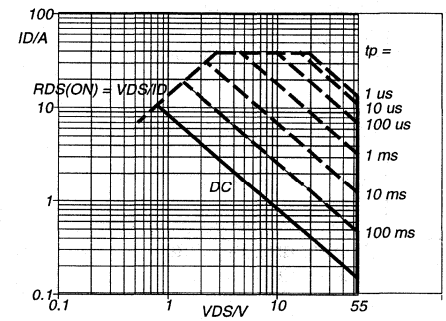


Fig.3. Safe operating area. T_{sp} = 25 ˚C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

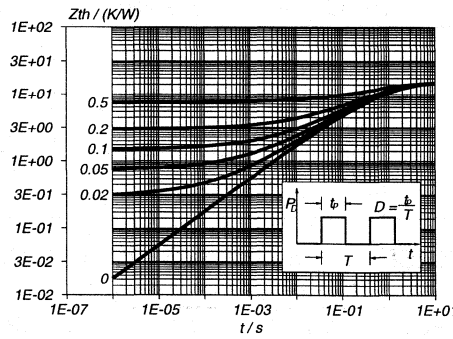


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}sp}$ = f(t); parameter D = t_p/T

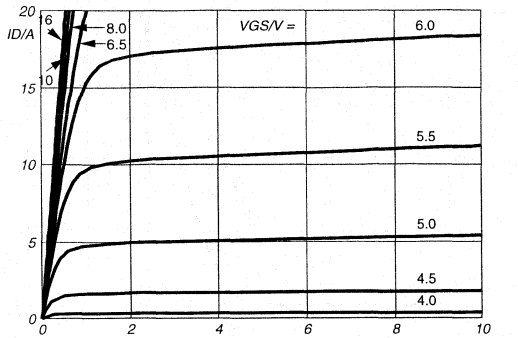


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

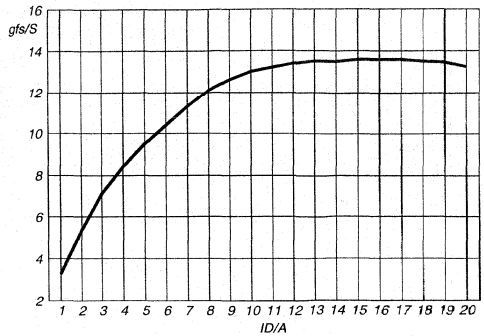


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

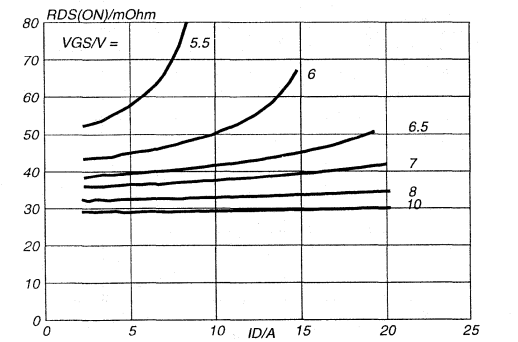


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

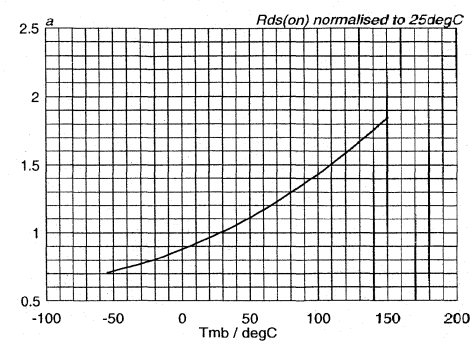


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 5 A; V_{GS} = 10 V

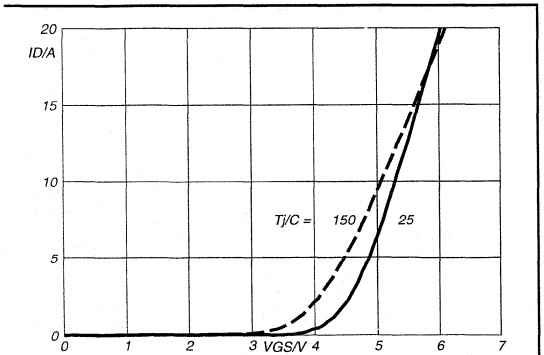


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

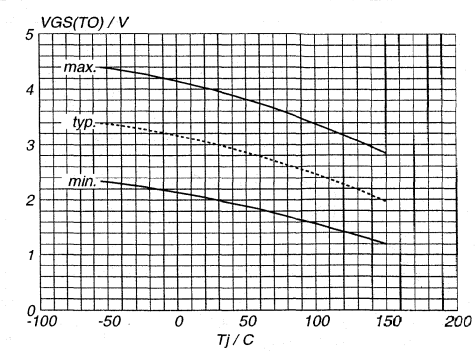


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

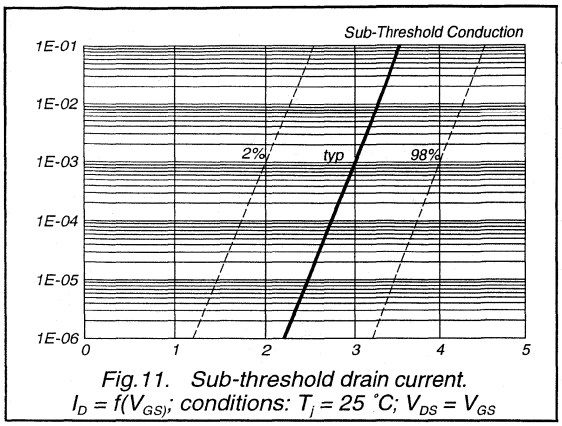


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

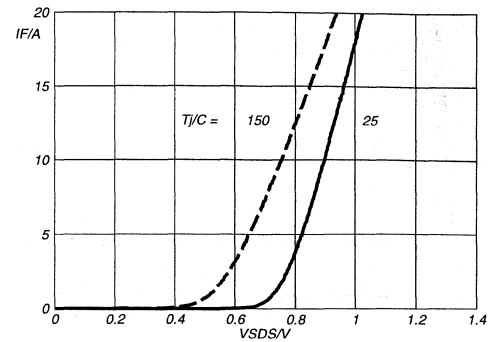


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

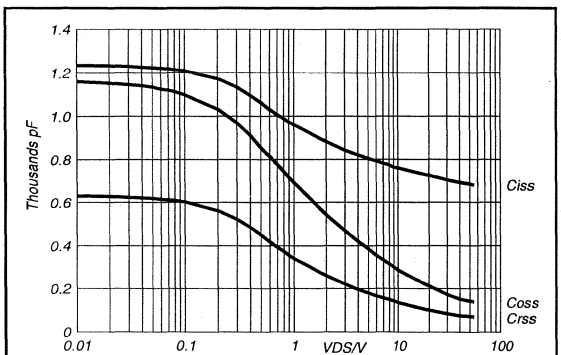


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

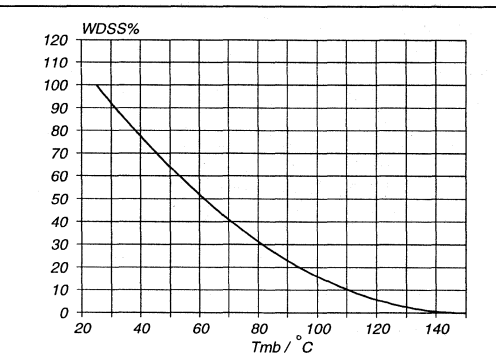


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{sp})$; conditions: $I_D = 3.6$ A

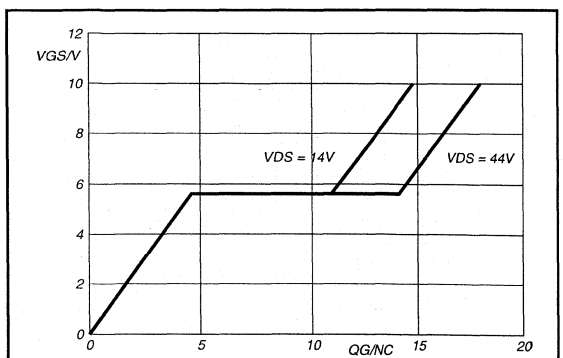


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 9$ A; parameter V_{DS}

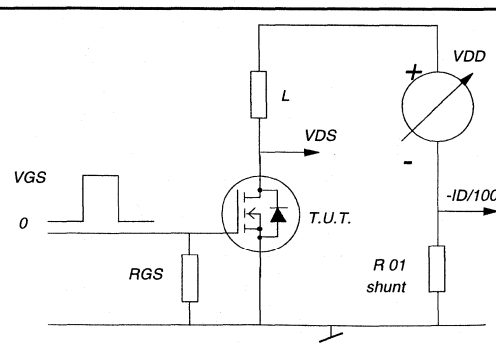


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

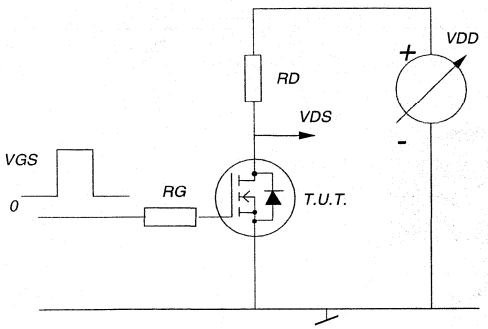


Fig.17. Switching test circuit.

PRINTED CIRCUIT BOARD

Dimensions in mm.

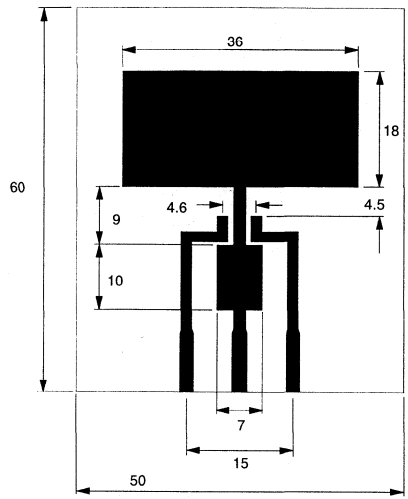


Fig.18. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).

renchMOS™ transistor
tandard level FET

BUK7880-55

ENERAL DESCRIPTION

-channel enhancement mode logic vel field-effect power transistor in a astic envelope suitable for surface ounting. Using **'trench'** technolgy e device features very low on-state sistance and has integral zener odes giving ESD protection. It is tended for use in automotive and eneral purpose switching pplications.

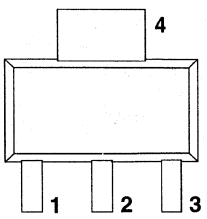
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current	7.5	A
P_{tot}	Total power dissipation	1.8	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	80	mΩ

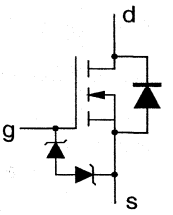
INNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



IMITING VALUES

imiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	16	V
I_D	Drain current (DC)	T_{sp} = 25 °C	-	7.5	A
I_D	Drain current (DC)	On PCB in Fig.2 T_{amb} = 25 °C	-	3.5	A
I_D	Drain current (DC)	On PCB in Fig.2 T_{amb} = 100 °C	-	2.2	A
I_{DM}	Drain current (pulse peak value)	T_{sp} = 25 °C	-	40	A
P_{tot}	Total power dissipation	T_{sp} = 25 °C	-	8.3	W
P_{tot}	Total power dissipation	On PCB in Fig.2 T_{amb} = 25 °C	-	1.8	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	150	°C

SD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}sp}$	From junction to solder point	Mounted on any PCB	12	15	K/W
$R_{th\ j\text{-}amb}$	From junction to ambient	Mounted on PCB of Fig.18	-	70	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2	3	4	V
		T_j = 150˚C	1.2	-	-	V
		T_j = -55˚C	-	-	4.4	
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 150˚C	-	-	100	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V	-	0.04	1	µA
		T_j = 150˚C	-	-	10	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A	-	65	80	mΩ
		T_j = 150˚C	-	-	148	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5 A; T_j = 25˚C	1	4	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	365	500	pF
C_{oss}	Output capacitance		-	110	135	pF
C_{rss}	Feedback capacitance		-	60	85	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 7 A;	-	9	14	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 10 Ω;	-	15	25	ns
$t_{d\ off}$	Turn-off delay time		-	18	27	ns
t_f	Turn-off fall time	T_j = 25˚C	-	12	18	ns

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = -55 to 175˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{sp} = 25˚C	-	-	7.5	A
I_{DRM}	Pulsed reverse drain current	T_{sp} = 25˚C	-	-	40	A
V_{SD}	Diode forward voltage	I_F = 5 A; V_{GS} = 0 V	-	0.85	1.1	V
t_{rr}	Reverse recovery time	I_F = 5 A; -dI_F/dt = 100 A/µs;	-	38	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.2	-	µC

\VALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 2.5 A; $V_{DD} \leq$ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{sp} = 25 °C	-	-	30	mJ

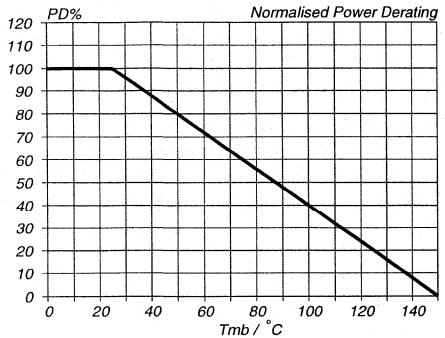


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{sp})

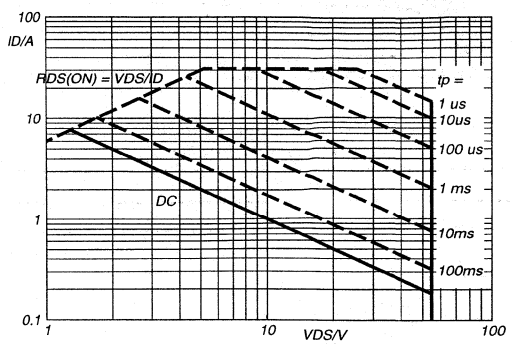


Fig.3. Safe operating area. T_{sp} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

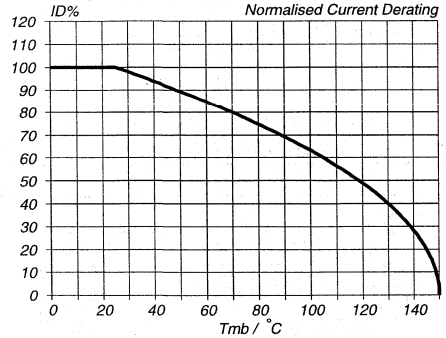


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{sp}); conditions: $V_{GS} \geq$ 10 V

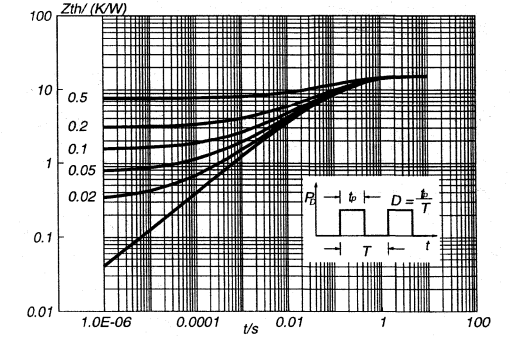


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}sp}$ = f(t); parameter D = t_p/T

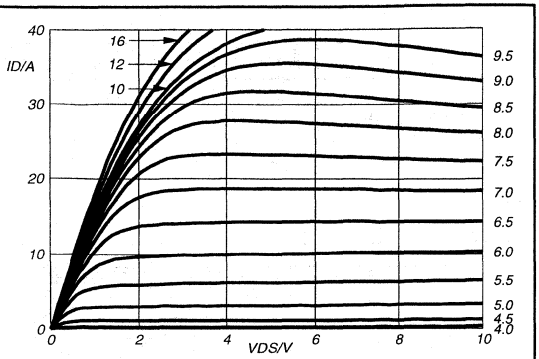


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

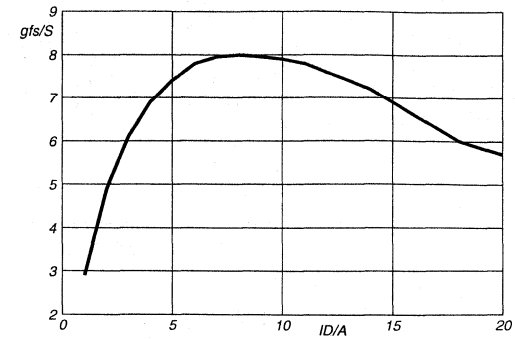


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

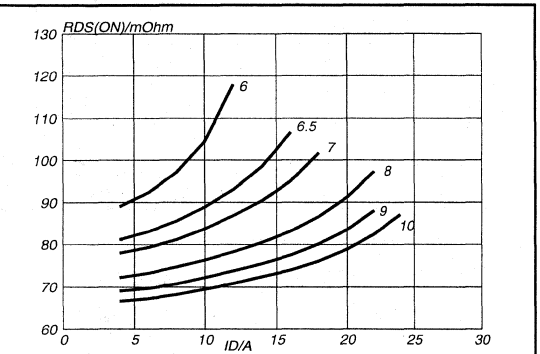


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

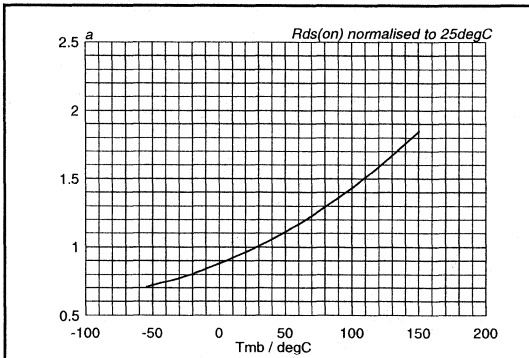


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\ ˚C} = f(T_j)$; I_D = 5 A; V_{GS} = 10 V

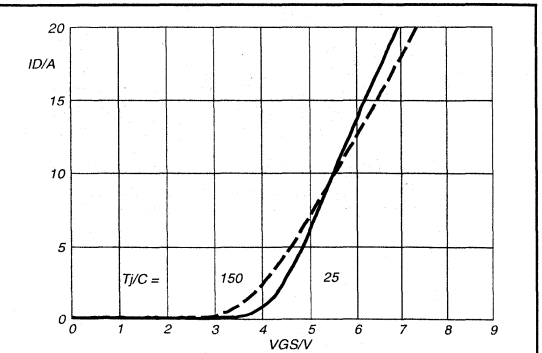


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

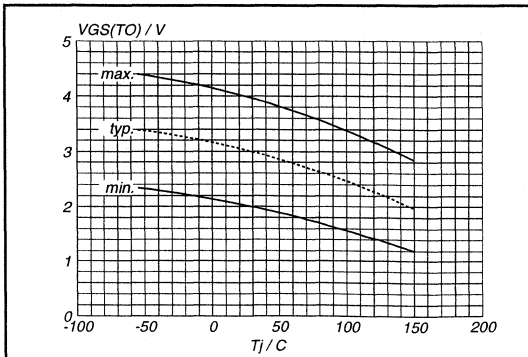


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

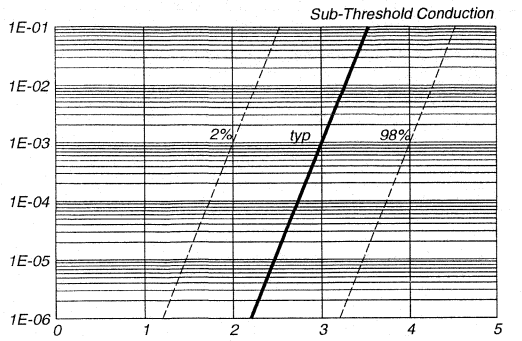


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

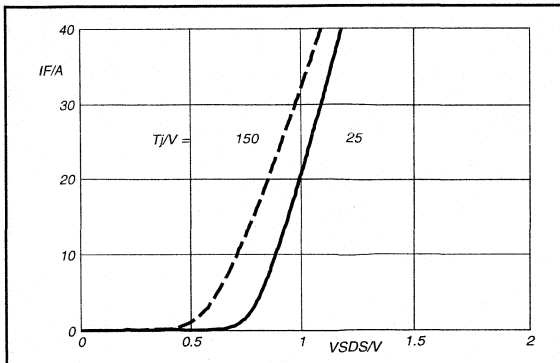


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

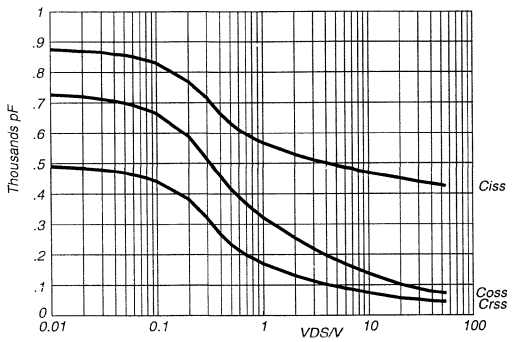


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

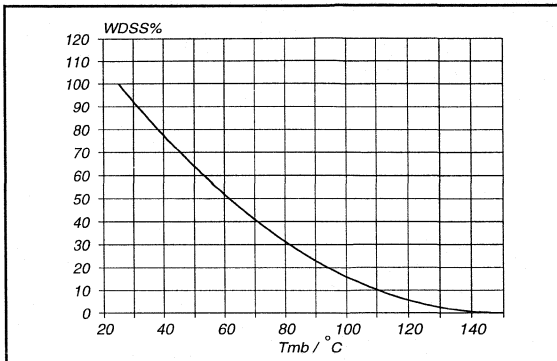


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{sp})$; conditions: $I_D = 2.5$ A

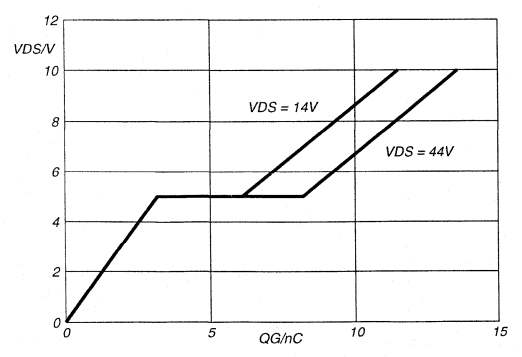


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 7$ A; parameter V_{DS}

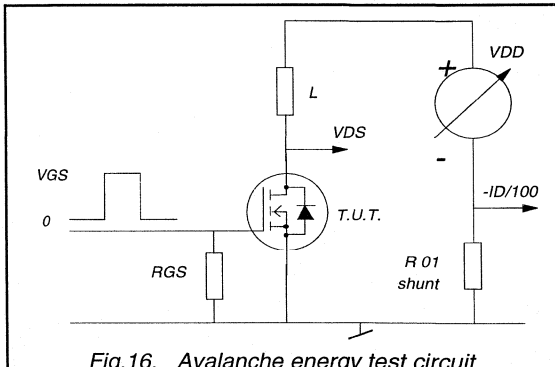


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

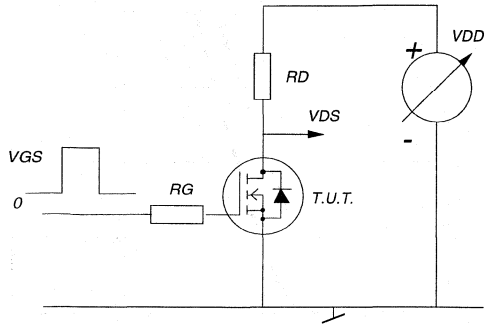


Fig.17. Switching test circuit.

RINTED CIRCUIT BOARD

Dimensions in mm.

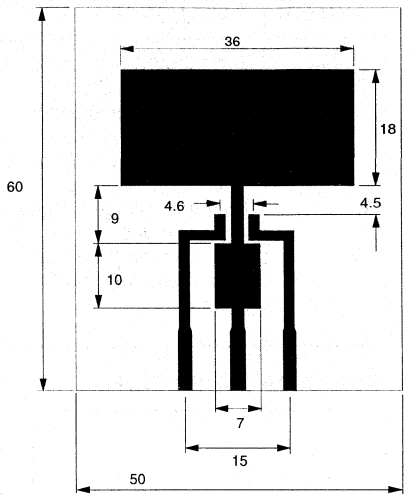


Fig.18. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).

PowerMOS transistor
Voltage clamped logic level FET
with temperature sensing diodes

BUK9120-48TC

GENERAL DESCRIPTION

Protected N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting. Using **'trench'** technology the device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV and active drain voltage clamping. Temperature sensitive diodes are incorporated for monitoring chip temperature.
The device is intended for use in automotive and general purpose switching applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSR}$	Drain-source clamp voltage	40	45	55	V
I_D	Drain current (DC)			52	A
P_{tot}	Total power dissipation			116	W
T_j	Junction temperature			175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V			20	mΩ
V_F	Forward voltage,temperature sense diodes	685	710	735	mV
$-S_F$	Negative temperature coefficient, temperature sense diodes	1.26	1.4	1.54	mV/K

PINNING - SOT426

PIN	DESCRIPTION
1	gate
2	T1
3	(connected to mb)
4	T2
5	source
mb	drain

PIN CONFIGURATION

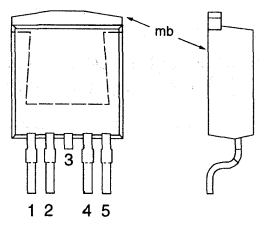


Fig. 1.

SYMBOL

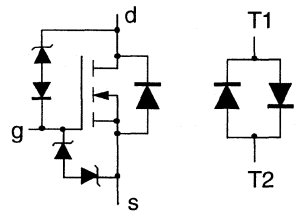


Fig. 2.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	continuous	-	40	V
V_{DG}	Drain-gate voltage	continuous	-	38	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	52	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	37	A
I_D	Drain current (DC)	T_{mb} = 140 °C	-	25	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	208	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	116	W
I_{GD}	Drain-gate clamp current	5ms pulse; Δ = 0.01	-	50	mA
I_{GS}	Gate-source clamp current	5ms pulse; Δ = 0.01	-	50	mA
V_{TS}	Source T1/T2 voltage	-	-	±100	V
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	- 55	175	°C

SD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge voltage, pins 1,3,5	Human body model (100pF,1.5KΩ)	-	2	kV

HERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.29	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board	-	50	-	K/W

TATIC CHARACTERISTICS

= 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DG}$	Drain-gate zener voltage	250uA; -55˚C ≤ T_j ≤ 175˚C	38	43		V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; I_D = 1 mA;	1.0	1.5	2.0	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = +35 V; V_{GS} = 0 V;	-	0.1	100	µA
		T_j =175 ˚C	-	-	250	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = +15 V; V_{GS} = 0 V;	-	0.004	2	µA
		T_j =175 ˚C	-	-	250	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V;	-	0.02	1	µA
		T_j =175 ˚C	-	-	10	µA
$\pm V_{(BR)GSS}$	Gate source breakdown voltage	±1 mA;	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 20 A	-	16	20	mΩ
		T_j =175 ˚C	-	-	42	mΩ
						V
V_F	Forward voltage, temperature sense diodes	I_F = 250 uA;	685	710	735	mV
$-S_F$	Negative temperature coefficient, temperature sense diodes from 25 ˚C to 140 ˚C	I_F = 250 uA	1.26	1.4	1.54	mV/K
V_{HYS}	Forward voltage hysteresis; temperature sense diodes	I_F = 125 uA to 250uA	25		50	mV

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSR}$	Drain source clamp voltage (peak value)	R_G = 10 kΩ; I_D = 10 A; -55 ≤ T_j ≤ 175°C	40	45	55	V
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 10 A	20	53	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	2200	2900	pF
C_{oss}	Output capacitance		-	400	500	pF
C_{rss}	Feedback capacitance		-	215	300	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	12	18	µs
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 kΩ;	-	55	80	µs
$t_{d\,off}$	Turn-off delay time		-	60	85	µs
t_f	Turn-off fall time		-	45	60	µs
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	52	A
I_{DRM}	Pulsed reverse drain current	-	-	-	208	A
V_{SD}	Diode forward voltage	I_F = 20 A ; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 40 A ; V_{GS} = 0 V	-	1	-	V

CLAMPED ENERGY LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSRS}	Non-repetitive drain-source clamped inductive turn off energy	T_j = 25°C prior to clamping; I_D = 20 A; V_{DD} ≤ 16 V; V_{GS} = 5 V; R_G = 10 kΩ; inductive load	-	450	mJ

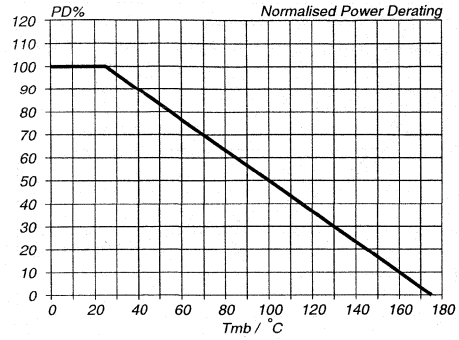


Fig.3. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

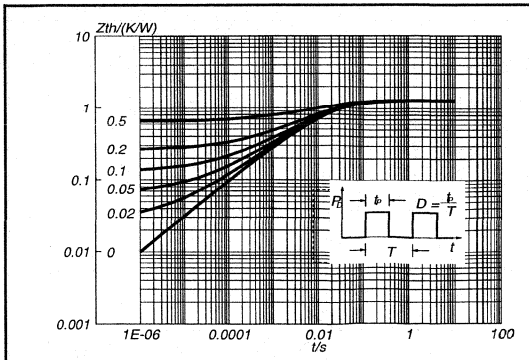


Fig.6. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

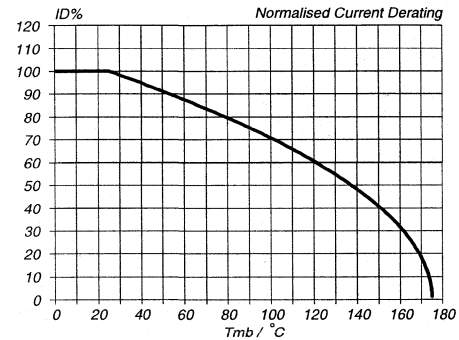


Fig.4. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq 5$ V

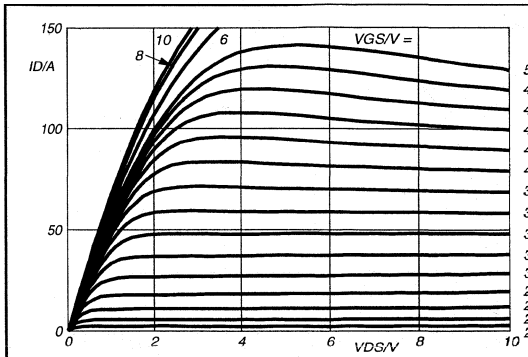


Fig.7. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

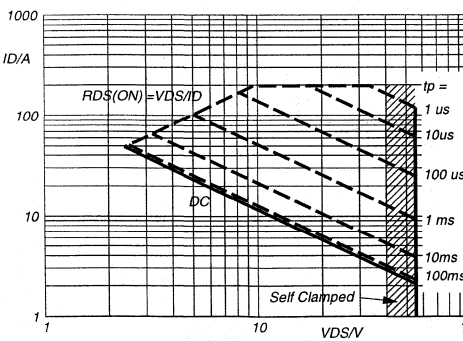


Fig.5. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

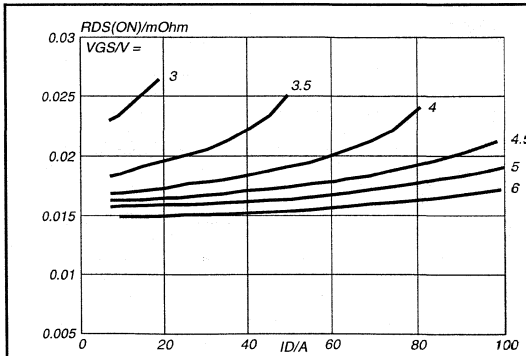


Fig.8. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

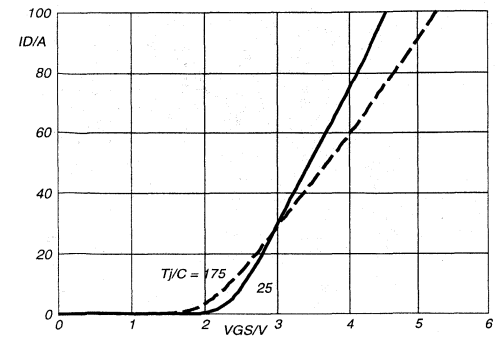


Fig.9. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

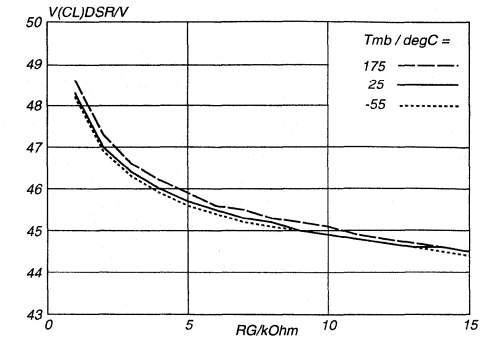


Fig.12. Typical clamping voltage
$V_{(CL)DSR} = f(R_G)$; conditions: I_D = 10 A

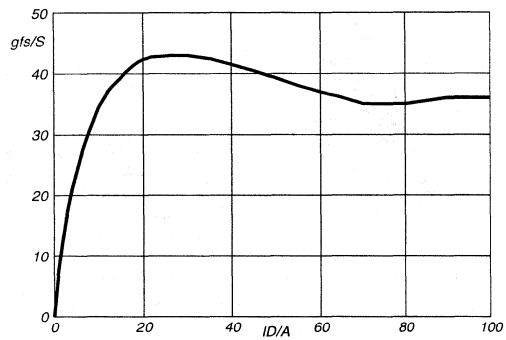


Fig.10. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

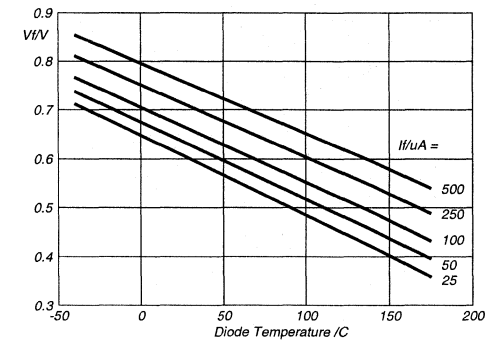


Fig.13. Typical Vf of sense diodes
$Vf = f(K)$; parameter I_f

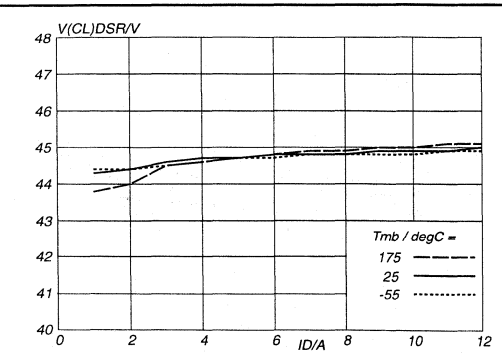


Fig.11. Typical clamping voltage
$V_{(CL)DSR} = f(I_D)$; conditions: R_G = 10 kOhm

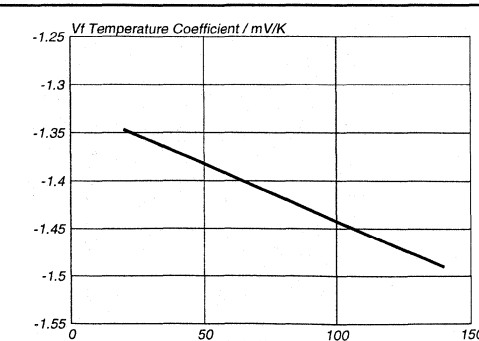


Fig.14. Typical Vf temperature coefficient
Vf Temp.Coef.= f(K); conditions: I_F = 250 uA

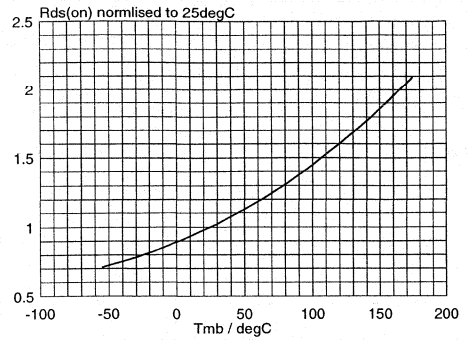


Fig.15. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

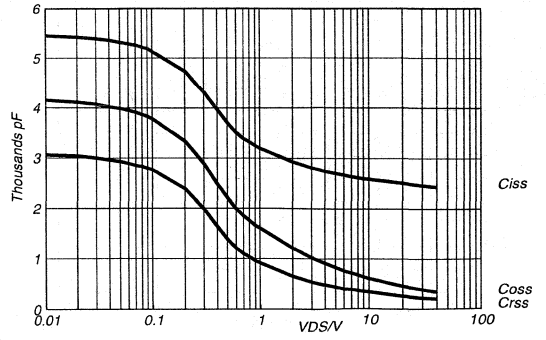


Fig.18. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

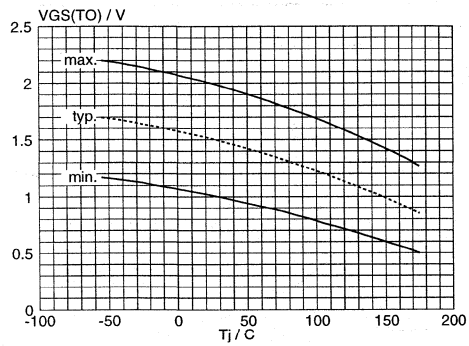


Fig.16. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

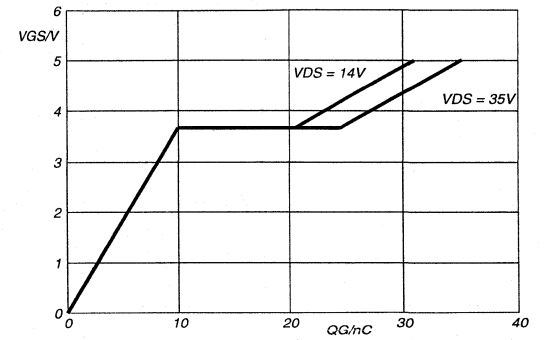


Fig.19. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 50 A; parameter V_{DS}

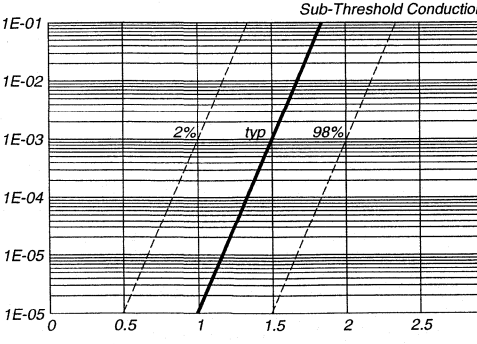


Fig.17. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

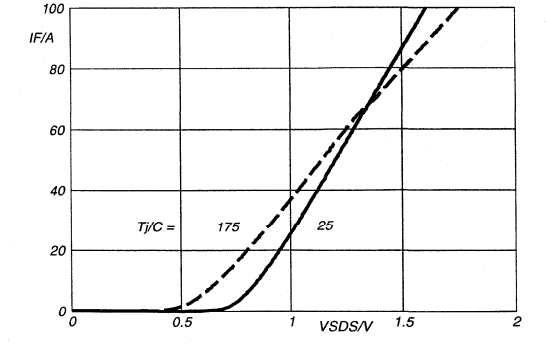


Fig.20. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

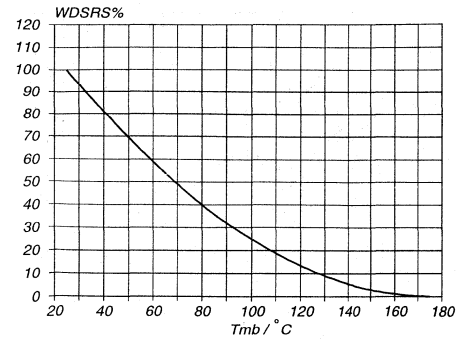


Fig.21. Normalised avalanche energy rating. $W_{DSRS}\% = f(T_{mb})$; conditions: $I_D = 20$ A

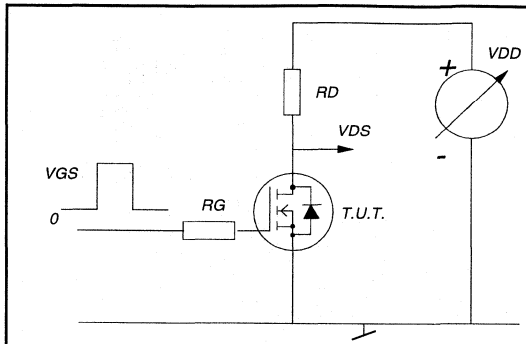


Fig.23. Switching test circuit.

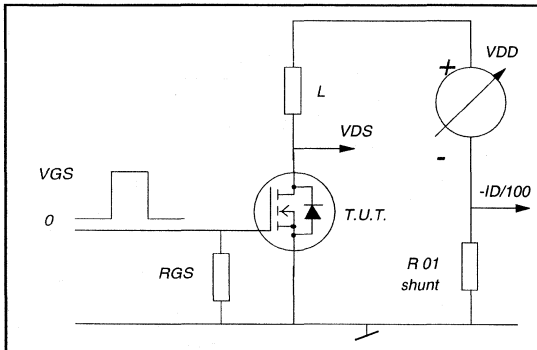


Fig.22. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

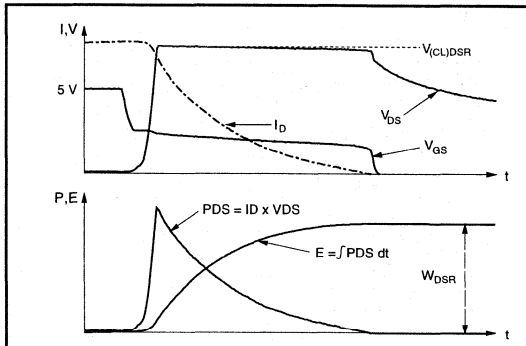


Fig.24. Typical Inductive Clamping Waveforms

TrenchMOS™ transistor Logic level FET

BUK9506-30

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using **'trench'** technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

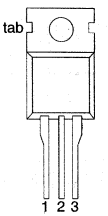
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	30	V
I_D	Drain current (DC)	75	A
P_{tot}	Total power dissipation	187	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	6	mΩ

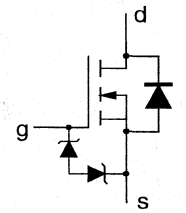
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	30	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	30	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	75	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	53	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	240	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	187	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	0.8	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	30	-	-	V
		T_j = -55˚C	27	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 30 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	10	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	5	6	mΩ
		T_j = 175˚C	-	-	11	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	20	40	-	S
$Q_{g(tot)}$	Total gate charge	I_D = 75 A; V_{DD} = 24 V; V_{GS} = 5 V	-	92	-	nC
Q_{gs}	Gate-source charge		-	10	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	36	-	nC
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	5000	-	pF
C_{oss}	Output capacitance		-	1150	-	pF
C_{rss}	Feedback capacitance		-	500	-	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 15 V; I_D = 25 A;	-	45	60	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 5 Ω	-	120	170	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	225	300	ns
t_f	Turn-off fall time		-	100	135	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

EVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

$_j$ = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	75	A
I_{DRM}	Pulsed reverse drain current		-	-	240	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.85	1.2	V
		I_F = 75 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 75 A; -dI_F/dt = 100 A/µs;	-	100	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 25 V	-	0.6	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 75 A; $V_{DD} \leq$ 15 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 ˚C	-	-	500	mJ

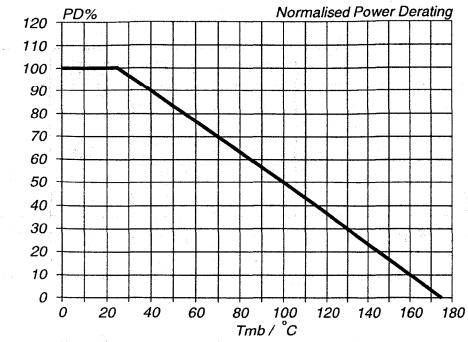


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

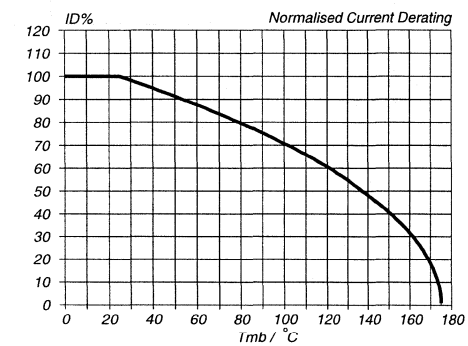


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq 5$ V

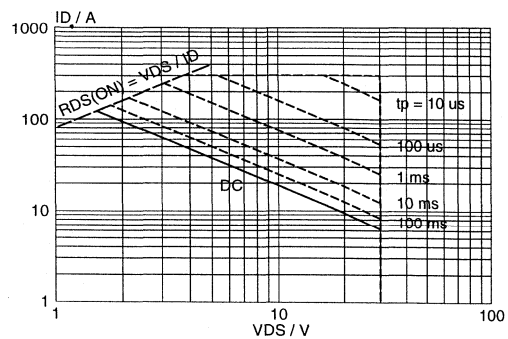


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

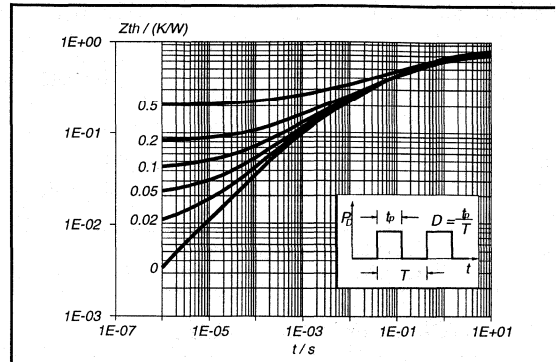


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

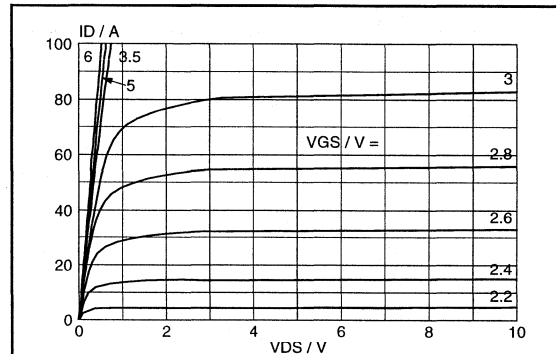


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

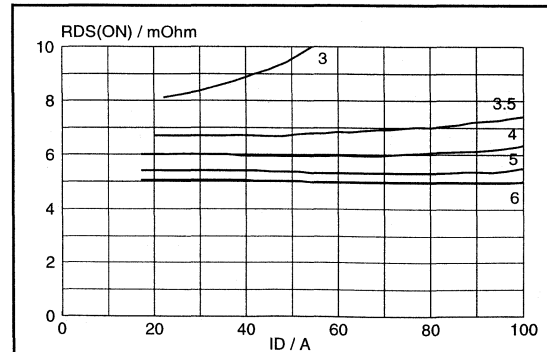


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

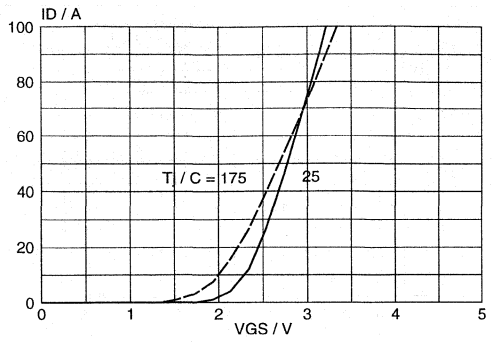


Fig.7. Typical transfer characteristics.
I_D = f(V_{GS}) ; conditions: V_{DS} = 25 V; parameter T_j

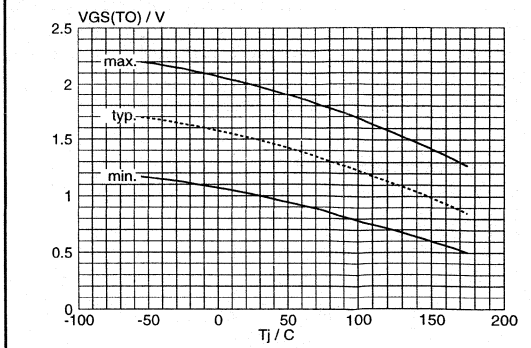


Fig.10. Gate threshold voltage.
$V_{GS(TO)}$ = f(T_j); conditions: I_D = 1 mA; V_{DS} = V_{GS}

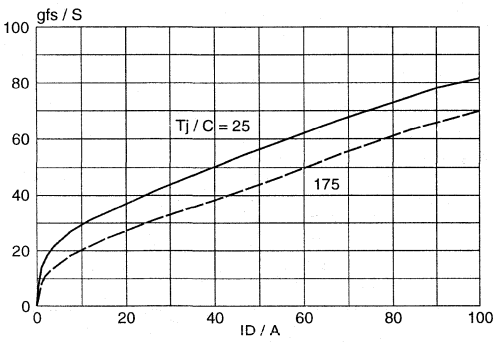


Fig.8. Typical transconductance, T_j = 25 °C.
g_{fs} = f(I_D); conditions: V_{DS} = 25 V

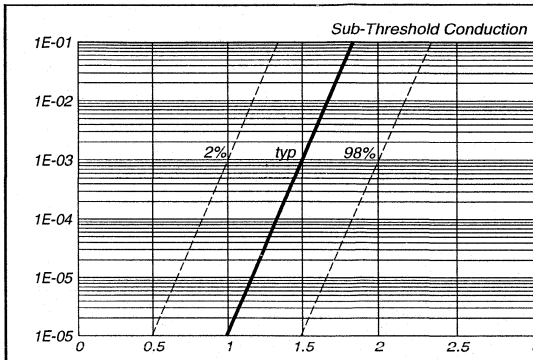


Fig.11. Sub-threshold drain current.
I_D = f(V_{GS}); conditions: T_j = 25 °C; V_{DS} = V_{GS}

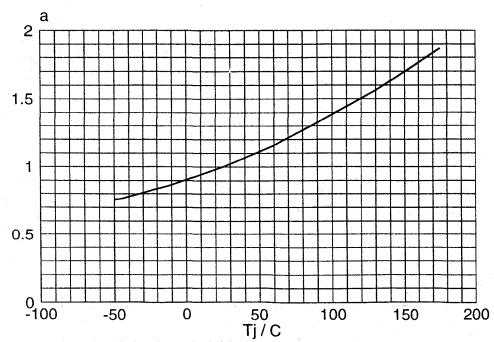


Fig.9. Normalised drain-source on-state resistance.
a = $R_{DS(ON)}$/$R_{DS(ON)25\,°C}$ = f(T_j); I_D = 25 A; V_{GS} = 5 V

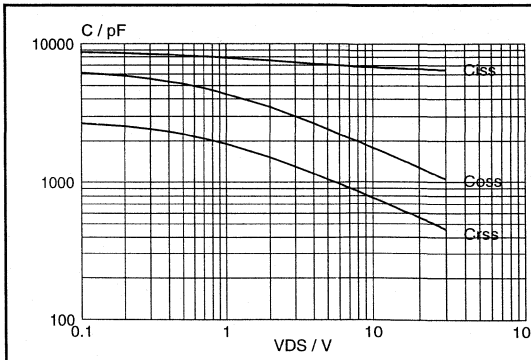


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
C = f(V_{DS}); conditions: V_{GS} = 0 V; f = 1 MHz

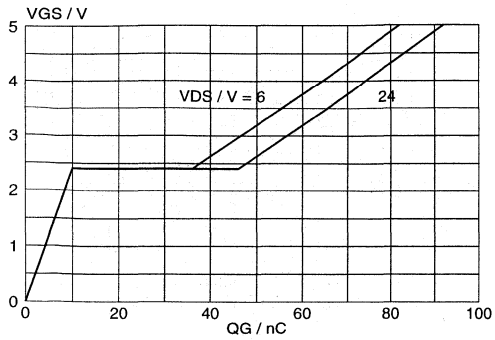


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: I_D = 75 A; parameter V_{DS}

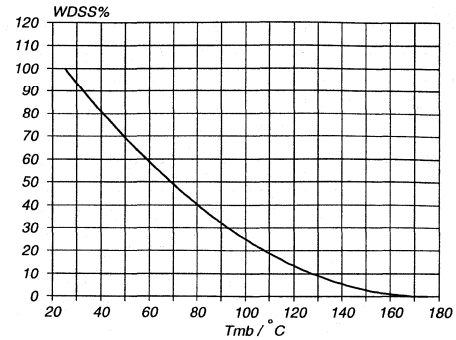


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: I_D = 75 A

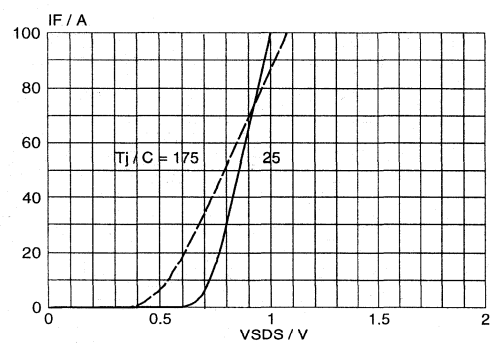


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

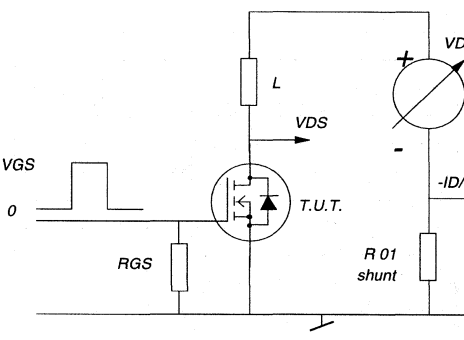


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

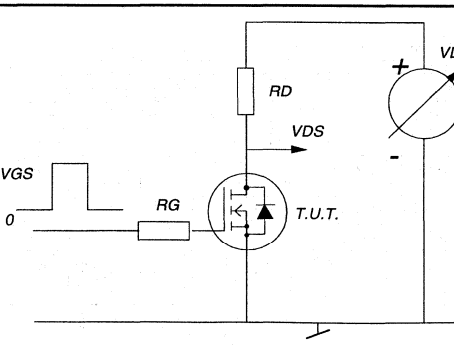


Fig.17. Switching test circuit.

rrenchMOS™ transistor
ogic level FET

BUK9508-55

ENERAL DESCRIPTION

-channel enhancement mode logic vel field-effect power transistor in a lastic envelope using **'trench'** chnology. The device features very w on-state resistance and has ntegral zener diodes giving ESD rotection up to 2kV. It is intended for se in automotive and general urpose switching applications.

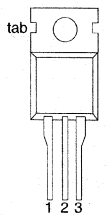
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	75	A
P_{tot}	Total power dissipation	187	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	8	mΩ

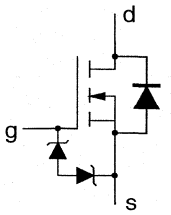
INNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



IMITING VALUES

imiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	75	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	65	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	240	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	187	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

SD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model (100 pF, 1.5 kΩ)	-	2	kV

HERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	0.8	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	uA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	10	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	6.5	8	mΩ
		T_j = 175˚C	-	-	17	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	40	90	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	5200	6900	pF
C_{oss}	Output capacitance		-	840	1000	pF
C_{rss}	Feedback capacitance		-	350	480	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	45	60	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω	-	120	170	ns
$t_{d\,off}$	Turn-off delay time		-	225	300	ns
t_f	Turn-off fall time		-	100	135	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	75	A
I_{DRM}	Pulsed reverse drain current		-	-	240	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.85	1.2	V
		I_F = 75 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 75 A; -dI_F/dt = 100 A/µs;	-	65	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.18	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 75 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	500	mJ

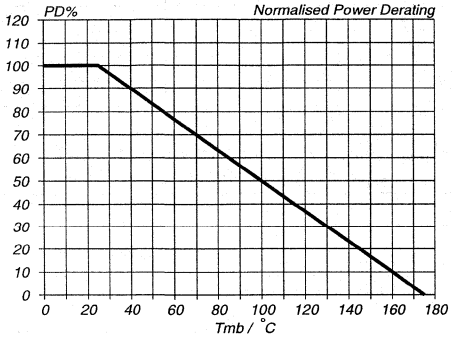


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

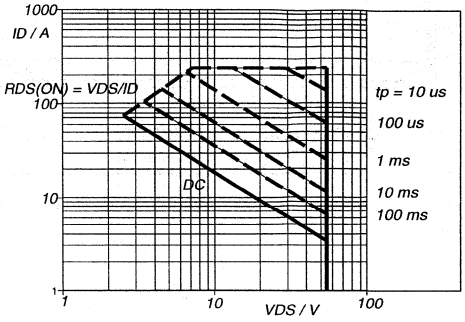


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

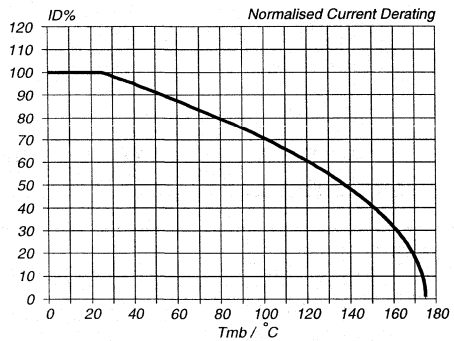


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

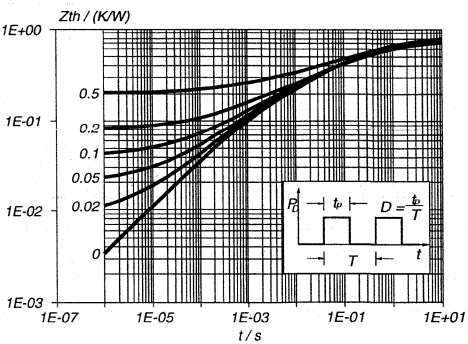


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

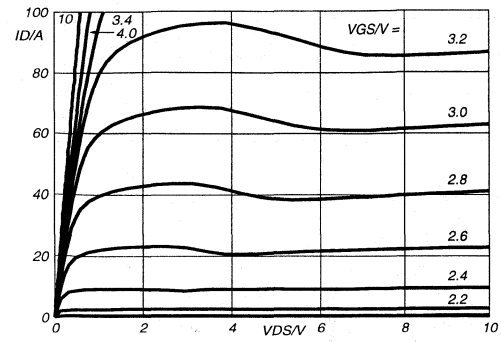


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

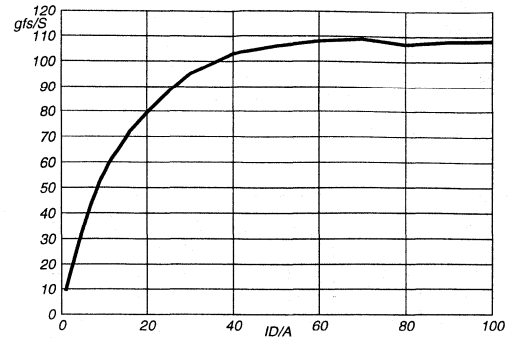


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

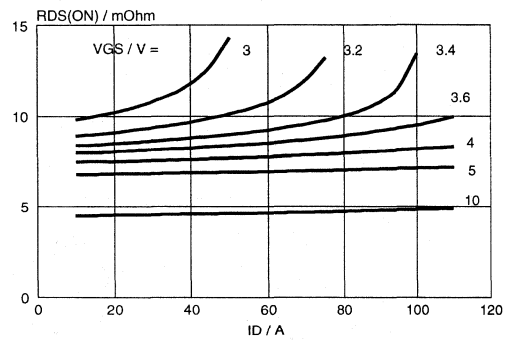


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

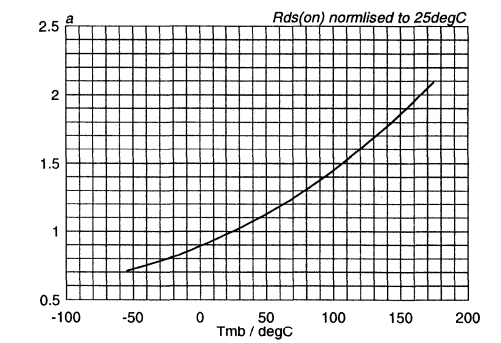


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,˚C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

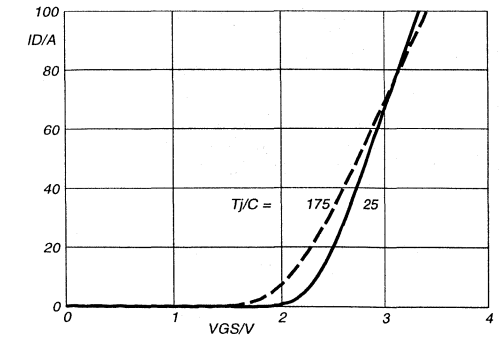


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

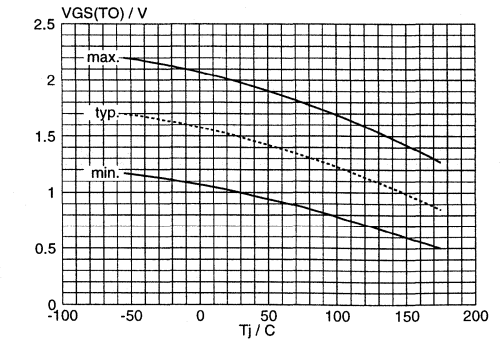


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

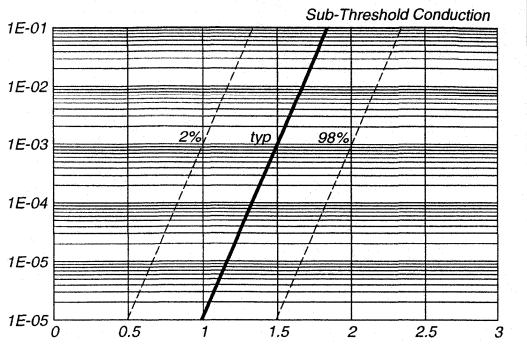


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

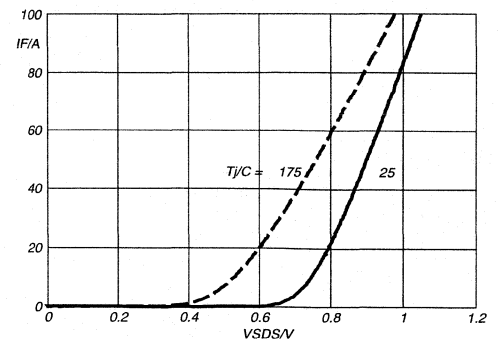


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

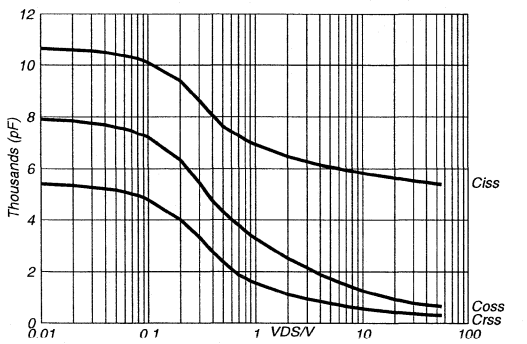


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

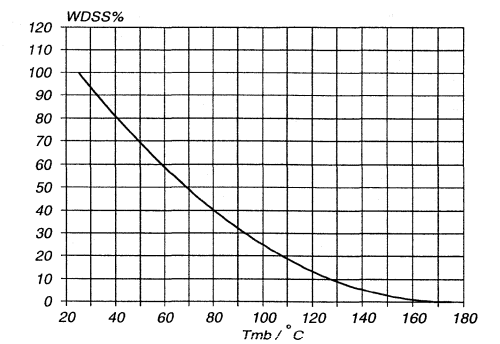


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 75$ A

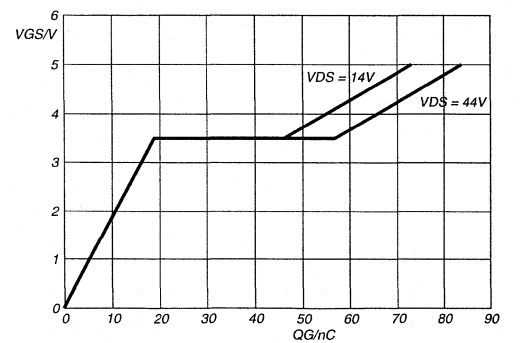


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 50$ A; parameter V_{DS}

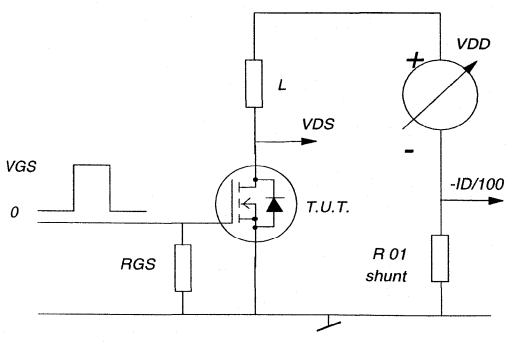


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

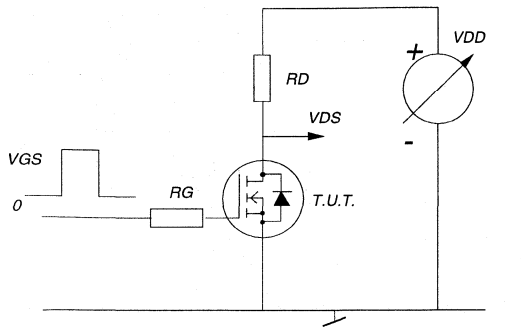


Fig.17. Switching test circuit.

TrenchMOS™ transistor Logic level FET

BUK9510-30

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using **'trench'** technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

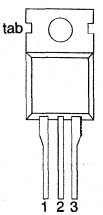
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	30	V
I_D	Drain current (DC)	75	A
P_{tot}	Total power dissipation	142	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	10.5	mΩ

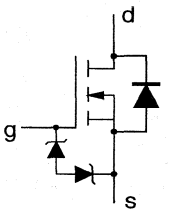
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	30	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	30	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	75	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	53	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	240	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	142	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.05	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model (100 pF, 1.5 kΩ)	-	2	kV

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	30	-	-	V
		T_j = -55˚C	27	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 30 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	uA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	10	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	9	10.5	mΩ
		T_j = 175˚C	-	-	19.5	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	12	25	-	S
$Q_{g(tot)}$	Total gate charge	I_D = 75 A; V_{DD} = 24 V; V_{GS} = 5 V	-	58	-	nC
Q_{gs}	Gate-source charge		-	6	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	24	-	nC
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	2500	-	pF
C_{oss}	Output capacitance		-	640	-	pF
C_{rss}	Feedback capacitance		-	320	-	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 15 V; I_D = 25 A;	-	35	50	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 5 Ω	-	95	145	ns
$t_{d\,off}$	Turn-off delay time		-	130	180	ns
t_f	Turn-off fall time		-	60	80	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	75	A
I_{DRM}	Pulsed reverse drain current		-	-	240	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 75 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 75 A; -dI_F/dt = 100 A/µs;	-	70	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 25 V	-	0.14	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 45 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	200	mJ

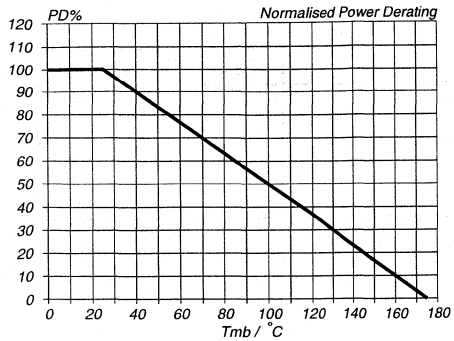


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

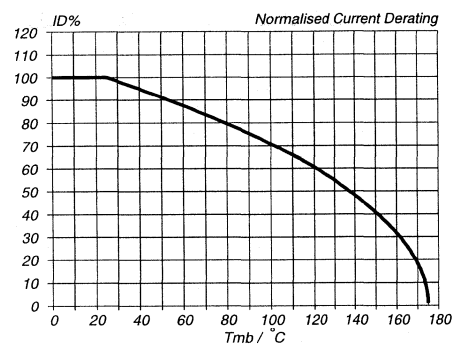


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq 5$ V

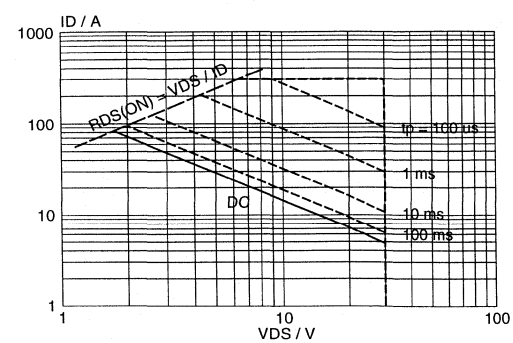


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

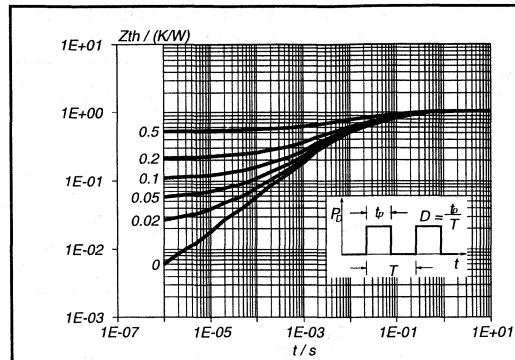


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

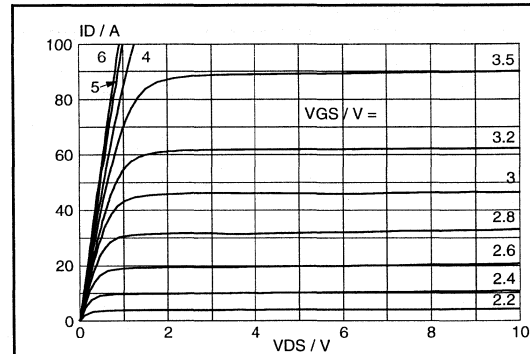


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

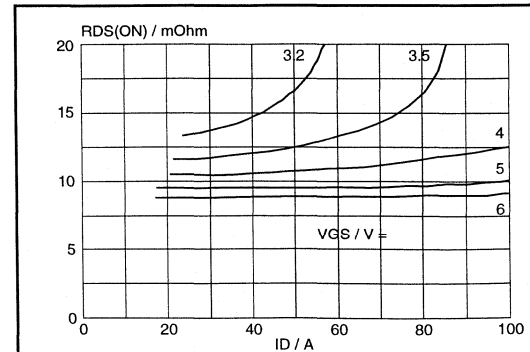


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

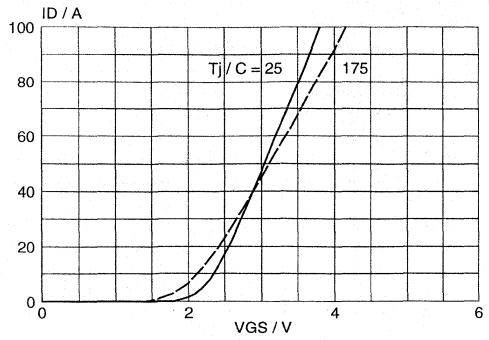


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

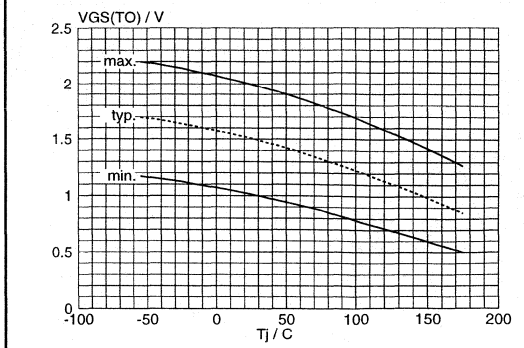


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

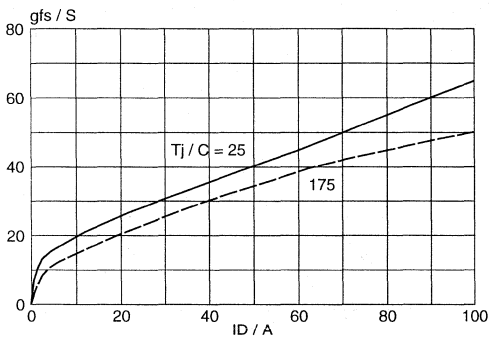


Fig.8. Typical transconductance, T_j = 25 ˚C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

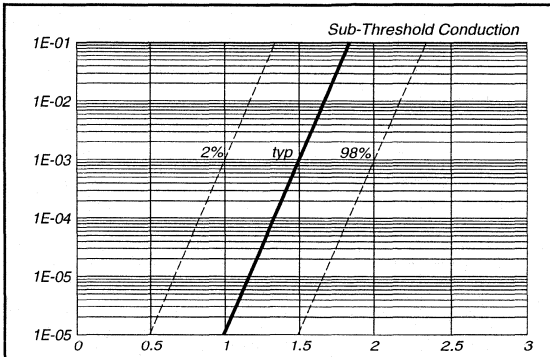


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

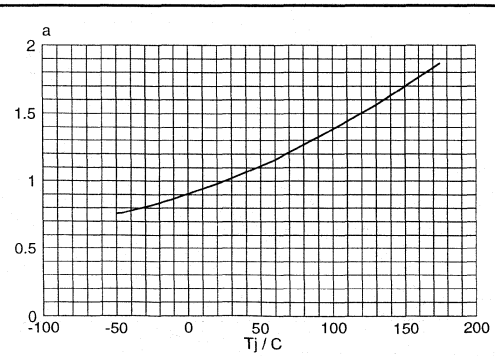


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,^{\circ}C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

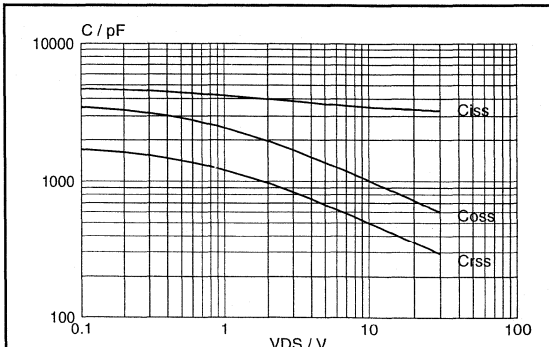


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

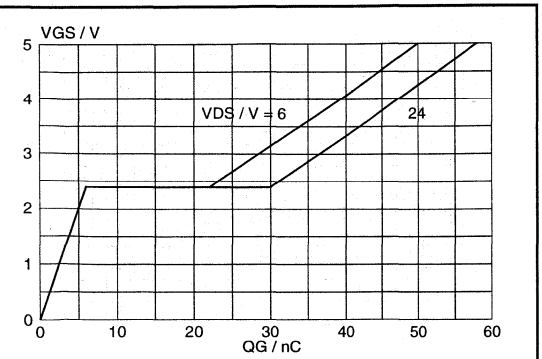


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: I_D = 75 A; parameter V_{DS}

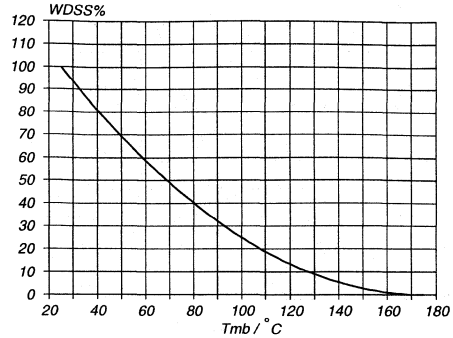


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: I_D = 45 A

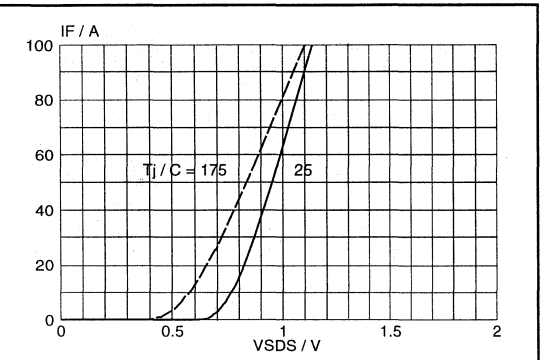


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

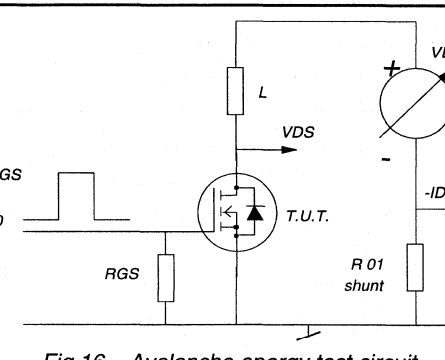


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

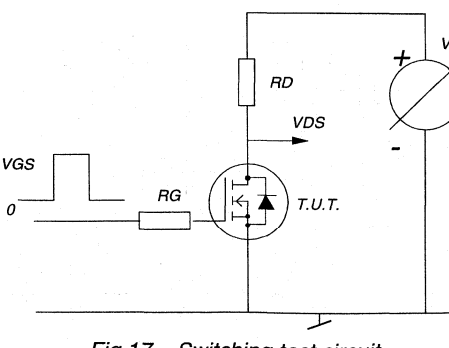


Fig.17. Switching test circuit.

TrenchMOS™ transistor Logic level FET

BUK9514-30

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using **'trench'** technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

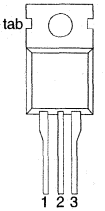
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	30	V
I_D	Drain current (DC)	69	A
P_{tot}	Total power dissipation	125	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	14	mΩ

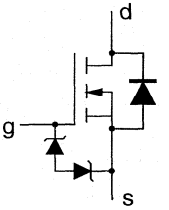
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	30	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	30	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	69	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	48	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	240	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model (100 pF, 1.5 kΩ)	-	2	kV

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	30	-	-	V
		T_j = -55˚C	27	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 30 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	uA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	10	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	12	14	mΩ
		T_j = 175˚C	-	-	26	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	12	25	-	S
$Q_{g(tot)}$	Total gate charge	I_D = 69 A; V_{DD} = 24 V; V_{GS} = 5 V	-	38	-	nC
Q_{gs}	Gate-source charge		-	5	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	15	-	nC
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	2000	-	pF
C_{oss}	Output capacitance		-	480	-	pF
C_{rss}	Feedback capacitance		-	220	-	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 15 V; I_D = 25 A;	-	30	45	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 5 Ω	-	80	130	ns
$t_{d\ off}$	Turn-off delay time		-	100	140	ns
t_f	Turn-off fall time		-	50	75	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	69	A
I_{DRM}	Pulsed reverse drain current		-	-	240	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 69 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 69 A; -dI_F/dt = 100 A/µs;	-	65	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 25 V	-	0.1	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 35 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 ˚C	-	-	125	mJ

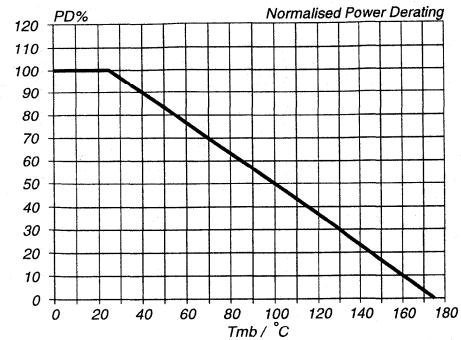


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

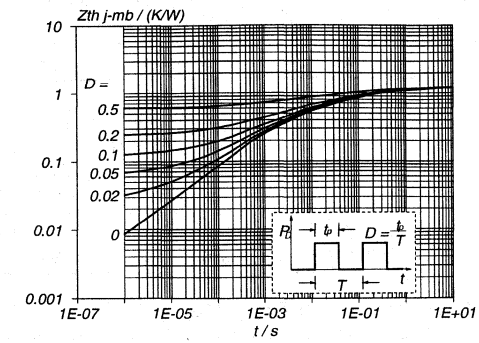


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

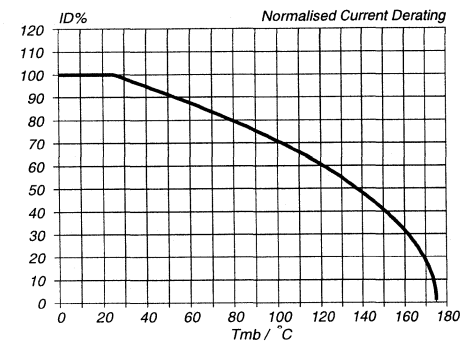


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 5 V

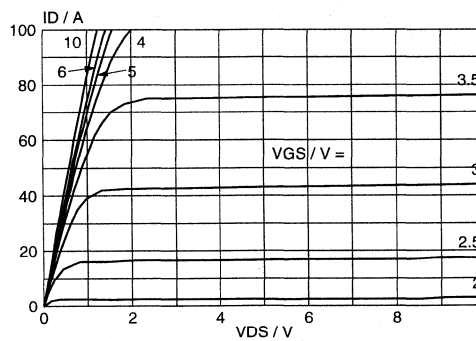


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

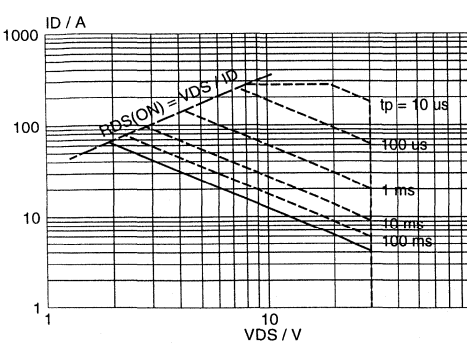


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

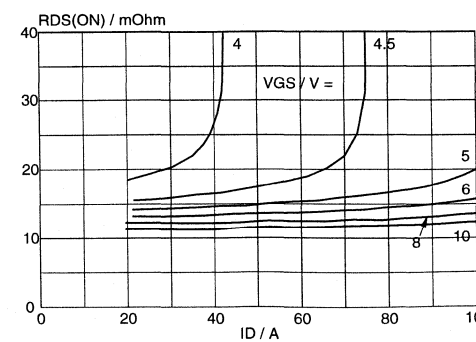


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

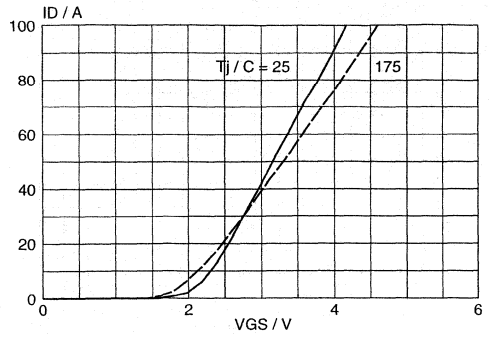


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

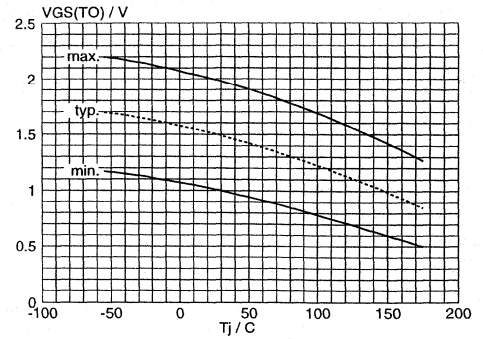


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

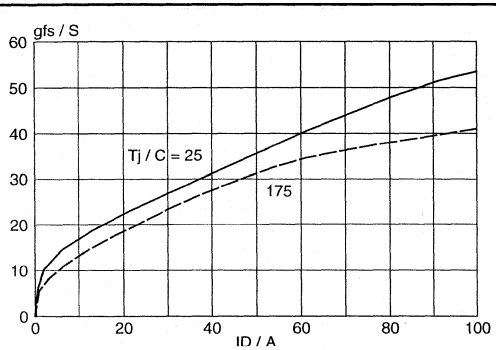


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

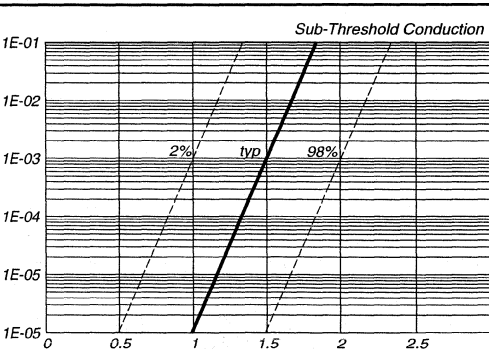


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

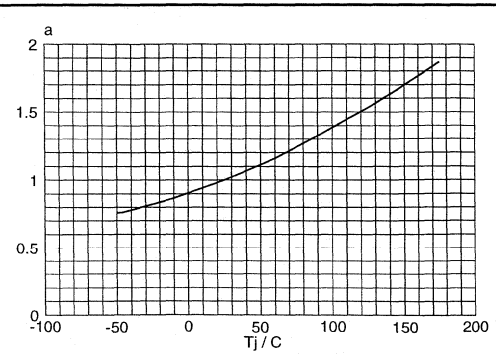


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

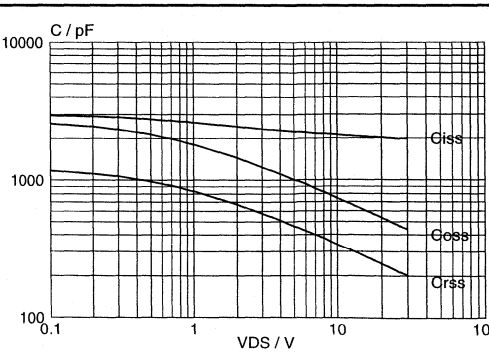


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

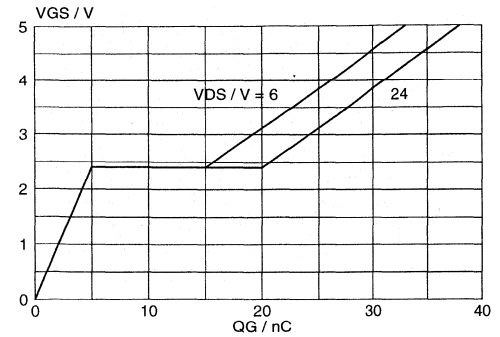


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 69$ A; parameter V_{DS}

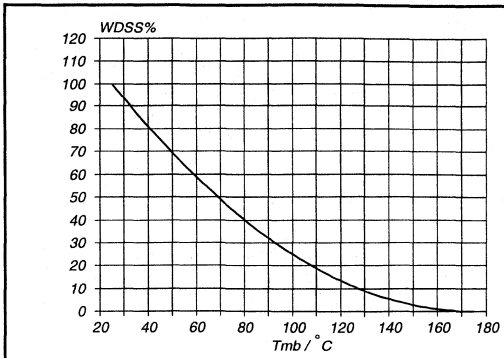


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 35$ A

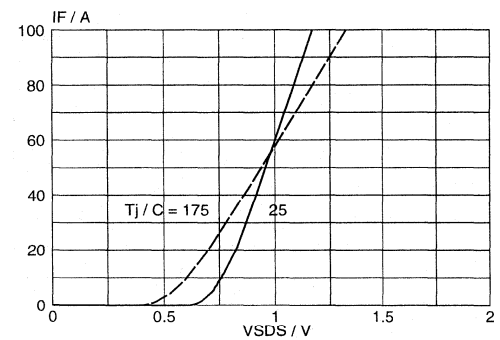


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

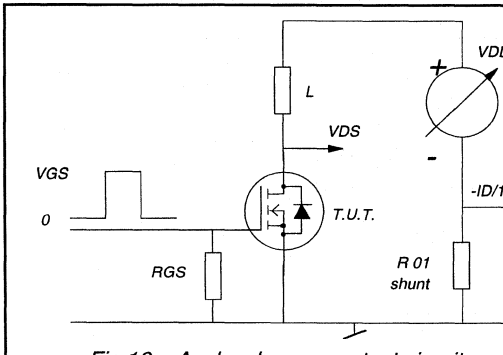


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

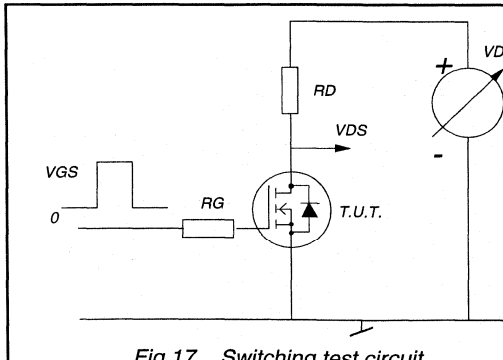


Fig.17. Switching test circuit.

TrenchMOS™ transistor Logic level FET

BUK9514-55

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using **'trench'** technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

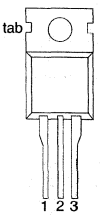
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	68	A
P_{tot}	Total power dissipation	142	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	14	mΩ

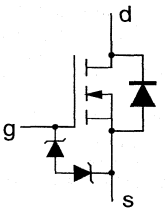
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	68	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	48	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	240	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	142	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.05	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	uA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	10	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	12	14	mΩ
		T_j = 175˚C	-	-	30	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	30	65	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	2900	3800	pF
C_{oss}	Output capacitance		-	500	600	pF
C_{rss}	Feedback capacitance		-	240	330	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	35	50	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω	-	95	145	ns
$t_{d\,off}$	Turn-off delay time		-	130	180	ns
t_f	Turn-off fall time		-	60	80	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	68	A
I_{DRM}	Pulsed reverse drain current		-	-	240	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 65 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 65 A; -dI_F/dt = 100 A/µs;	-	57	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.14	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 65 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	200	mJ

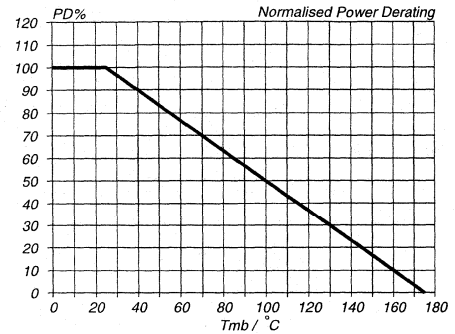


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

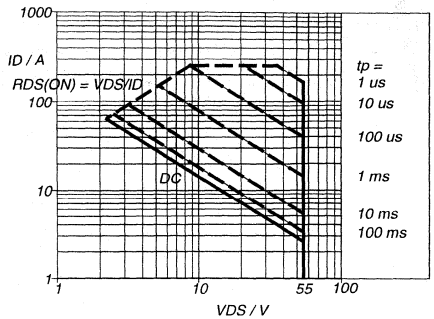


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

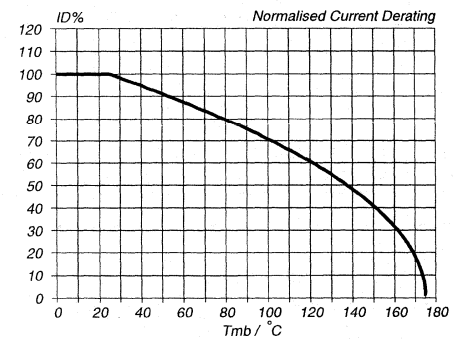


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

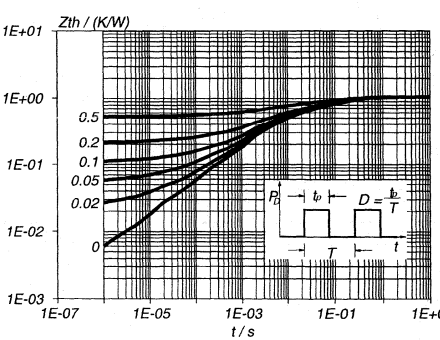


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

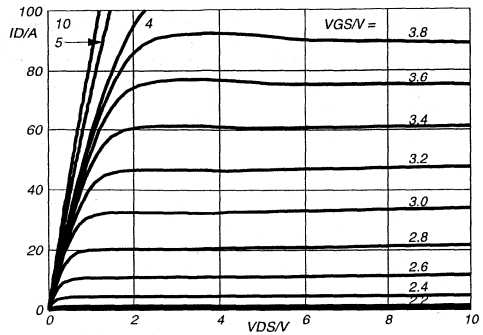


Fig.5. Typical output characteristics, T_j = 25 °C. $I_D = f(V_{DS})$; parameter V_{GS}

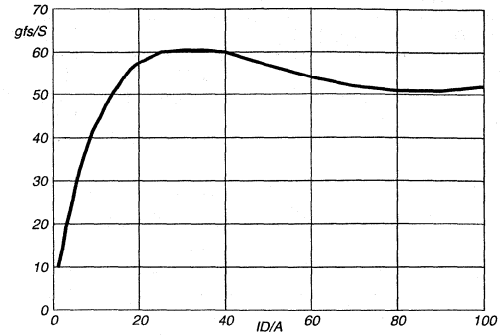


Fig.8. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

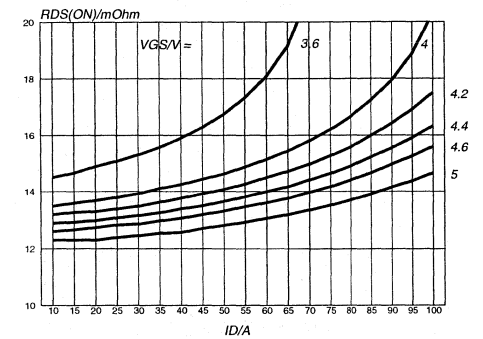


Fig.6. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

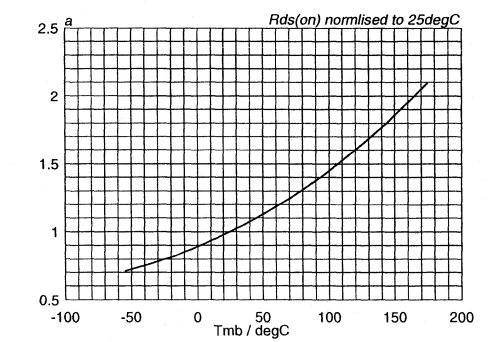


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

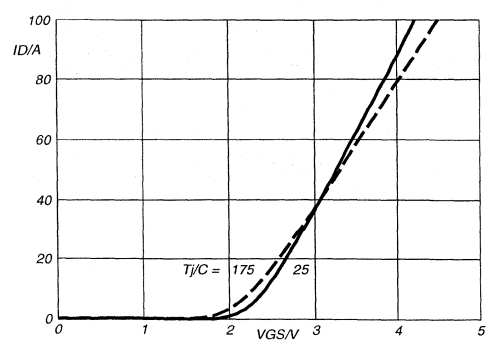


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

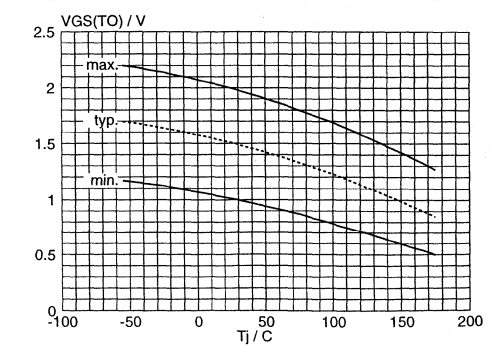


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

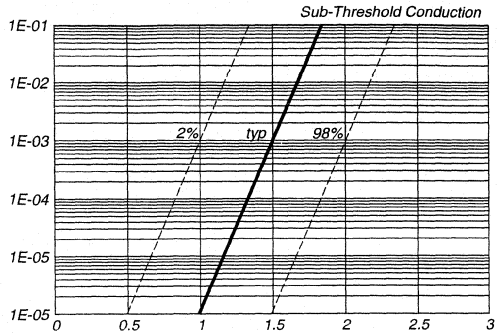


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

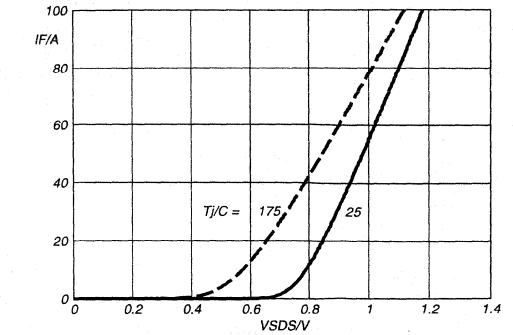


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

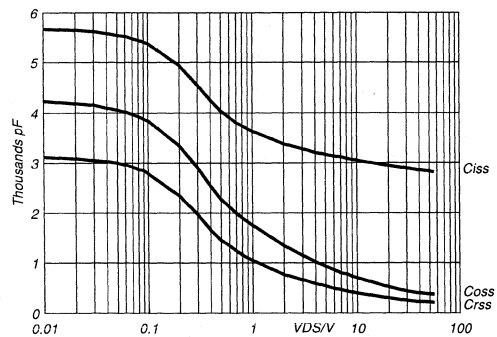


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

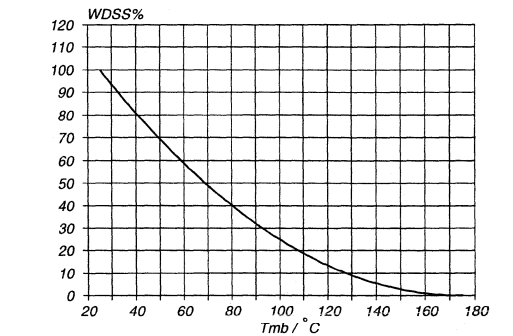


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 75$ A

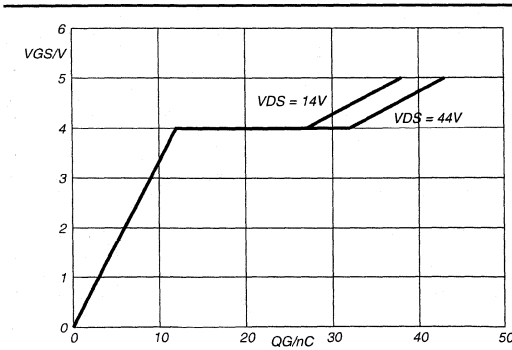


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 50$ A; parameter V_{DS}

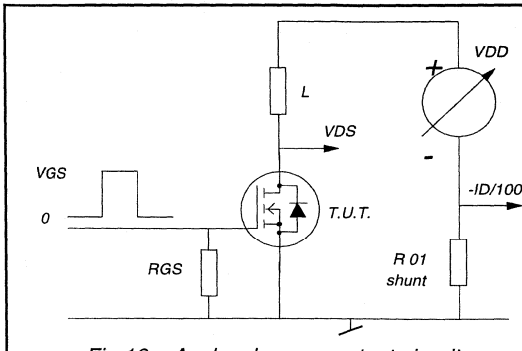


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

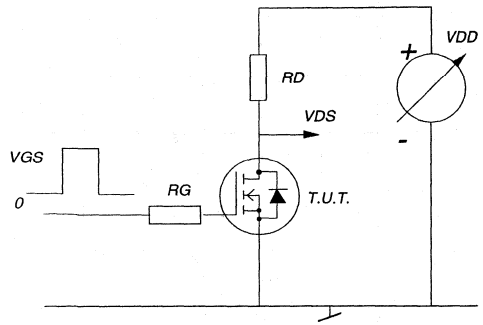


Fig.17. Switching test circuit.

TrenchMOS™ transistor Logic level FET

BUK9518-30

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using '**trench**' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

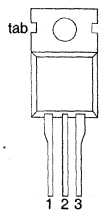
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	30	V
I_D	Drain current (DC)	55	A
P_{tot}	Total power dissipation	103	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	18	mΩ

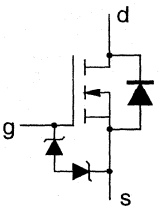
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	30	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	30	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	55	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	38	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	220	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	103	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.45	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	30	-	-	V
		T_j = -55˚C	27	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	1.5	2	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	
I_{DSS}	Zero gate voltage drain current	V_{DS} = 30 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-		10	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	15	18	mΩ
		T_j = 175˚C	-	-	34	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	10	20	-	S
$Q_{g(tot)}$	Total gate charge	I_D = 55 A; V_{DD} = 24 V; V_{GS} = 5 V	-	31	-	nC
Q_{gs}	Gate-source charge		-	4	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	13	-	nC
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1450	-	pF
C_{oss}	Output capacitance		-	390	-	pF
C_{rss}	Feedback capacitance		-	200	-	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 15 V; I_D = 25 A;	-	30	45	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 5 Ω	-	80	130	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	95	135	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	55	A
I_{DRM}	Pulsed reverse drain current		-	-	220	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 55 A; V_{GS} = 0 V	-	1.0	-	
t_{rr}	Reverse recovery time	I_F = 55 A; -dI_F/dt = 100 A/µs;	-	70	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 25 V	-	0.1	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 28 A; $V_{DD} \leq$ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	80	mJ

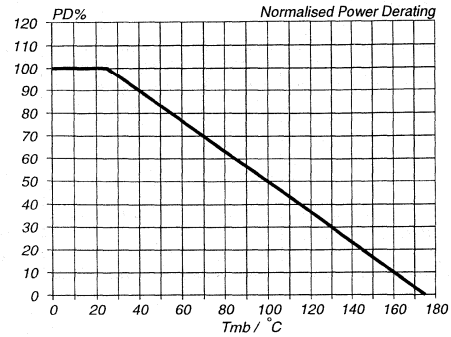


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D / P_{D\,25\,°C} = f(T_{mb})$

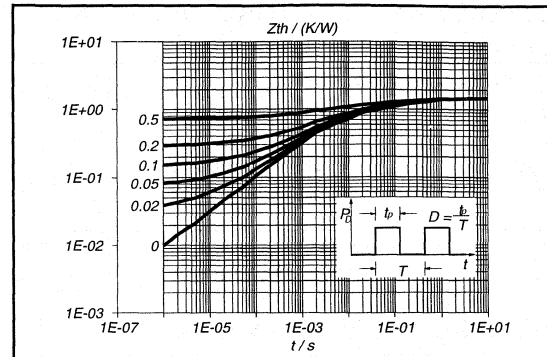


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb} = f(t)$; parameter $D = t_p/T$

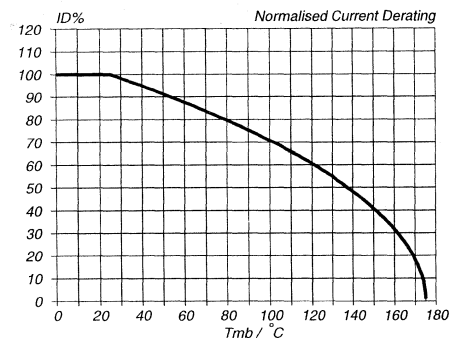


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D / I_{D\,25\,°C} = f(T_{mb})$; conditions: $V_{GS} \geq 5$ V

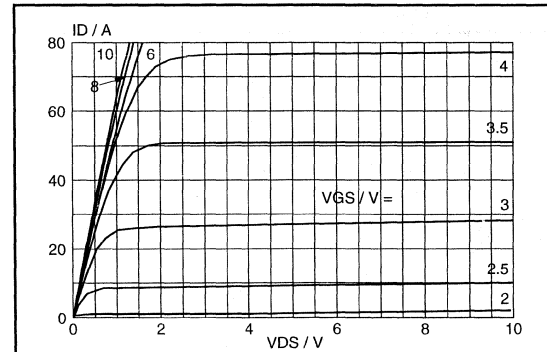


Fig.5. Typical output characteristics, $T_j = 25$ °C.
$I_D = f(V_{DS})$; parameter V_{GS}

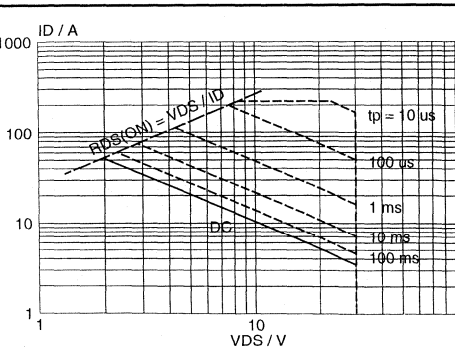


Fig.3. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

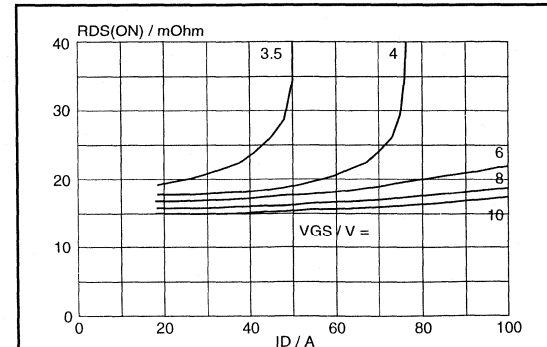


Fig.6. Typical on-state resistance, $T_j = 25$ °C.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

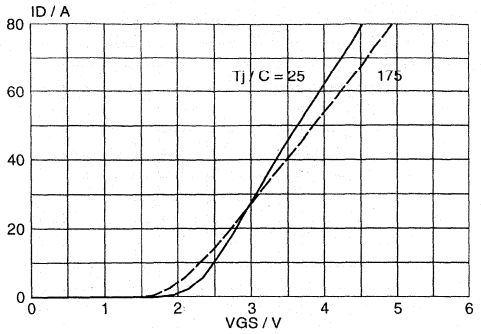


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

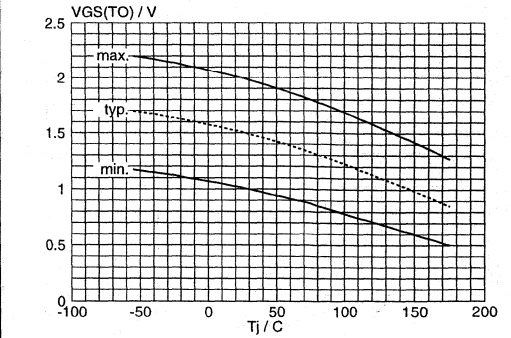


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

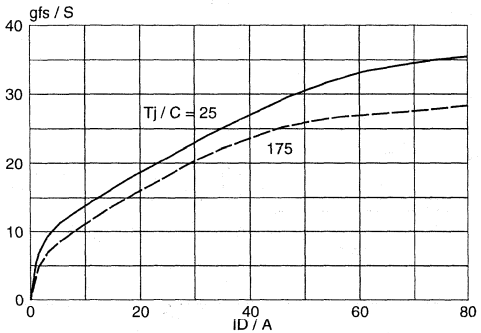


Fig.8. Typical transconductance, T_j = 25 ˚C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

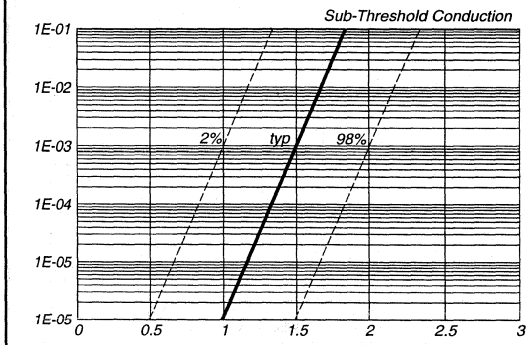


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

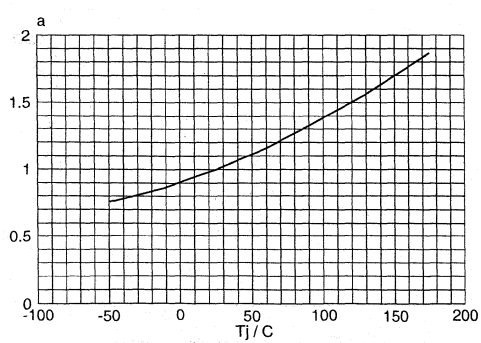


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ ˚C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

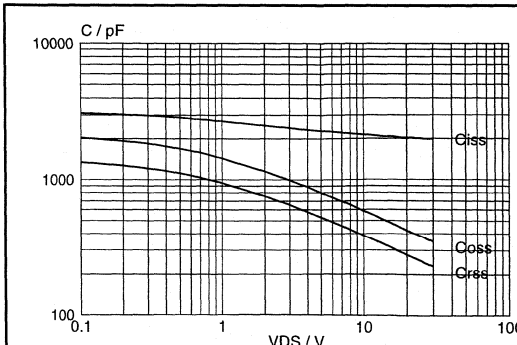


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

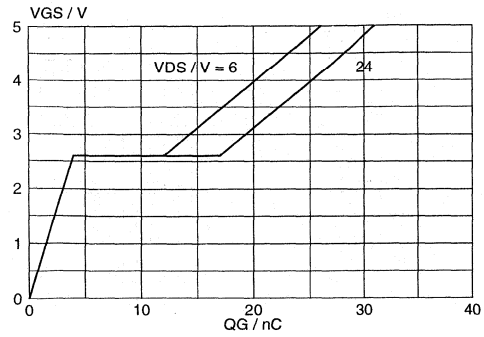


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: I_D = 55 A; parameter V_{DS}

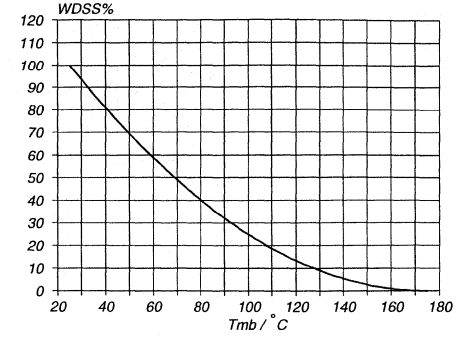


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: I_D = 28 A

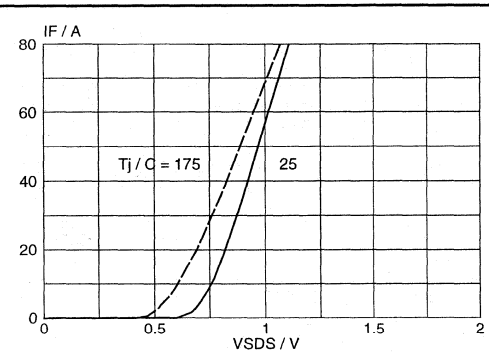


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

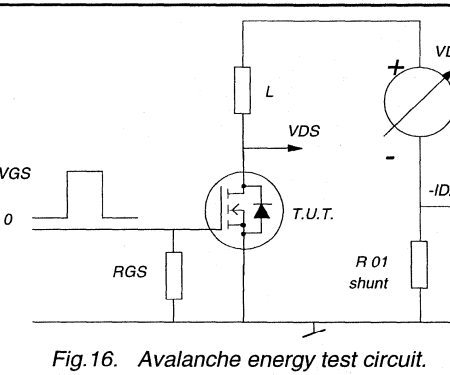


Fig.16. Avalanche energy test circuit.
$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

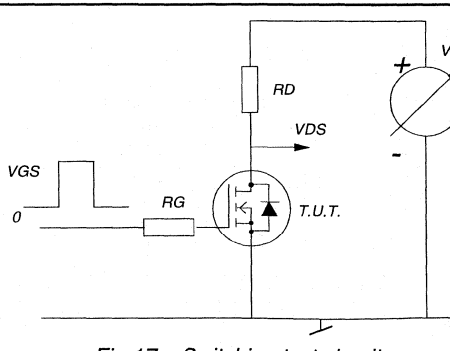


Fig.17. Switching test circuit.

TrenchMOS™ transistor
Logic level FET

BUK9518-55

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using **'trench'** technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

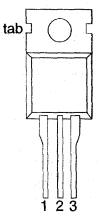
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	57	A
P_{tot}	Total power dissipation	125	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	18	mΩ

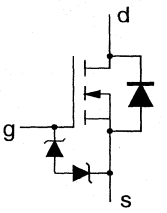
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	57	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	40	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	228	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	uA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	10	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	15	18	mΩ
		T_j = 175˚C	-	-	38	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	25	52	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	2000	2600	pF
C_{oss}	Output capacitance		-	390	490	pF
C_{rss}	Feedback capacitance		-	200	290	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	30	45	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω	-	80	130	ns
$t_{d\,off}$	Turn-off delay time		-	100	140	ns
t_f	Turn-off fall time		-	50	75	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	57	A
I_{DRM}	Pulsed reverse drain current		-	-	200	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 50 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 50 A; -dI_F/dt = 100 A/µs;	-	48	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.1	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 50 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	125	mJ

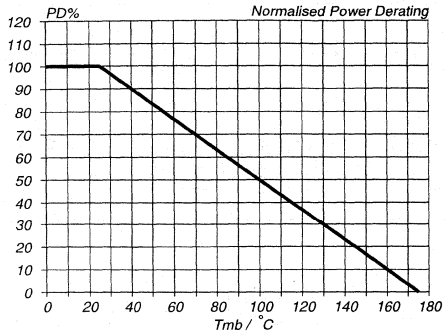


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

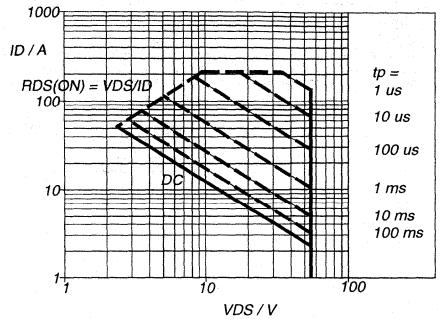


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

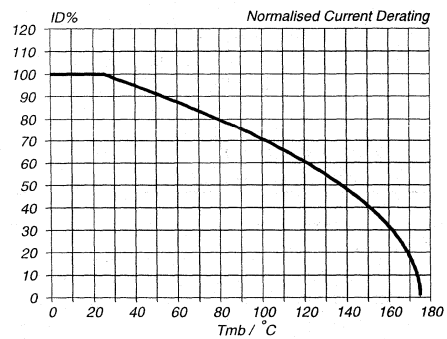


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

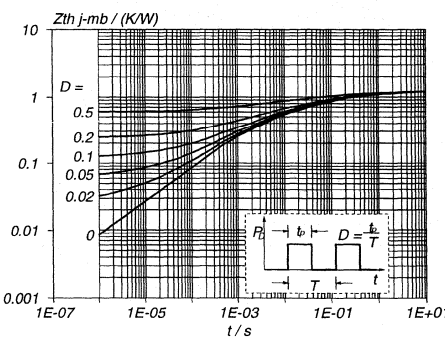


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

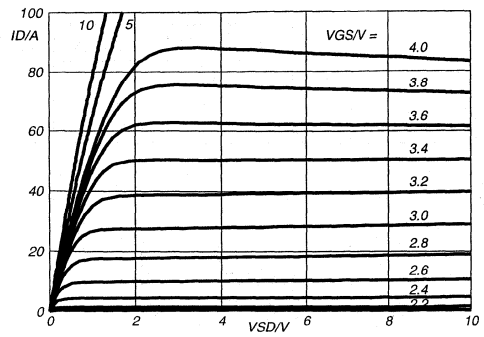


Fig.5. Typical output characteristics, T_j = 25 °C. $I_D = f(V_{DS})$; parameter V_{GS}

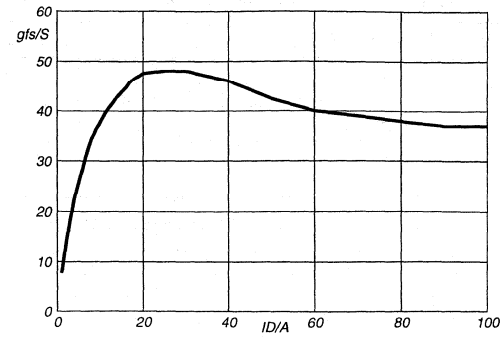


Fig.8. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

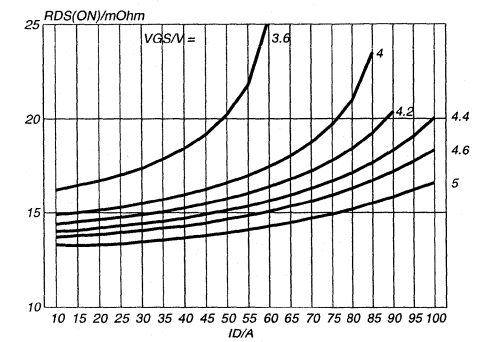


Fig.6. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

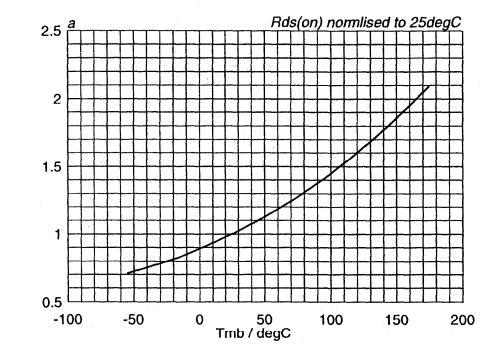


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

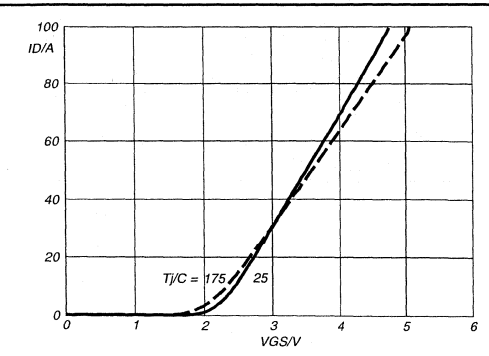


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

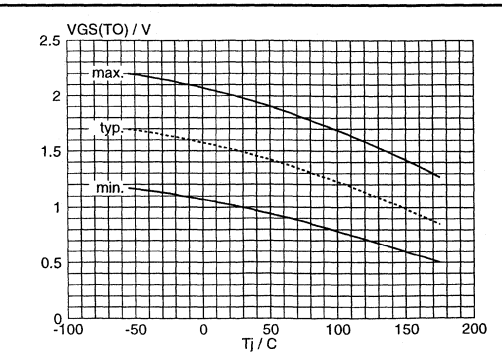


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

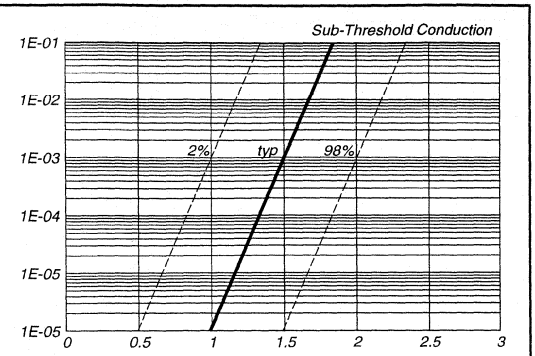


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; *conditions:* $T_j = 25$ °C; $V_{DS} = V_{GS}$

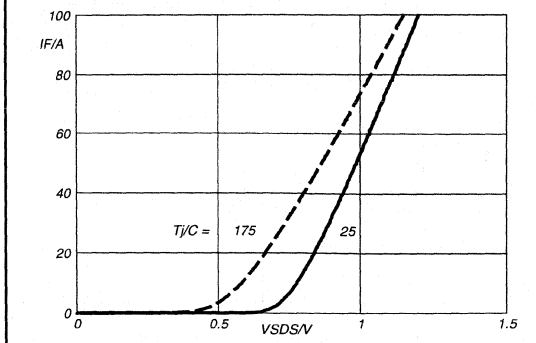


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; *conditions:* $V_{GS} = 0$ V; *parameter* T_j

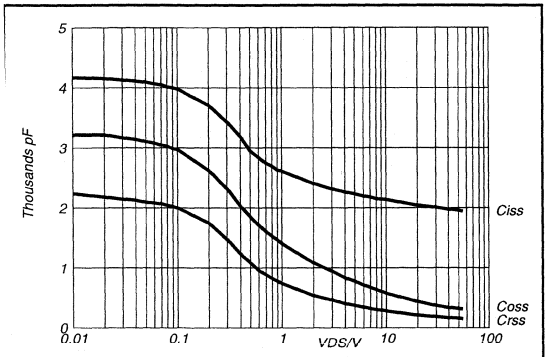


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; *conditions:* $V_{GS} = 0$ V; $f = 1$ MHz

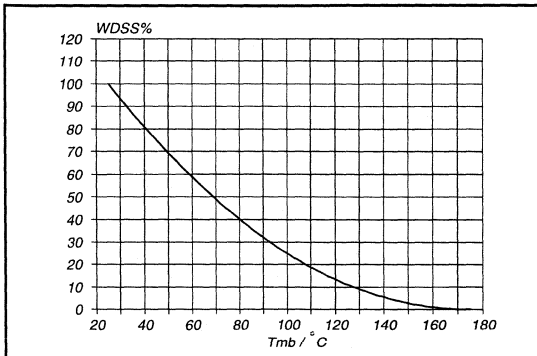


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; *conditions:* $I_D = 75$ A

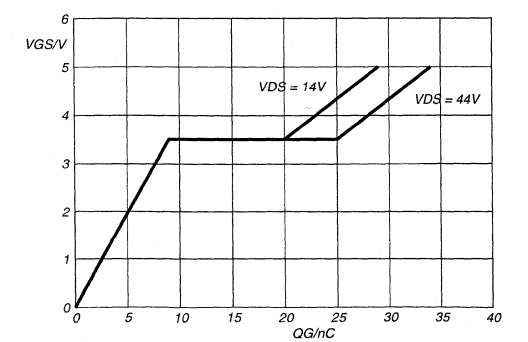


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; *conditions:* $I_D = 50$ A; *parameter* V_{DS}

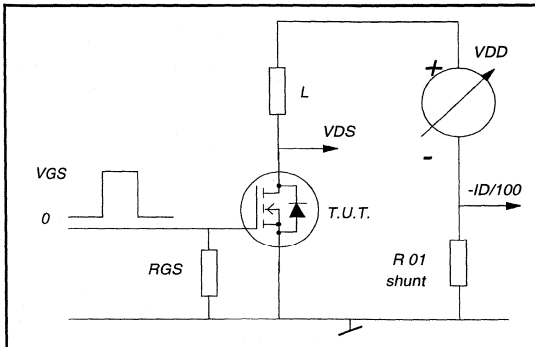


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

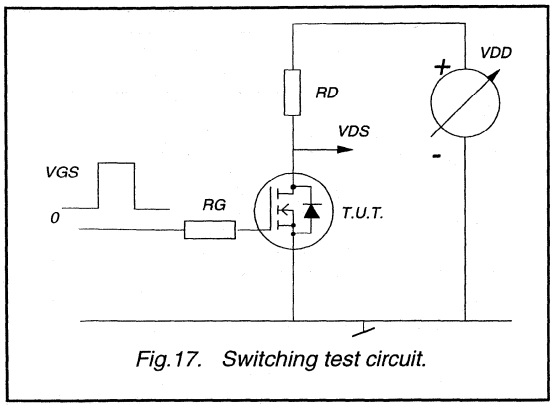


Fig.17. Switching test circuit.

TrenchMOS™ transistor Logic level FET

BUK9520-55

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using **'trench'** technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

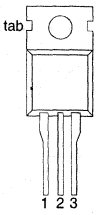
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	52	A
P_{tot}	Total power dissipation	116	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	20	mΩ

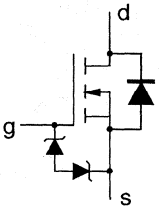
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	52	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	37	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	208	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	116	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.29	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	1.5	2	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-		10	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	15	20	mΩ
		T_j = 175˚C	-	-	42	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	20	-	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1800	2400	pF
C_{oss}	Output capacitance		-	350	420	pF
C_{rss}	Feedback capacitance		-	170	235	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	28	40	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω	-	110	160	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	95	135	ns
t_f	Turn-off fall time		-	70	90	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	52	A
I_{DRM}	Pulsed reverse drain current		-	-	208	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 40 A; V_{GS} = 0 V	-	1.0	-	
t_{rr}	Reverse recovery time	I_F = 40 A; -dI_F/dt = 100 A/µs;	-	47	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.15	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 45 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	110	mJ

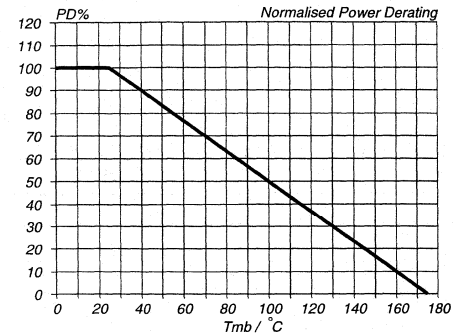


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

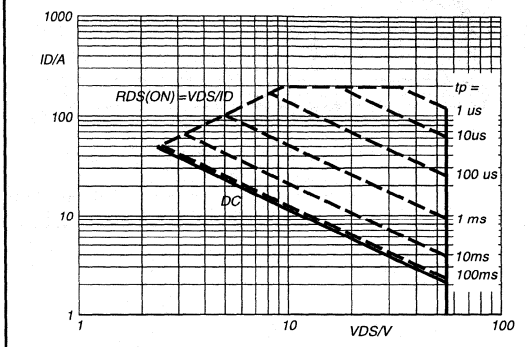


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

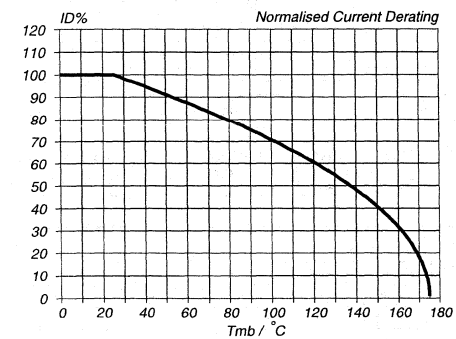


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

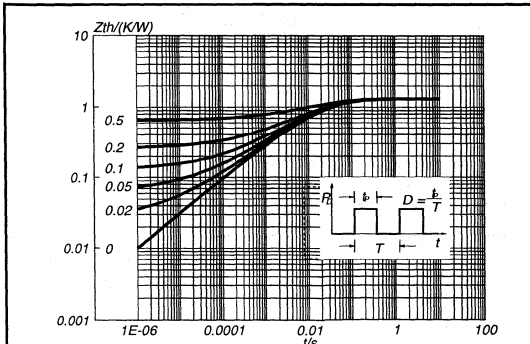


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

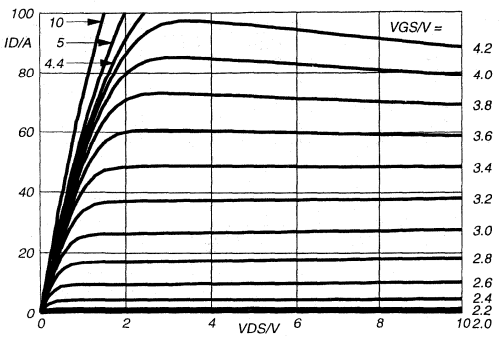


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

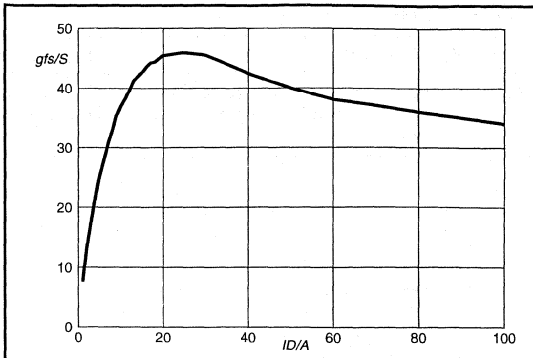


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

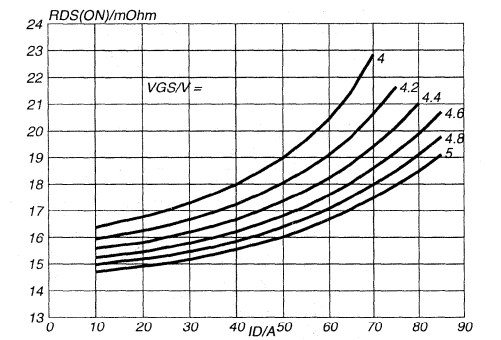


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

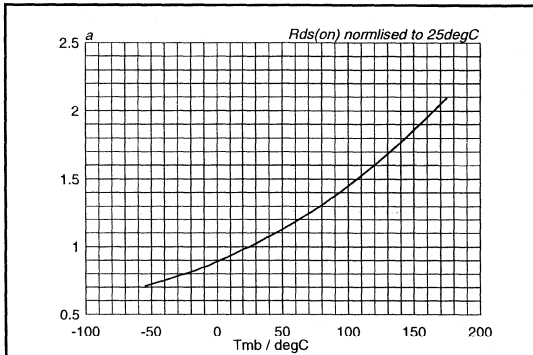


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,˚C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

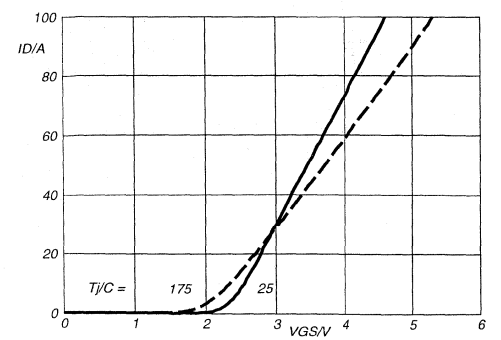


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

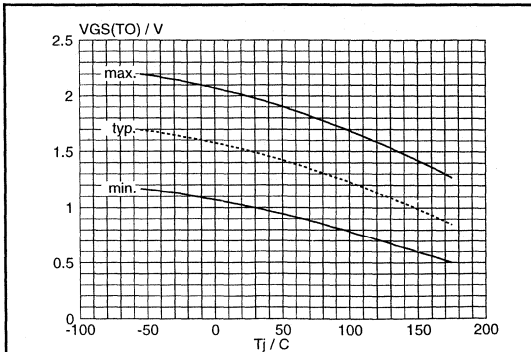


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

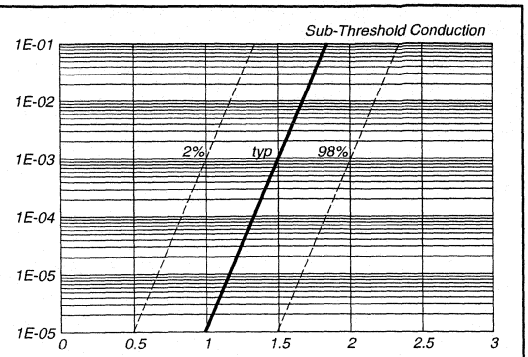


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

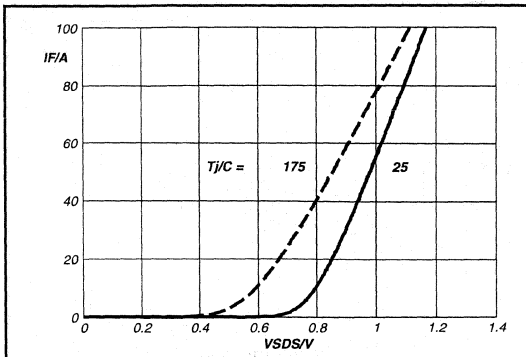


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

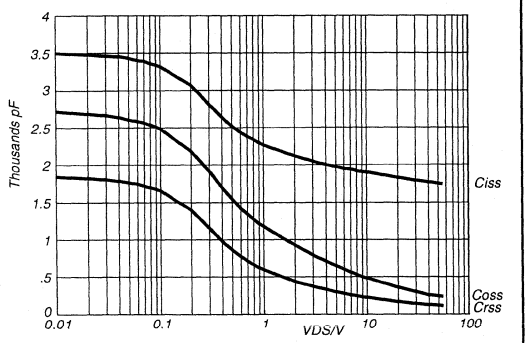


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

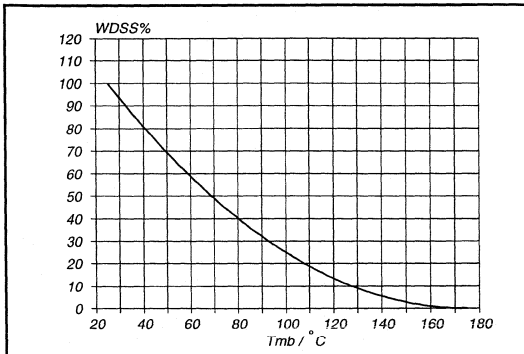


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 49$ A

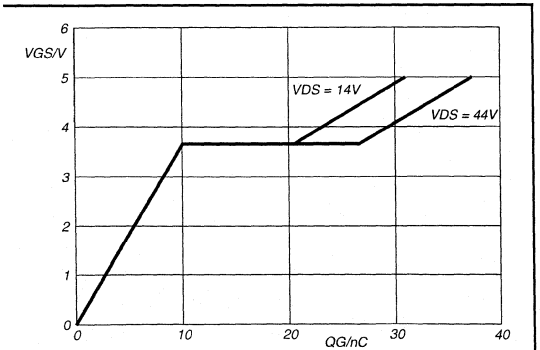


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 50$ A; parameter V_{DS}

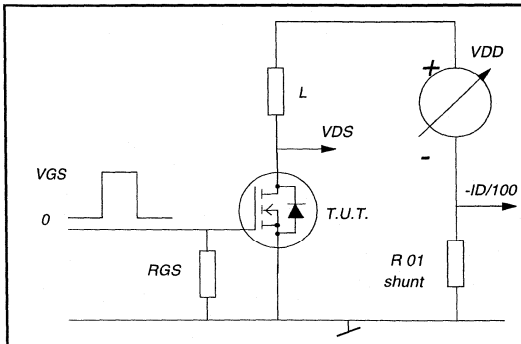


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

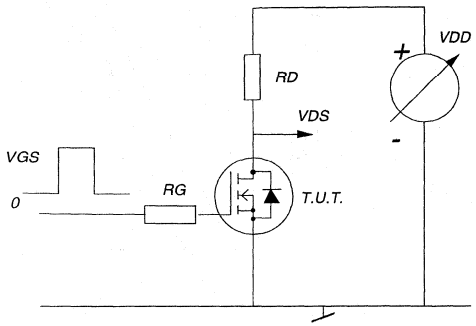


Fig.17. Switching test circuit.

TrenchMOS™ transistor Logic level FET

BUK9524-55

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using **'trench'** technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

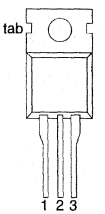
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	45	A
P_{tot}	Total power dissipation	103	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	24	mΩ

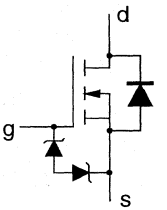
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	45	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	31	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	180	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	103	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.45	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	1.5	2	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-		10	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	19	24	mΩ
		T_j = 175˚C	-	-	50	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	15	40	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1500	2000	pF
C_{oss}	Output capacitance		-	300	360	pF
C_{rss}	Feedback capacitance		-	150	200	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	30	45	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω	-	80	130	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	95	135	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	45	A
I_{DRM}	Pulsed reverse drain current		-	-	160	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 40 A; V_{GS} = 0 V	-	1.0	-	
t_{rr}	Reverse recovery time	I_F = 40 A; -dI_F/dt = 100 A/µs;	-	40	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.07	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 40 A; $V_{DD} \leq$ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	80	mJ

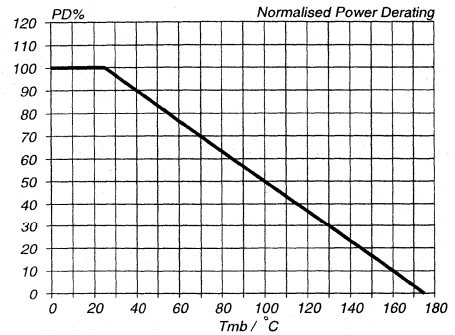


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

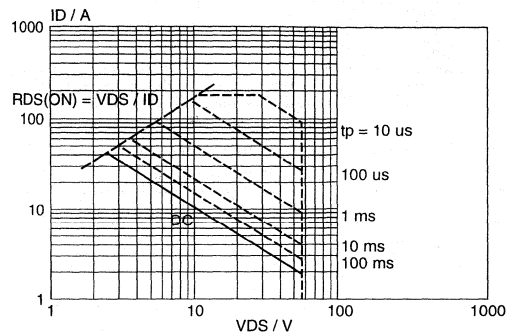


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

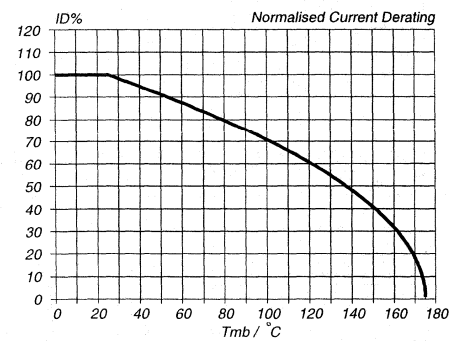


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

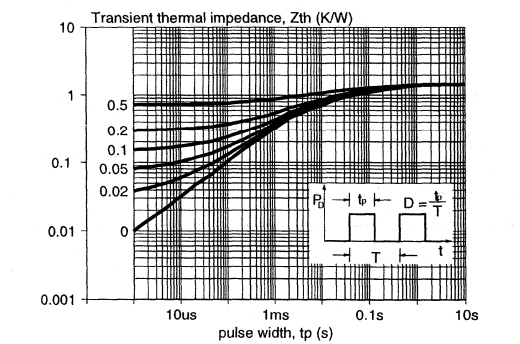


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

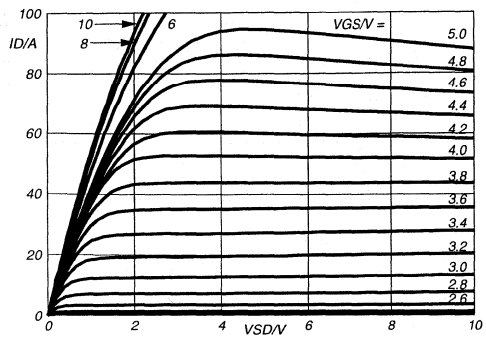


Fig.5. Typical output characteristics, T_j = 25 °C. $I_D = f(V_{DS})$; parameter V_{GS}

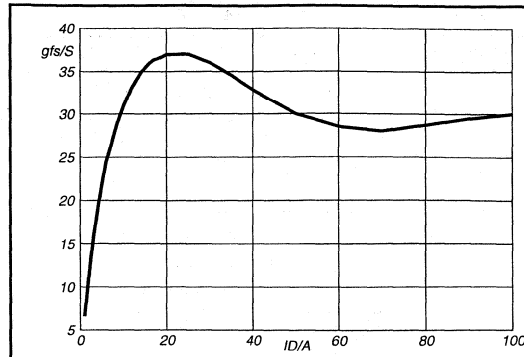


Fig.8. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

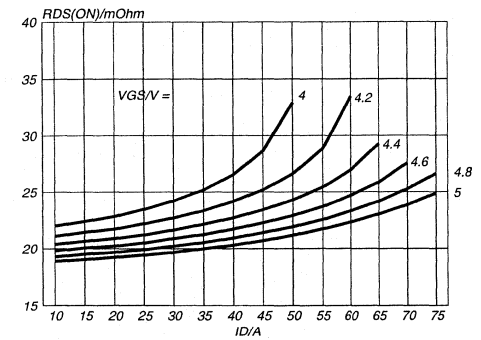


Fig.6. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

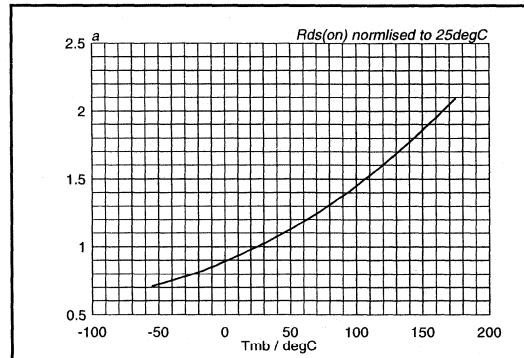


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

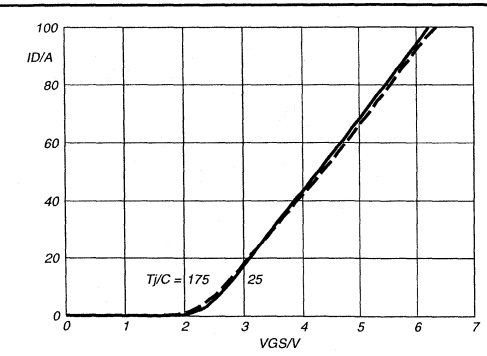


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

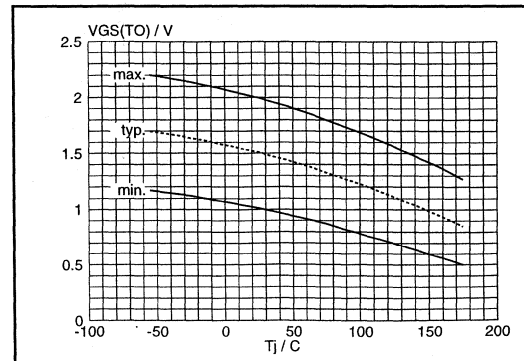


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

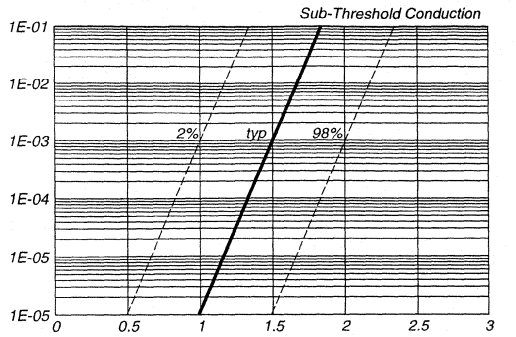


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

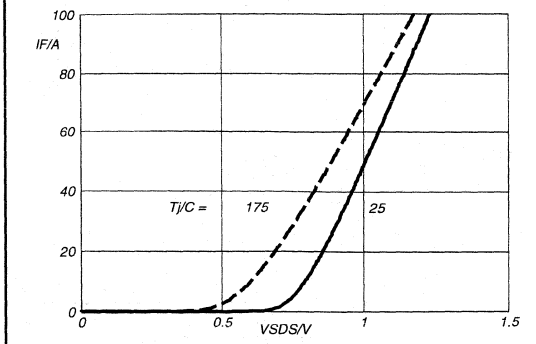


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

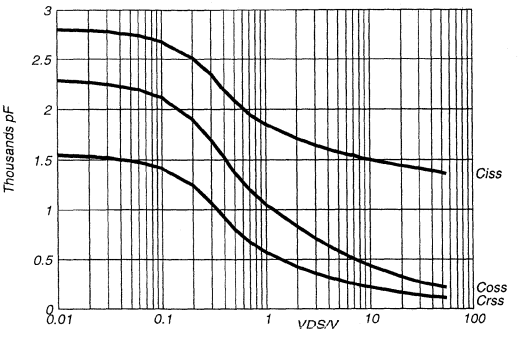


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

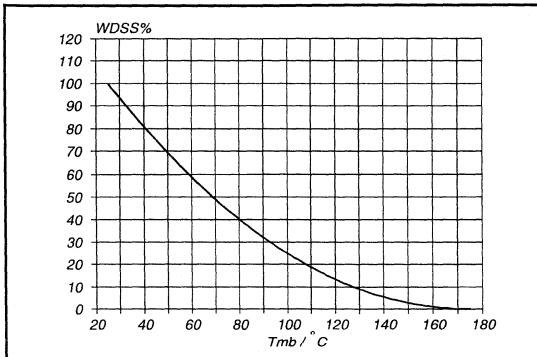


Fig.15. Normalised avalanche energy rating.
W_{DSS}% = $f(T_{mb})$; conditions: I_D = 75 A

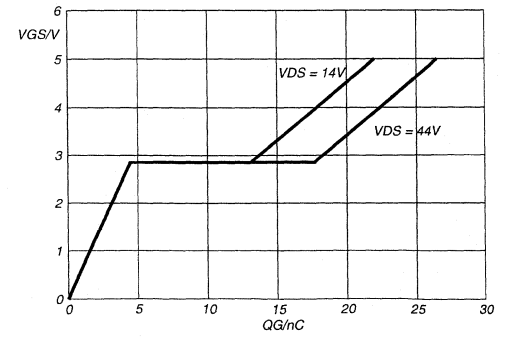


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 50 A; parameter V_{DS}

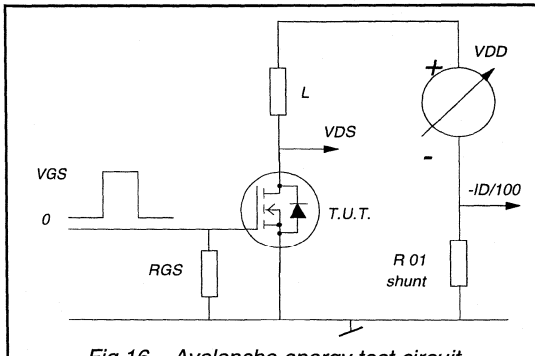


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

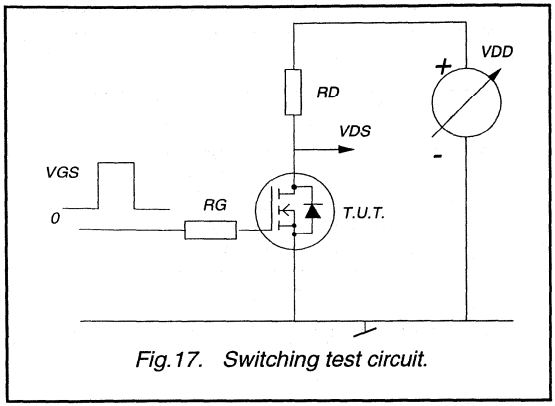


Fig.17. Switching test circuit.

TrenchMOS™ transistor Logic level FET

BUK9528-55

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using '**trench**' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

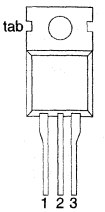
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	40	A
P_{tot}	Total power dissipation	96	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	28	mΩ

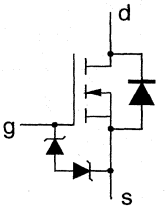
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	40	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	28	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	160	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	96	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.56	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	1.5	2	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-		10	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 20 A	-	22	28	mΩ
		T_j = 175˚C	-	-	59	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	13	-	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1300	1700	pF
C_{oss}	Output capacitance		-	250	300	pF
C_{rss}	Feedback capacitance		-	130	180	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	22	32	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω	-	85	125	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	70	95	ns
t_f	Turn-off fall time		-	64	85	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	40	A
I_{DRM}	Pulsed reverse drain current		-	-	160	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 40 A; V_{GS} = 0 V	-	1.0	-	
t_{rr}	Reverse recovery time	I_F = 40 A; -dI_F/dt = 100 A/µs;	-	41	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.16	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 35 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	70	mJ

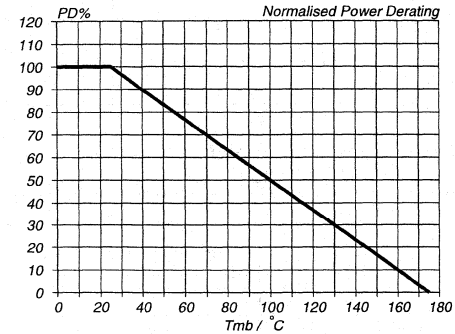


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

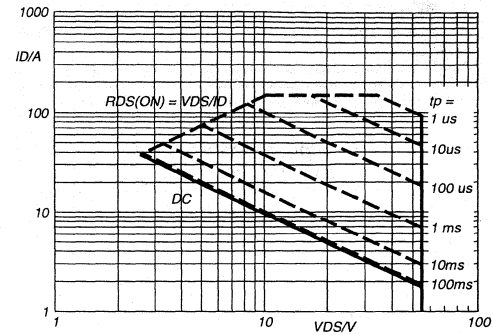


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

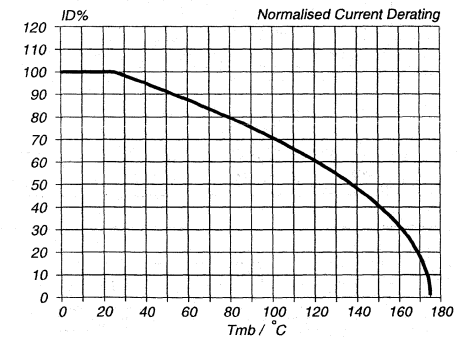


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

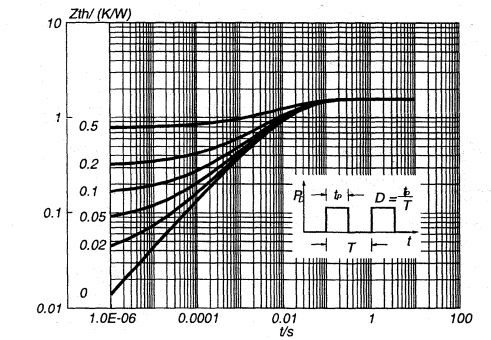


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

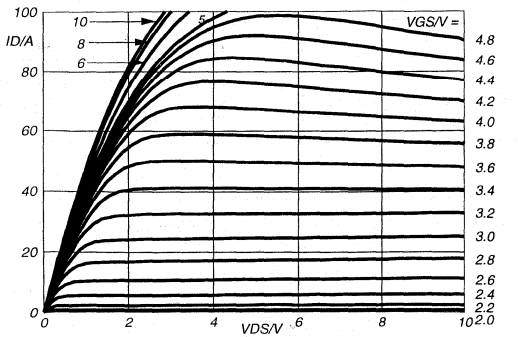


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

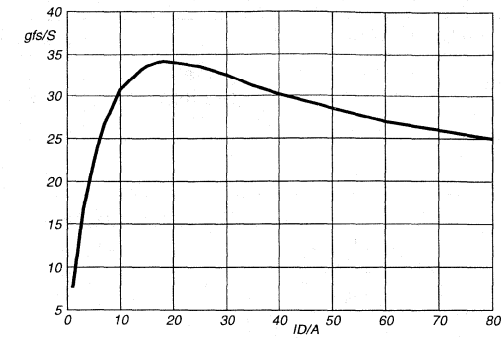


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

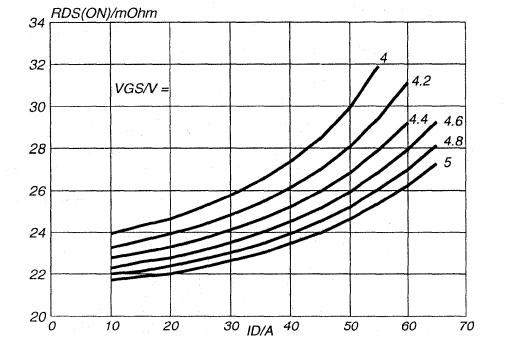


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

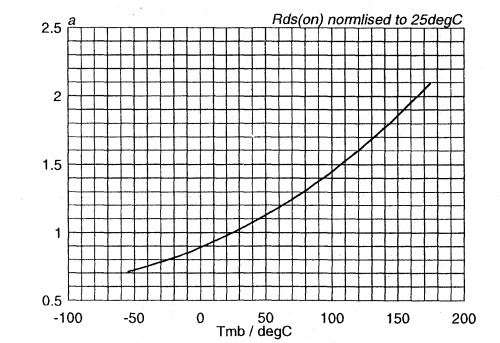


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,˚C} = f(T_j)$; I_D = 20 A; V_{GS} = 5 V

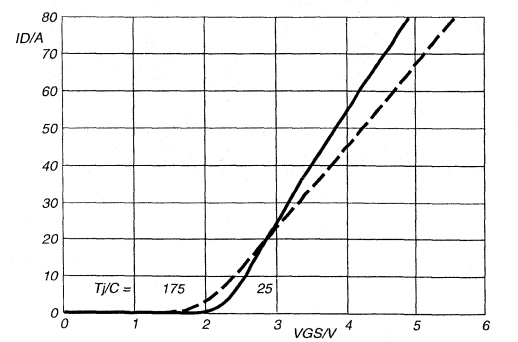


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

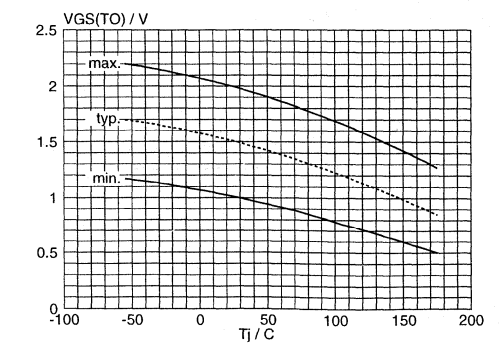


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

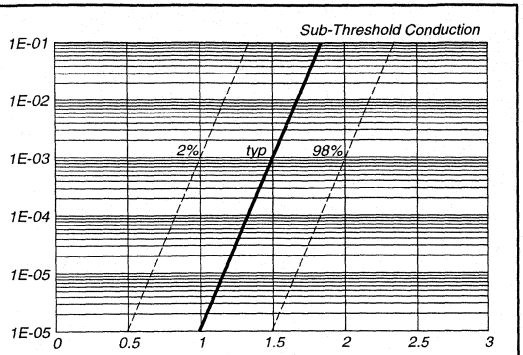


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

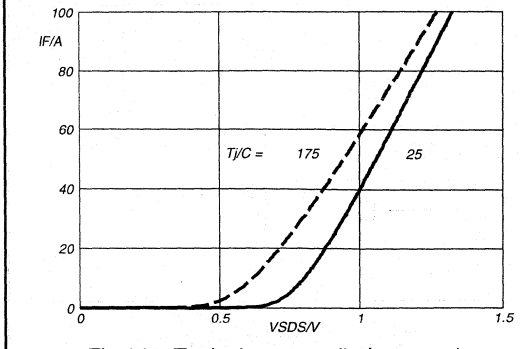


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

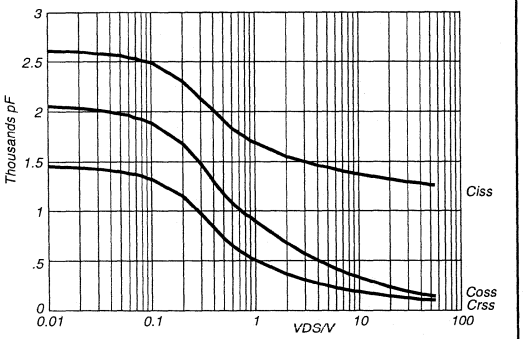


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

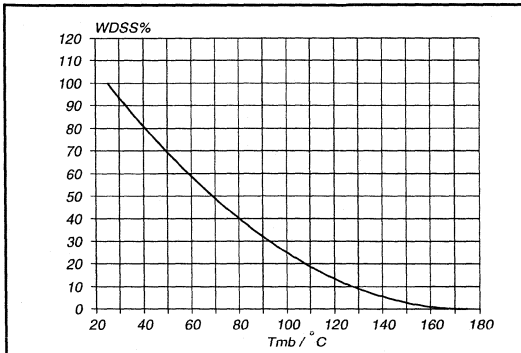


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 40$ A

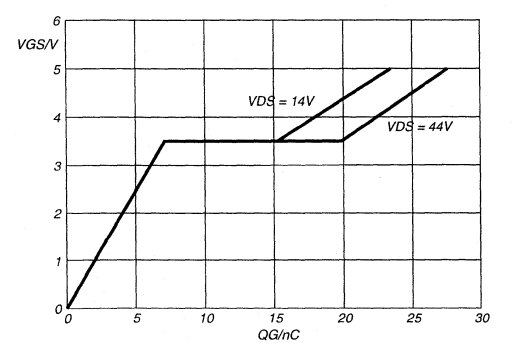


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 40$ A; parameter V_{DS}

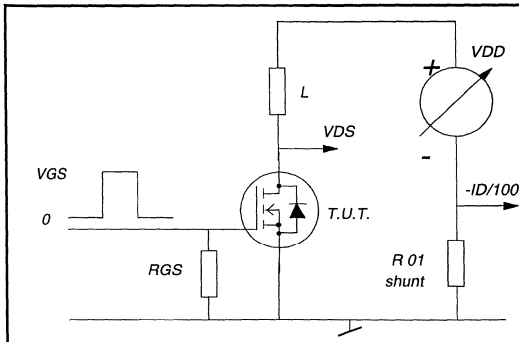


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

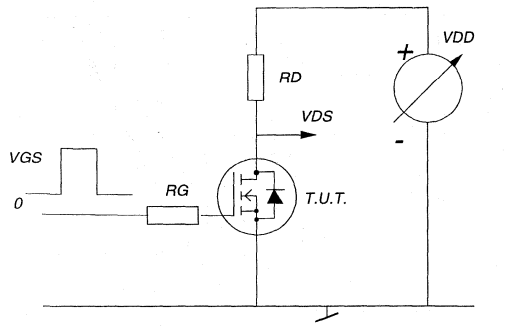


Fig.17. Switching test circuit.

TrenchMOS™ transistor Logic level FET

BUK9535-55

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using '**trench**' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

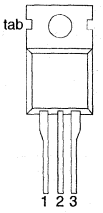
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	34	A
P_{tot}	Total power dissipation	85	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	35	mΩ

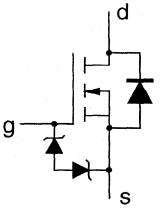
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	34	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	24	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	136	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	85	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.75	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	1.5	2	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-		10	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 17 A	-	28	35	mΩ
		T_j = 175˚C	-	-	74	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 15 A	12	-	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1050	1400	pF
C_{oss}	Output capacitance		-	205	245	pF
C_{rss}	Feedback capacitance		-	110	150	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 15 A;	-	14	21	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω	-	77	110	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	55	80	ns
t_f	Turn-off fall time		-	48	65	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	34	A
I_{DRM}	Pulsed reverse drain current		-	-	136	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 34 A; V_{GS} = 0 V	-	1.0	-	
t_{rr}	Reverse recovery time	I_F = 34 A; -dI_F/dt = 100 A/µs;	-	40	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.16	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 20 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	45	mJ

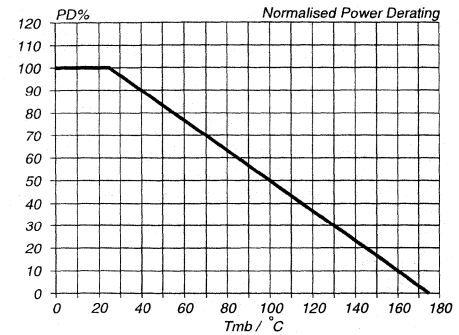


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

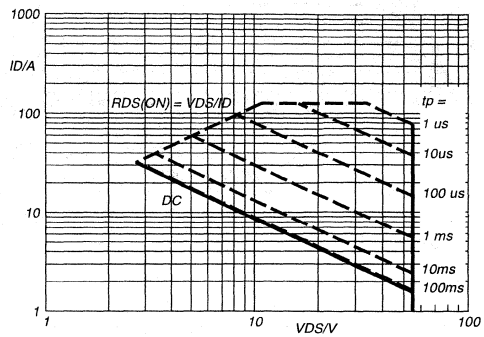


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

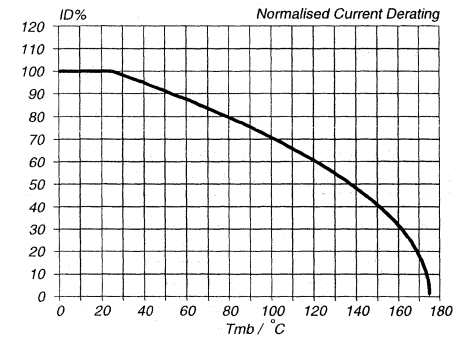


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

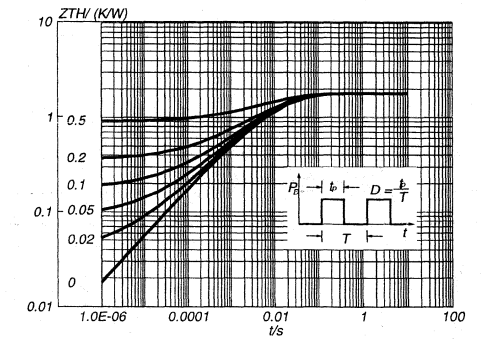


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

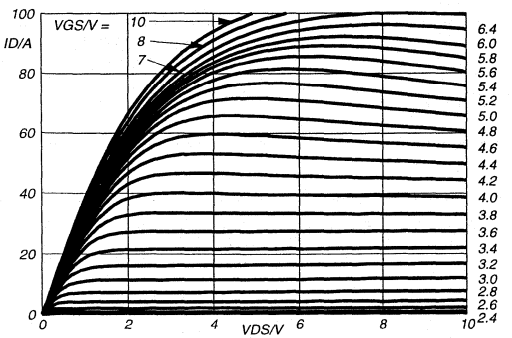


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

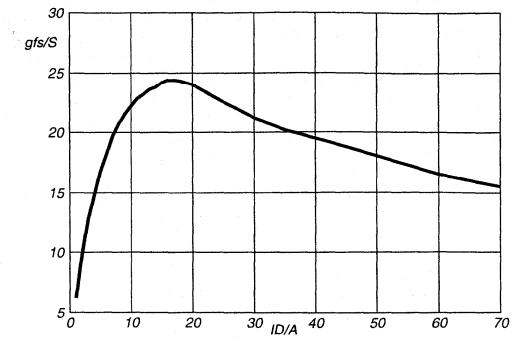


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

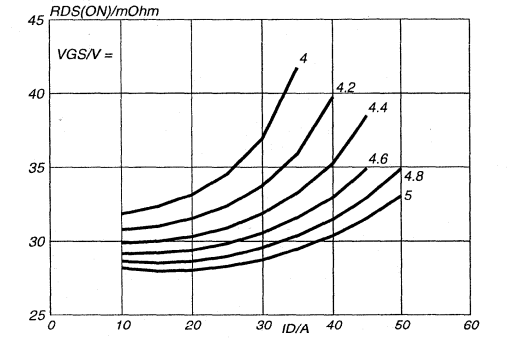


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

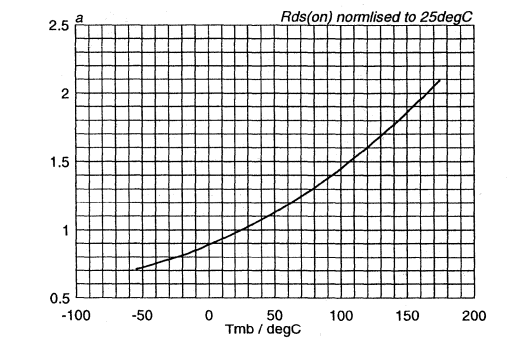


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,^{\circ}C} = f(T_j)$; I_D = 17 A; V_{GS} = 5 V

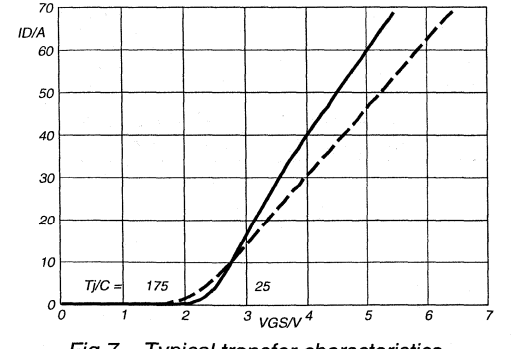


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

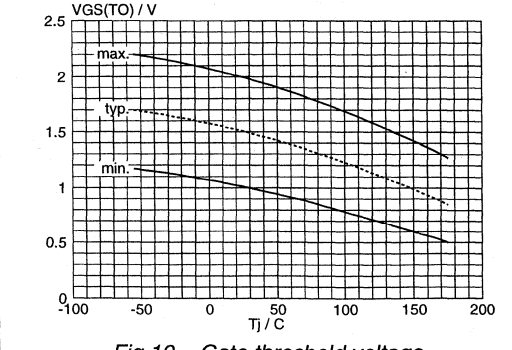


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

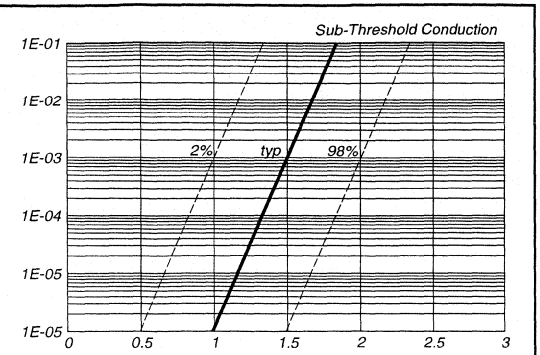


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

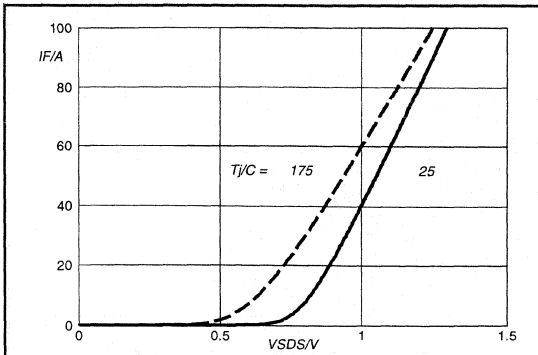


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

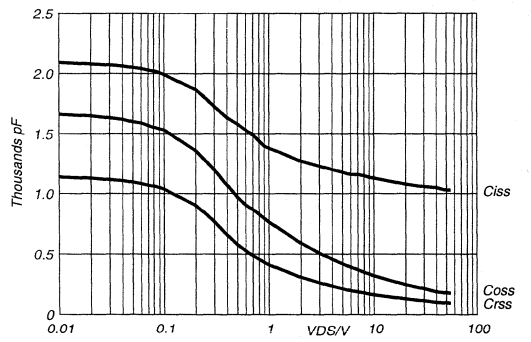


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

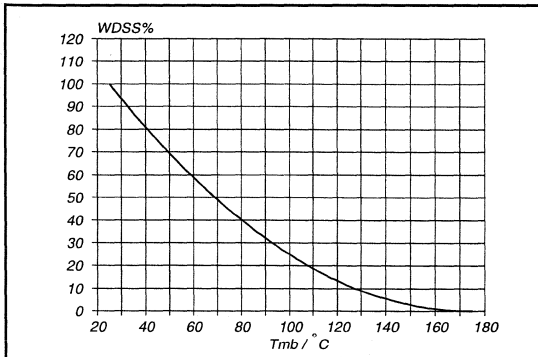


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 32$ A

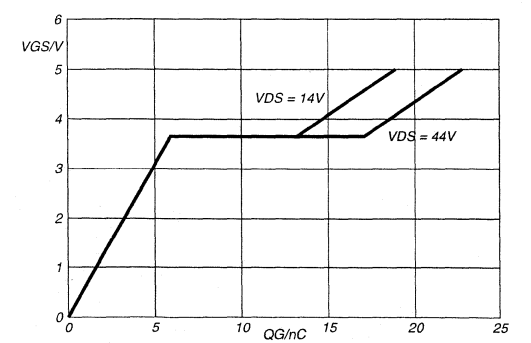


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 30$ A; parameter V_{DS}

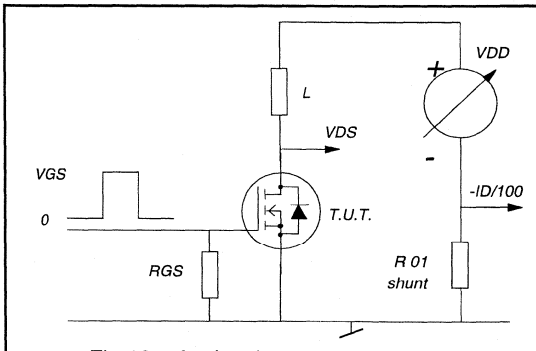


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

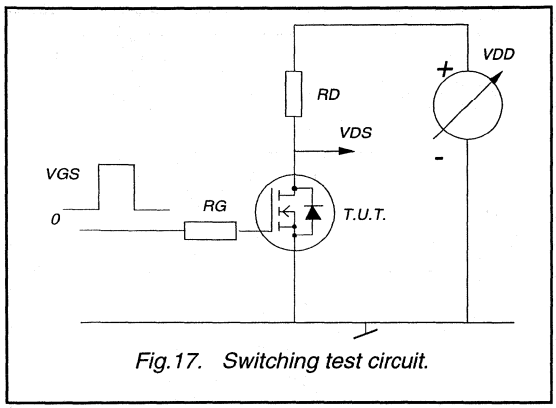


Fig.17. Switching test circuit.

TrenchMOS™ transistor
Logic level FET

BUK9575-55

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using **'trench'** technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

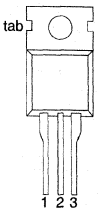
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	19.7	A
P_{tot}	Total power dissipation	61	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	75	mΩ

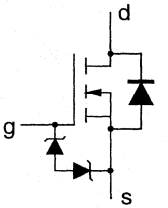
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	19.7	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	13.9	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	79	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	61	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	2.46	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	1.5	2	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-		10	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 10 A	-	60	75	mΩ
		T_j = 175˚C	-	-	157	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 10 A	5	-	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	500	650	pF
C_{oss}	Output capacitance		-	110	135	pF
C_{rss}	Feedback capacitance		-	60	85	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 10 A;	-	10	15	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω	-	47	70	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	28	40	ns
t_f	Turn-off fall time		-	33	45	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	19.7	A
I_{DRM}	Pulsed reverse drain current		-	-	79	A
V_{SD}	Diode forward voltage	I_F = 19.7 A; V_{GS} = 0 V	-	0.95	1.2	V
t_{rr}	Reverse recovery time	I_F = 19.7 A; -dI_F/dt = 100 A/µs;	-	32	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.12	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 10 A; $V_{DD} \leq 25$ V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	30	mJ

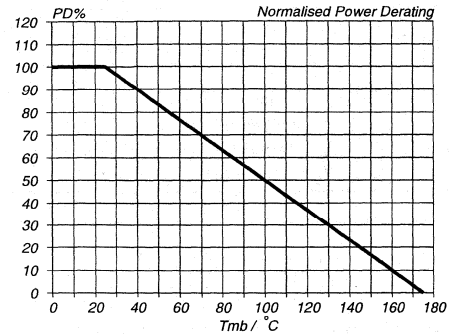


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

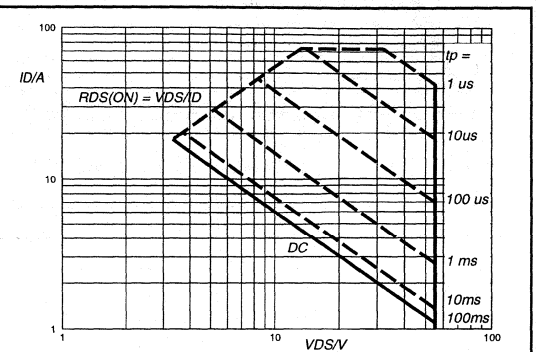


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

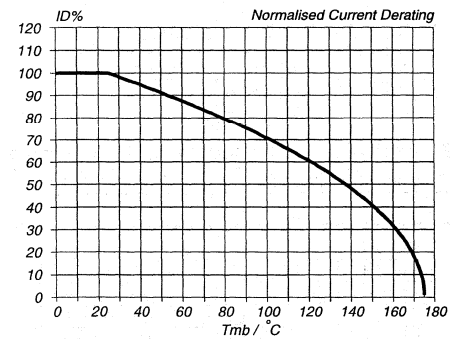


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq 5$ V

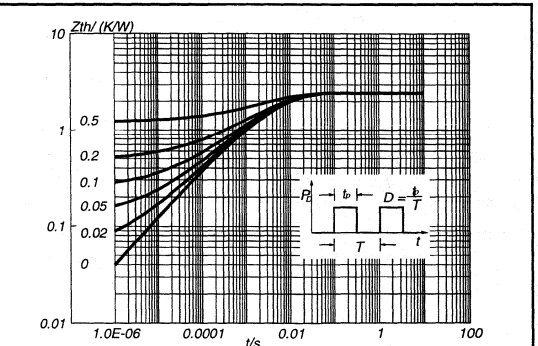


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

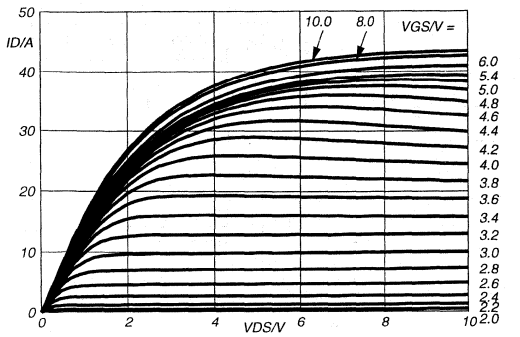


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

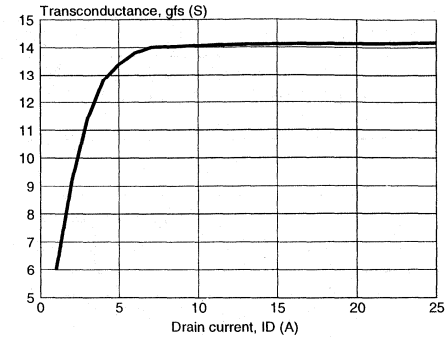


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

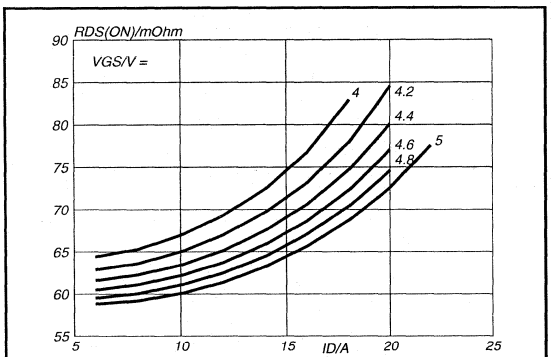


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

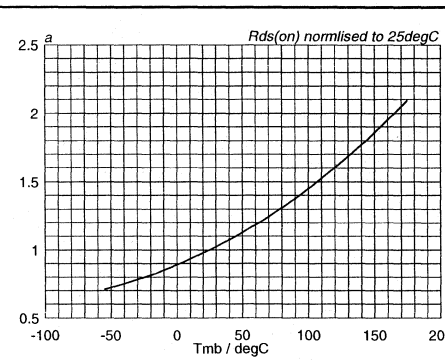


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,˚C} = f(T_j)$; I_D = 10 A; V_{GS} = 5 V

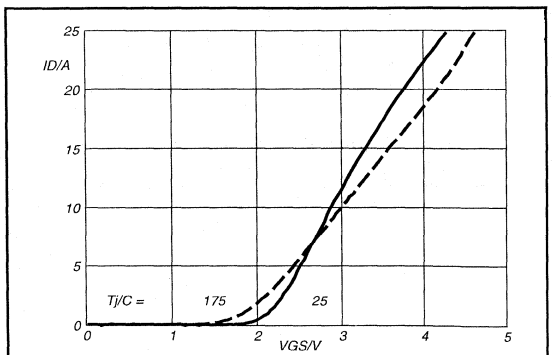


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

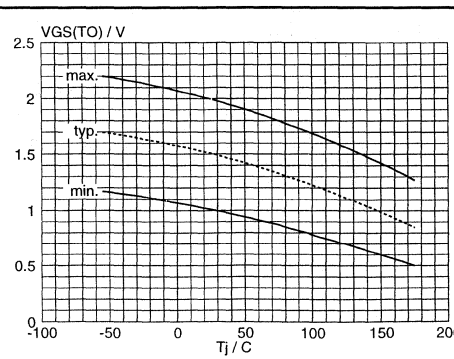


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

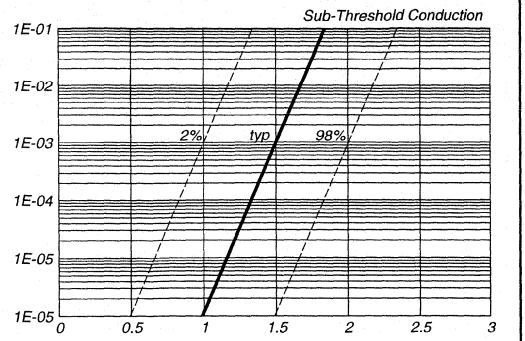


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

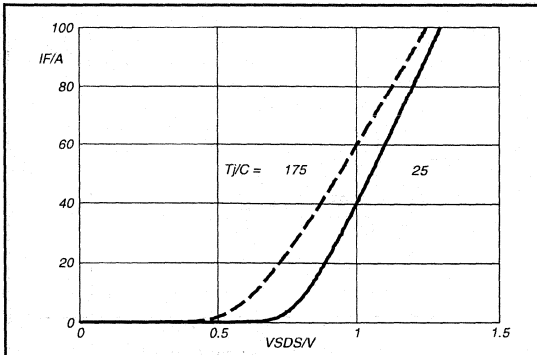


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

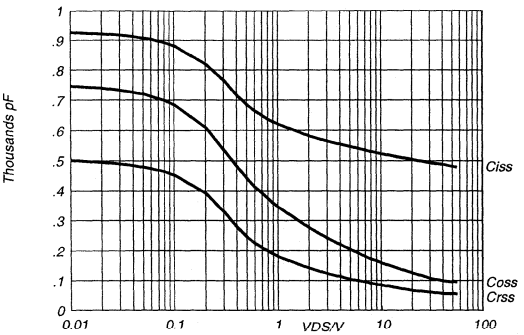


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

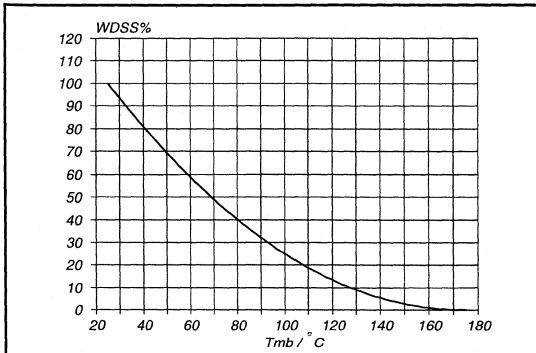


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 17$ A

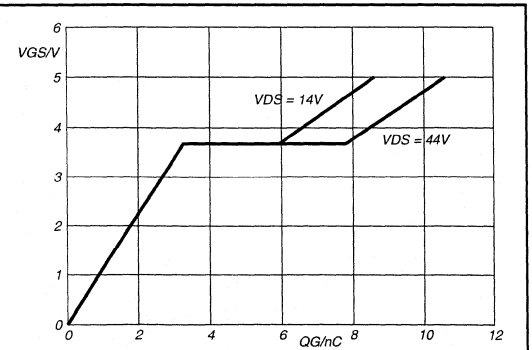


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 20$ A; parameter V_{DS}

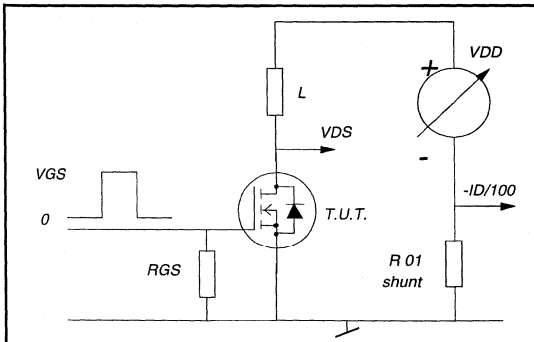


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

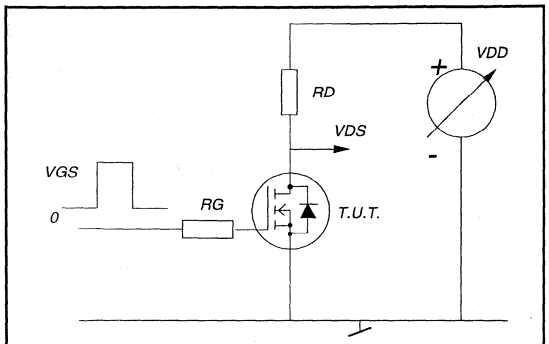


Fig.17. Switching test circuit.

TrenchMOS™ transistor Logic level FET

BUK9606-30

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting using '**trench**' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

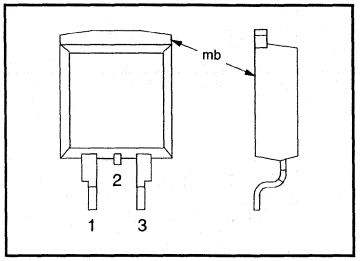
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	30	V
I_D	Drain current (DC)	75	A
P_{tot}	Total power dissipation	187	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	6	mΩ

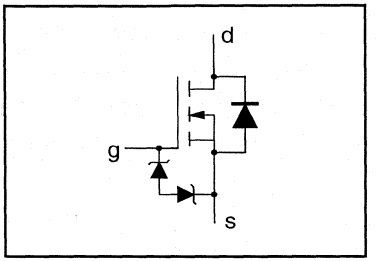
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	30	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	30	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	75	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	53	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	240	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	187	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	0.8	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board	50	-	K/W

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	30	-	-	V
		T_j = -55˚C	27	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 30 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	10	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	5	6	mΩ
		T_j = 175˚C	-	-	11	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	20	40	-	S
$Q_{g(tot)}$	Total gate charge	I_D = 75 A; V_{DD} = 24 V; V_{GS} = 5 V	-	92	-	nC
Q_{gs}	Gate-source charge		-	10	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	36	-	nC
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	5000	-	pF
C_{oss}	Output capacitance		-	1150	-	pF
C_{rss}	Feedback capacitance		-	500	-	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 15 V; I_D = 25 A;	-	45	60	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 5 Ω	-	120	170	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	225	300	ns
t_f	Turn-off fall time		-	100	135	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead solder point to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead solder point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	75	A
I_{DRM}	Pulsed reverse drain current		-	-	240	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.85	1.2	V
		I_F = 75 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 75 A; -dI_F/dt = 100 A/µs;	-	100	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 25 V	-	0.6	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 75 A; $V_{DD} \leq$ 15 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	500	mJ

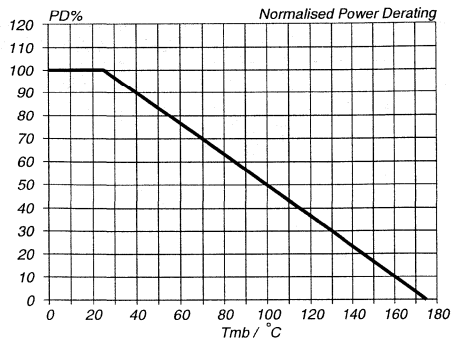


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

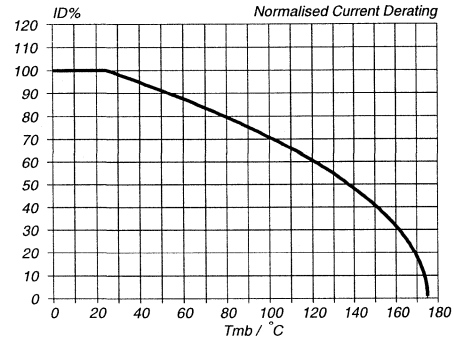


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 5 V

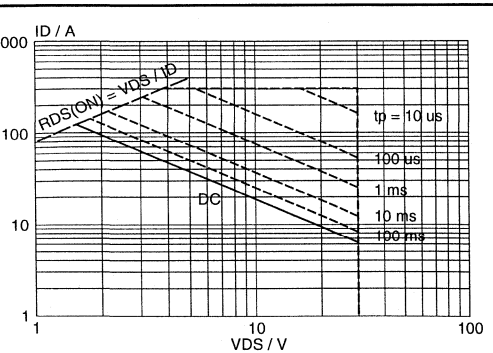


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

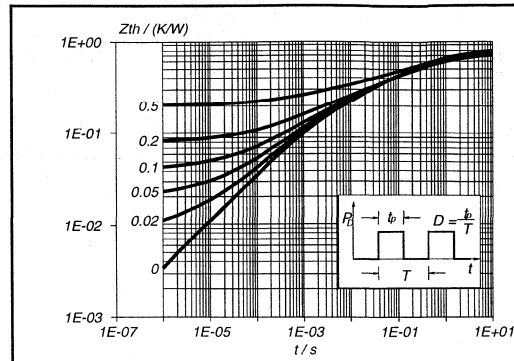


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

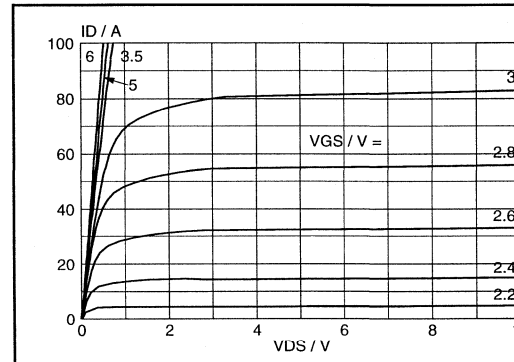


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

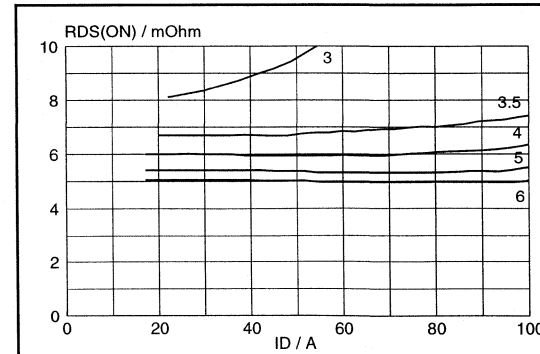


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

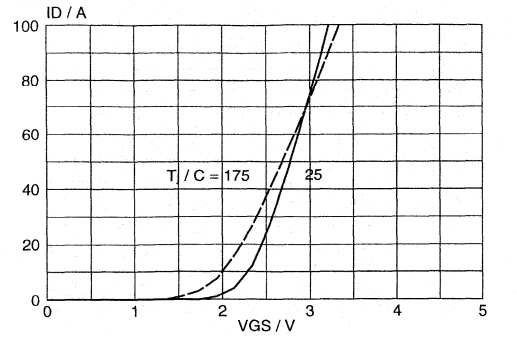


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

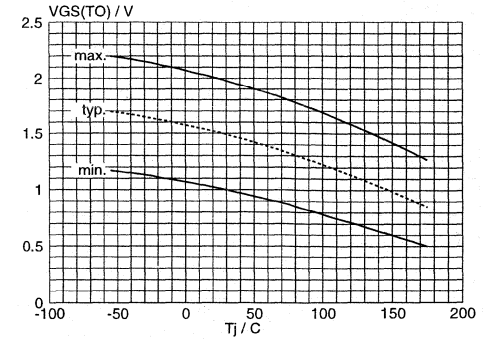


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

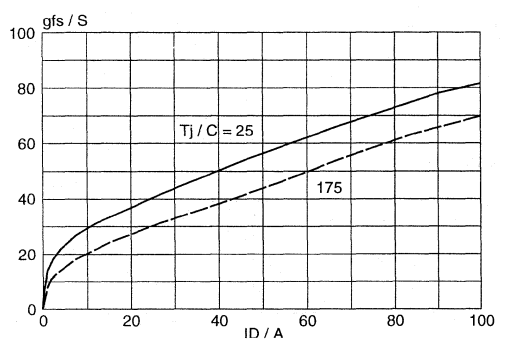


Fig.8. Typical transconductance, T_j = 25 ˚C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

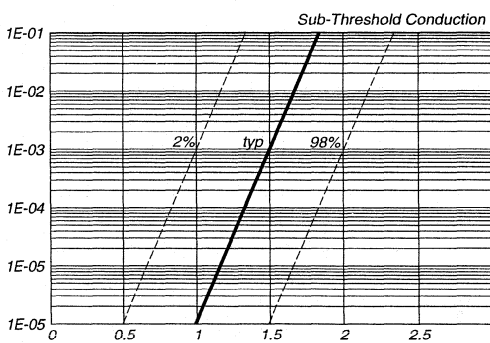


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

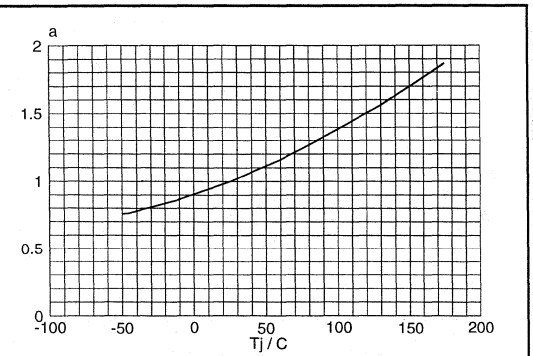


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

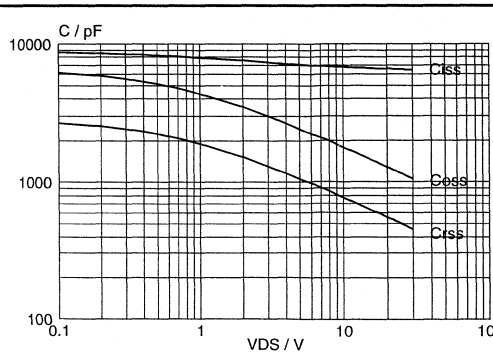


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

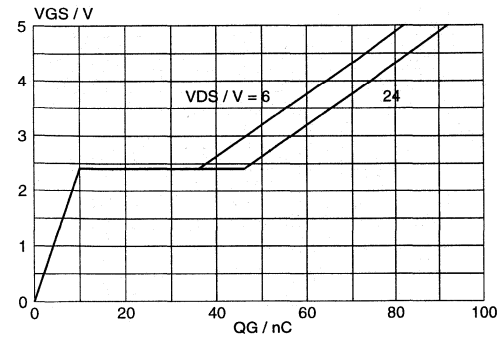


Fig.13. Typical turn-on gate-charge characteristics.
V_{GS} = f(Q_G); conditions: I_D = 75 A; parameter V_{DS}

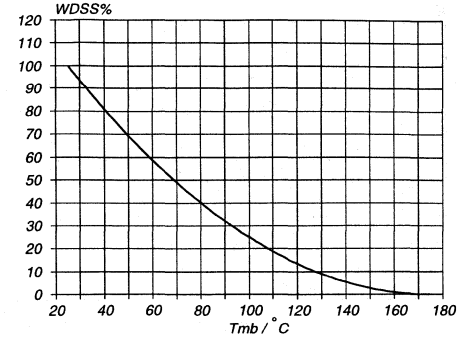


Fig.15. Normalised avalanche energy rating.
W_{DSS}% = f(T_{mb}); conditions: I_D = 75 A

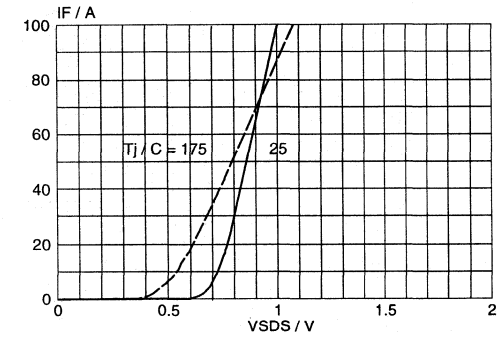


Fig.14. Typical reverse diode current.
I_F = f(V_{SDS}); conditions: V_{GS} = 0 V; parameter T_j

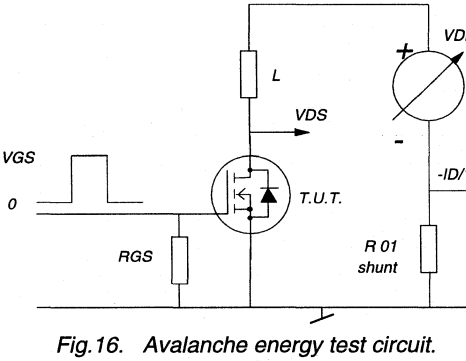


Fig.16. Avalanche energy test circuit.
$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

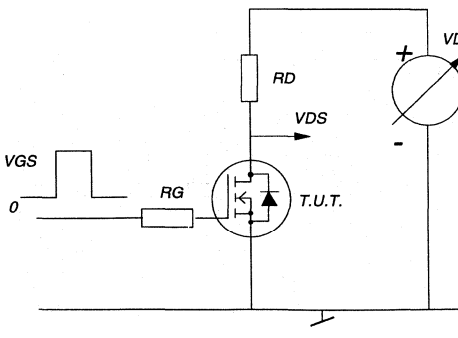


Fig.17. Switching test circuit.

TrenchMOS™ transistor Logic level FET

BUK9608-55

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting Using **'trench'** technology the device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

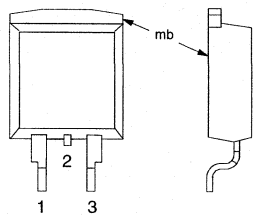
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	75	A
P_{tot}	Total power dissipation	187	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	8	mΩ

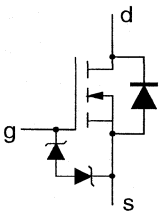
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	75	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	65	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	240	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	187	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	0.8	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	Minimum footprint,FR4 board	50	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	uA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	10	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	6.5	8	mΩ
		T_j = 175˚C	-	-	17	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	40	90	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	5200	6900	pF
C_{oss}	Output capacitance		-	840	1000	pF
C_{rss}	Feedback capacitance		-	350	480	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	45	60	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω	-	120	170	ns
$t_{d\,off}$	Turn-off delay time		-	225	300	ns
t_f	Turn-off fall time		-	100	135	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	3.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	75	A
I_{DRM}	Pulsed reverse drain current		-	-	240	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.85	1.2	V
		I_F = 75 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 75 A; -dI_F/dt = 100 A/µs;	-	65	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.18	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 75 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	500	mJ

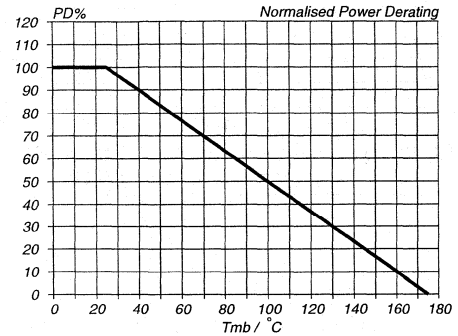


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

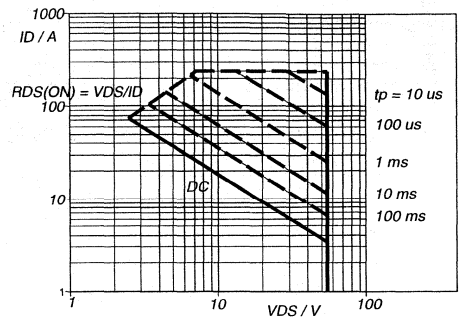


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

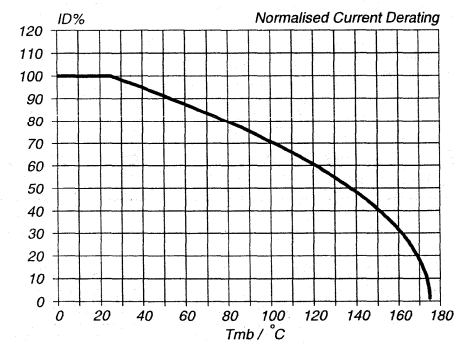


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

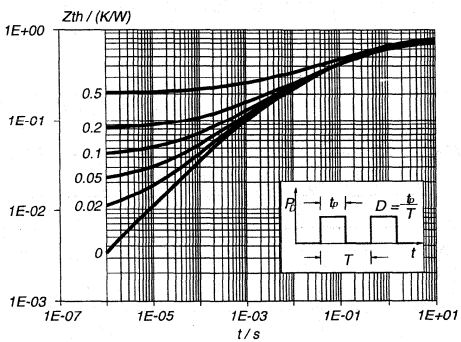


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

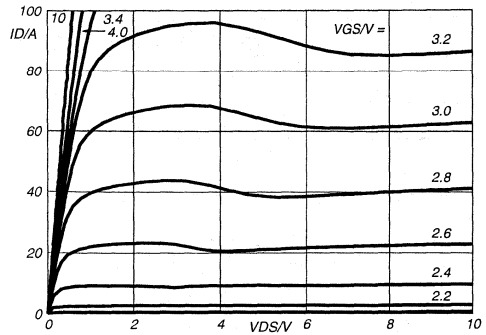


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

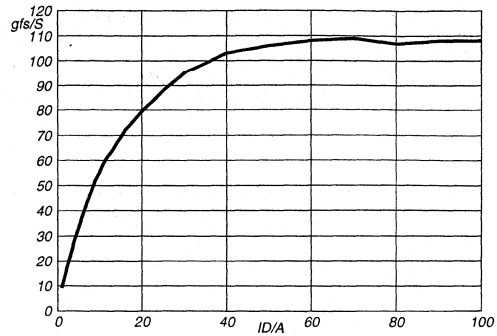


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

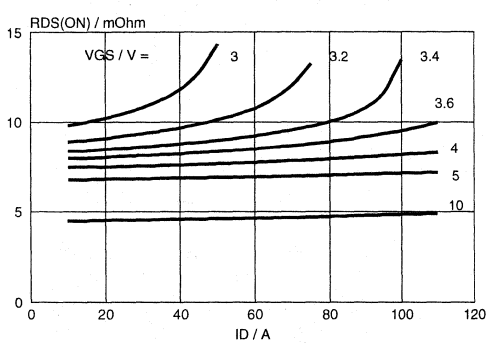


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

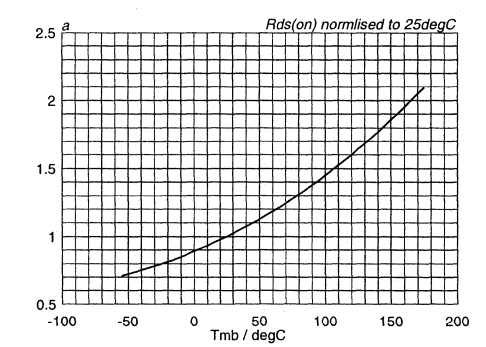


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,˚C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

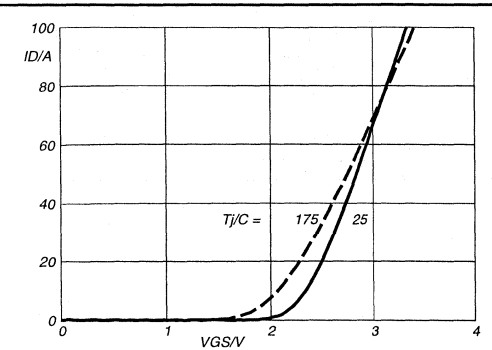


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

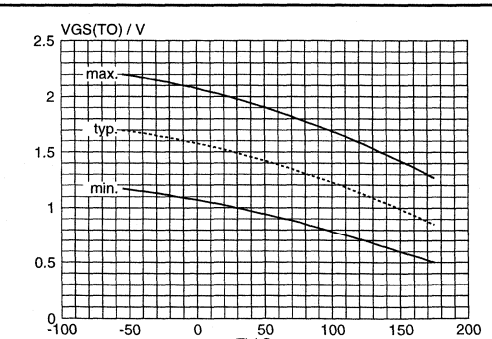


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

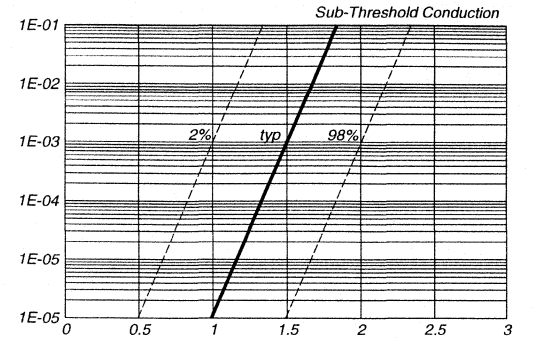


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

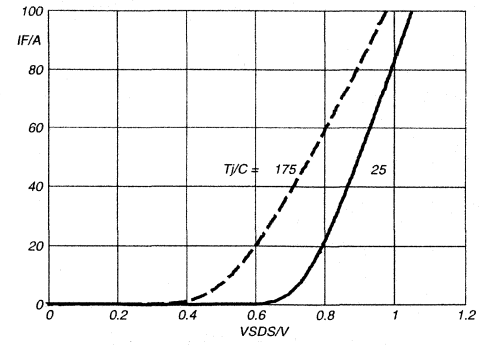


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

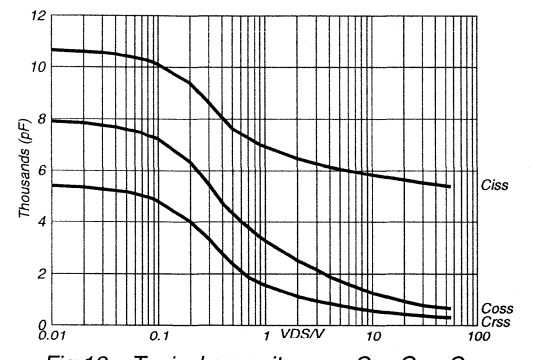


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

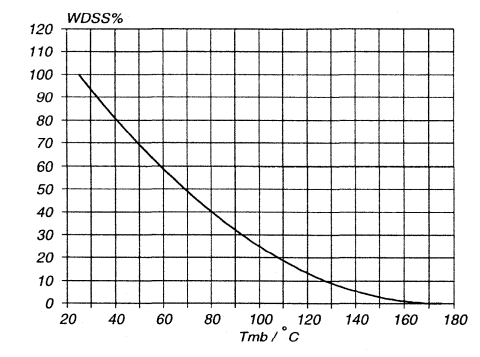


Fig.15. Normalised avalanche energy rating.
W_{DSS}% = $f(T_{mb})$; conditions: I_D = 75 A

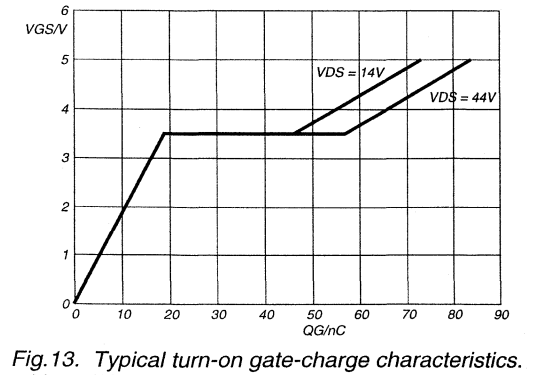


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 50 A; parameter V_{DS}

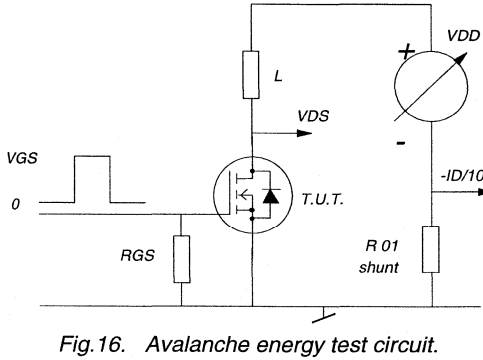


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

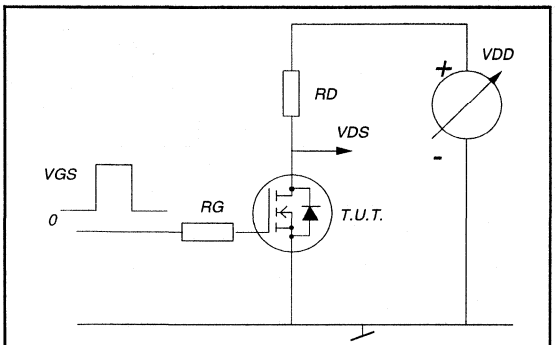


Fig.17. Switching test circuit.

TrenchMOS™ transistor
Logic level FET

BUK9610-30

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting using '**trench**' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

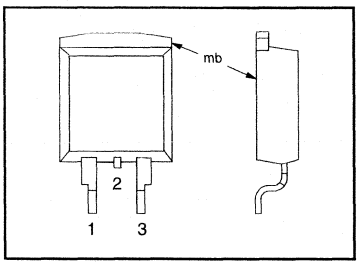
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	30	V
I_D	Drain current (DC)	75	A
P_{tot}	Total power dissipation	142	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	10.5	mΩ

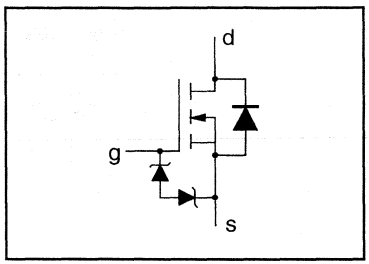
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	30	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	30	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	75	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	53	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	240	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	142	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.05	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board	50	-	K/W

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model (100 pF, 1.5 kΩ)	-	2	kV

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;		30	-	-	V
			T_j = -55˚C	27	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA		1.0	1.5	2.0	V
			T_j = 175˚C	0.5	-	-	V
			T_j = -55˚C	-	-	2.3	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 30 V; V_{GS} = 0 V;		-	0.05	10	µA
			T_j = 175˚C	-	-	500	uA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V		-	0.02	1	µA
			T_j = 175˚C	-	-	10	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;		10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A		-	9	10.5	mΩ
			T_j = 175˚C	-	-	19.5	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	12	25	-	S
$Q_{g(tot)}$	Total gate charge	I_D = 75 A; V_{DD} = 24 V; V_{GS} = 5 V	-	58	-	nC
Q_{gs}	Gate-source charge		-	6	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	24	-	nC
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	2500	-	pF
C_{oss}	Output capacitance		-	640	-	pF
C_{rss}	Feedback capacitance		-	320	-	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 15 V; I_D = 25 A;	-	35	50	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 5 Ω	-	95	145	ns
$t_{d\,off}$	Turn-off delay time		-	130	180	ns
t_f	Turn-off fall time		-	60	80	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead solder point to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead solder point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	75	A
I_{DRM}	Pulsed reverse drain current		-	-	240	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 75 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 75 A; -dI_F/dt = 100 A/µs;	-	70	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 25 V	-	0.14	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 45 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	200	mJ

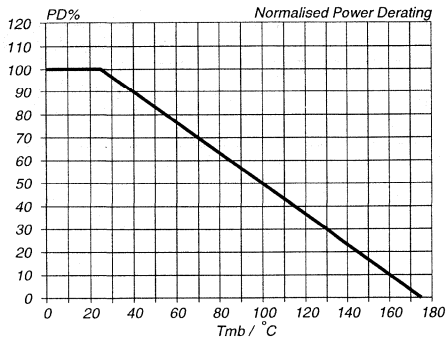


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

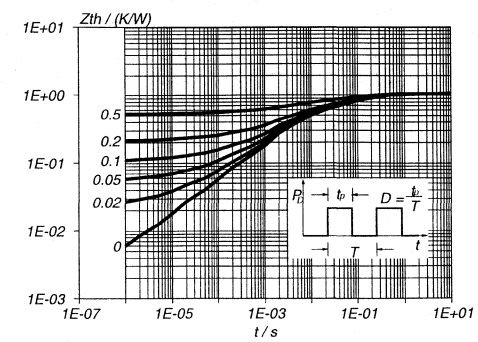


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

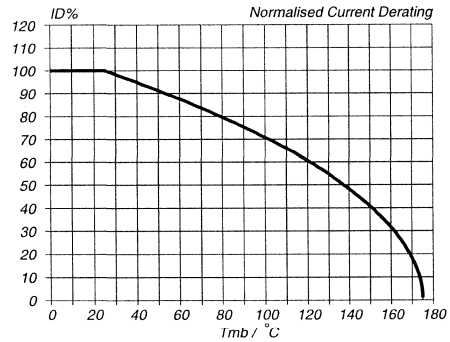


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 5 V

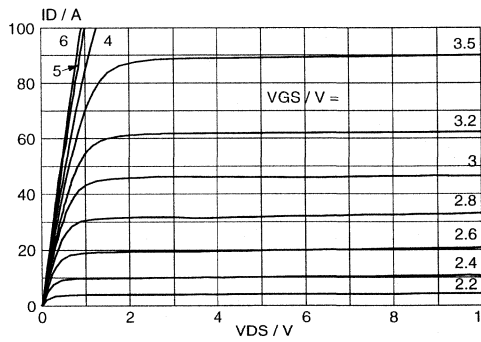


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

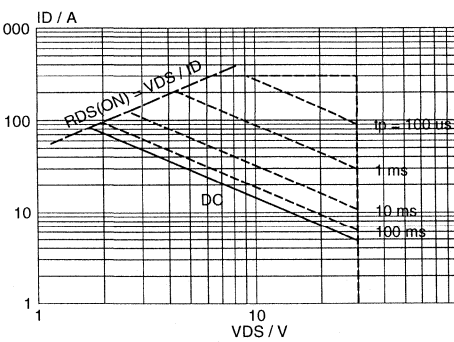


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

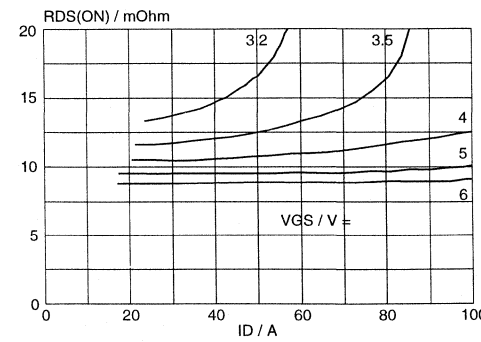


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

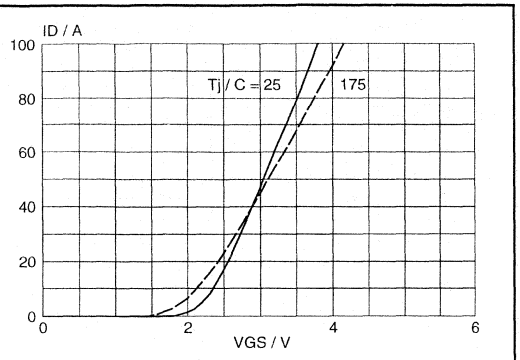


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

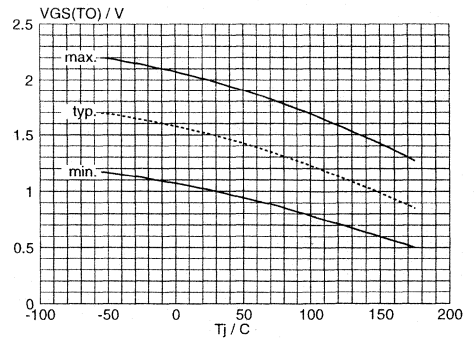


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

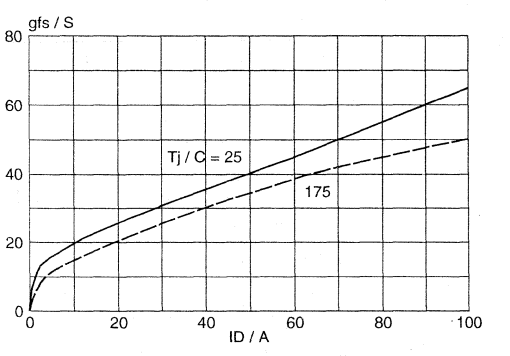


Fig.8. Typical transconductance, T_j = 25 ˚C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

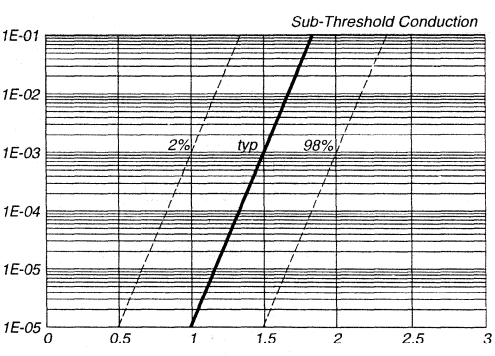


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

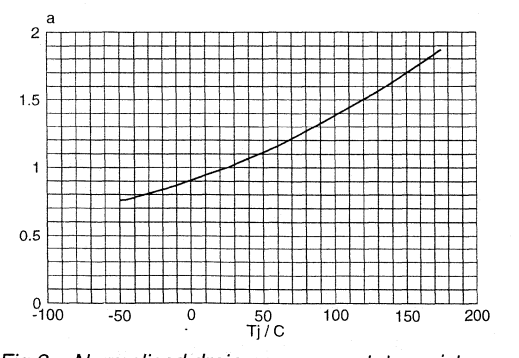


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,˚C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

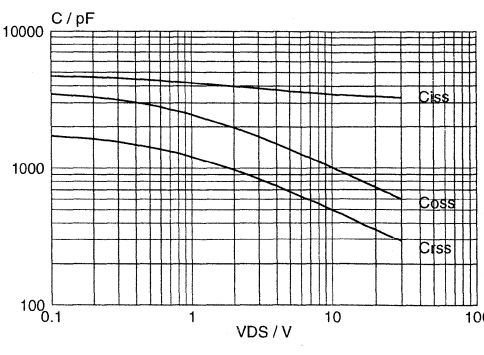


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

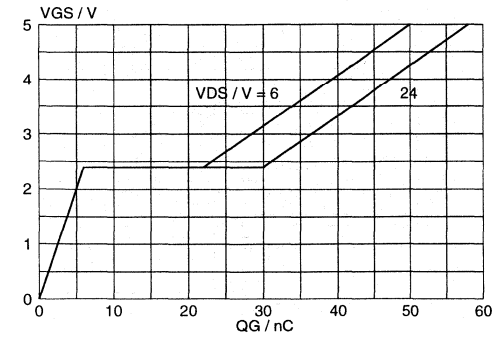


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 75$ A; parameter V_{DS}

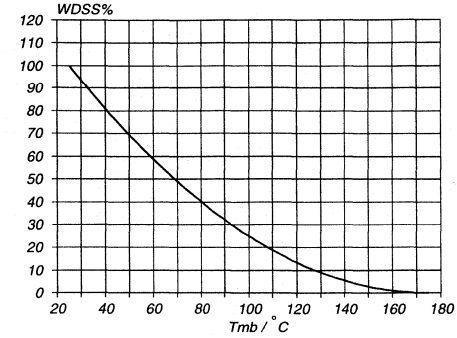


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 45$ A

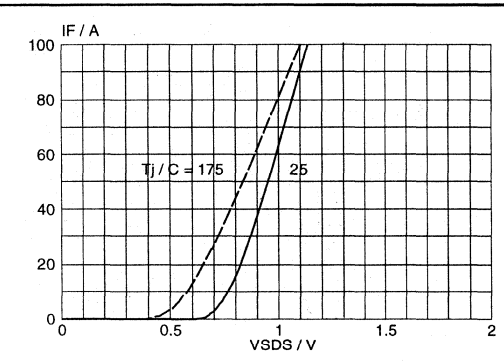


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

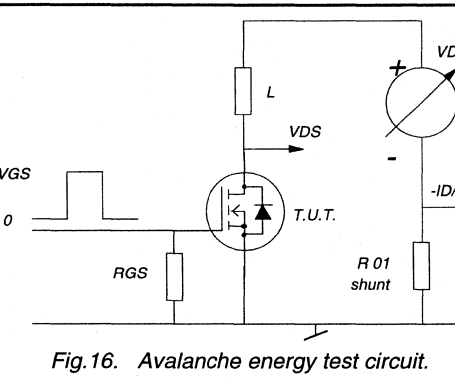


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

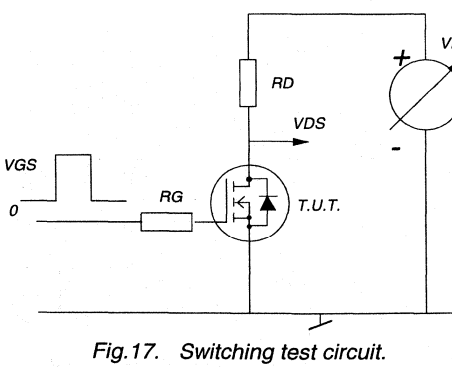


Fig.17. Switching test circuit.

TrenchMOS™ transistor Logic level FET

BUK9614-30

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting using '**trench**' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

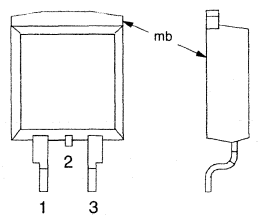
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	30	V
I_D	Drain current (DC)	69	A
P_{tot}	Total power dissipation	125	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	14	mΩ

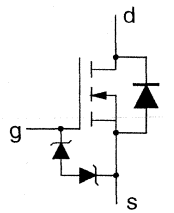
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	30	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	30	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	69	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	48	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	240	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board	50	-	K/W

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model (100 pF, 1.5 kΩ)	-	2	kV

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	30	-	-	V
		T_j = -55˚C	27	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 30 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	uA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	10	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	12	14	mΩ
		T_j = 175˚C	-	-	26	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	12	25	-	S
$Q_{g(tot)}$	Total gate charge	I_D = 69 A; V_{DD} = 24 V; V_{GS} = 5 V	-	38	-	nC
Q_{gs}	Gate-source charge		-	5	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	15	-	nC
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	2000	-	pF
C_{oss}	Output capacitance		-	480	-	pF
C_{rss}	Feedback capacitance		-	220	-	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 15 V; I_D = 25 A;	-	30	45	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 5 Ω	-	80	130	ns
$t_{d\,off}$	Turn-off delay time		-	100	140	ns
t_f	Turn-off fall time		-	50	75	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead solder point to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead solder point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	69	A
I_{DRM}	Pulsed reverse drain current		-	-	240	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 69 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 69 A; -dI_F/dt = 100 A/µs;	-	65	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 25 V	-	0.1	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 35 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	125	mJ

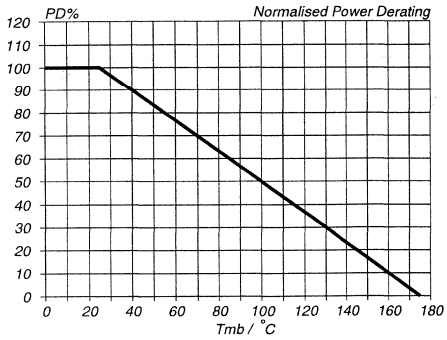


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

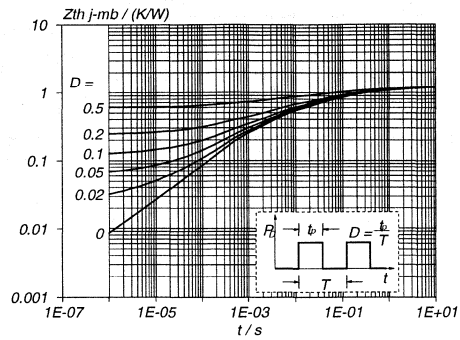


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

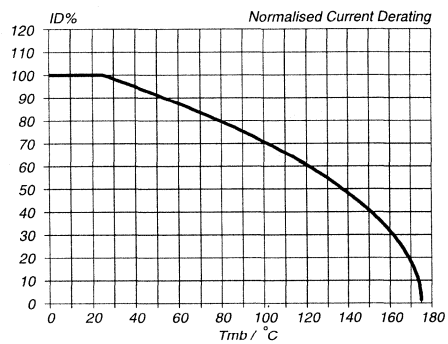


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 5 V

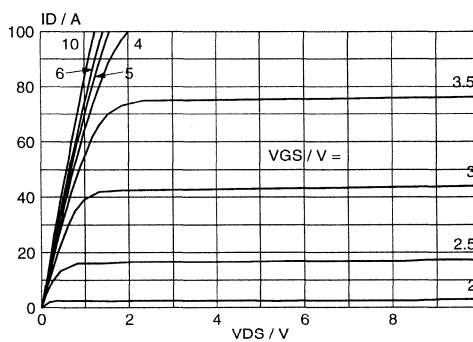


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

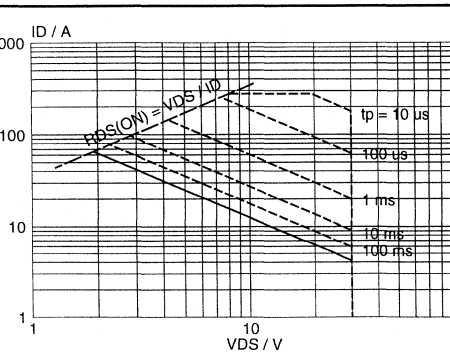


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

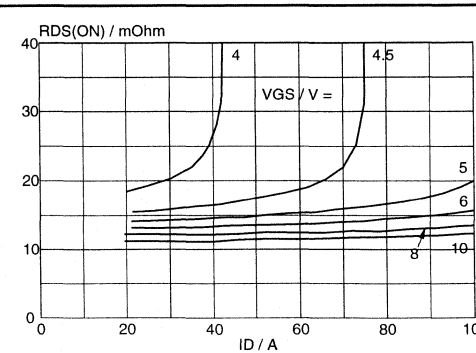


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

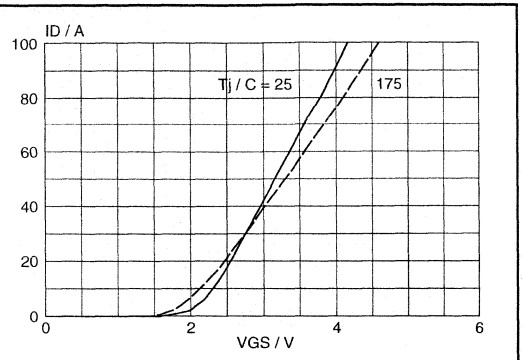


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

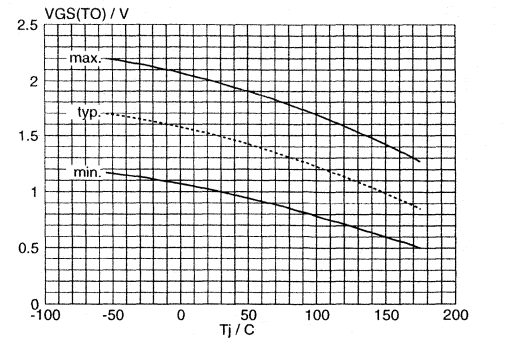


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

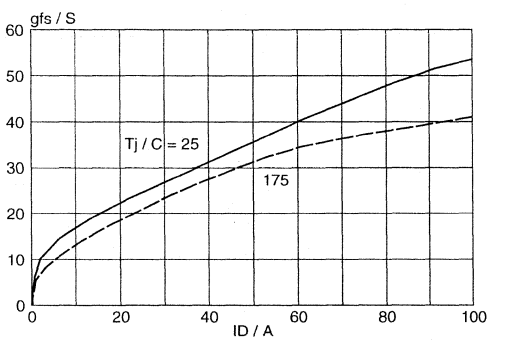


Fig.8. Typical transconductance, $T_j = 25$ ˚C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

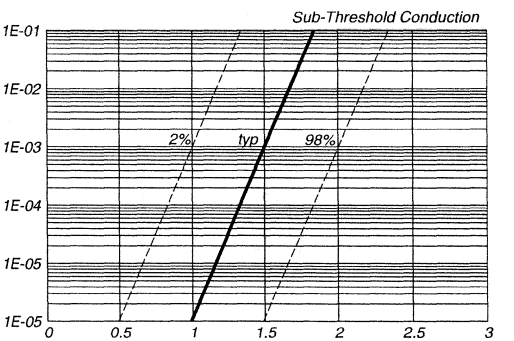


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ ˚C; $V_{DS} = V_{GS}$

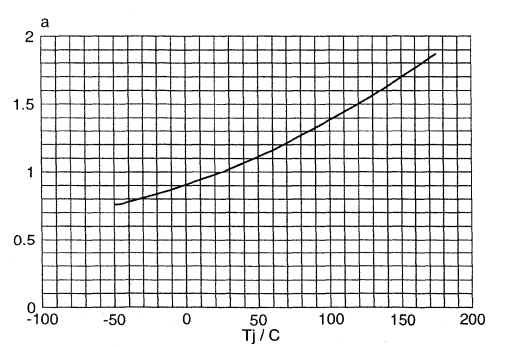


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ ^\circ C} = f(T_j)$; $I_D = 25$ A; $V_{GS} = 5$ V

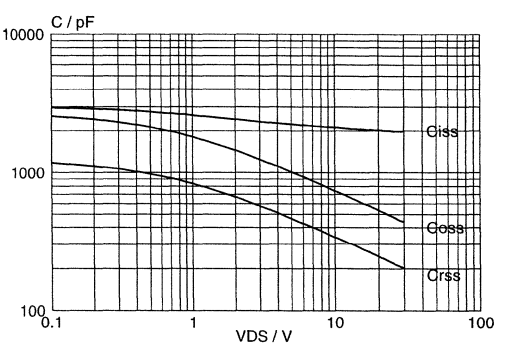


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

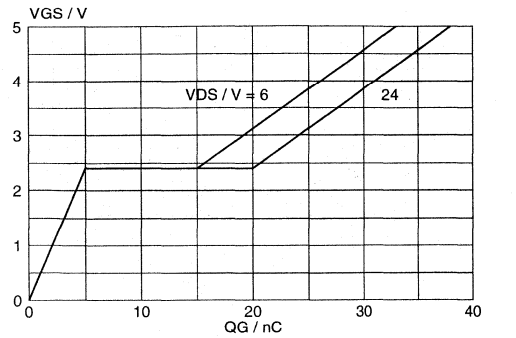


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 69 A; parameter V_{DS}

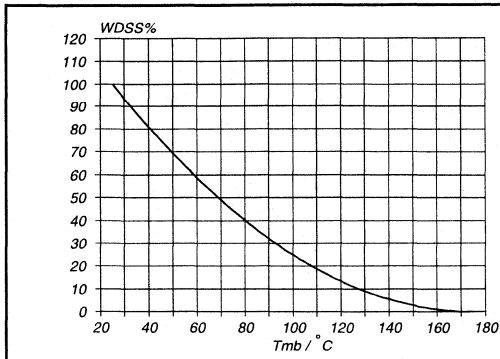


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: I_D = 35 A

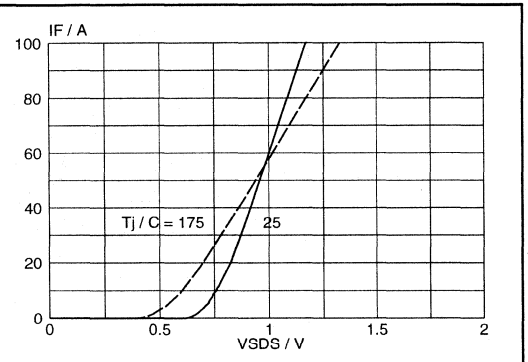


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

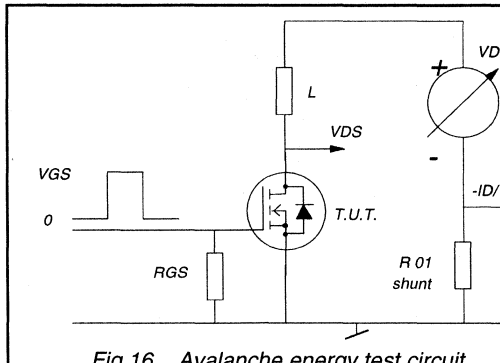


Fig.16. Avalanche energy test circuit.
$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

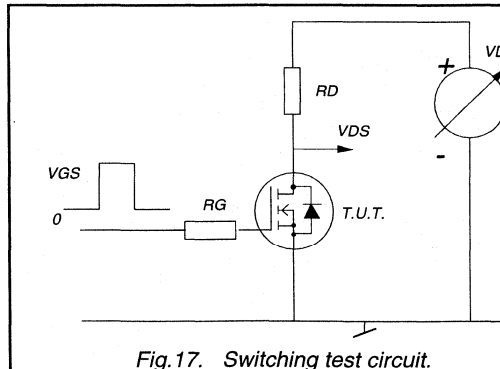


Fig.17. Switching test circuit.

TrenchMOS™ transistor Logic level FET

BUK9614-55

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting. Using '**trench**' technology the device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

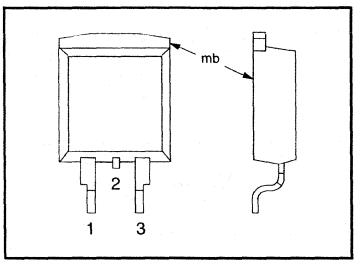
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	68	A
P_{tot}	Total power dissipation	142	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	14	mΩ

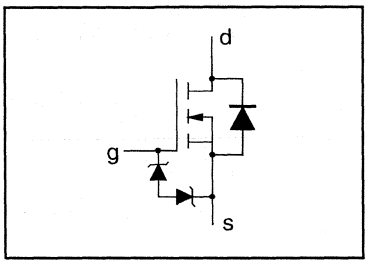
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	68	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	48	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	240	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	142	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.05	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	Minimum footprint, FR4 board	50	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	uA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	10	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	12	14	mΩ
		T_j = 175˚C	-	-	30	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	30	65	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	2900	3800	pF
C_{oss}	Output capacitance		-	500	600	pF
C_{rss}	Feedback capacitance		-	240	330	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	35	50	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω	-	95	145	ns
$t_{d\,off}$	Turn-off delay time		-	130	180	ns
t_f	Turn-off fall time		-	60	80	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	68	A
I_{DRM}	Pulsed reverse drain current		-	-	240	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 65 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 65 A; -dI_F/dt = 100 A/µs;	-	57	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.14	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 65 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	200	mJ

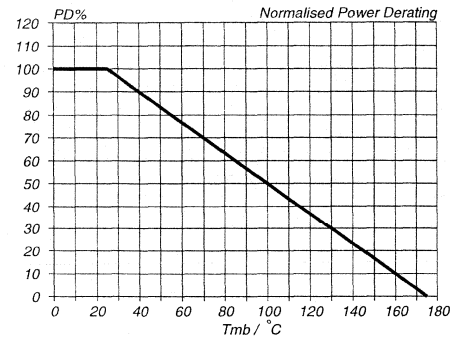


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

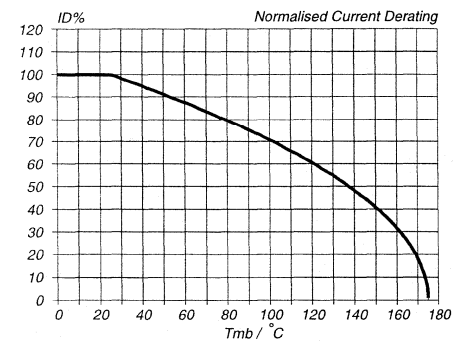


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

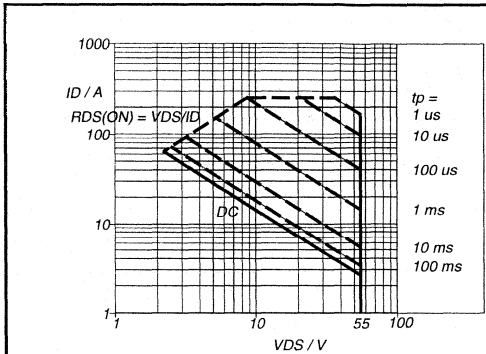


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

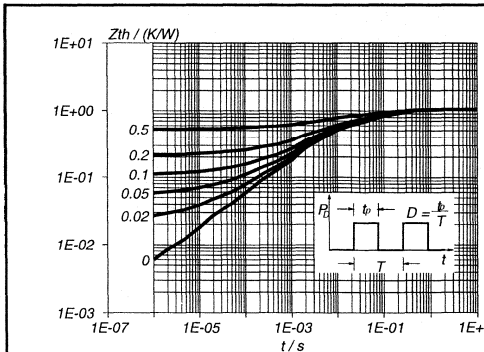


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

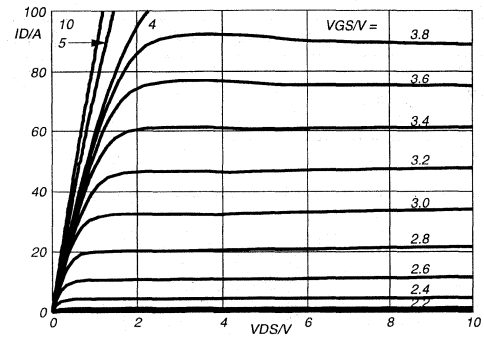


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

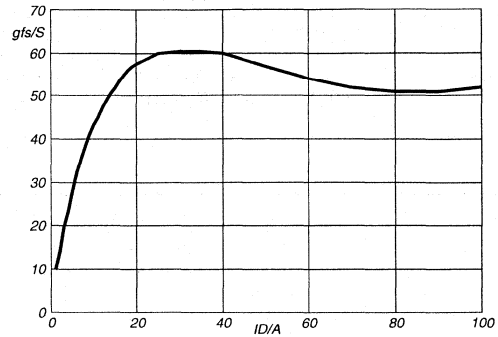


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

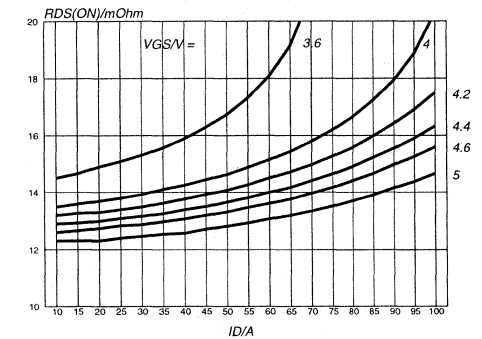


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

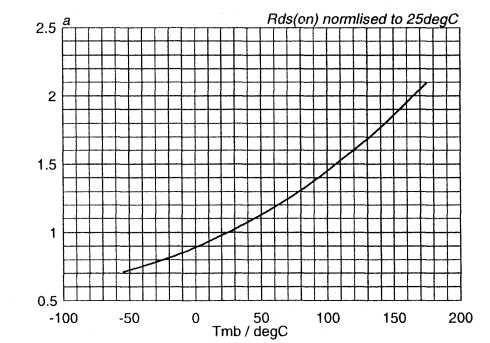


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\ ^\circ C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

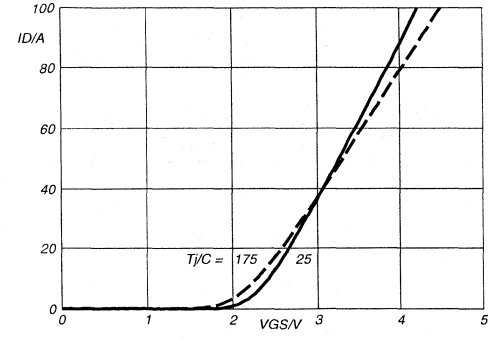


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

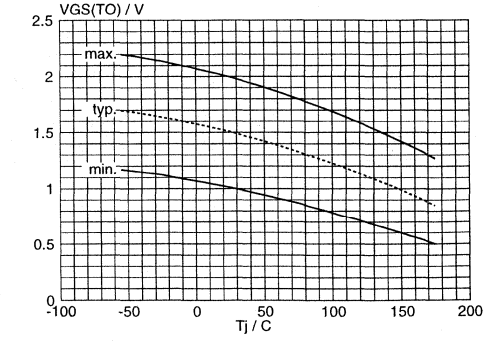


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

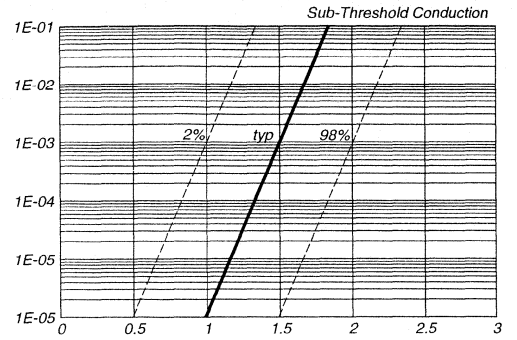


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; *conditions:* $T_j = 25$ °C; $V_{DS} = V_{GS}$

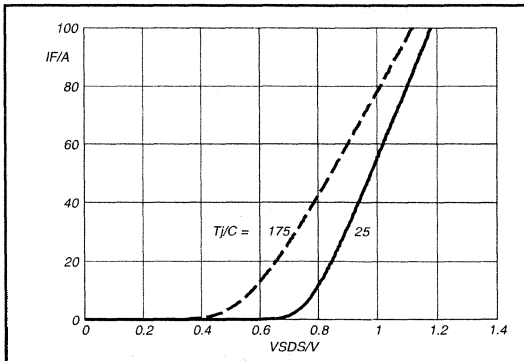


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; *conditions:* $V_{GS} = 0$ V; *parameter* T_j

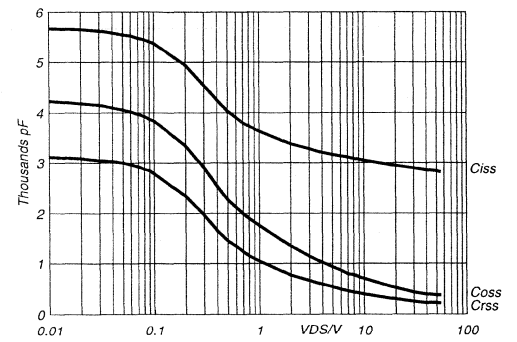


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; *conditions:* $V_{GS} = 0$ V; $f = 1$ MHz

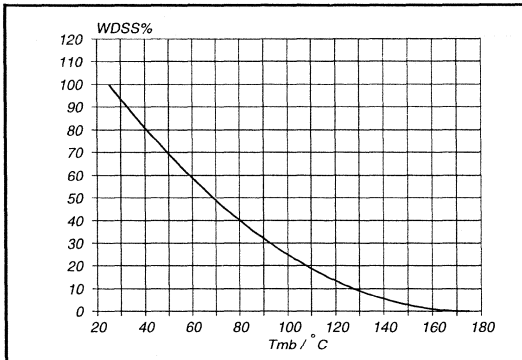


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; *conditions:* $I_D = 75$ A

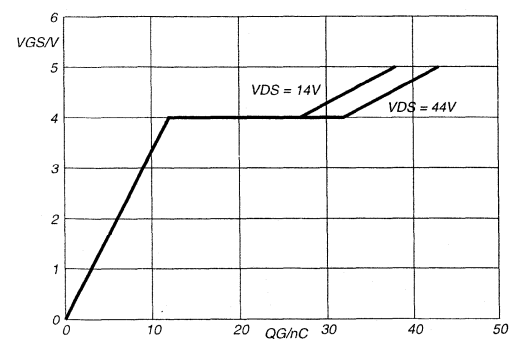


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; *conditions:* $I_D = 50$ A; *parameter* V_{DS}

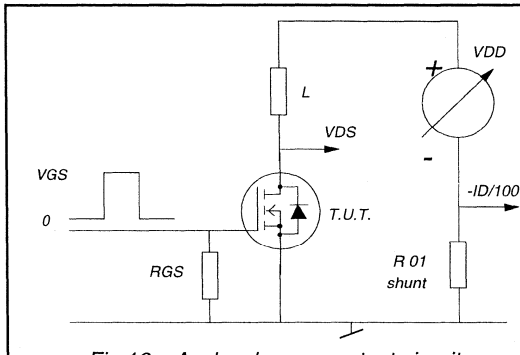


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

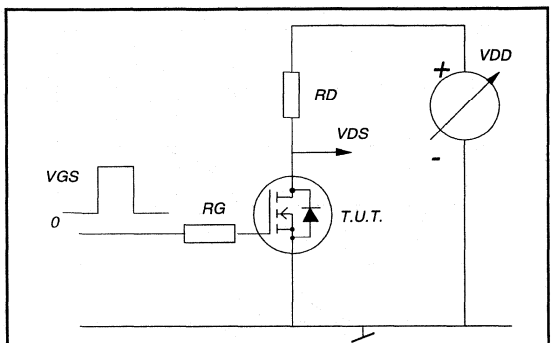


Fig.17. Switching test circuit.

TrenchMOS™ transistor Logic level FET

BUK9618-30

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting using '**trench**' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

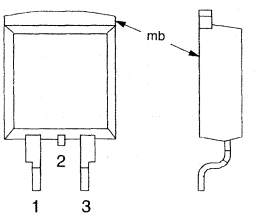
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	30	V
I_D	Drain current (DC)	55	A
P_{tot}	Total power dissipation	103	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	18	mΩ

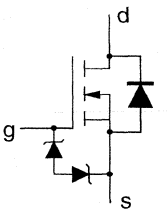
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	30	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	30	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	55	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	38	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	220	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	103	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.45	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board	50	-	K/W

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	30	-	-	V
		T_j = -55˚C	27	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	1.5	2	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	
I_{DSS}	Zero gate voltage drain current	V_{DS} = 30 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-		10	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	15	18	mΩ
		T_j = 175˚C	-	-	34	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	10	20	-	S
$Q_{g(tot)}$	Total gate charge	I_D = 55 A; V_{DD} = 24 V; V_{GS} = 5 V	-	31	-	nC
Q_{gs}	Gate-source charge		-	4	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	13	-	nC
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1450	-	pF
C_{oss}	Output capacitance		-	390	-	pF
C_{rss}	Feedback capacitance		-	200	-	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 15 V; I_D = 25 A;	-	30	45	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 5 Ω	-	80	130	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	95	135	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead solder point to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead solder point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	55	A
I_{DRM}	Pulsed reverse drain current		-	-	220	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 55 A; V_{GS} = 0 V	-	1.0	-	
t_{rr}	Reverse recovery time	I_F = 55 A; -dI_F/dt = 100 A/µs;	-	70	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 25 V	-	0.1	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 28 A; $V_{DD} \leq$ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	80	mJ

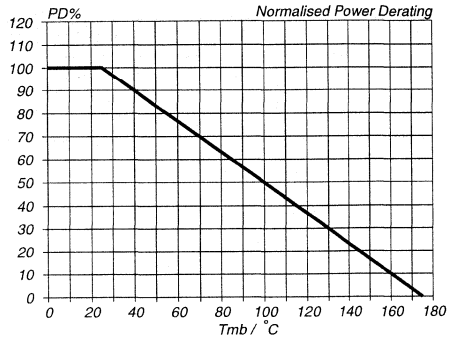


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

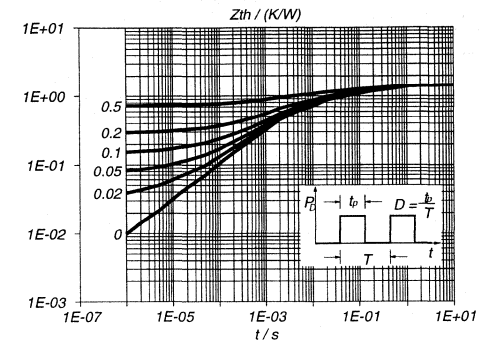


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

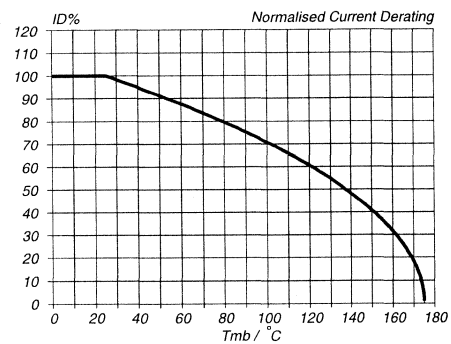


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 5 V

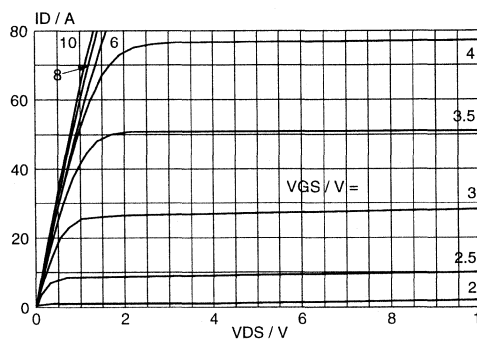


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

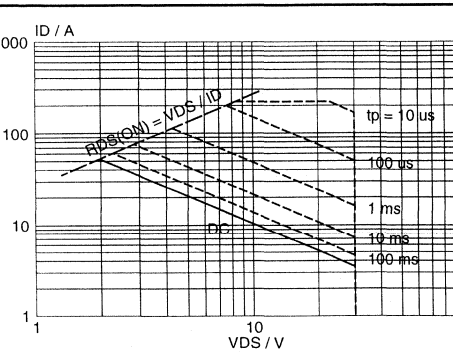


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

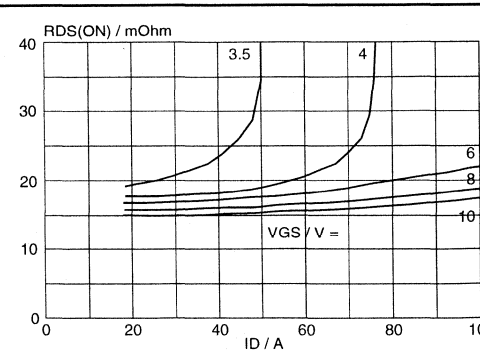


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

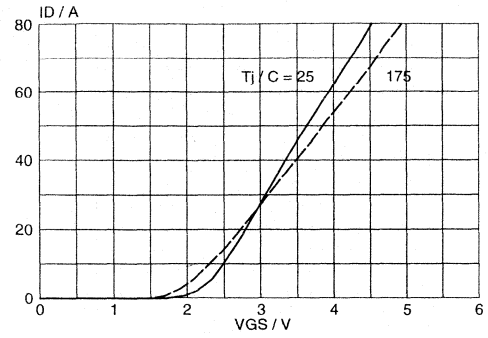


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

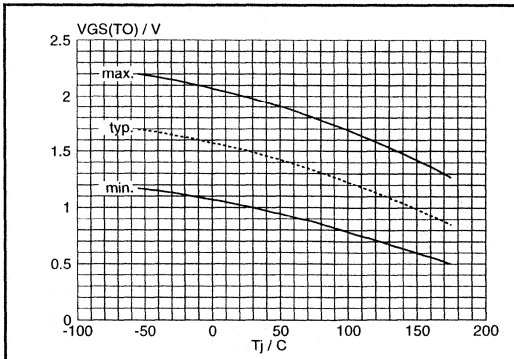


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

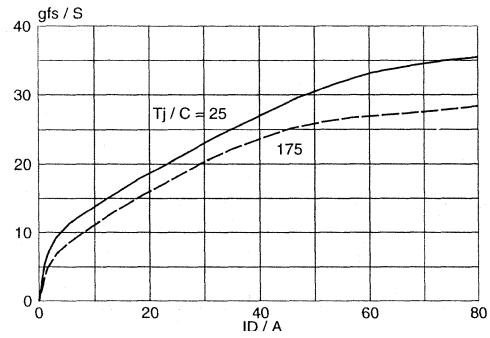


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

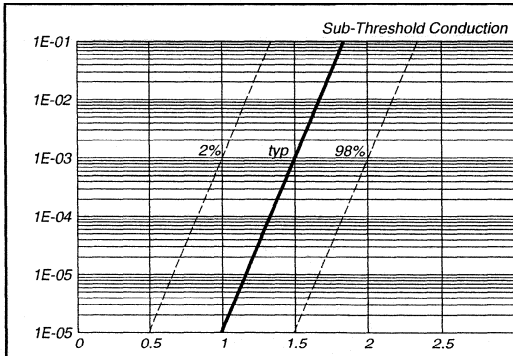


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

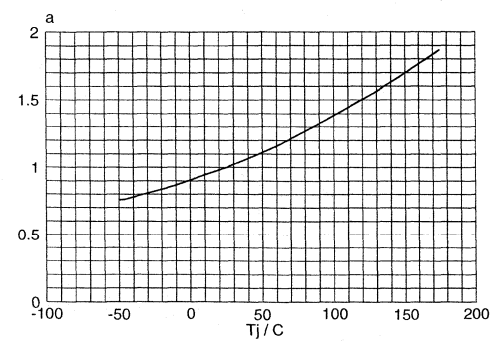


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

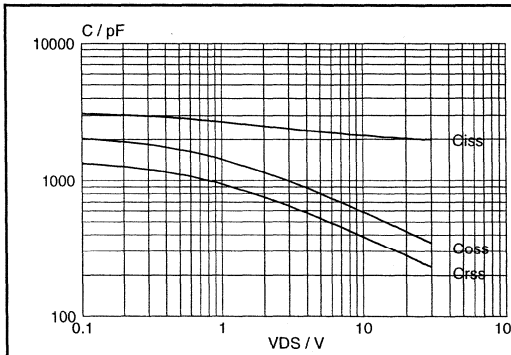


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

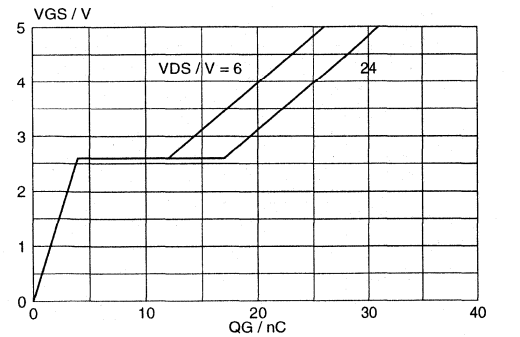


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: I_D = 55 A; parameter V_{DS}

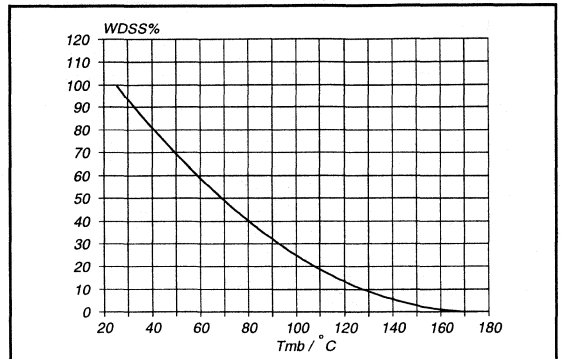


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: I_D = 28 A

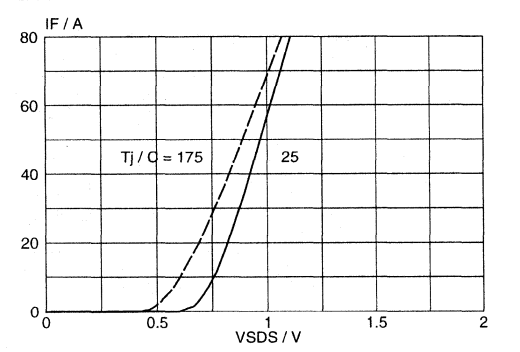


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

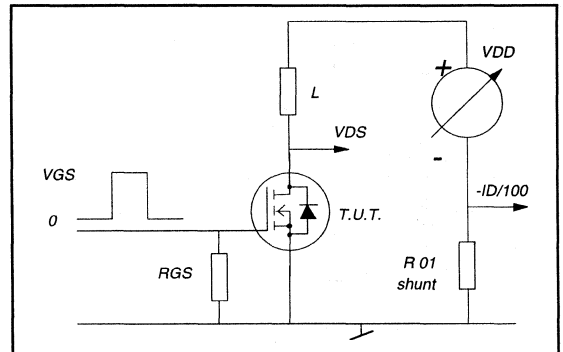


Fig.16. Avalanche energy test circuit.
$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

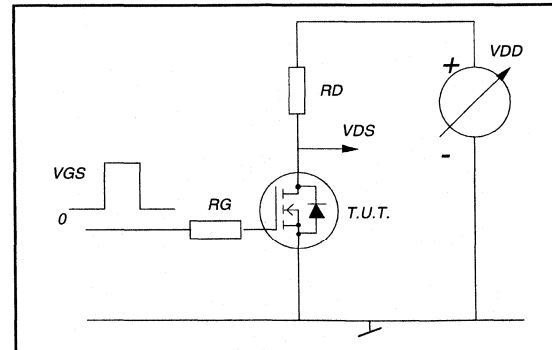


Fig.17. Switching test circuit.

TrenchMOS™ transistor Logic level FET

BUK9618-55

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting. Using '**trench**' technology the device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

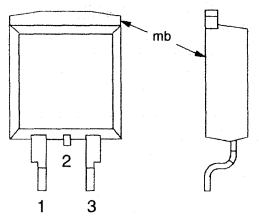
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	57	A
P_{tot}	Total power dissipation	125	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	18	mΩ

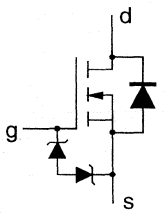
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	57	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	40	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	228	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	Minimum footprint, FR4 board	50	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	uA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	10	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	15	18	mΩ
		T_j = 175˚C	-	-	38	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	25	52	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	2000	2600	pF
C_{oss}	Output capacitance		-	390	490	pF
C_{rss}	Feedback capacitance		-	200	290	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	30	45	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω	-	80	130	ns
$t_{d\,off}$	Turn-off delay time		-	100	140	ns
t_f	Turn-off fall time		-	50	75	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	57	A
I_{DRM}	Pulsed reverse drain current		-	-	200	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 50 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 50 A; -dI_F/dt = 100 A/µs;	-	48	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.1	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 50 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	125	mJ

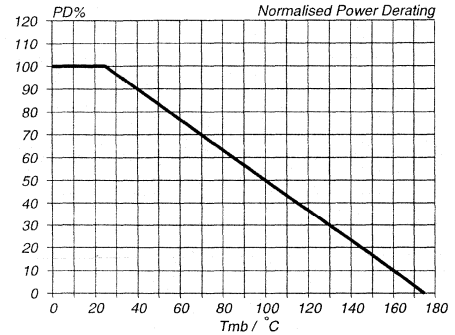


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

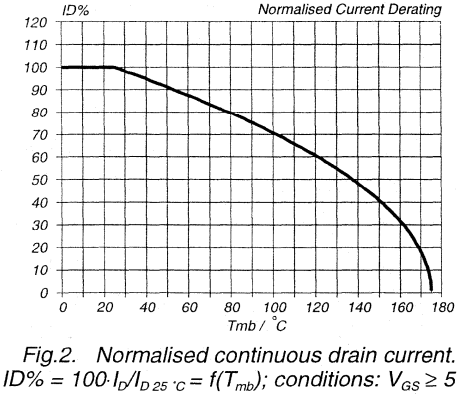


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

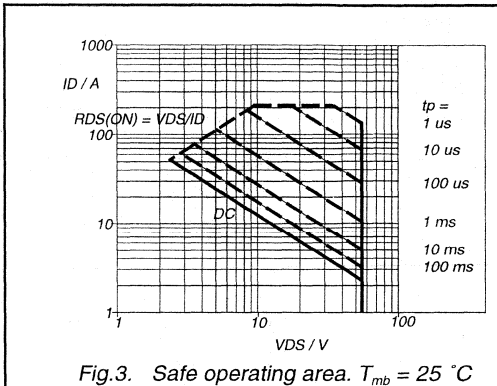


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

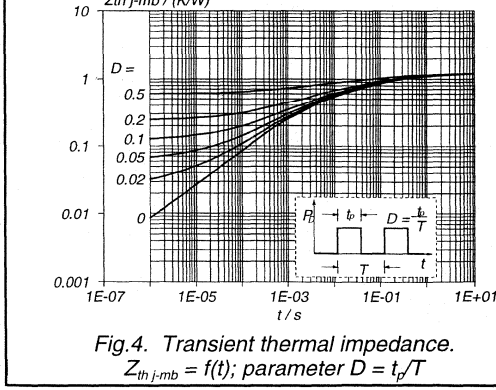


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

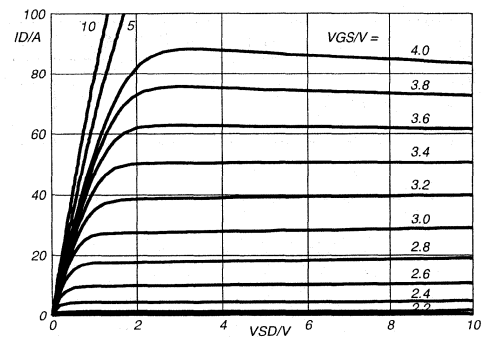


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

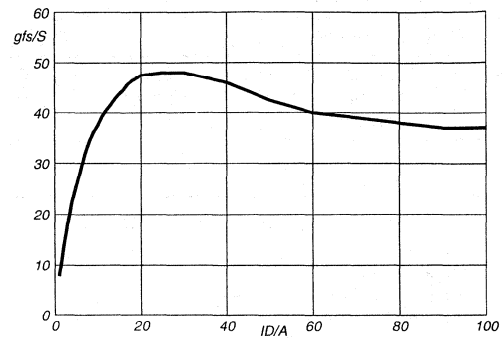


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

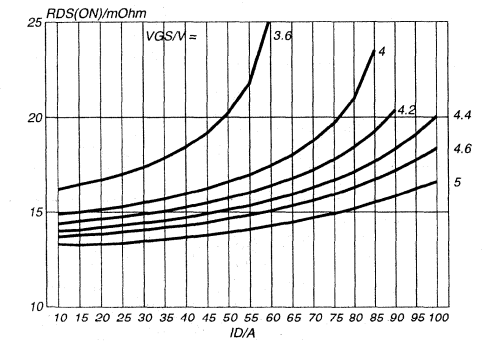


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

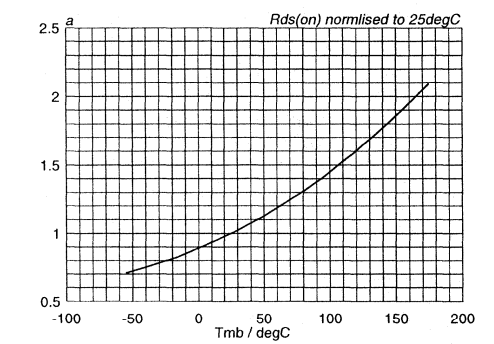


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,˚C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

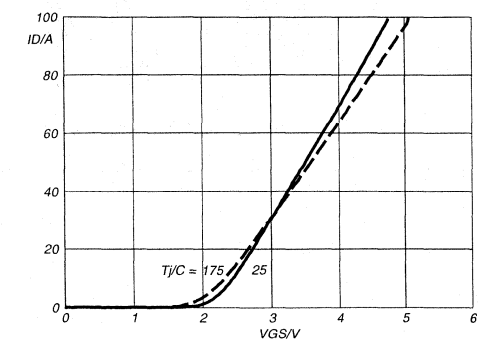


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

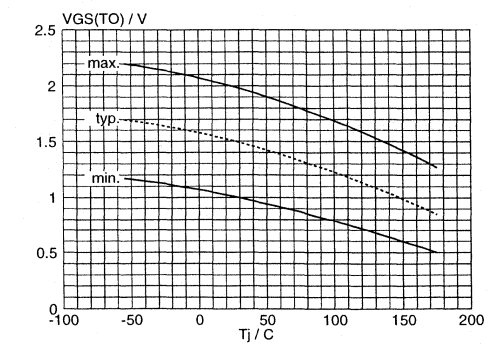


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

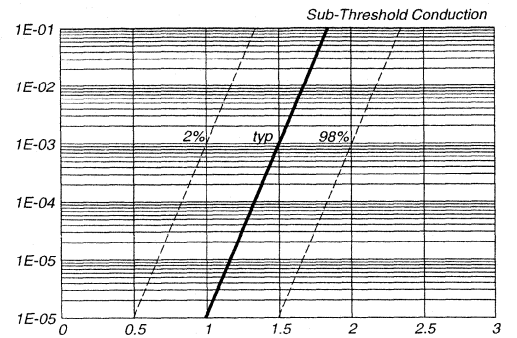


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; *conditions:* $T_j = 25$ °C; $V_{DS} = V_{GS}$

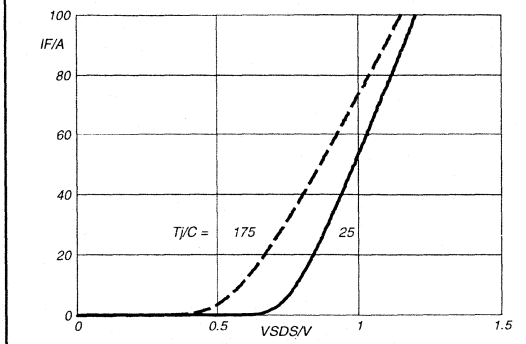


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; *conditions:* $V_{GS} = 0$ V; *parameter* T_j

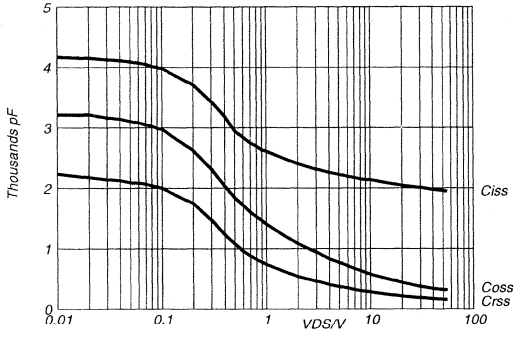


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; *conditions:* $V_{GS} = 0$ V; $f = 1$ MHz

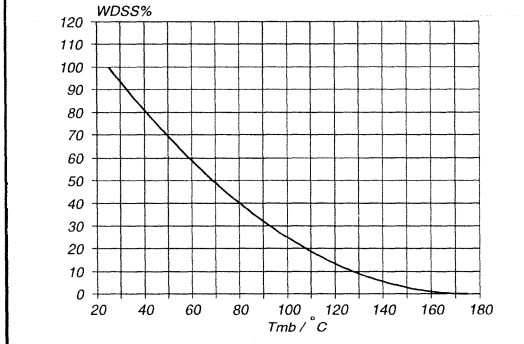


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; *conditions:* $I_D = 75$ A

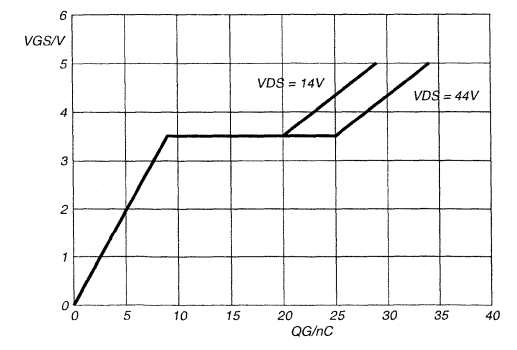


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; *conditions:* $I_D = 50$ A; *parameter* V_{DS}

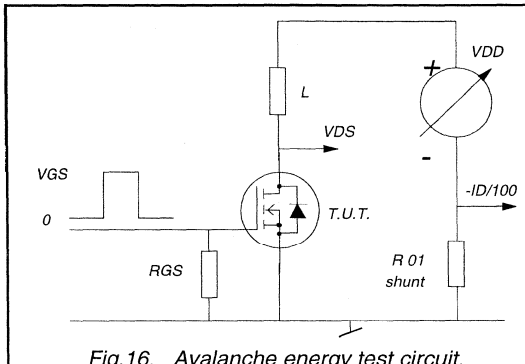


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

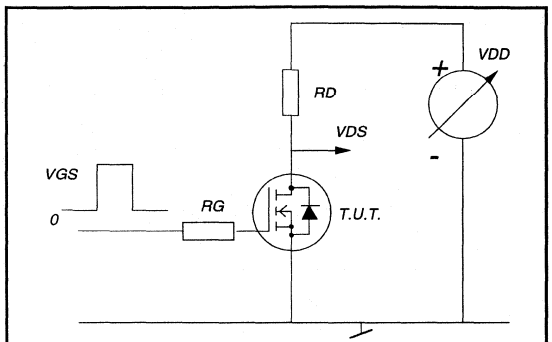


Fig.17. Switching test circuit.

TrenchMOS™ transistor Logic level FET

BUK9620-55

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting. Using '**trench**' technology the device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

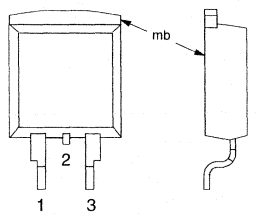
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	52	A
P_{tot}	Total power dissipation	116	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	20	mΩ

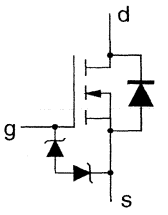
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	52	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	37	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	208	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	116	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.29	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	Minimum footprint, FR4 board	50	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	1.5	2	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-		10	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	15	20	mΩ
		T_j = 175˚C	-	-	42	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	20	-	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1800	2400	pF
C_{oss}	Output capacitance		-	350	420	pF
C_{rss}	Feedback capacitance		-	170	235	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	28	40	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω	-	110	160	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	95	135	ns
t_f	Turn-off fall time		-	70	90	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	52	A
I_{DRM}	Pulsed reverse drain current		-	-	208	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 40 A; V_{GS} = 0 V	-	1.0	-	
t_{rr}	Reverse recovery time	I_F = 40 A; -dI_F/dt = 100 A/µs;	-	47	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.15	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 45 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	110	mJ

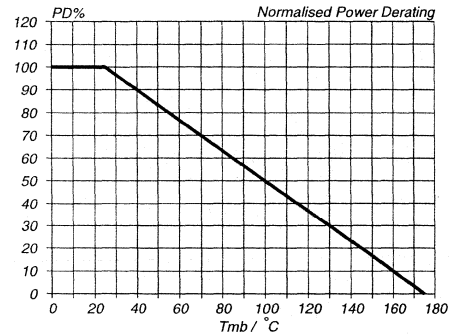


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

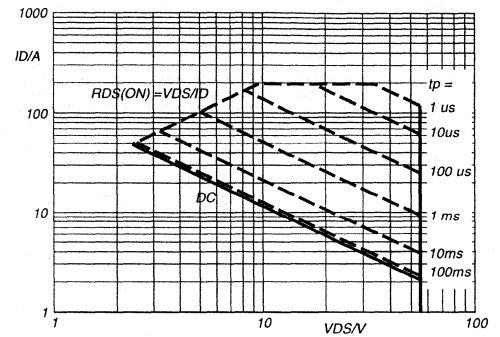


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

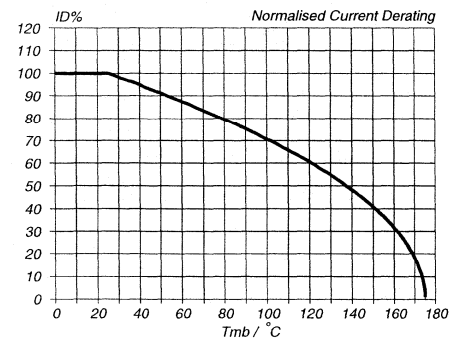


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

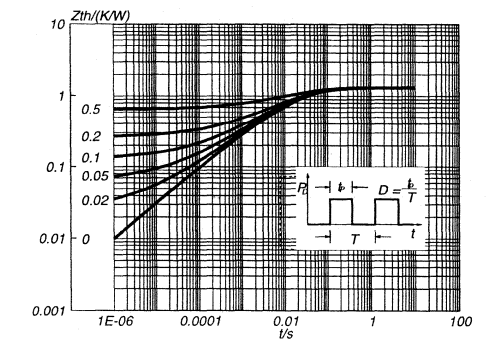


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

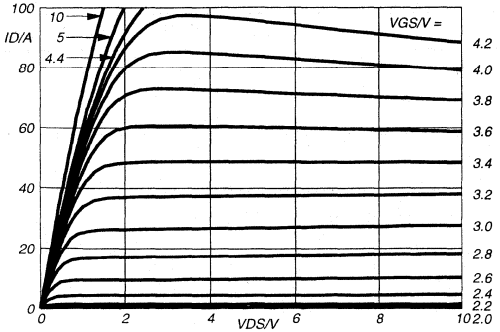


Fig.5. Typical output characteristics, T_j = 25 °C. $I_D = f(V_{DS})$; parameter V_{GS}

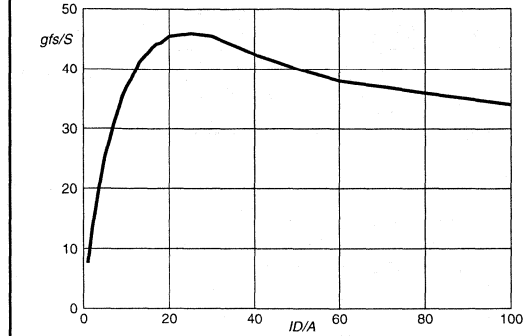


Fig.8. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

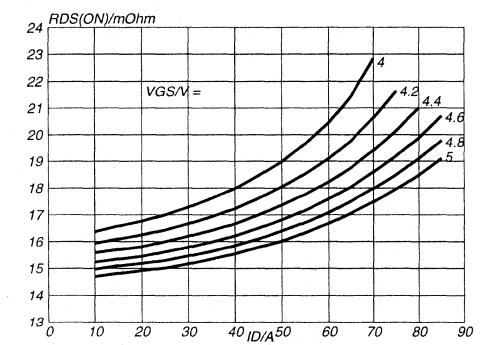


Fig.6. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

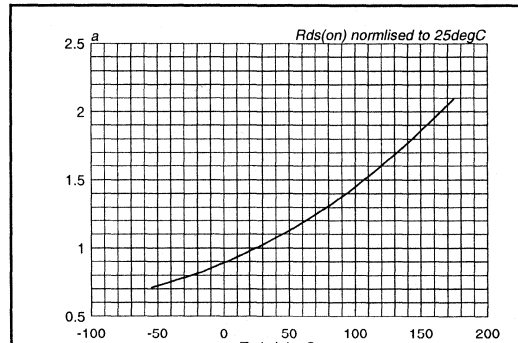


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

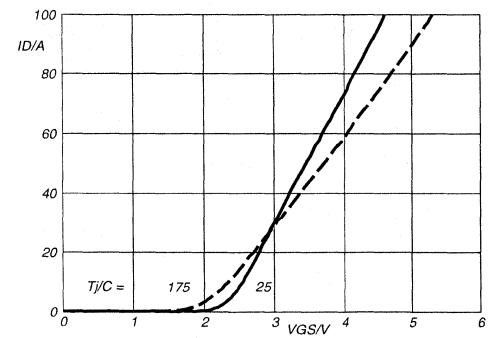


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

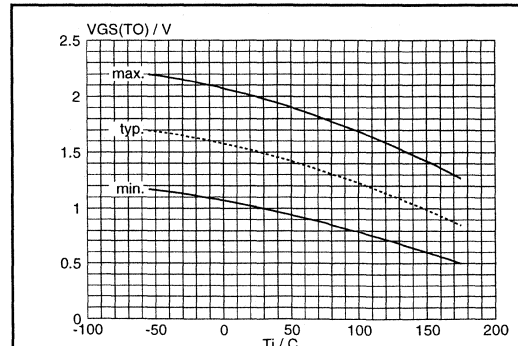


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

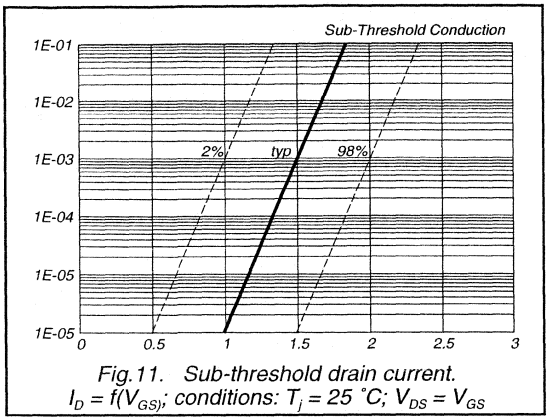


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

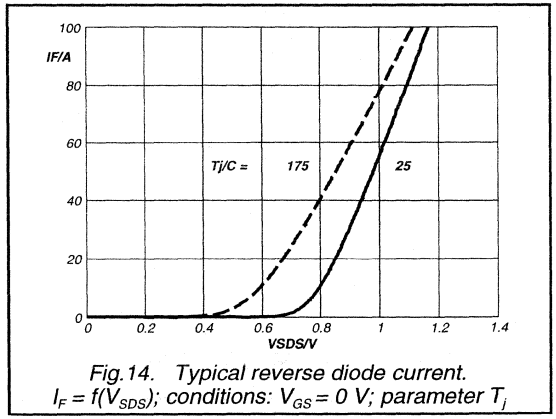


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

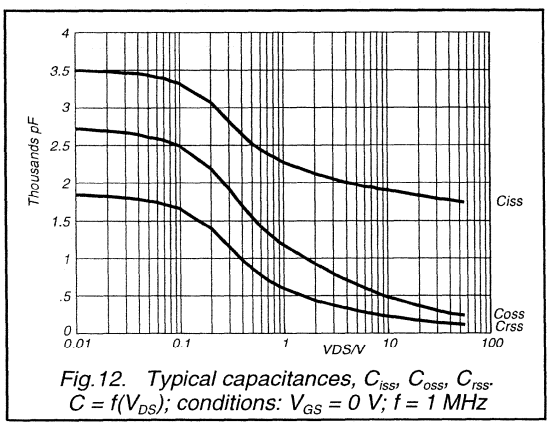


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; f = 1 MHz

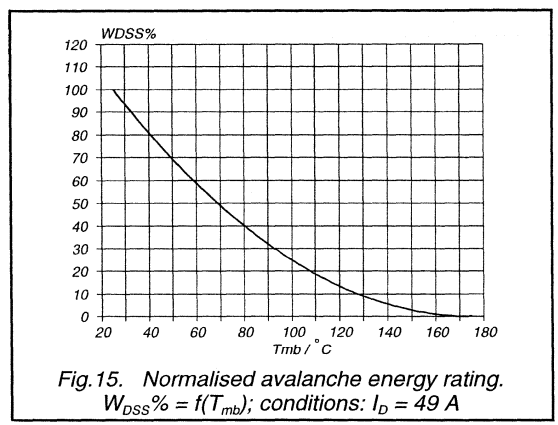


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 49$ A

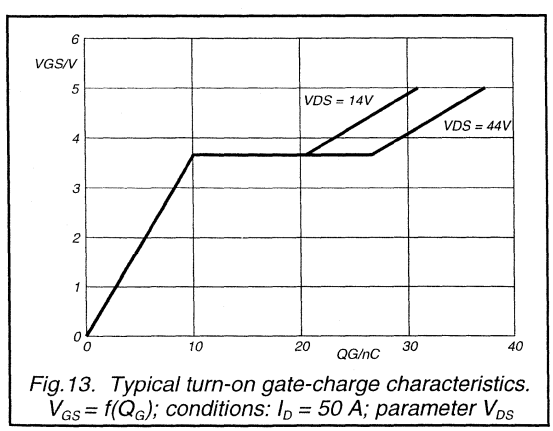


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 50$ A; parameter V_{DS}

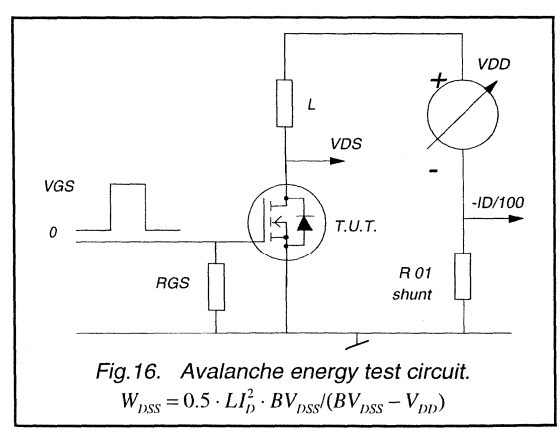


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

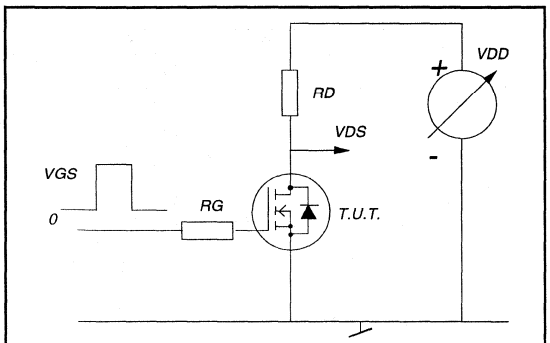


Fig.17. Switching test circuit.

TrenchMOS™ transistor Logic level FET

BUK9624-55

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting. Using '**trench**' technology the device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

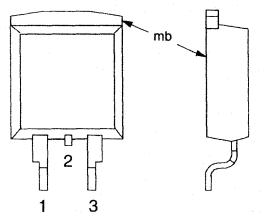
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	45	A
P_{tot}	Total power dissipation	103	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	24	mΩ

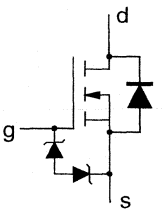
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	45	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	31	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	180	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	103	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.45	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	Minimum footprint, FR4 board	50	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	1.5	2	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-		10	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	19	24	mΩ
		T_j = 175˚C	-	-	50	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	15	40	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1500	2000	pF
C_{oss}	Output capacitance		-	300	360	pF
C_{rss}	Feedback capacitance		-	150	200	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	30	45	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω	-	80	130	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	95	135	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	45	A
I_{DRM}	Pulsed reverse drain current		-	-	160	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 40 A; V_{GS} = 0 V	-	1.0	-	
t_{rr}	Reverse recovery time	I_F = 40 A; -dI_F/dt = 100 A/µs;	-	40	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.07	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 40 A; $V_{DD} \leq$ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	80	mJ

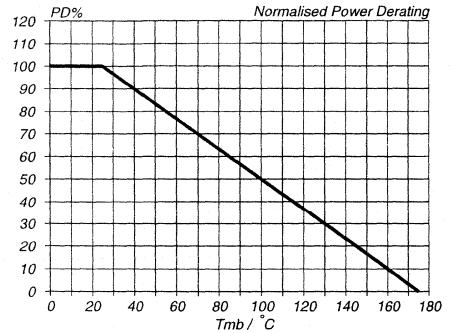


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

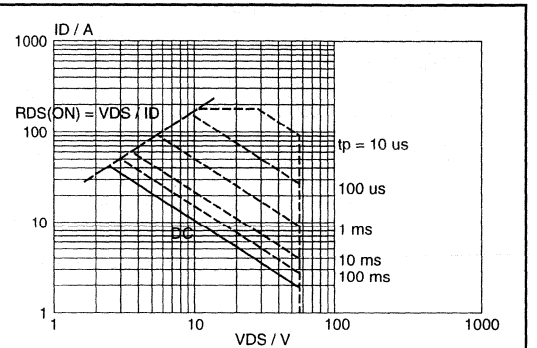


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

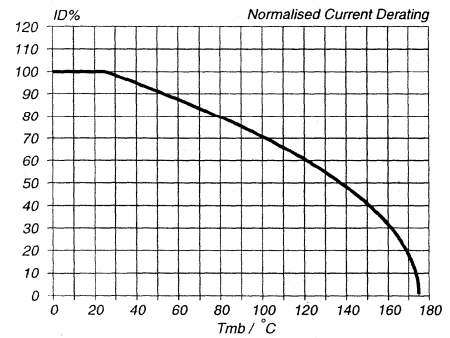


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

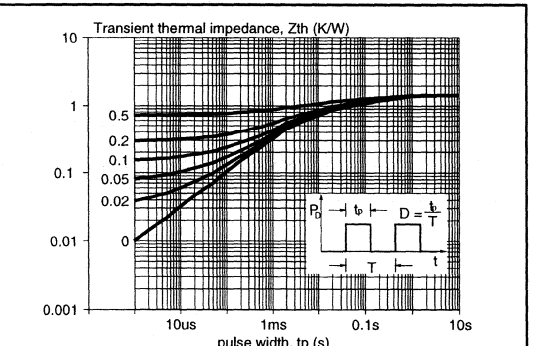


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

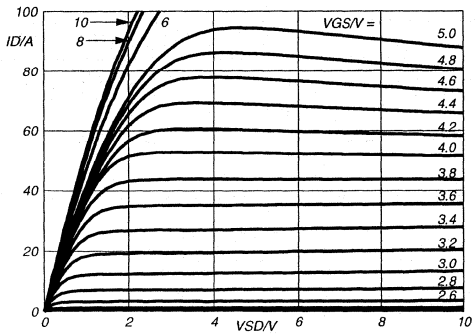


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

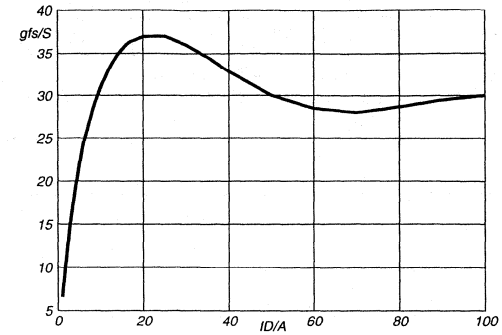


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

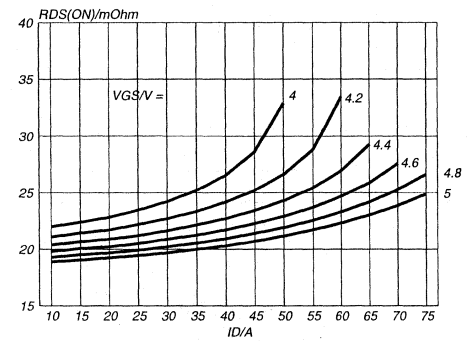


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

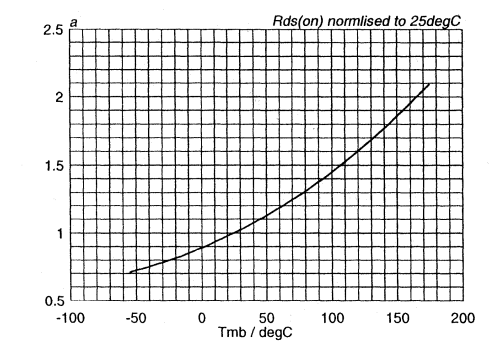


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\ ˚C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

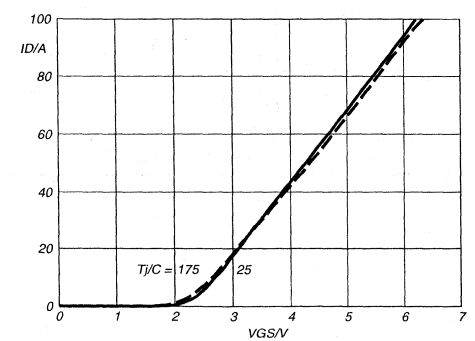


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

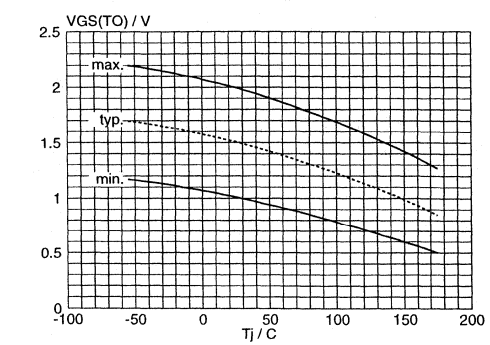


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

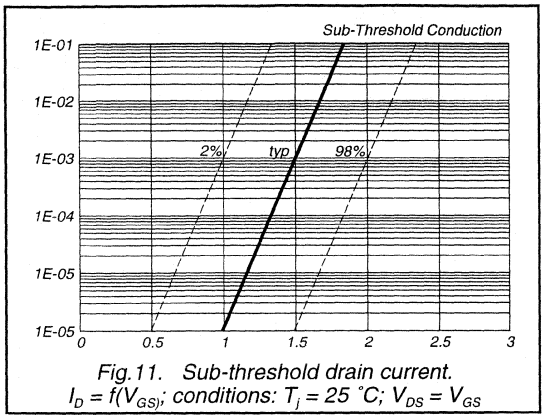


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

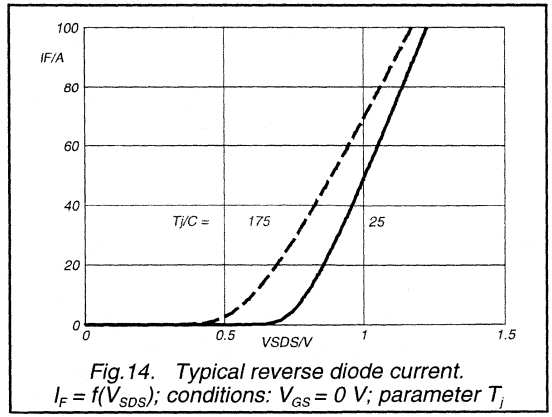


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

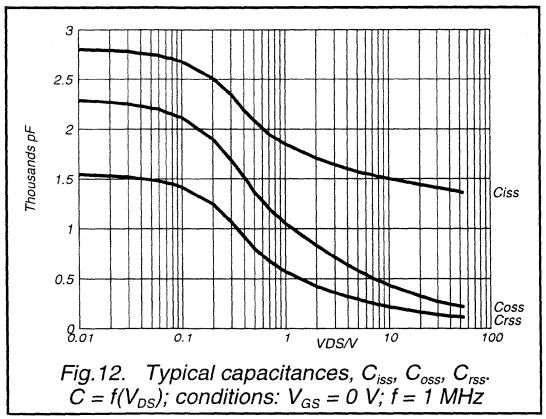


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

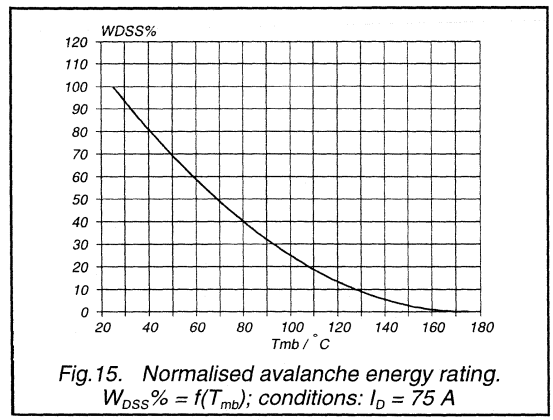


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: I_D = 75 A

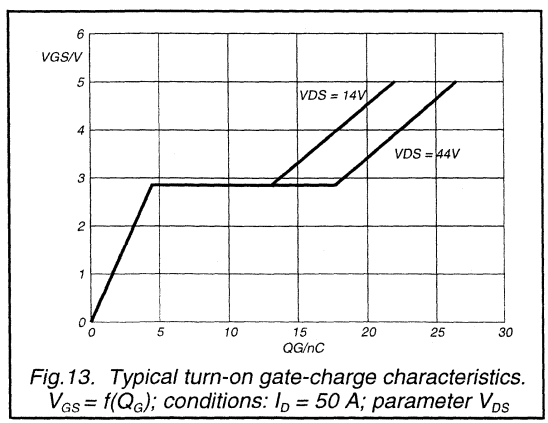


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 50 A; parameter V_{DS}

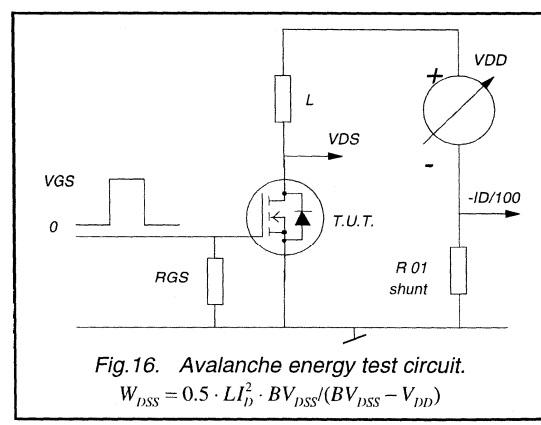


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

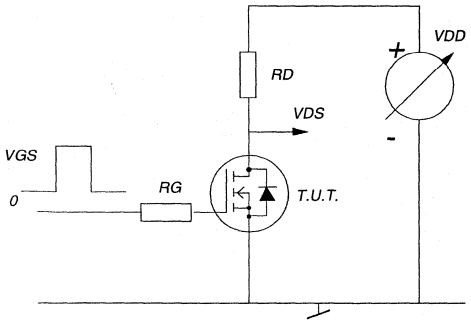


Fig.17. Switching test circuit.

TrenchMOS™ transistor Logic level FET

BUK9628-55

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting. Using '**trench**' technology the device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

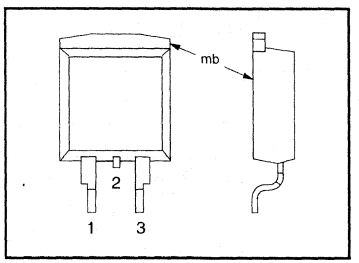
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	40	A
P_{tot}	Total power dissipation	96	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	28	mΩ

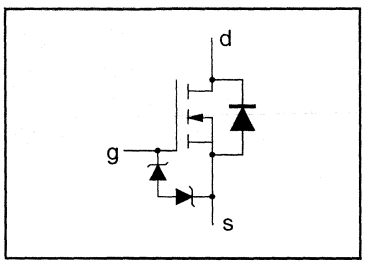
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	40	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	28	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	160	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	96	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.56	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	Minimum footprint, FR4 board	50	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	1.5	2	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-		10	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 20 A	-	22	28	mΩ
		T_j = 175˚C	-	-	59	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	13	-	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1300	1700	pF
C_{oss}	Output capacitance		-	250	300	pF
C_{rss}	Feedback capacitance		-	130	180	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	22	32	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω	-	85	125	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	70	95	ns
t_f	Turn-off fall time		-	64	85	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	40	A
I_{DRM}	Pulsed reverse drain current		-	-	160	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 40 A; V_{GS} = 0 V	-	1.0	-	
t_{rr}	Reverse recovery time	I_F = 40 A; -dI_F/dt = 100 A/µs;	-	41	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.16	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 35 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	70	mJ

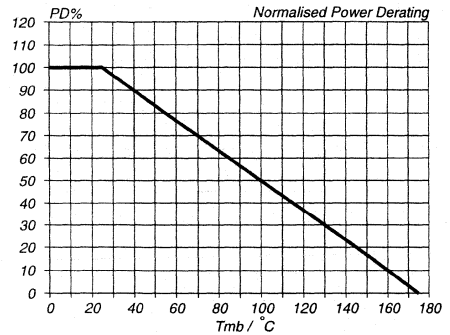


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

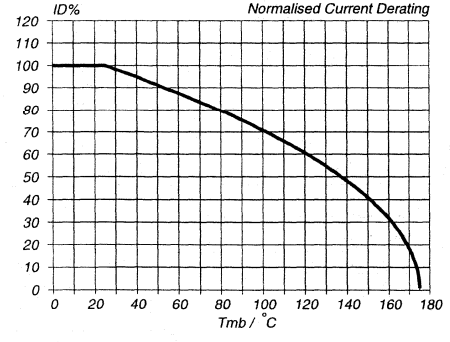


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

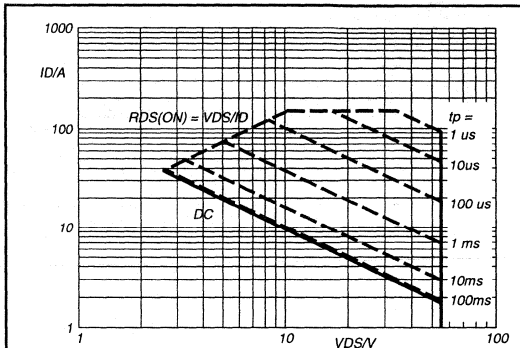


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

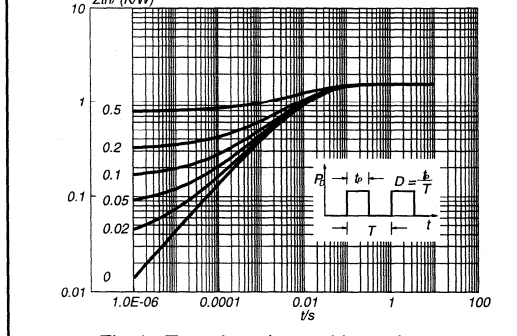


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

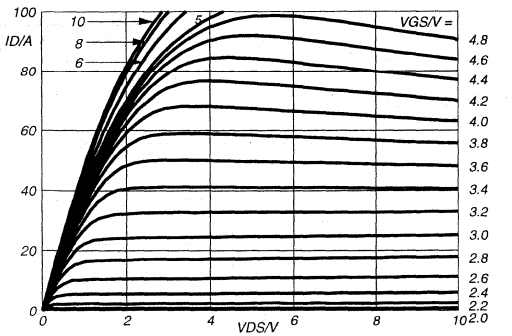


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

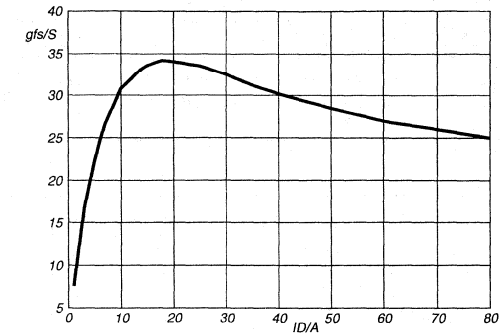


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

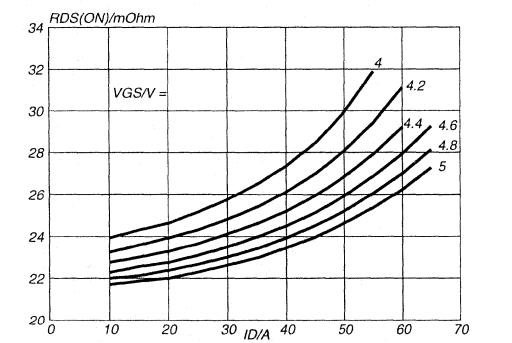


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

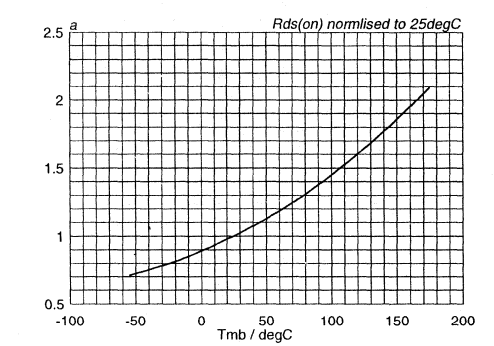


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,˚C} = f(T_j)$; I_D = 20 A; V_{GS} = 5 V

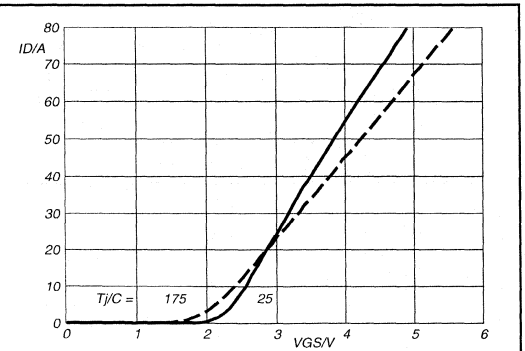


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

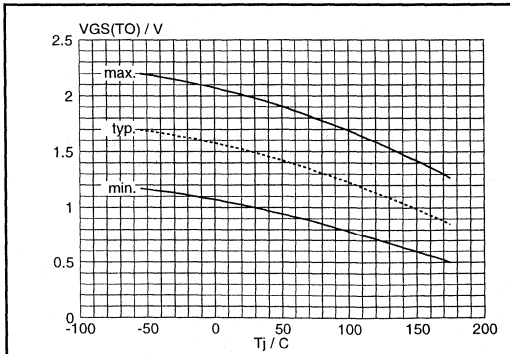


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

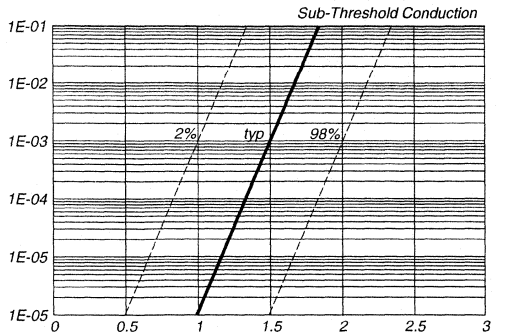


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; *conditions:* $T_j = 25$ °C; $V_{DS} = V_{GS}$

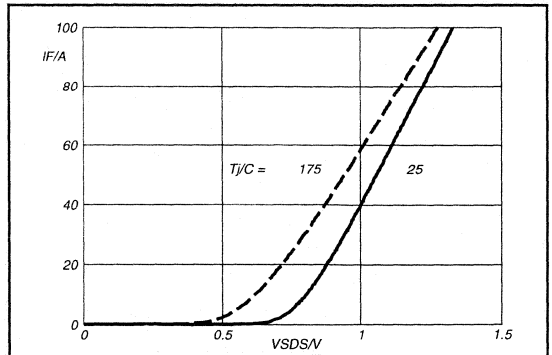


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; *conditions:* $V_{GS} = 0$ V; *parameter* T_j

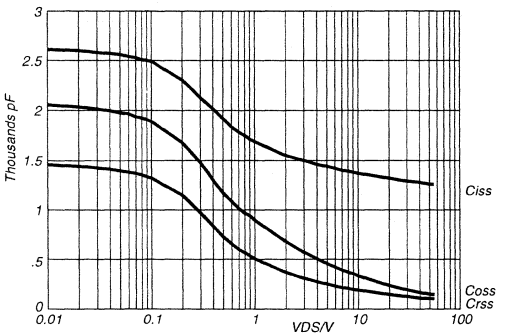


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; *conditions:* $V_{GS} = 0$ V; $f = 1$ MHz

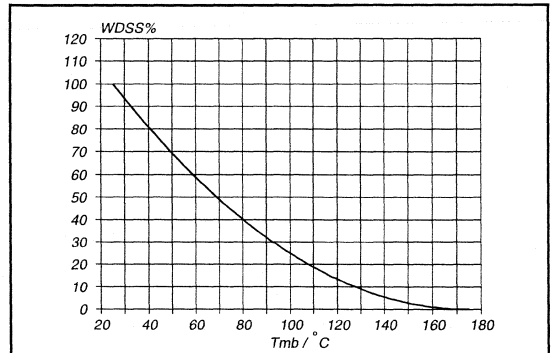


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; *conditions:* $I_D = 40$ A

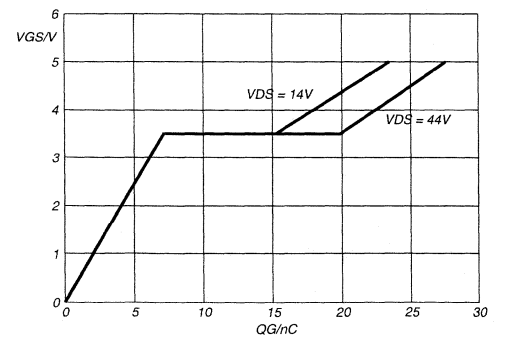


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; *conditions:* $I_D = 40$ A; *parameter* V_{DS}

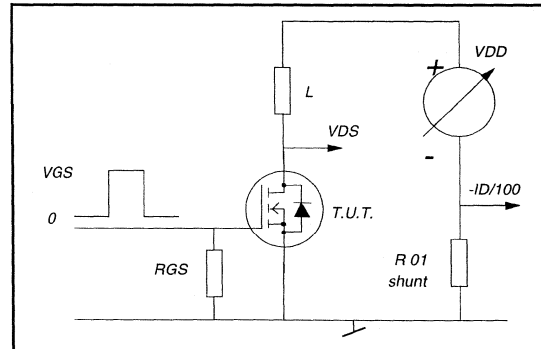


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

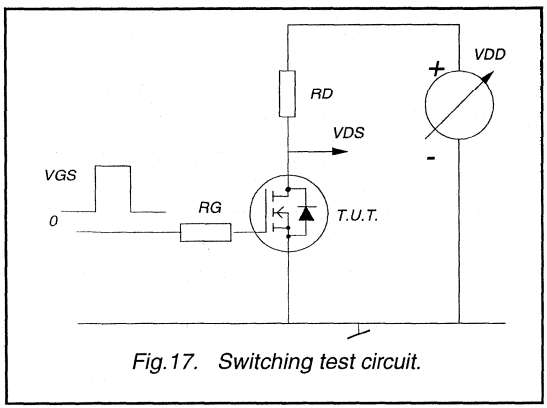


Fig.17. Switching test circuit.

TrenchMOS™ transistor Logic level FET

BUK9635-55

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting. Using '**trench**' technology the device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

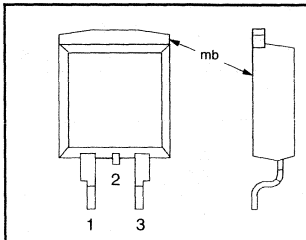
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	34	A
P_{tot}	Total power dissipation	85	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	35	mΩ

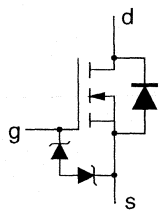
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	34	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	24	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	136	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	85	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.75	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	Minimum footprint, FR4 board	50	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;		55	-	-	V
			T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA		1	1.5	2	V
			T_j = 175˚C	0.5	-	-	V
			T_j = -55˚C	-	-	2.3	
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;		-	0.05	10	µA
			T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V		-	0.02	1	µA
			T_j = 175˚C	-		10	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;		10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 17 A		-	28	35	mΩ
			T_j = 175˚C	-	-	74	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 15 A	12	-	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1050	1400	pF
C_{oss}	Output capacitance		-	205	245	pF
C_{rss}	Feedback capacitance		-	110	150	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 15 A;	-	14	21	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω	-	77	110	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	55	80	ns
t_f	Turn-off fall time		-	48	65	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	34	A
I_{DRM}	Pulsed reverse drain current		-	-	136	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 34 A; V_{GS} = 0 V	-	1.0	-	
t_{rr}	Reverse recovery time	I_F = 34 A; -dI_F/dt = 100 A/µs;	-	40	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.16	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 20 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	45	mJ

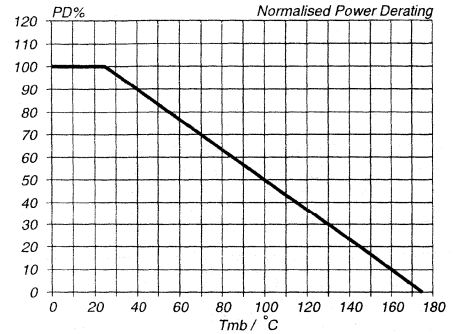


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

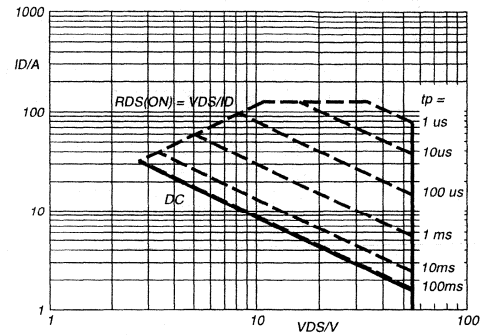


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

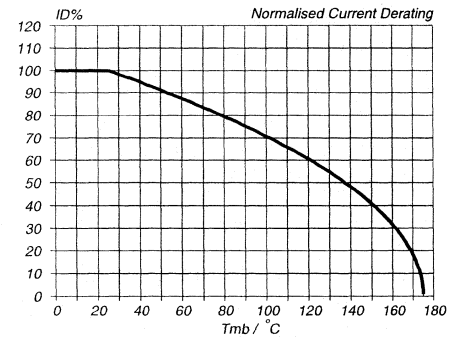


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

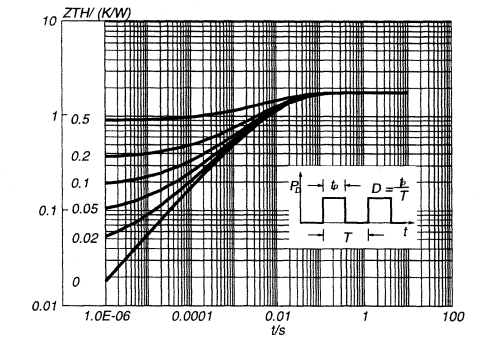


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

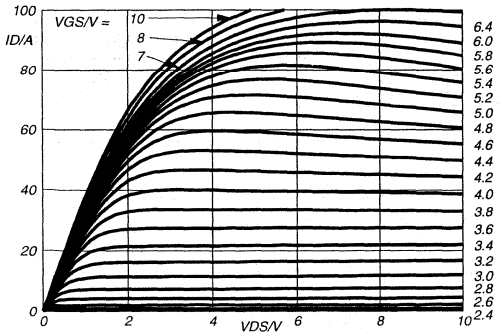


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

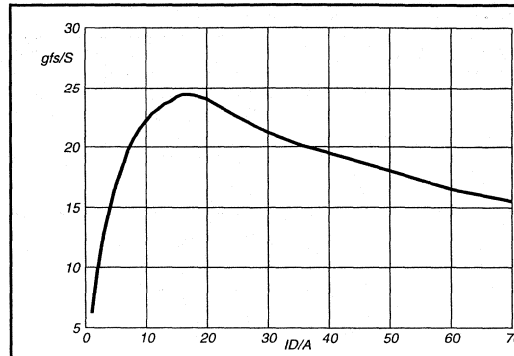


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

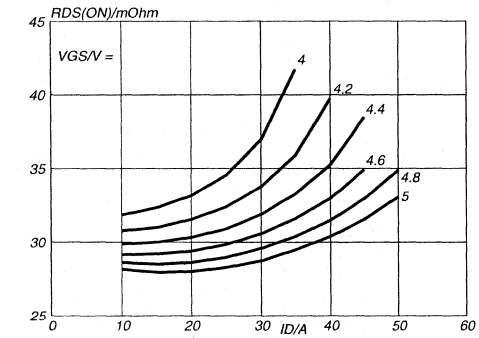


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

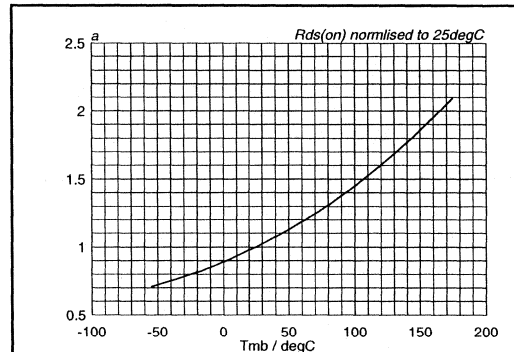


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 17 A; V_{GS} = 5 V

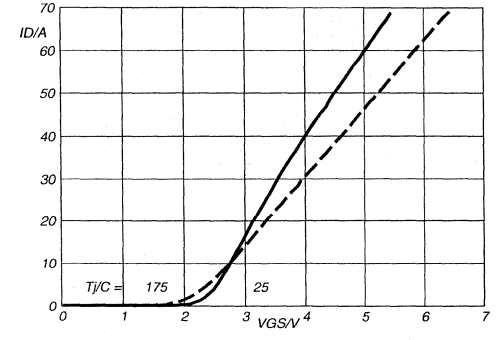


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

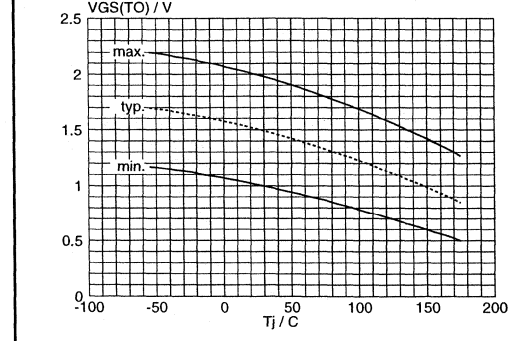


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

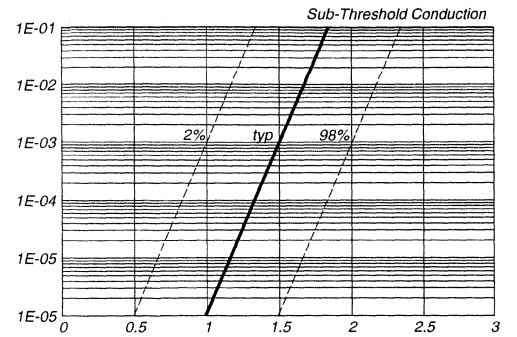


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; *conditions:* $T_j = 25$ °C; $V_{DS} = V_{GS}$

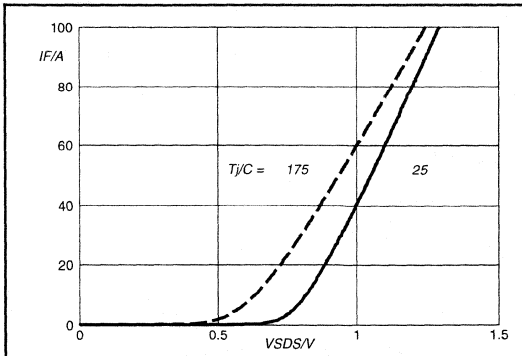


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; *conditions:* $V_{GS} = 0$ V; *parameter* T_j

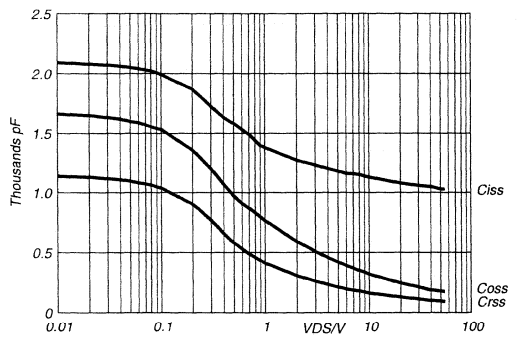


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; *conditions:* $V_{GS} = 0$ V; $f = 1$ MHz

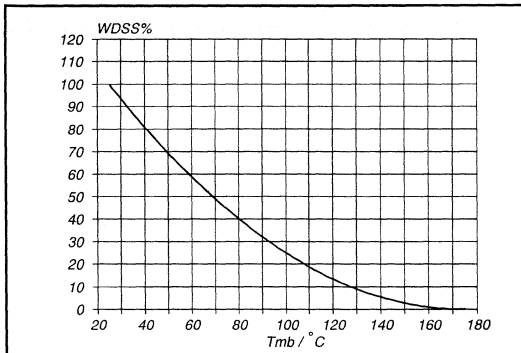


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; *conditions:* $I_D = 32$ A

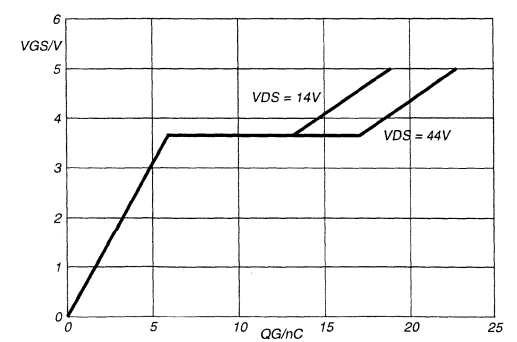


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; *conditions:* $I_D = 30$ A; *parameter* V_{DS}

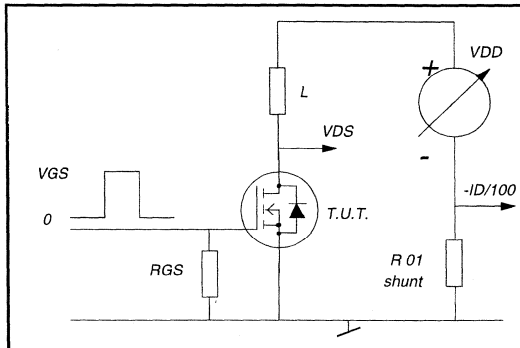


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

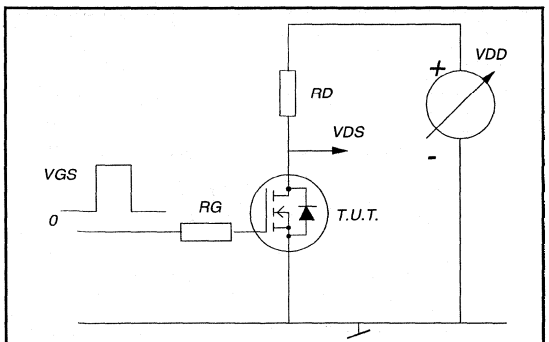


Fig.17. Switching test circuit.

TrenchMOS™ transistor Logic level FET

BUK9675-55

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting. Using '**trench**' technology the device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

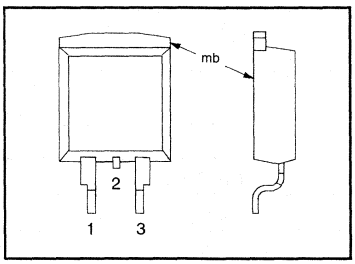
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	19.7	A
P_{tot}	Total power dissipation	61	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	75	mΩ

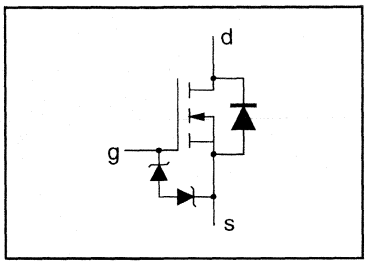
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	19.7	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	13.9	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	79	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	61	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	2.46	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	Minimum footprint, FR4 board	50	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	1.5	2	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-		10	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 10 A	-	60	75	mΩ
		T_j = 175˚C	-	-	157	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 10 A	5	-	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	500	650	pF
C_{oss}	Output capacitance		-	110	135	pF
C_{rss}	Feedback capacitance		-	60	85	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 10 A;	-	10	15	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω	-	47	70	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	28	40	ns
t_f	Turn-off fall time		-	33	45	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	19.7	A
I_{DRM}	Pulsed reverse drain current		-	-	79	A
V_{SD}	Diode forward voltage	I_F = 19.7 A; V_{GS} = 0 V	-	0.95	1.2	V
t_{rr}	Reverse recovery time	I_F = 19.7 A; -dI_F/dt = 100 A/µs;	-	32	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.12	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 10 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	30	mJ

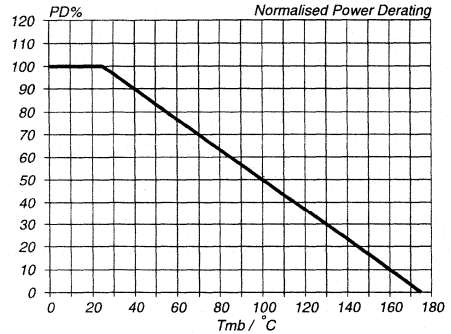


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

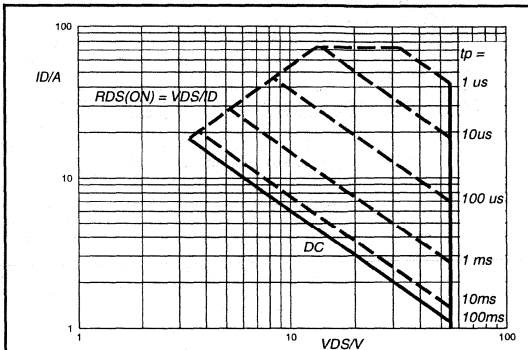


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

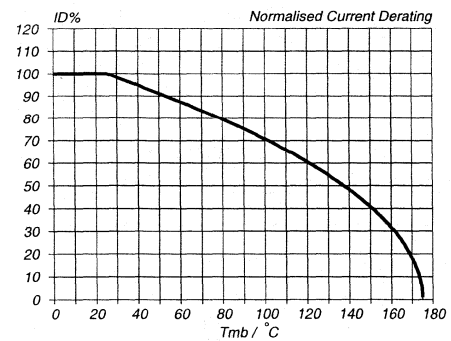


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

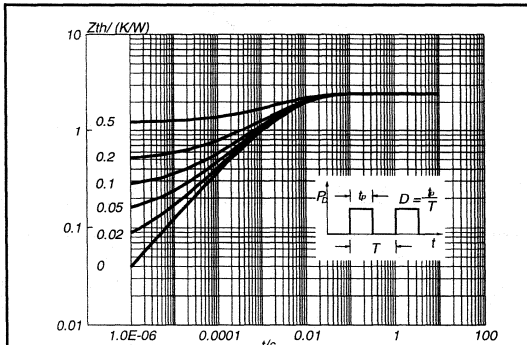


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

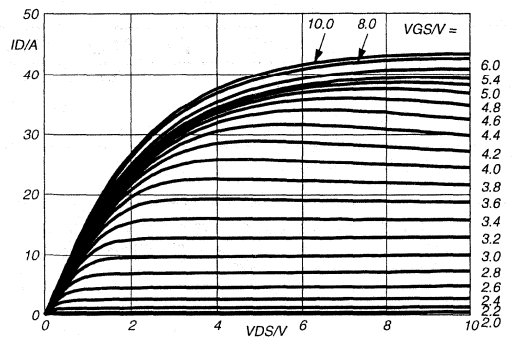


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

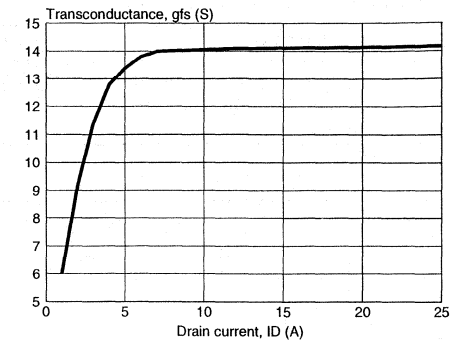


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

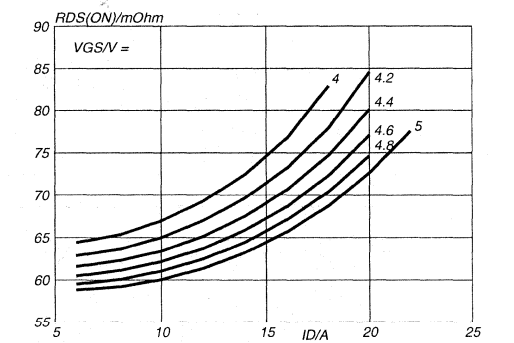


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

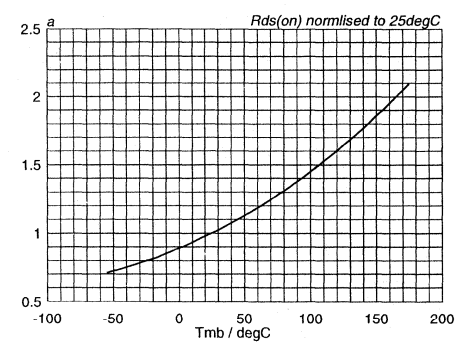


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,^{\circ}C} = f(T_j)$; I_D = 10 A; V_{GS} = 5 V

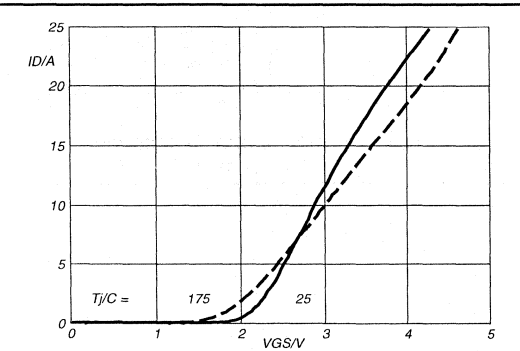


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

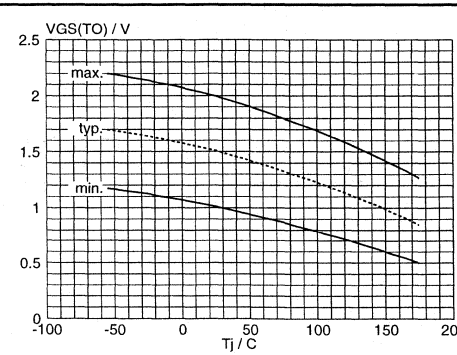


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

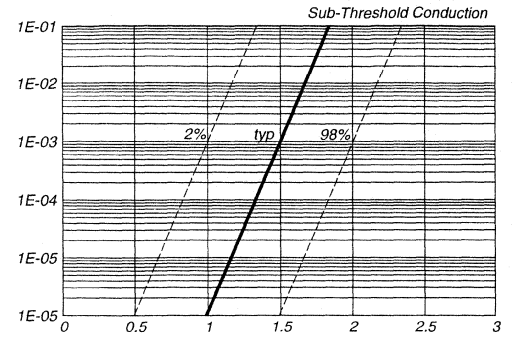


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

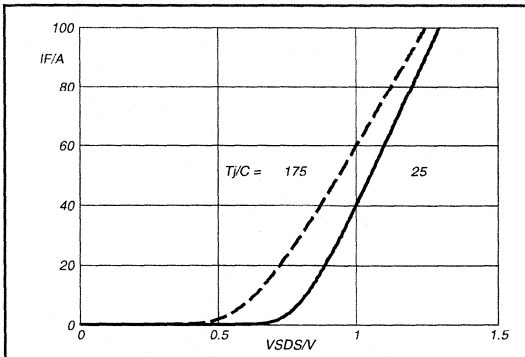


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

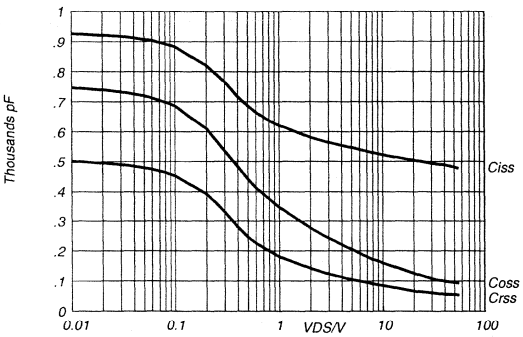


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

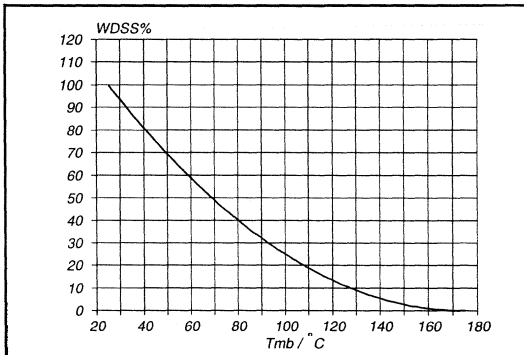


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 17$ A

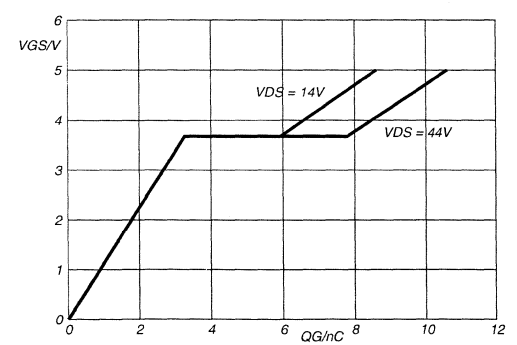


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 20$ A; parameter V_{DS}

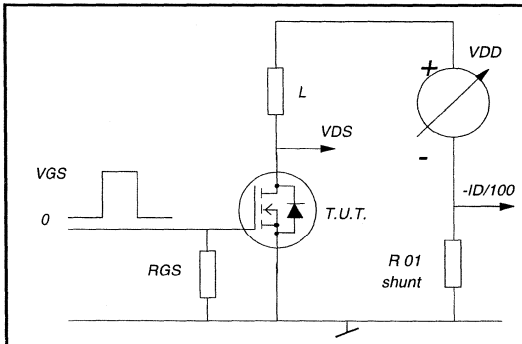


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

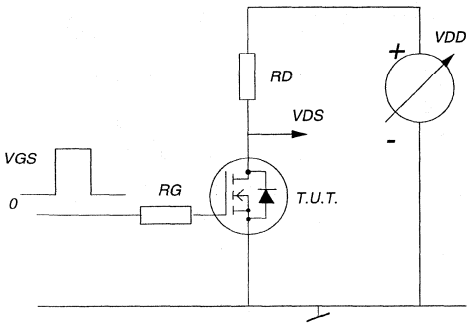


Fig.17. Switching test circuit.

TrenchMOS™ transistor Logic level FET

BUK9775-55

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic full-pack envelope using '**trench**' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

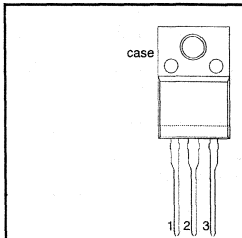
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	11.7	A
P_{tot}	Total power dissipation	19	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	75	mΩ

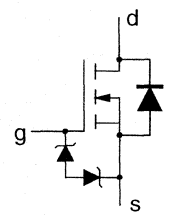
PINNING - SOT186A

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	11.7	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	7.4	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	47	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	19	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	150	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to heatsink	with heatsink compound	-	6.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	55	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	1.5	2	V
		T_j = 150˚C	0.6	-	-	V
		T_j = -55˚C	-	-	2.3	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 150˚C	-	-	100	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 150˚C	-		5	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 7 A	-	58	75	mΩ
		T_j = 150˚C	-	-	139	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 10 A	5	10	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	500	650	pF
C_{oss}	Output capacitance		-	110	135	pF
C_{rss}	Feedback capacitance		-	60	85	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 10 A;	-	10	15	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω	-	47	70	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	28	40	ns
t_f	Turn-off fall time		-	33	45	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{ISOL}	R.M.S isolation voltage from all three terminals to external heatsink	f = 50-60Hz; sinusoidal waveform; R.H.≤65% clean & dustfree	-	-	2500	V
C_{ISOL}	Capacitance from T2 to external heatsink	f = 1 MHZ	-	10	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	11.7	A
I_{DRM}	Pulsed reverse drain current		-	-	47	A
V_{SD}	Diode forward voltage	I_F = 11.7 A; V_{GS} = 0 V	-	0.95	1.2	V
t_{rr}	Reverse recovery time	I_F = 11.7 A; -dI_F/dt = 100 A/µs;	-	32	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.12	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 10 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	30	mJ

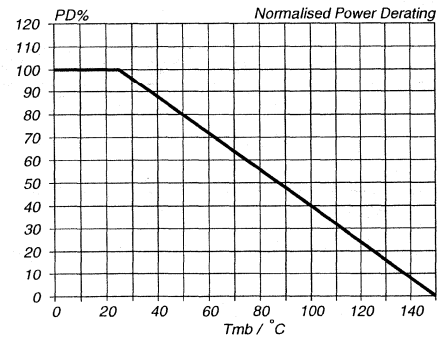


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

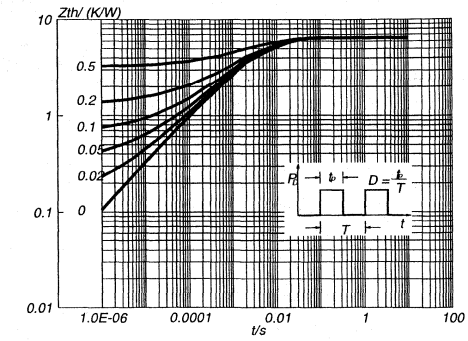


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

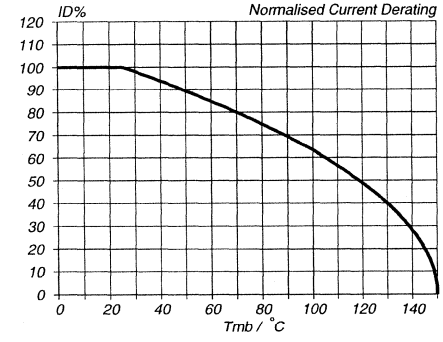


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 5 V

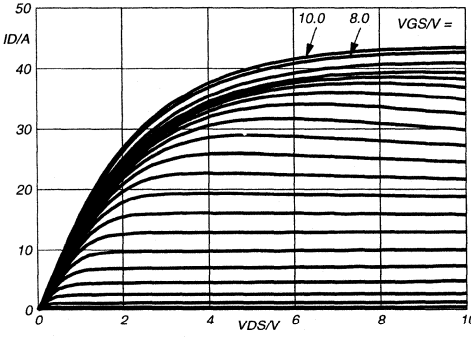


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

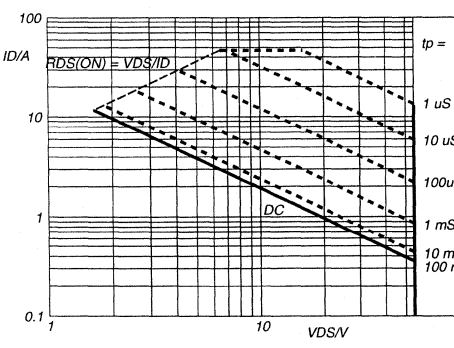


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

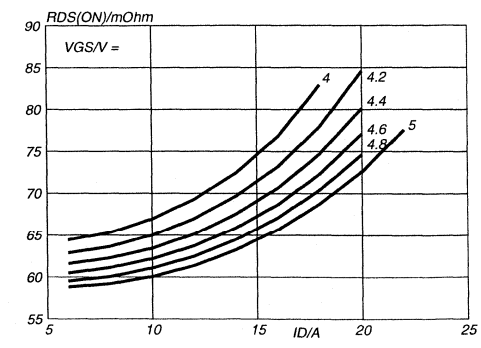


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

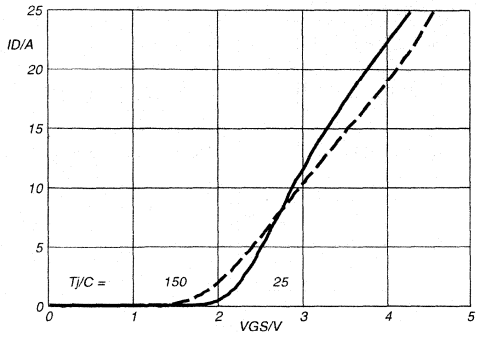


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

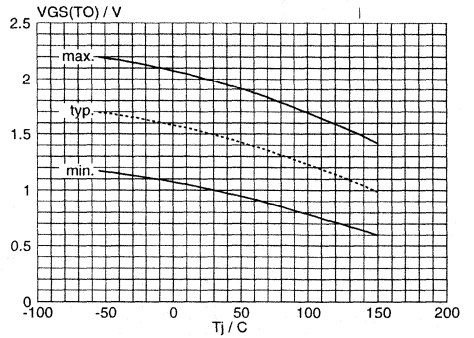


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

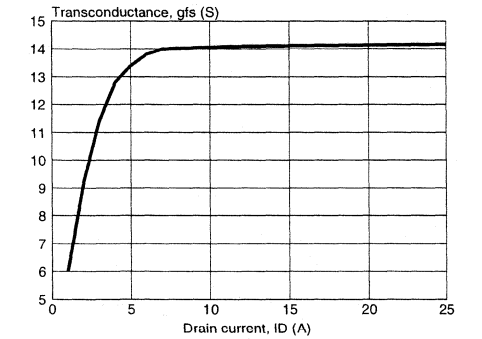


Fig.8. Typical transconductance, $T_j = 25$ °C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

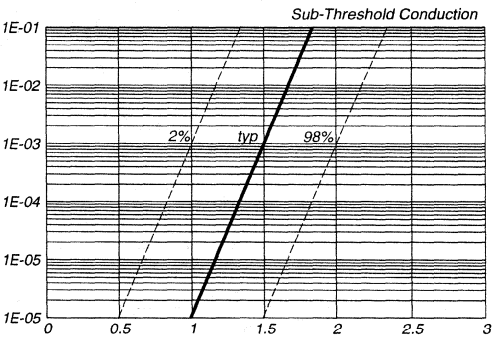


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

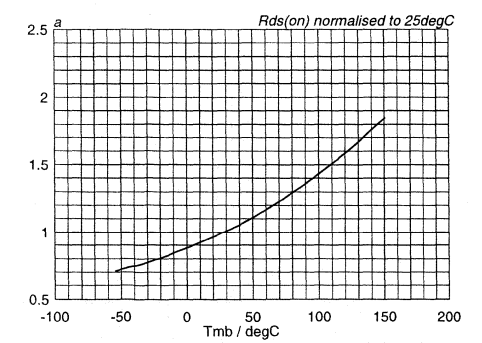


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 10$ A; $V_{GS} = 5$ V

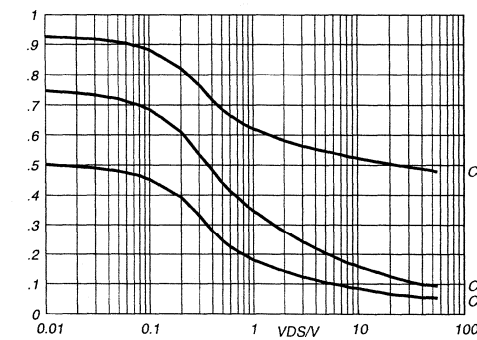


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

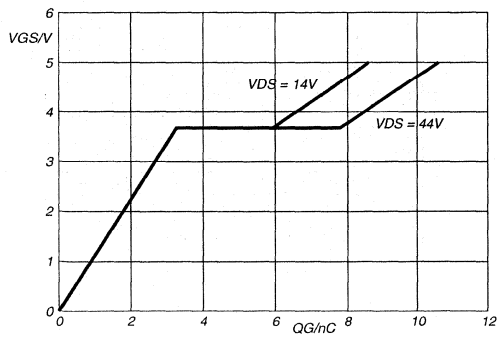


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 20$ A; parameter V_{DS}

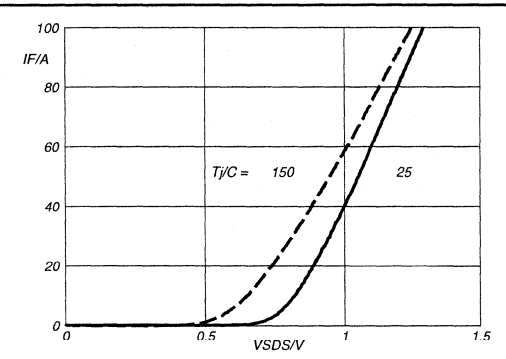


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

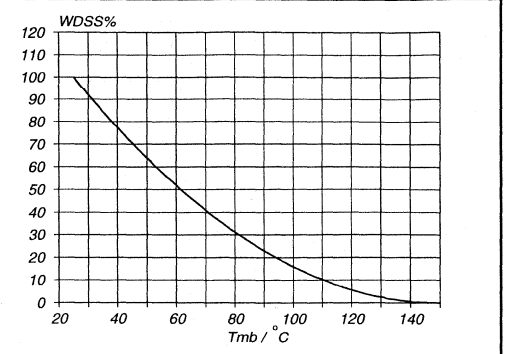


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 17$ A

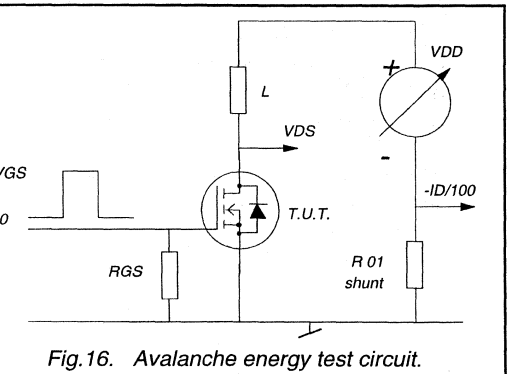


Fig.16. Avalanche energy test circuit.
$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

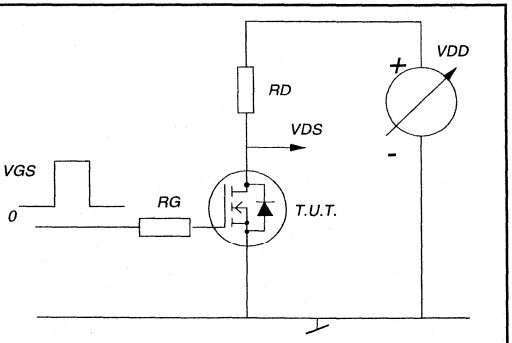


Fig.17. Switching test circuit.

TrenchMOS™ transistor Logic level FET

BUK9830-30

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting. Using **'trench'** technology, the device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

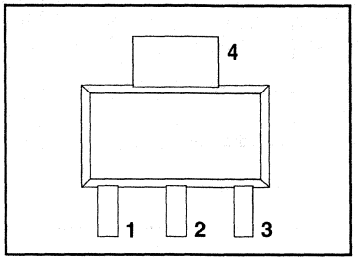
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	30	V
I_D	Drain current (DC) T_{sp} = 25 °C	12.8	A
	Drain current (DC) T_{amb} = 25 °C	5.9	A
P_{tot}	Total power dissipation	8.3	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	30	mΩ

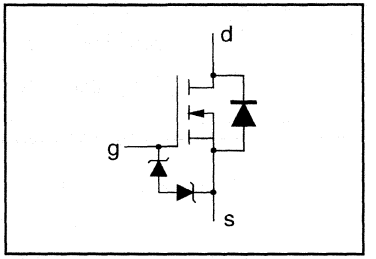
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	30	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	30	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{sp} = 25 °C	-	12.8	A
		T_{amb} = 25 °C	-	5.9	A
I_D	Drain current (DC)	T_{sp} = 100 °C	-	9	A
		T_{amb} = 100 °C	-	4.1	A
I_{DM}	Drain current (pulse peak value)	T_{sp} = 25 °C	-	51	A
		T_{amb} = 25 °C	-	23.6	A
P_{tot}	Total power dissipation	T_{sp} = 25 °C	-	8.3	W
		T_{amb} = 25 °C	-	1.8	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}sp}$	Thermal resistance junction to solder point	Mounted on any PCB	12	15	K/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction to ambient	Mounted on PCB of Fig.19	-	70	K/W

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	30	-	-	V
		T_j = -55˚C	27	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	1.5	2	V
		T_j = 150˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	
I_{DSS}	Zero gate voltage drain current	V_{DS} = 30 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 150˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 150˚C	-		10	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 3.2 A	-	24	30	mΩ
		T_j = 150˚C	-	-	51	mΩ

DYNAMIC CHARACTERISTICS

T_{sp} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5.9 A	7	14	-	S
$Q_{g(tot)}$	Total gate charge	I_D = 5.9 A; V_{DD} = 24 V; V_{GS} = 5 V	-	24	-	nC
Q_{gs}	Gate-source charge		-	3	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	11	-	nC
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1050	-	pF
C_{oss}	Output capacitance		-	270	-	pF
C_{rss}	Feedback capacitance		-	140	-	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 15 V; I_D = 5.9 A;	-	30	45	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 5 Ω	-	80	130	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	95	135	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	40	A
I_{DRM}	Pulsed reverse drain current		-	-	160	A
V_{SD}	Diode forward voltage	I_F = 3.2 A; V_{GS} = 0 V	-	0.75	1.2	V
		I_F = 5.9 A; V_{GS} = 0 V	-	0.85	-	
t_{rr}	Reverse recovery time	I_F = 5.9 A; -dI_F/dt = 100 A/µs;	-	100	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 25 V	-	0.4	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 5.9 A; $V_{DD} \leq$ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{sp} = 25 ˚C	-	-	60	mJ

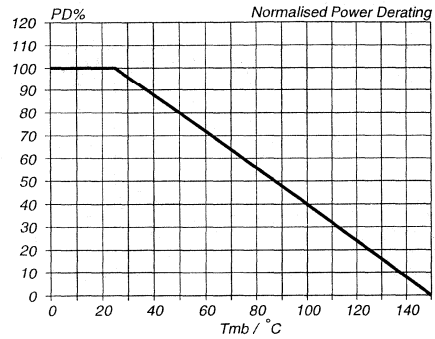


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

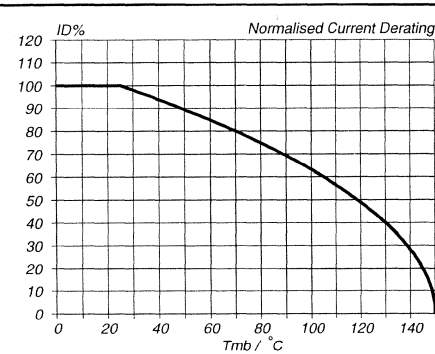


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq 5$ V

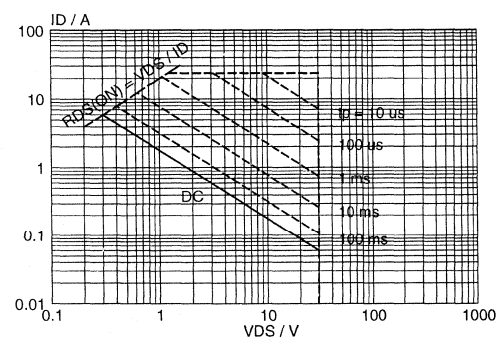


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

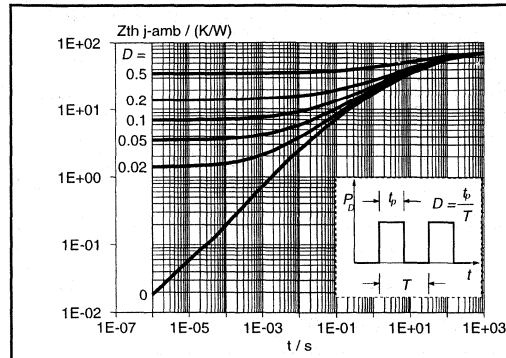


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

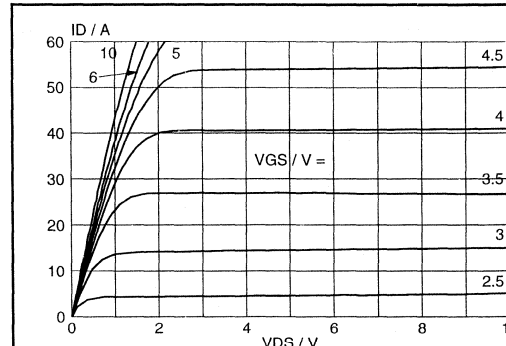


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

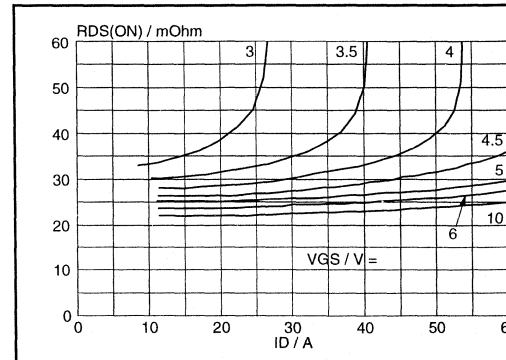


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

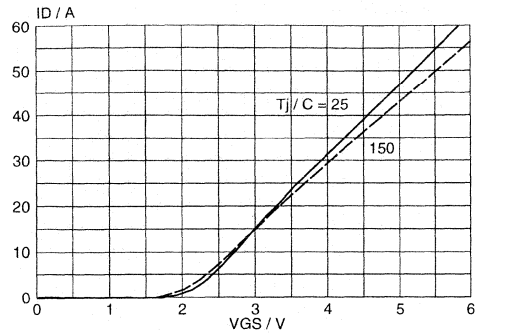


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

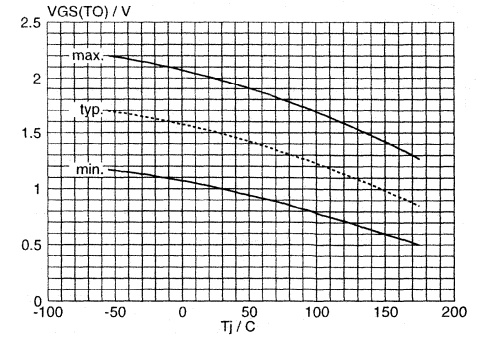


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

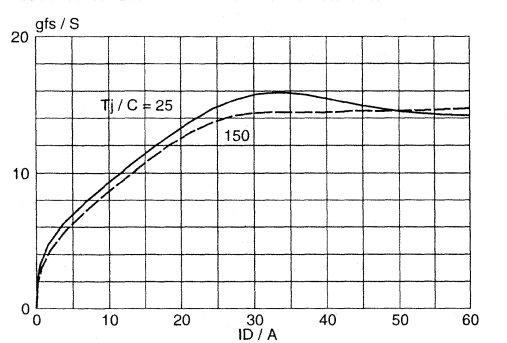


Fig.8. Typical transconductance, T_j = 25 ˚C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

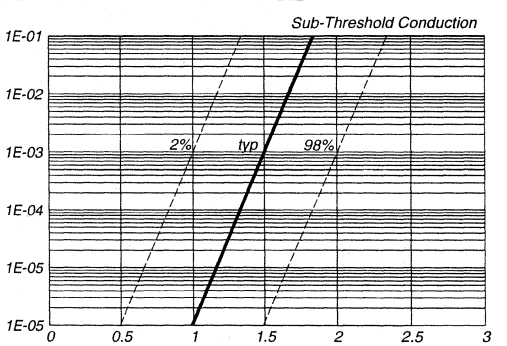


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

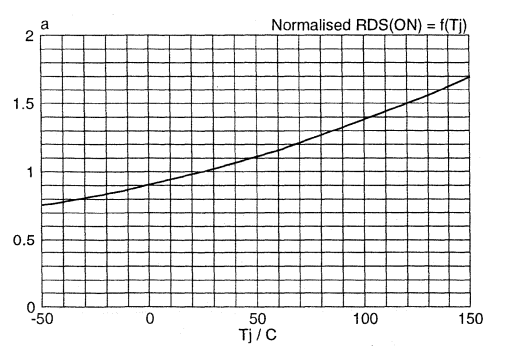


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 3.2 A; V_{GS} = 5 V

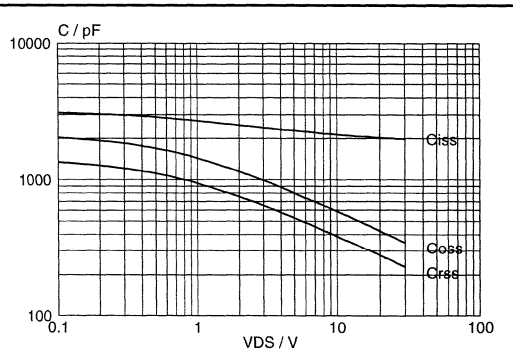


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

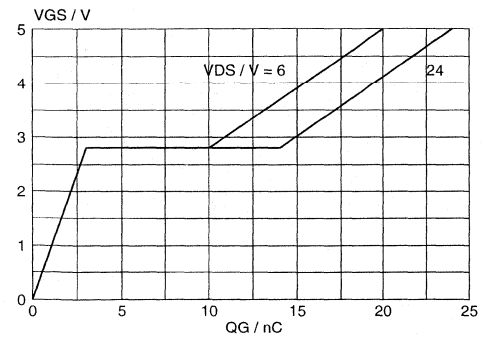


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 5.9$ A; parameter V_{DS}

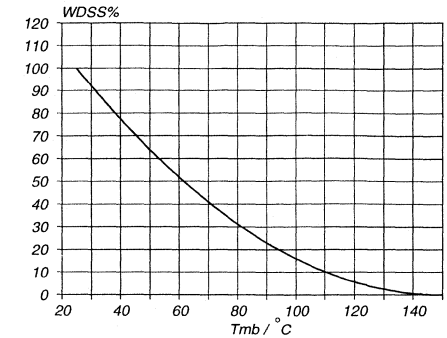


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 5.9$ A

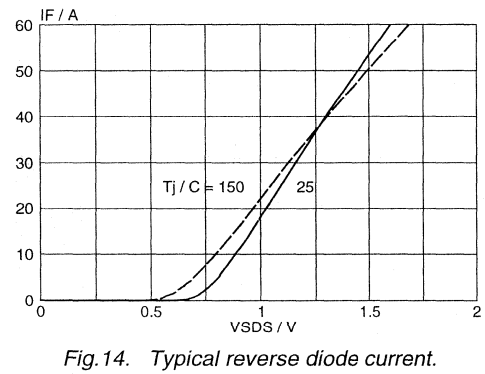


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

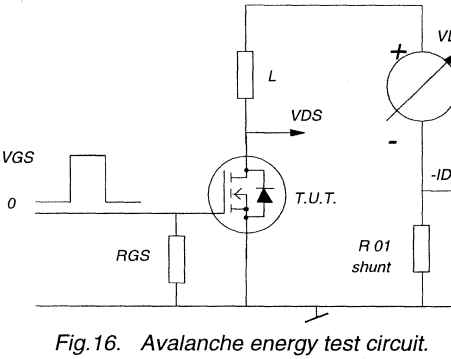


Fig.16. Avalanche energy test circuit.
$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

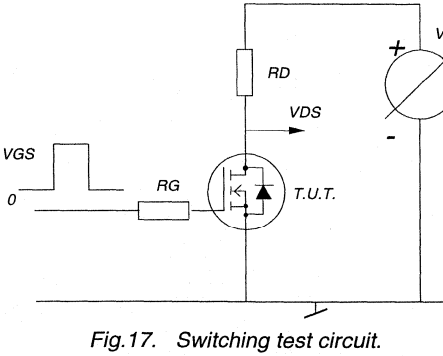


Fig.17. Switching test circuit.

MOUNTING INSTRUCTIONS

Dimensions in mm.

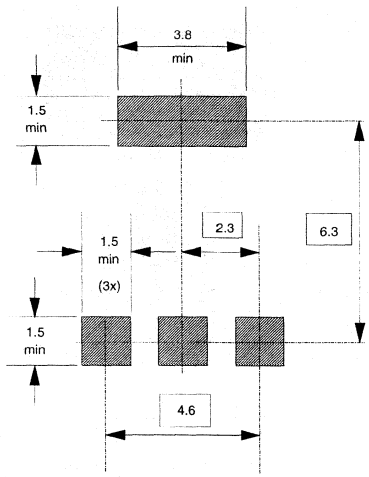


Fig.18. soldering pattern for surface mounting SOT223.

PRINTED CIRCUIT BOARD

Dimensions in mm.

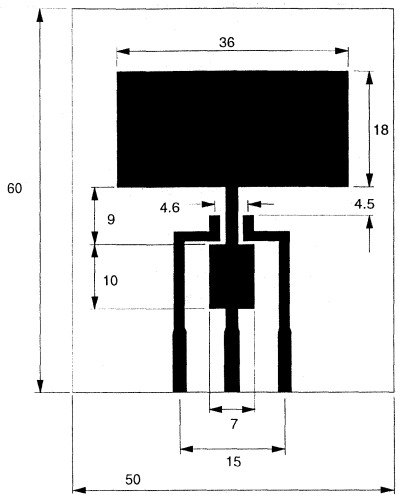


Fig.19. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).

TrenchMOS™ transistor Logic level FET

BUK9840-55

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting. The device features very low on-state resistance and has integral zener diodes giving ESD protection. It is intended for use in automotive and general purpose switching applications.

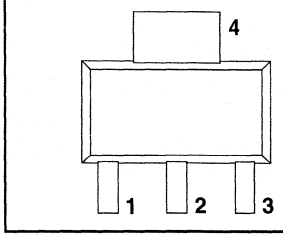
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current	10.7	A
P_{tot}	Total power dissipation	1.8	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	40	mΩ

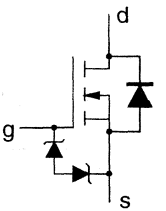
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{sp} = 25 °C	-	10.7	A
I_D	Drain current (DC)	On PCB in Fig.19 T_{amb} = 25 °C	-	5	A
I_D	Drain current (DC)	On PCB in Fig.19 T_{amb} = 100 °C	-	3.1	A
I_{DM}	Drain current (pulse peak value)	T_{sp} = 25 °C	-	40	A
P_{tot}	Total power dissipation	T_{sp} = 25 °C	-	8.3	W
P_{tot}	Total power dissipation	On PCB in Fig.19 T_{amb} = 25 °C	-	1.8	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	150	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}sp}$	From junction to solder point	Mounted on any PCB	12	15	K/W
$R_{th\ j\text{-}amb}$	From junction to ambient	Mounted on PCB of Fig.18	-	70	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
		T_j = 150˚C	0.6	-	-	V
		T_j = -55˚C	-	-	2.3	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 150˚C	-	-	100	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V	-	0.02	1	µA
		T_j = 150˚C	-	-	5	µA
$\pm V_{(BR)GSS}$	Gate source breakdown voltage	I_G = ±1 mA	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 5 A	-	30	40	mΩ
		T_j = 150˚C	-	-	74	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5 A; T_j = 25˚C	11	19	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1050	1400	pF
C_{oss}	Output capacitance		-	205	245	pF
C_{rss}	Feedback capacitance		-	110	150	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 9 A;	-	17	25	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω;	-	65	100	ns
$t_{d\ off}$	Turn-off delay time		-	70	105	ns
t_f	Turn-off fall time	T_j = 25˚C	-	70	105	ns

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = -55 to 175˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{sp} = 25˚C	-	-	10.7	A
I_{DRM}	Pulsed reverse drain current	T_{sp} = 25˚C	-	-	40	A
V_{SD}	Diode forward voltage	I_F = 5 A; V_{GS} = 0 V	-	0.85	1.1	V
t_{rr}	Reverse recovery time	I_F = 5 A; -dI_F/dt = 100 A/µs;	-	45	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	.3	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 3.6 A; $V_{DD} \leq 25$ V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{sp} = 25 °C	-	-	60	mJ

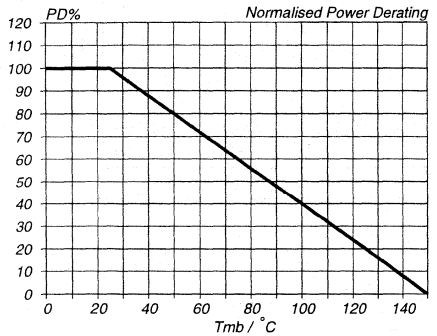


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{sp})

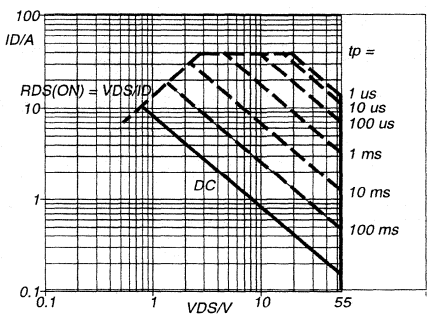


Fig.3. Safe operating area. T_{sp} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

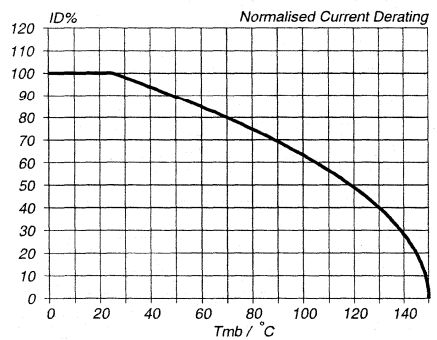


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{sp}); conditions: $V_{GS} \geq 5$ V

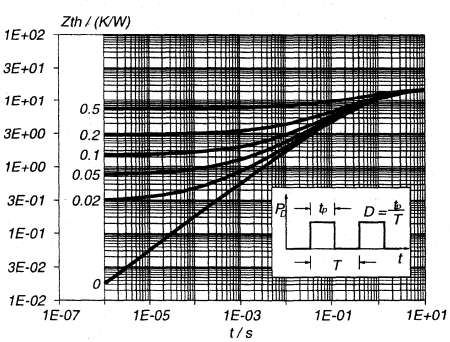


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}sp}$ = f(t); parameter D = t_p/T

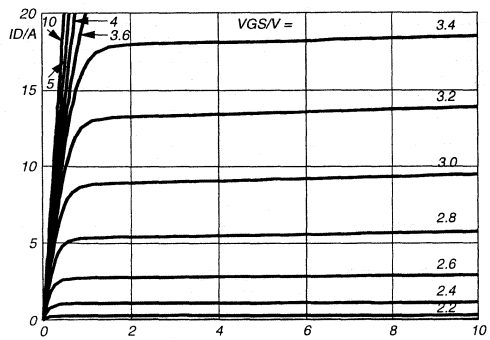


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

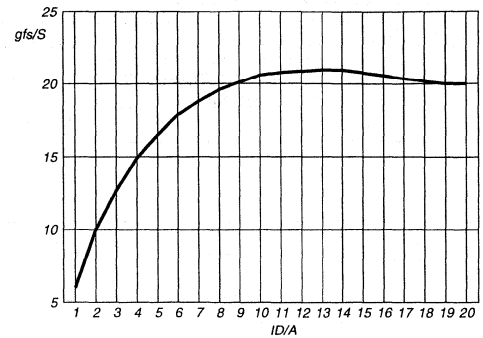


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

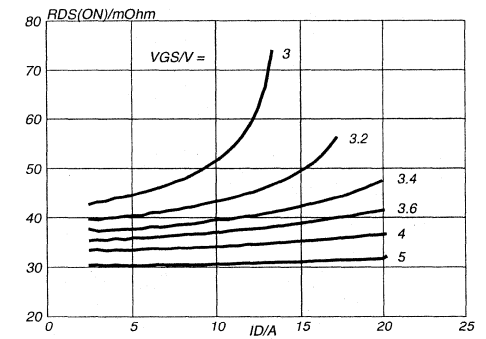


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

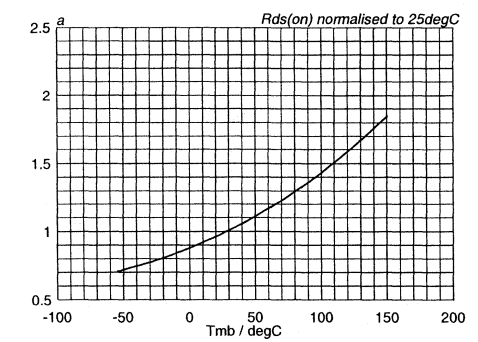


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,˚C} = f(T_j)$; I_D = 5 A; V_{GS} = 5 V

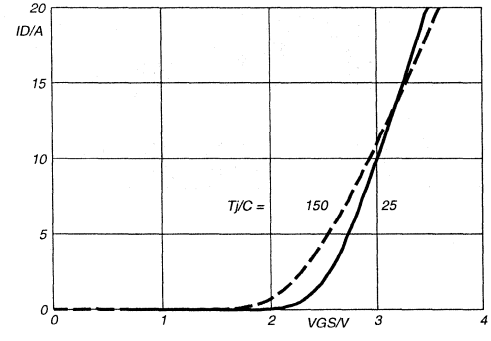


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

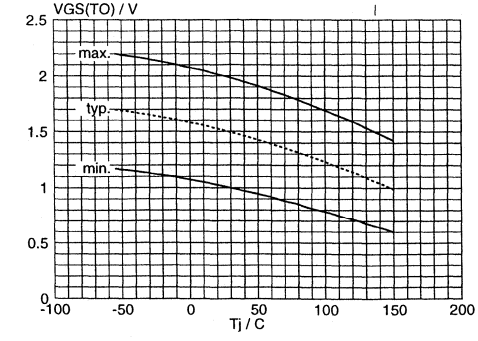


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

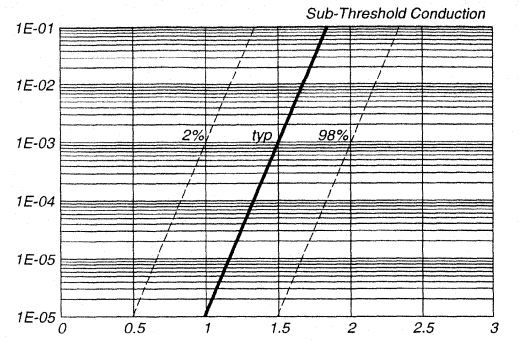


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; *conditions:* $T_j = 25$ °C; $V_{DS} = V_{GS}$

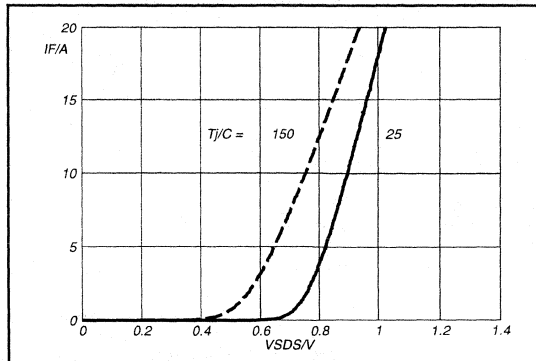


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; *conditions:* $V_{GS} = 0$ V; *parameter* T_j

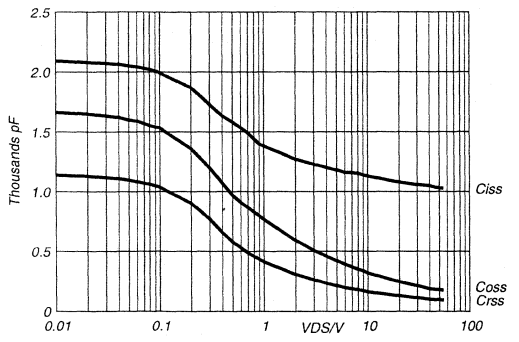


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; *conditions:* $V_{GS} = 0$ V; $f = 1$ MHz

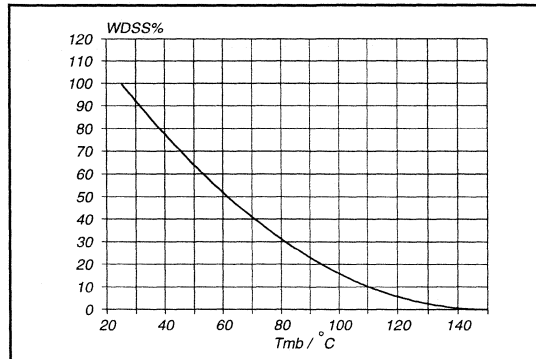


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{sp})$; *conditions:* $I_D = 3.6$ A

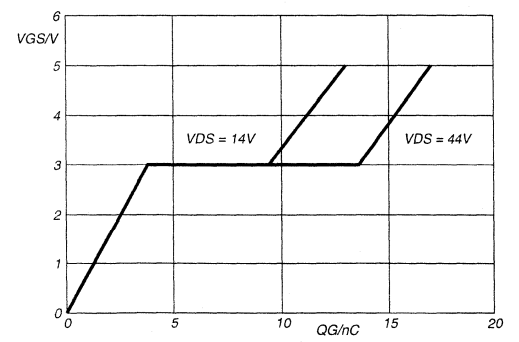


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; *conditions:* $I_D = 9$ A; *parameter* V_{DS}

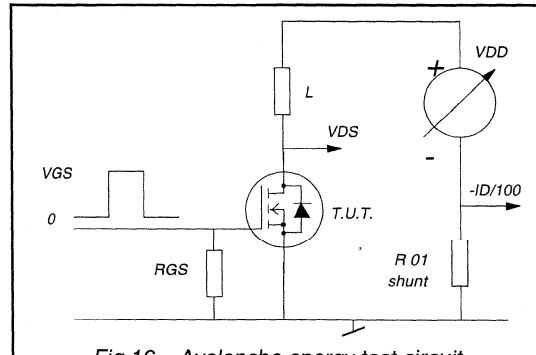


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

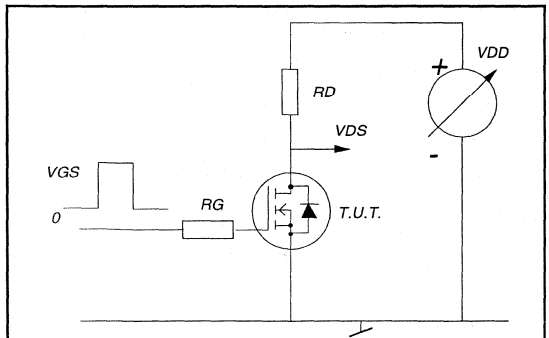


Fig.17. Switching test circuit.

PRINTED CIRCUIT BOARD

Dimensions in mm.

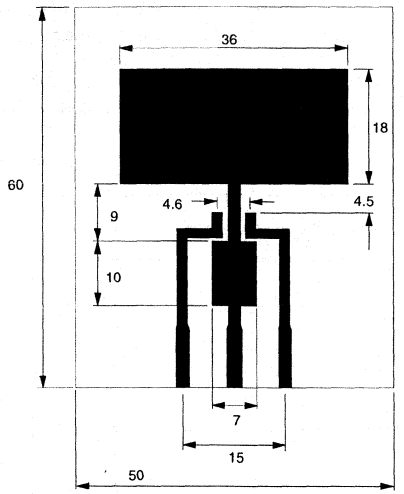


Fig.18. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).

TrenchMOS™ transistor
Logic level FET

BUK9880-55

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting. The device features very low on-state resistance and has integral zener diodes giving ESD protection. It is intended for use in automotive and general purpose switching applications.

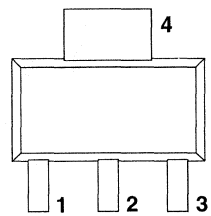
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current	7.5	A
P_{tot}	Total power dissipation	1.8	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	80	mΩ

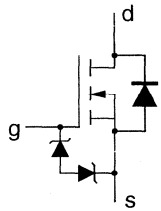
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{sp} = 25 °C	-	7.5	A
I_D	Drain current (DC)	On PCB in Fig.2 T_{amb} = 25 °C	-	3.5	A
I_D	Drain current (DC)	On PCB in Fig.2 T_{amb} = 100 °C	-	2.2	A
I_{DM}	Drain current (pulse peak value)	T_{sp} = 25 °C	-	40	A
P_{tot}	Total power dissipation	T_{sp} = 25 °C	-	8.3	W
P_{tot}	Total power dissipation	On PCB in Fig.2 T_{amb} = 25 °C	-	1.8	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	150	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}sp}$	From junction to solder point	Mounted on any PCB	12	15	K/W
$R_{th\ j\text{-}amb}$	From junction to ambient	Mounted on PCB of Fig.18	-	70	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
		T_j = 150˚C	0.6	-	-	V
		T_j = -55˚C	-	-	2.3	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 150˚C	-	-	100	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V	-	0.02	1	µA
		T_j = 150˚C	-	-	5	µA
$\pm V_{(BR)GSS}$	Gate source breakdown voltage	I_G = ±1 mA	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 5 A	-	65	80	mΩ
		T_j = 150˚C	-	-	148	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5 A; T_j = 25˚C	4	8	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	500	650	pF
C_{oss}	Output capacitance		-	110	135	pF
C_{rss}	Feedback capacitance		-	60	85	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 7 A;	-	10	15	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω;	-	30	50	ns
$t_{d\ off}$	Turn-off delay time		-	30	45	ns
t_f	Turn-off fall time	T_j = 25˚C	-	30	40	ns

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = -55 to 175˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{sp} = 25˚C	-	-	7.5	A
I_{DRM}	Pulsed reverse drain current	T_{sp} = 25˚C	-	-	40	A
V_{SD}	Diode forward voltage	I_F = 5 A; V_{GS} = 0 V	-	0.85	1.1	V
t_{rr}	Reverse recovery time	I_F = 5 A; -dI_F/dt = 100 A/µs;	-	38	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.2	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 2.5 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{sp} = 25 °C	-	-	30	mJ

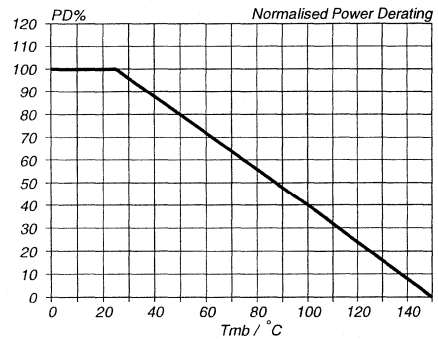


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{sp})

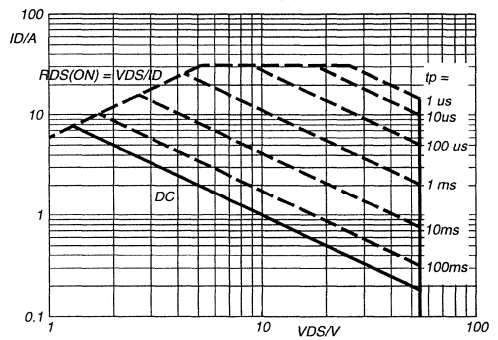


Fig.3. Safe operating area. T_{sp} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

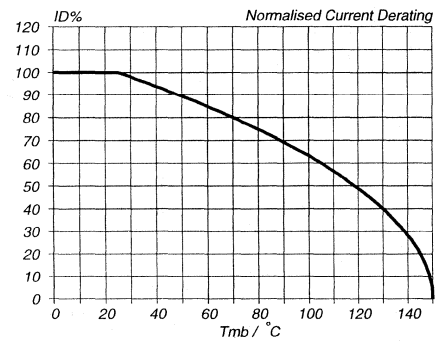


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{sp}); conditions: $V_{GS} \geq$ 5 V

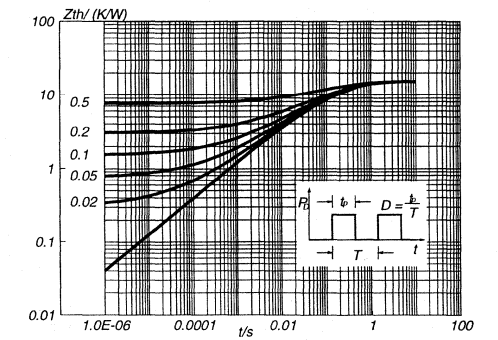


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}sp}$ = f(t); parameter D = t_p/T

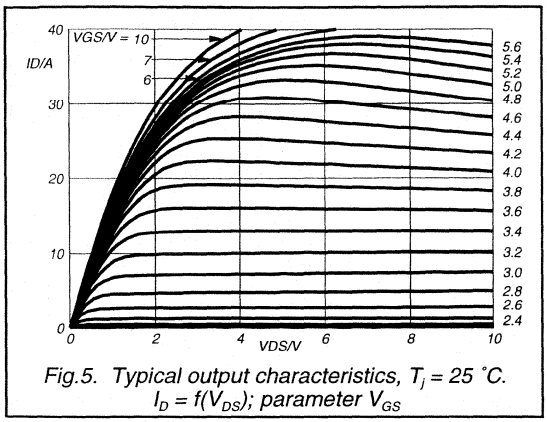


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

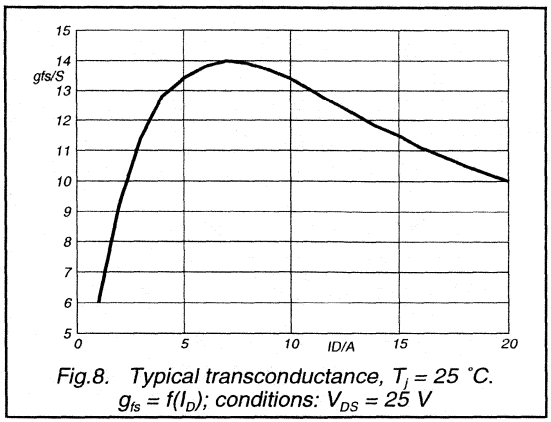


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

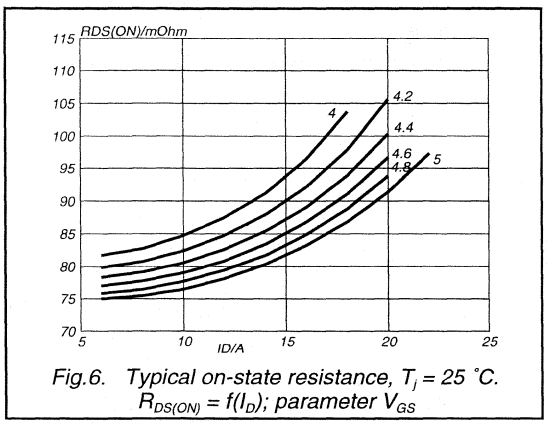


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

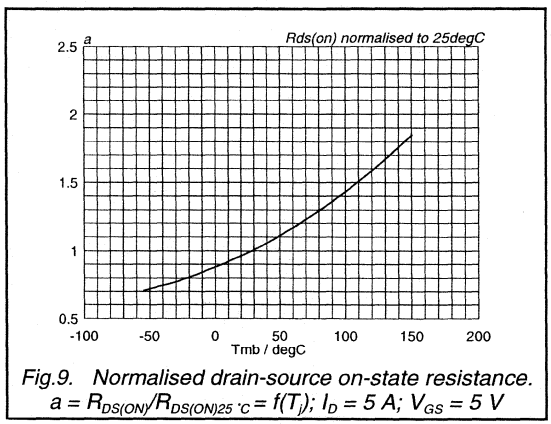


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,˚C} = f(T_j)$; I_D = 5 A; V_{GS} = 5 V

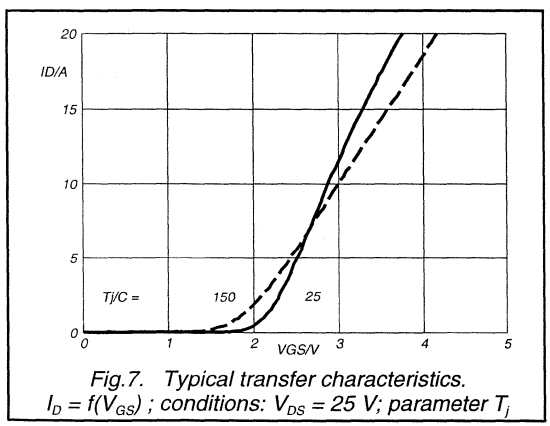


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

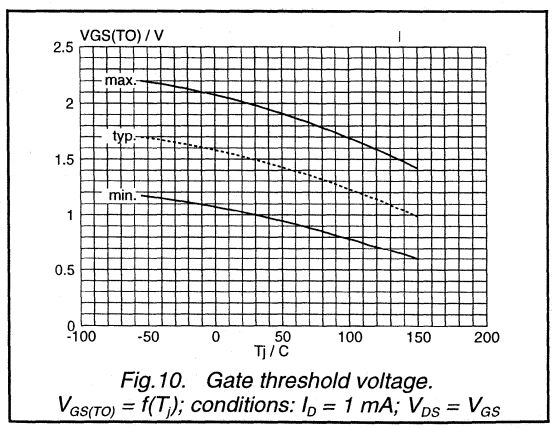


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

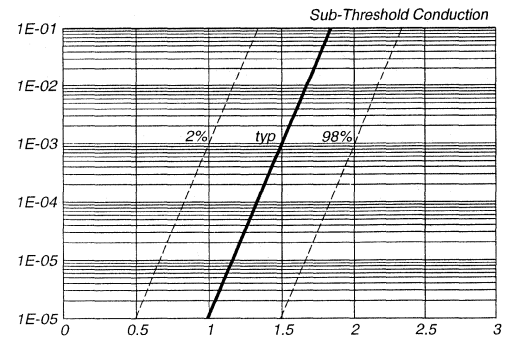


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

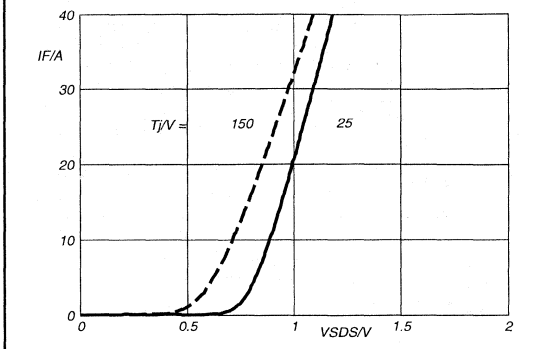


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

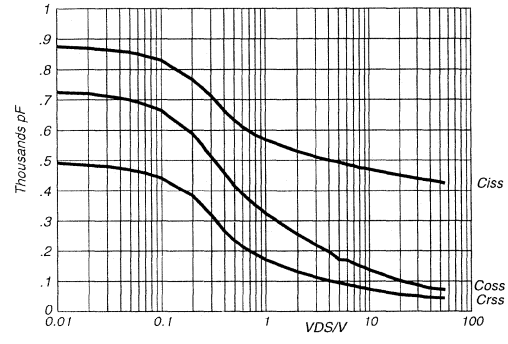


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

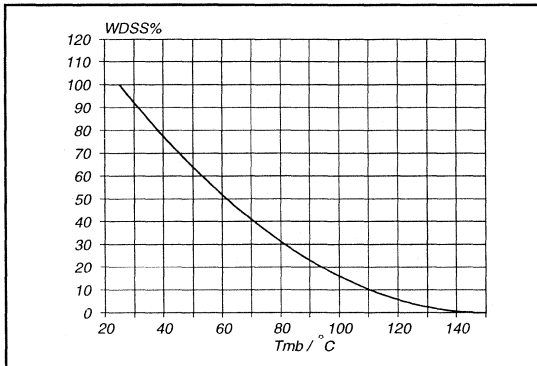


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{sp})$; conditions: $I_D = 2.5$ A

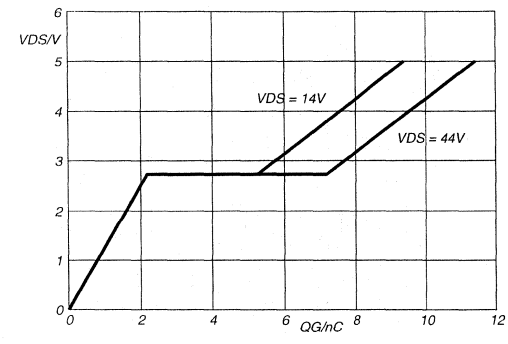


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 7$ A; parameter V_{DS}

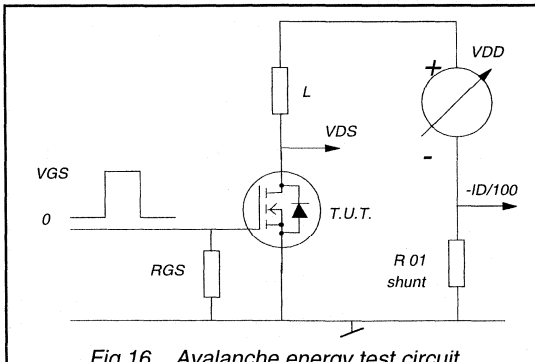


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

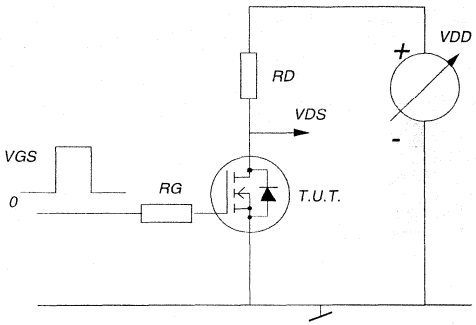


Fig.17. Switching test circuit.

PRINTED CIRCUIT BOARD

Dimensions in mm.

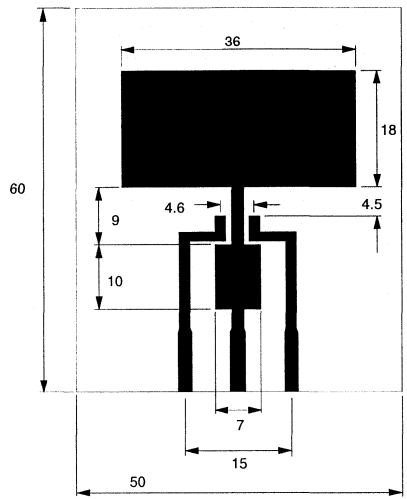


Fig.18. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).

TrenchMOS™ transistor
Standard level FET

BUK78150-55

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting. Using **'trench'** technology the device features very low on-state resistance and has integral zener diodes giving ESD protection. It is intended for use in automotive and general purpose switching applications.

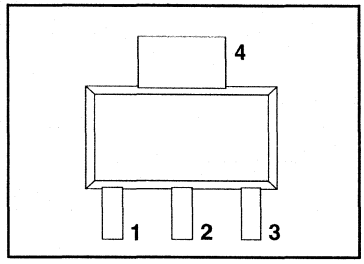
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current	5.5	A
P_{tot}	Total power dissipation	1.8	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	150	mΩ

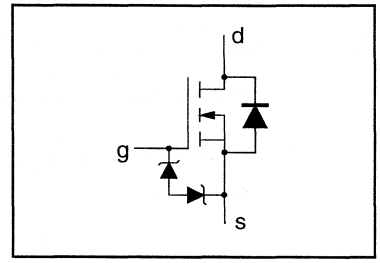
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	16	V
I_D	Drain current (DC)	T_{sp} = 25 °C	-	5.5	A
I_D	Drain current (DC)	On PCB in Fig.19 T_{amb} = 25 °C	-	2.6	A
I_D	Drain current (DC)	On PCB in Fig.19 T_{amb} = 100 °C	-	1.6	A
I_{DM}	Drain current (pulse peak value)	T_{sp} = 25 °C	-	30	A
P_{tot}	Total power dissipation	T_{sp} = 25 °C	-	8.3	W
P_{tot}	Total power dissipation	On PCB in Fig.19 T_{amb} = 25 °C	-	1.8	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	150	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}sp}$	From junction to solder point	Mounted on any PCB	12	15	K/W
$R_{th\ j\text{-}amb}$	From junction to ambient	Mounted on PCB of Fig.18	-	70	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.0	3.0	4.0	V
		T_j = 150˚C	1.2	-	-	V
		T_j = -55˚C	-	-	4.4	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 150˚C	-	-	100	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V	-	0.04	1	µA
		T_j = 150˚C	-	-	10	µA
$\pm V_{(BR)GSS}$	Gate source breakdown voltage	I_G = ±1 mA	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A	-	120	150	mΩ
		T_j = 150˚C	-	-	277	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5 A; T_j = 25˚C	0.5	2.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	190	240	pF
C_{oss}	Output capacitance		-	65	80	pF
C_{rss}	Feedback capacitance		-	32	45	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 5 A;	-	9	14	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 10 Ω;	-	28	42	ns
$t_{d\ off}$	Turn-off delay time		-	15	23	ns
t_f	Turn-off fall time	T_j = 25˚C	-	8	12	ns

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = -55 to 175˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{sp} = 25˚C	-	-	5.5	A
I_{DRM}	Pulsed reverse drain current	T_{sp} = 25˚C	-	-	30	A
V_{SD}	Diode forward voltage	I_F = 2 A; V_{GS} = 0 V	-	0.85	1.1	V
t_{rr}	Reverse recovery time	I_F = 2 A; -dI_F/dt = 100 A/µs;	-	43	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.16	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 1.9 A; $V_{DD} \leq 25$ V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{sp} = 25 °C	-	-	15	mJ

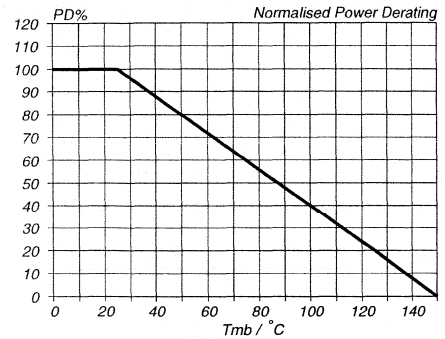


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{sp})

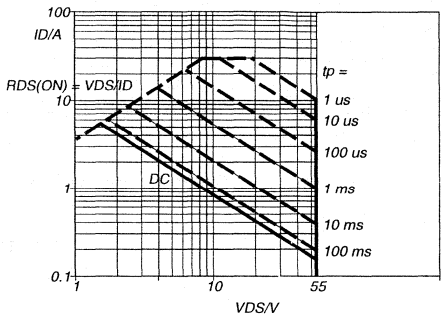


Fig.3. Safe operating area. T_{sp} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

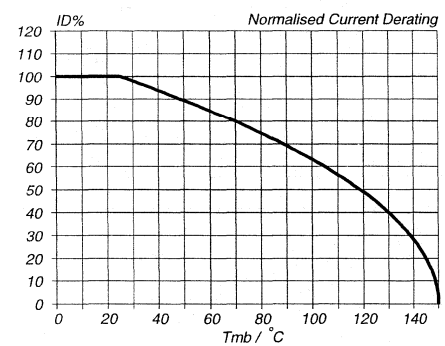


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{sp}); conditions: $V_{GS} \geq$ 10 V

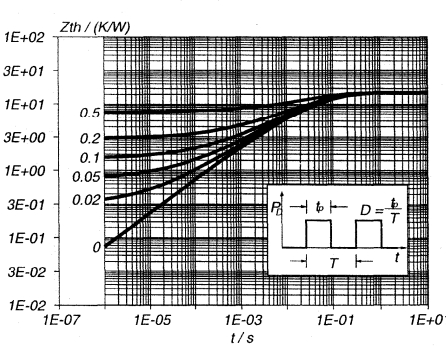


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}sp}$ = f(t); parameter D = t_p/T

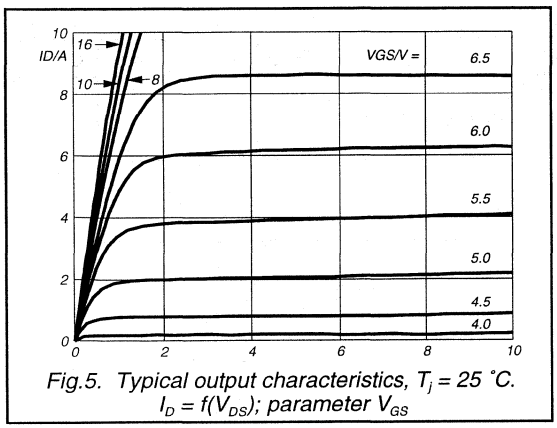


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

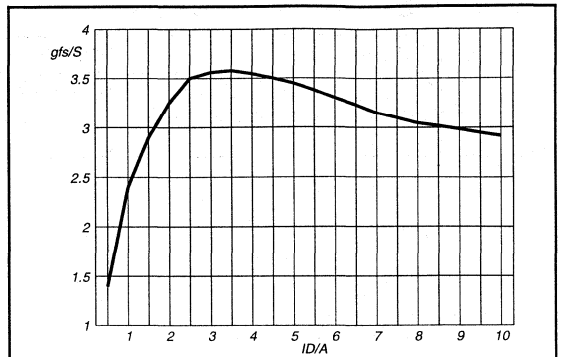


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

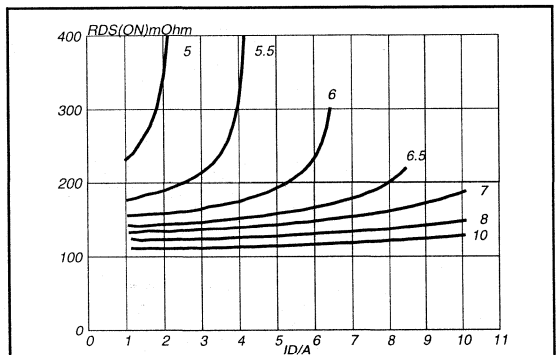


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

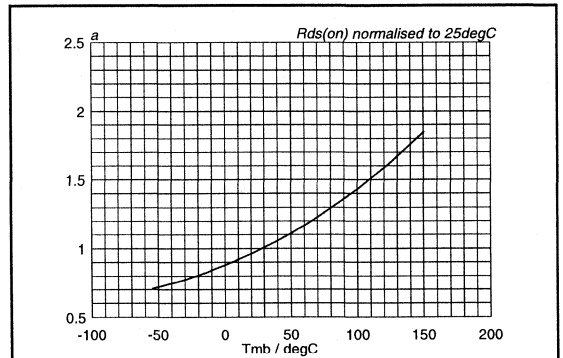


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\ ^{\circ}C} = f(T_j)$; I_D = 5 A; V_{GS} = 10 V

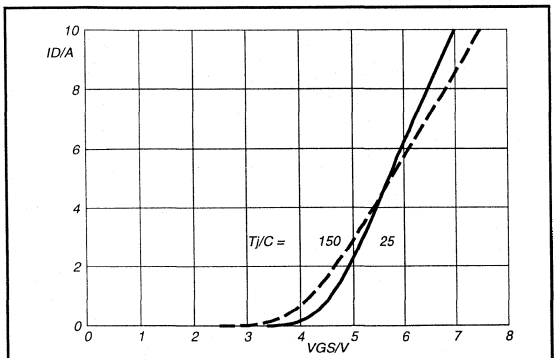


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

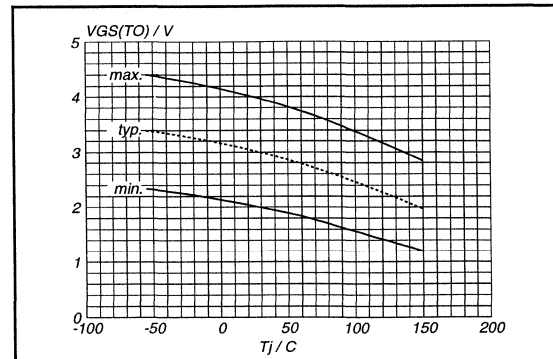


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

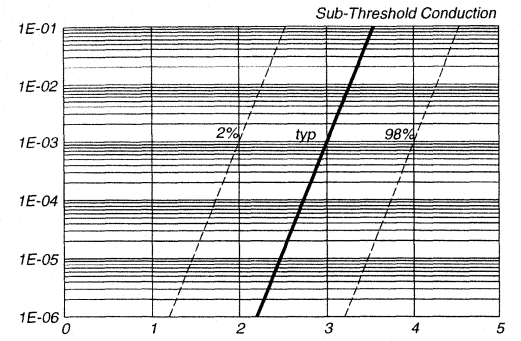


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; *conditions:* $T_j = 25$ °C; $V_{DS} = V_{GS}$

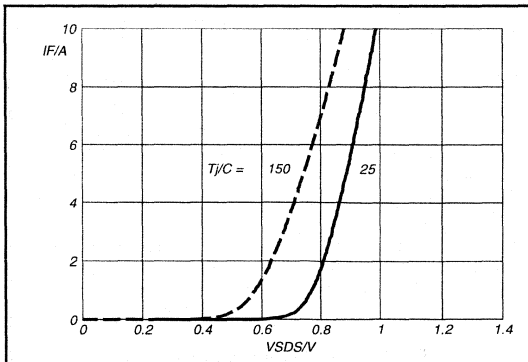


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; *conditions:* $V_{GS} = 0$ V; *parameter* T_j

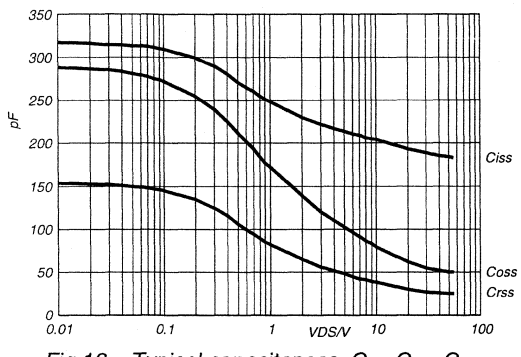


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; *conditions:* $V_{GS} = 0$ V; $f = 1$ MHz

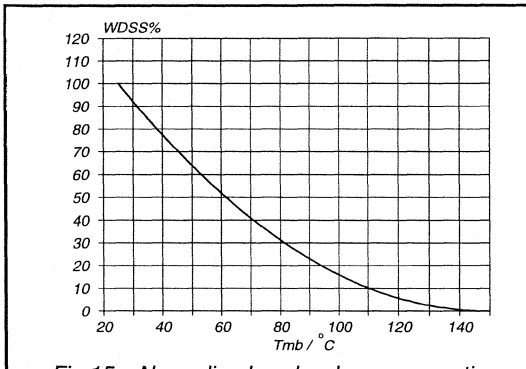


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{sp})$; *conditions:* $I_D = 1.9$ A

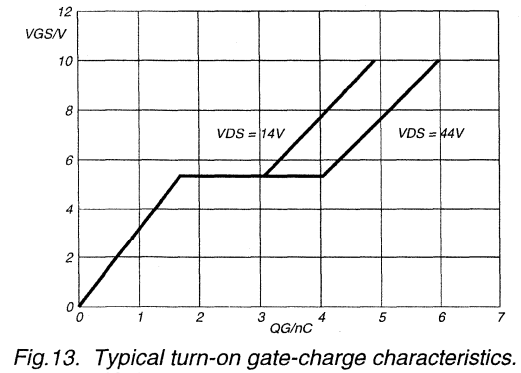


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; *conditions:* $I_D = 5$ A; *parameter* V_{DS}

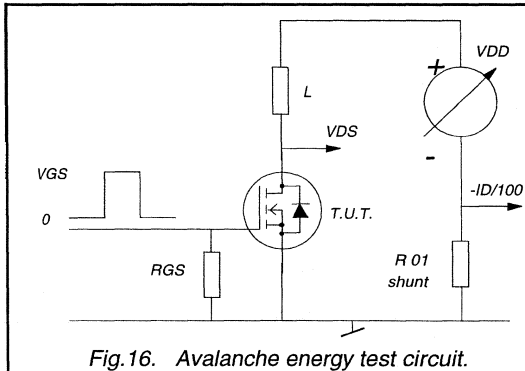


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

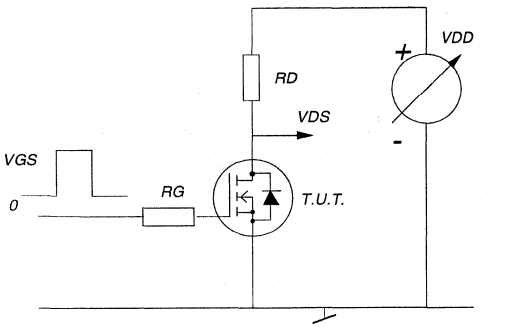


Fig.17. Switching test circuit.

PRINTED CIRCUIT BOARD

Dimensions in mm.

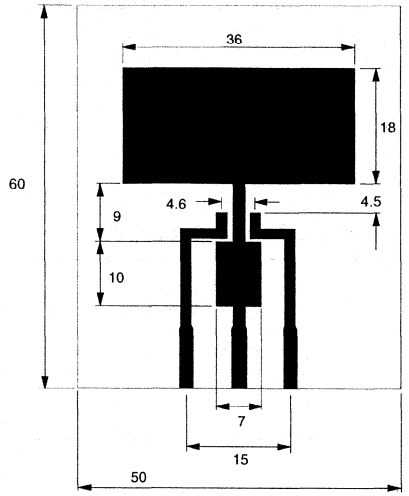


Fig.18. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).

TrenchMOS™ transistor
Logic level FET

BUK98150-55

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting. The device features very low on-state resistance and has integral zener diodes giving ESD protection. It is intended for use in automotive and general purpose switching applications.

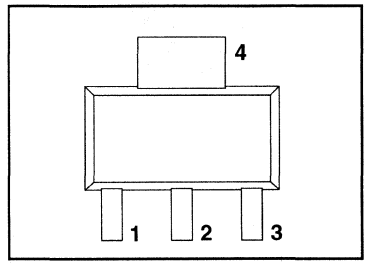
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current	5.5	A
P_{tot}	Total power dissipation	1.8	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	150	mΩ

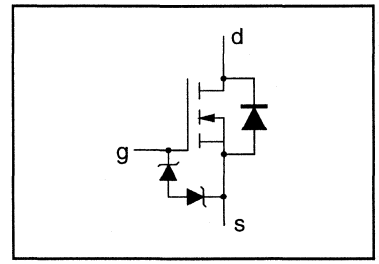
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{sp} = 25 °C	-	5.5	A
I_D	Drain current (DC)	On PCB in Fig.19 T_{amb} = 25 °C	-	2.6	A
I_D	Drain current (DC)	On PCB in Fig.19 T_{amb} = 100 °C	-	1.6	A
I_{DM}	Drain current (pulse peak value)	T_{sp} = 25 °C	-	30	A
P_{tot}	Total power dissipation	T_{sp} = 25 °C	-	8.3	W
P_{tot}	Total power dissipation	On PCB in Fig.19 T_{amb} = 25 °C	-	1.8	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	150	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}sp}$	From junction to solder point	Mounted on any PCB	12	15	K/W
$R_{th\ j\text{-}amb}$	From junction to ambient	Mounted on PCB of Fig.18	-	70	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
		T_j = 150˚C	0.6	-	-	V
		T_j = -55˚C	-	-	2.3	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 150˚C	-	-	100	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V	-	0.02	1	µA
		T_j = 150˚C	-	-	5	µA
$\pm V_{(BR)GSS}$	Gate source breakdown voltage	V_{GS} = ±1 mA	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 5 A	-	120	150	mΩ
		T_j = 150˚C	-	-	277	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5 A; T_j = 25˚C	3	5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	250	330	pF
C_{oss}	Output capacitance		-	65	80	pF
C_{rss}	Feedback capacitance		-	35	50	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 5 A;	-	11	17	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω;	-	38	60	ns
$t_{d\ off}$	Turn-off delay time		-	25	38	ns
t_f	Turn-off fall time	T_j = 25˚C	-	20	38	ns

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = -55 to 175˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{sp} = 25˚C	-	-	5.5	A
I_{DRM}	Pulsed reverse drain current	T_{sp} = 25˚C	-	-	30	A
V_{SD}	Diode forward voltage	I_F = 2 A; V_{GS} = 0 V	-	0.85	1.1	V
t_{rr}	Reverse recovery time	I_F = 2 A; -dI_F/dt = 100 A/µs;	-	43	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.16	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 1.9 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{sp} = 25 °C	-	-	15	mJ

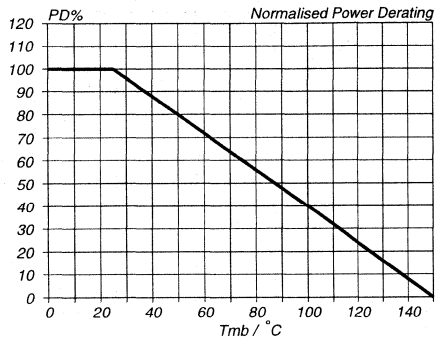


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{sp})

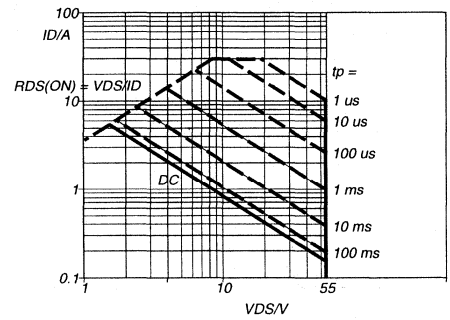


Fig.3. Safe operating area. T_{sp} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

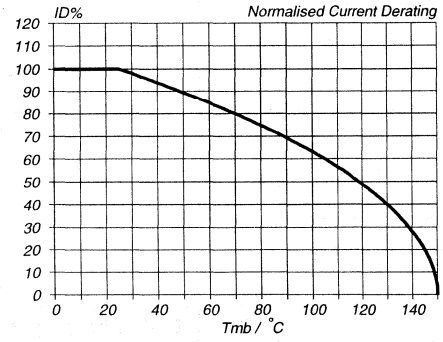


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{sp}); conditions: $V_{GS} \geq$ 5 V

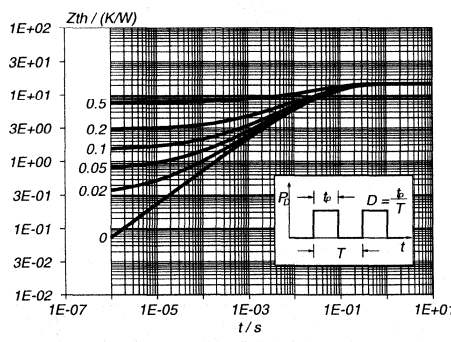


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}sp}$ = f(t); parameter D = t_p/T

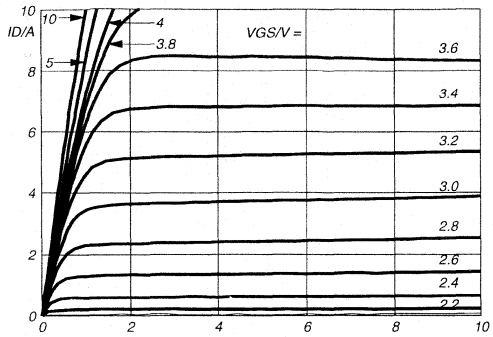


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

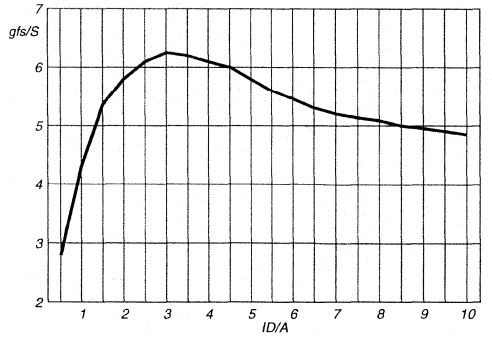


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

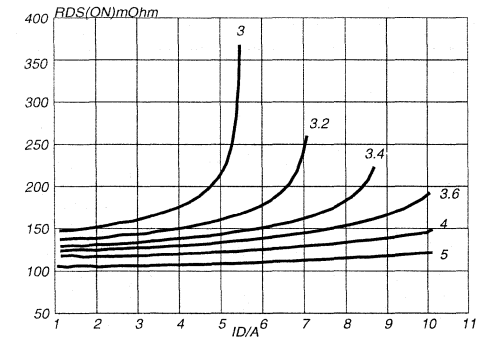


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

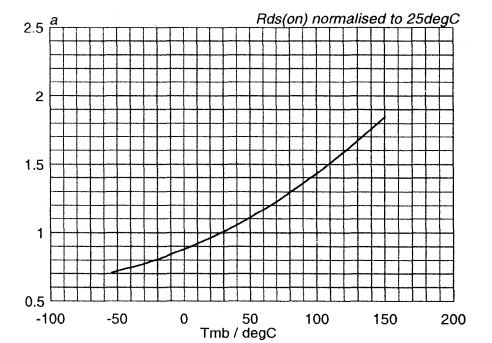


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,˚C} = f(T_j)$; I_D = 5 A; V_{GS} = 5 V

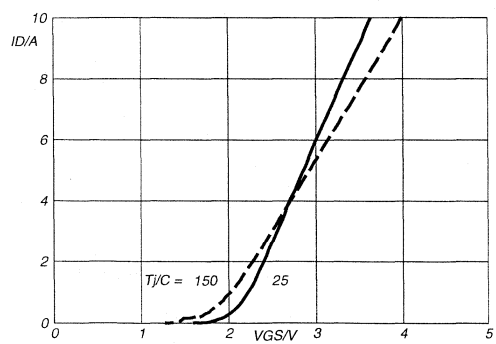


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

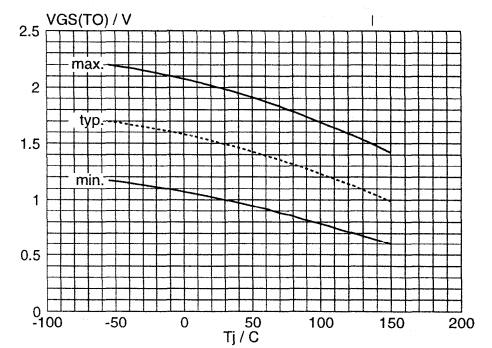


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

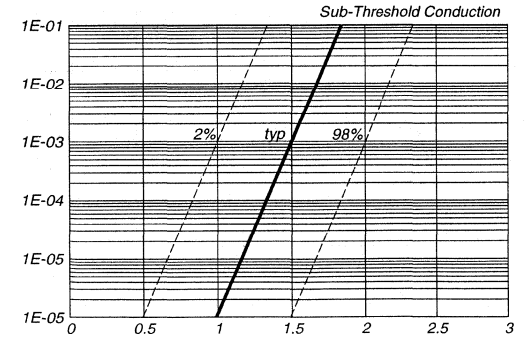


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

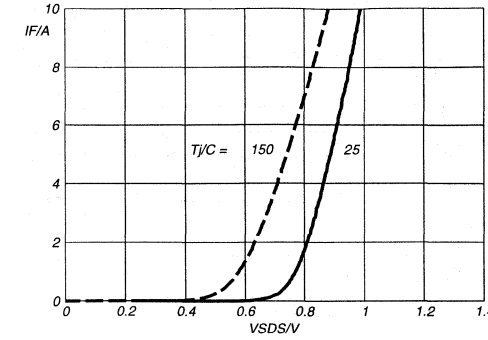


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

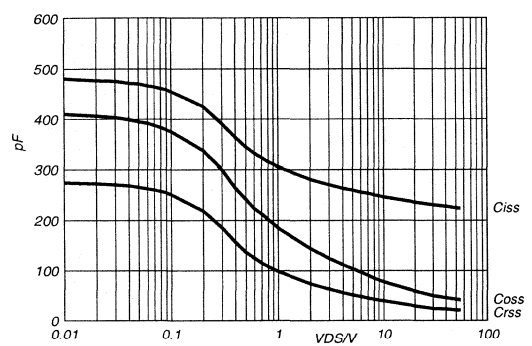


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

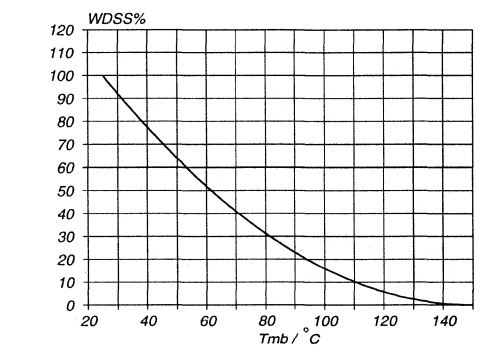


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{sp})$; conditions: I_D = 1.9 A

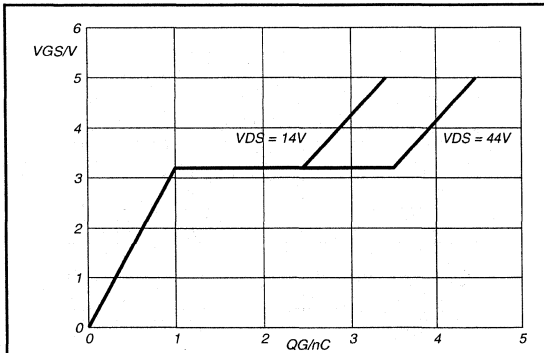


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 5 A; parameter V_{DS}

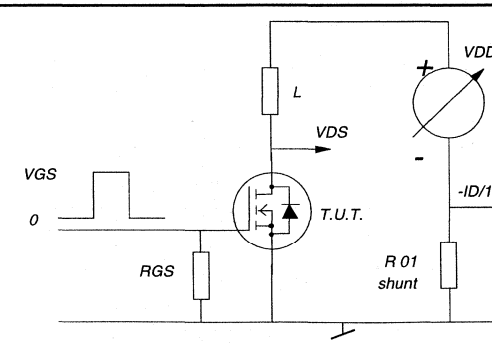


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

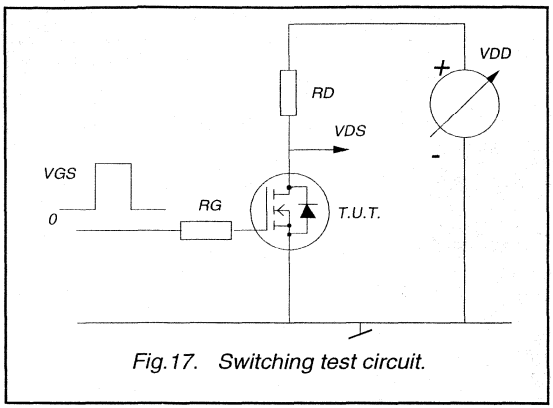


Fig.17. Switching test circuit.

PRINTED CIRCUIT BOARD

Dimensions in mm.

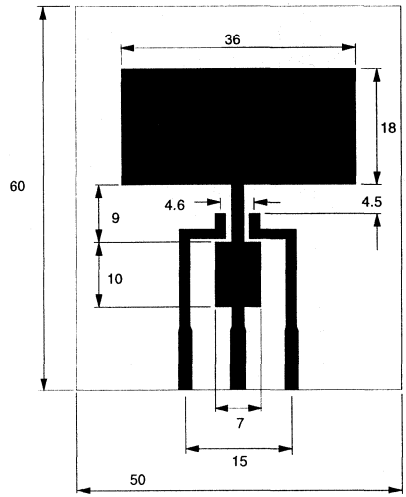


Fig.18. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).

Complementary enhancement mode MOS transistors

PHC2300

FEATURES

- High-speed switching
- No secondary breakdown.

APPLICATIONS

- Universal line interface in telephone sets
- Relay, high-speed and line transformer drivers.

DESCRIPTION

One N-channel and one P-channel enhancement mode MOS transistor in an 8-pin plastic SOT96-1 (SO8) package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s_1	source 1
2	g_1	gate 1
3	s_2	source 2
4	g_2	gate 2
5	d_2	drain 2
6	d_2	drain 2
7	d_1	drain 1
8	d_1	drain 1

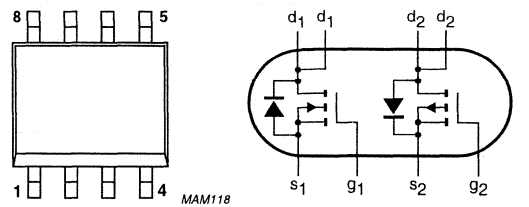


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per FET					
V_{DS}	drain-source voltage (DC)				
	N-channel		–	300	V
	P-channel		–	–300	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage				V
	N-channel	$V_{DS} = V_{GS}$; I_D = 1 mA	0.8	2	V
	P-channel	$V_{DS} = V_{GS}$; I_D = –1 mA	–0.8	–2	V
I_D	drain current (DC)	T_s = 80 °C			
	N-channel		–	340	mA
	P-channel		–	–235	mA
R_{DSon}	drain-source on-state resistance				
	N-channel	V_{GS} = 10 V; I_D = 170 mA	–	8	Ω
	P-channel	V_{GS} = –10 V; I_D = –115 mA	–	17	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	1.6	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per FET					
V_{DS}	drain-source voltage (DC)				
	N-channel		–	300	V
	P-channel		–	–300	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1			
	N-channel		–	340	mA
	P-channel		–	–235	mA
I_{DM}	peak drain current	note 2			
	N-channel		–	1.4	A
	P-channel		–	–0.9	A
P_{tot}	total power dissipation	T_s = 80 °C; note 3	–	1.6	W
		T_{amb} = 25 °C; note 4	–	1.8	W
		T_{amb} = 25 °C; note 5	–	0.9	W
		T_{amb} = 25 °C; note 6	–	1.2	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C

Notes

1. T_s is the temperature at the soldering point of the drain leads.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Maximum permissible dissipation per MOS transistor. (So both devices may be loaded up to 1.6 W at the same time).
4. Maximum permissible dissipation per MOS transistor. Value based on a printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
5. Maximum permissible dissipation per MOS transistor. Value based on a printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.
6. Maximum permissible dissipation if only one MOS transistor dissipates. Value based on a printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

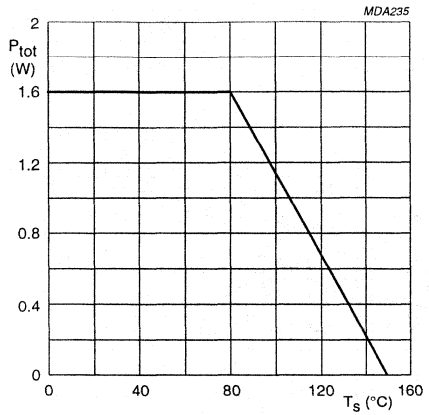
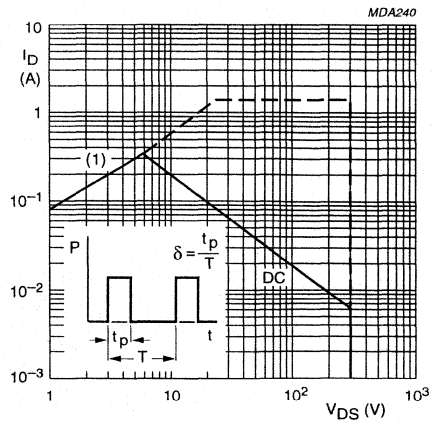
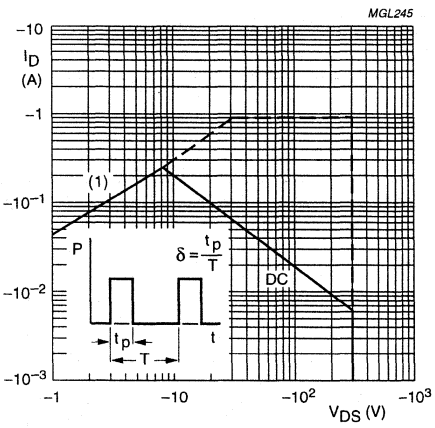


Fig.2 Power derating curve.



$\delta = 0.01$; $T_s = 80$ °C.
(1) R_{DSon} limitation.

Fig.3 SOAR; N-channel.

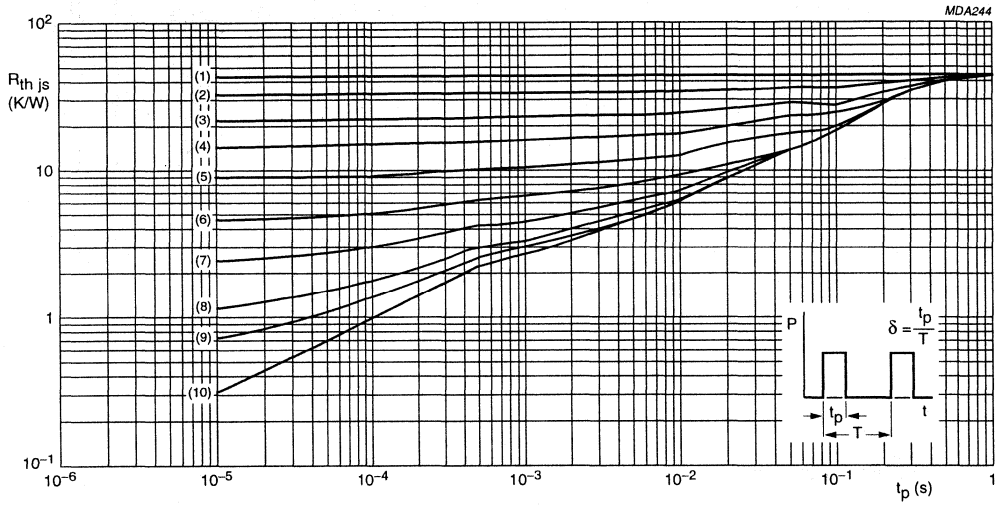


$\delta = 0.01$; $T_s = 80$ °C.
(1) R_{DSon} limitation.

Fig.4 SOAR; P-channel.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	43	K/W



(1) δ = 1.00. (2) δ = 0.75. (3) δ = 0.5. (4) δ = 0.33. (5) δ = 0.2.
(6) δ = 0.1. (7) δ = 0.05. (8) δ = 0.02. (9) δ = 0.01. (10) δ = 0.

Fig.5 Transient thermal resistance from junction to soldering point as a function of pulse time for N- and P-channels; typical values.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per FET						
$V_{(BR)DSS}$	drain-source breakdown voltage					
	N-channel	V_{GS} = 0; I_D = 10 μA	300	–	–	V
	P-channel	V_{GS} = 0; I_D = −10 μA	−300	–	–	V
V_{GSth}	gate-source threshold voltage					
	N-channel	V_{GS} = V_{DS}; I_D = 1 mA	0.8	–	2	V
	P-channel	V_{GS} = V_{DS}; I_D = −1 mA	−0.8	–	−2	V
I_{DSS}	drain-source leakage current					
	N-channel	V_{GS} = 0; V_{DS} = 240 V	–	–	100	nA
	P-channel	V_{GS} = 0; V_{DS} = −240 V	–	–	−100	nA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0				
	N-channel		–	–	±100	nA
	P-channel		–	–	±100	nA
R_{DSon}	drain-source on-state resistance					
	N-channel	V_{GS} = 10 V; I_D = 170 mA	–	–	8	Ω
	P-channel	V_{GS} = –10 V; I_D = – 115 mA	–	–	17	Ω
C_{iss}	input capacitance					
	N-channel	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	57	–	pF
	P-channel	V_{GS} = 0; V_{DS} = –50 V; f = 1 MHz	–	45	–	pF
C_{oss}	output capacitance					
	N-channel	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	15	–	pF
	P-channel	V_{GS} = 0; V_{DS} = –50 V; f = 1 MHz	–	15	–	pF
C_{rss}	reverse transfer capacitance					
	N-channel	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	2.6	–	pF
	P-channel	V_{GS} = 0; V_{DS} = –50 V; f = 1 MHz	–	3	–	pF
Q_G	total gate charge					
	N-channel	V_{GS} = 10 V; V_{DS} = 50 V; I_D = 170 mA	–	2097	–	pC
	P-channel	V_{GS} = –10 V; V_{DS} = –50 V; I_D = –115 mA	–	2137	–	pC
Q_{GS}	gate-source charge					
	N-channel	V_{GS} = 10 V; V_{DS} = 50 V; I_D = 170 mA	–	75	–	pC
	P-channel	V_{GS} = –10 V; V_{DS} = –50 V; I_D = –115 mA	–	68	–	pC
Q_{GD}	gate-drain charge					
	N-channel	V_{GS} = 10 V; V_{DS} = 50 V; I_D = 170 mA	–	527	–	pC
	P-channel	V_{GS} = –10 V; V_{DS} = –50 V; I_D = –115 mA	–	674	–	pC
Switching times						
t_{on}	turn-on time					
	N-channel	V_{GS} = 0 to 10 V; V_{DD} = 50 V; I_D = 170 mA	–	2.5	10	ns
	P-channel	V_{GS} = 0 to –10 V; V_{DD} = –50 V; I_D = –115 mA	–	4	10	ns
t_{off}	turn-off time					
	N-channel	V_{GS} = 10 to 0 V; V_{DD} = 50 V; I_D = 170 mA	–	17	30	ns
	P-channel	V_{GS} = –10 to 0 V; V_{DD} = –50 V; I_D = –115 mA	–	25	35	ns

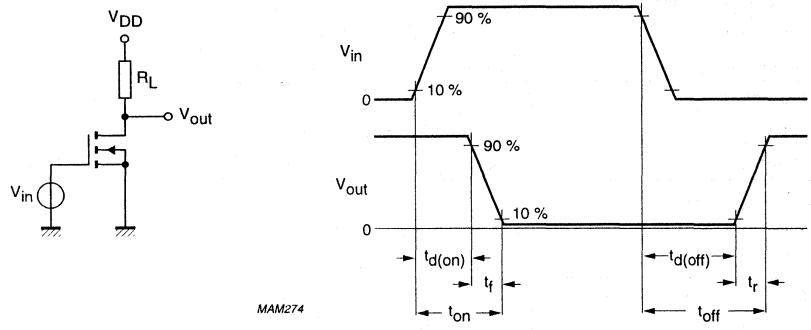


Fig.6 Switching times test circuit with input and output waveforms; N-channel.

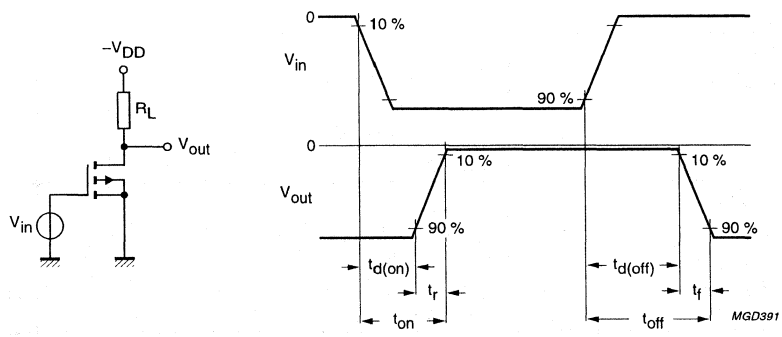
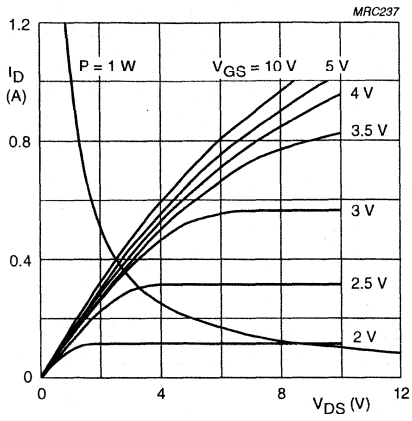
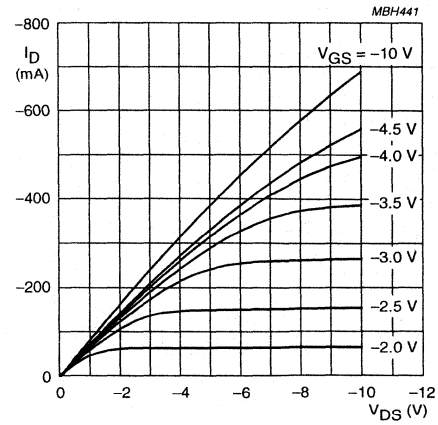


Fig.7 Switching times test circuit with input and output waveforms; P-channel.



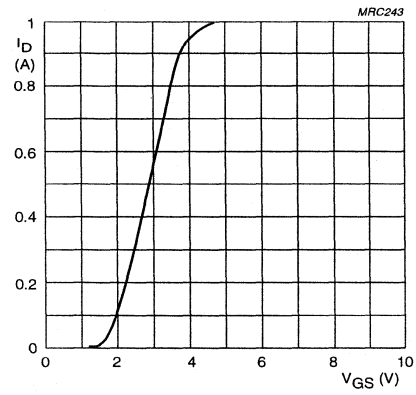
T_{amb} = 25 °C; t_p = 80 µs; δ = 0.

Fig.8 Output characteristics; N-channel typical values.



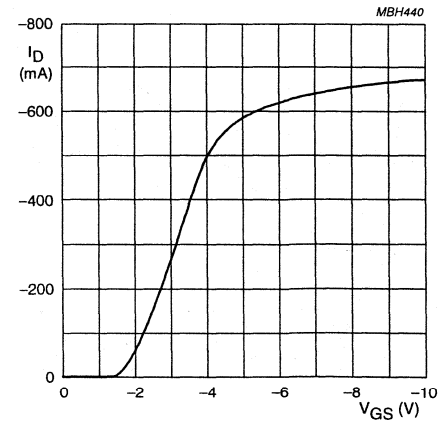
T_{amb} = 25 °C; t_p = 80 µs; δ = 0.

Fig.9 Output characteristics; P-channel typical values.



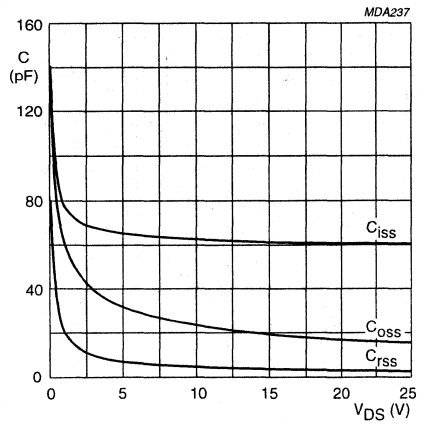
V_{DS} = 10 V; T_{amb} = 25 °C; t_p = 80 µs; δ = 0.

Fig.10 Transfer characteristic; N-channel typical values.



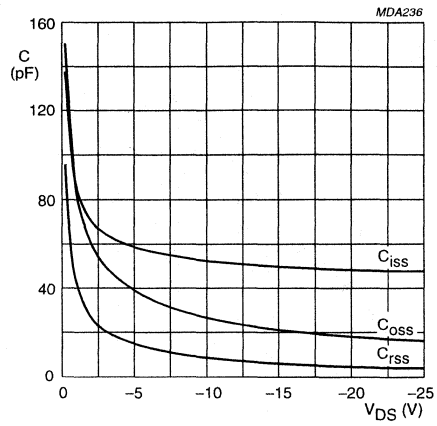
V_{DS} = −10 V; T_{amb} = 25 °C; t_p = 80 µs; δ = 0.

Fig.11 Transfer characteristic; P-channel typical values.



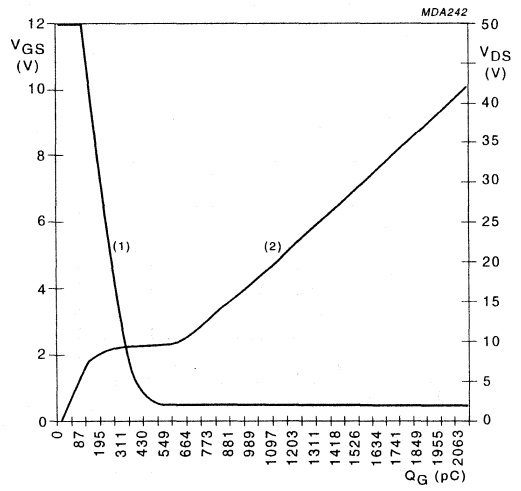
f = 1 MHz; T_{amb} = 25 °C.

Fig.12 Capacitance as a function of drain-source voltage; N-channel typical values.



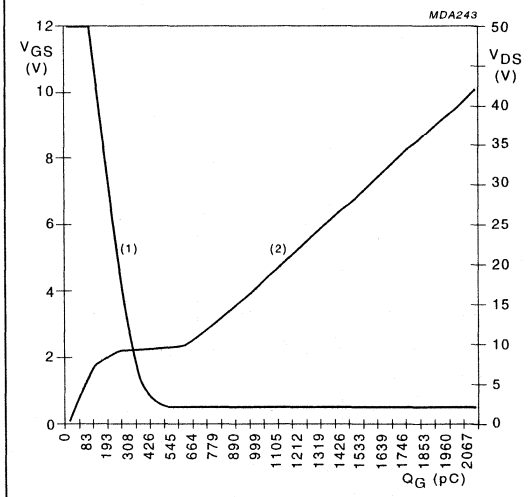
f = 1 MHz; T_{amb} = 25 °C.

Fig.13 Capacitance as a function of drain-source voltage; P-channel typical values.



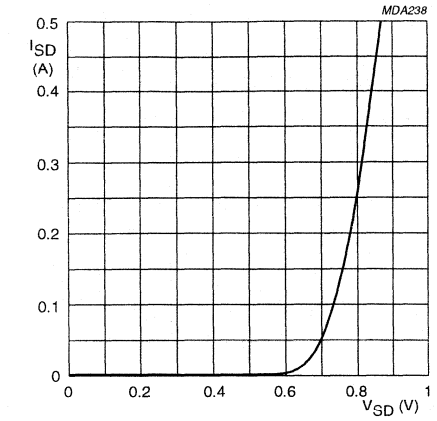
V_{DD} = 50 V; I_D = 170 mA; T_{amb} = 25 °C.
(1) V_{DS}.
(2) V_{GS}.

Fig.14 Gate-source voltage and drain-source voltage as a function of total gate charge; N-channel typical values.



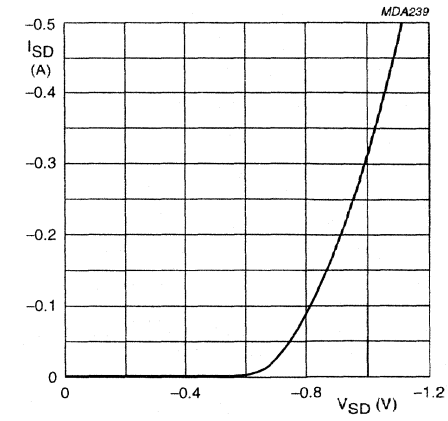
V_{DD} = −50 V; I_D = −115 mA; T_{amb} = 25 °C.
(1) V_{DS}.
(2) V_{GS}.

Fig.15 Gate-source voltage and drain-source voltage as a function of total gate charge; P-channel typical values.



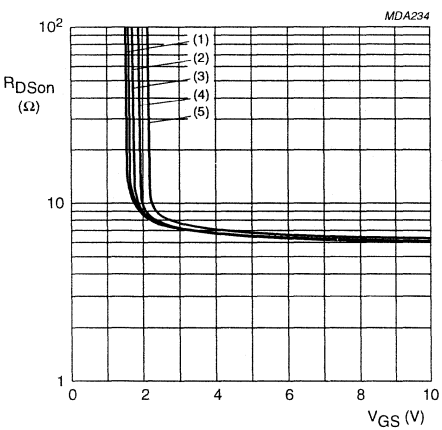
V_{GD} = 0.

Fig.16 Source-drain current as a function of source-drain diode forward voltage; N-channel typical values.



V_{GD} = 0.

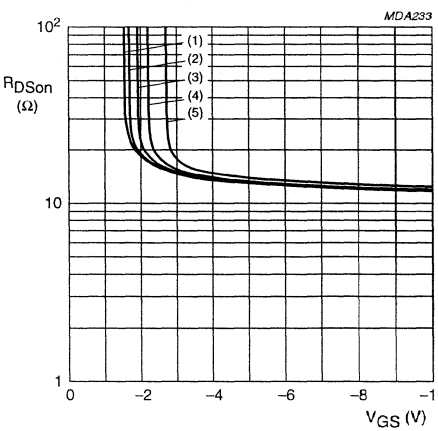
Fig.17 Source-drain current as a function of source-drain diode forward voltage; P-channel typical values.



$V_{DS} \geq I_D \times R_{DSon}$; T_{amb} = 25 °C;
t_p = 300 µs; δ = 0.

(1) I_D = 10 mA.
(2) I_D = 20 mA.
(3) I_D = 50 mA.
(4) I_D = 100 mA.
(5) I_D = 200 mA.

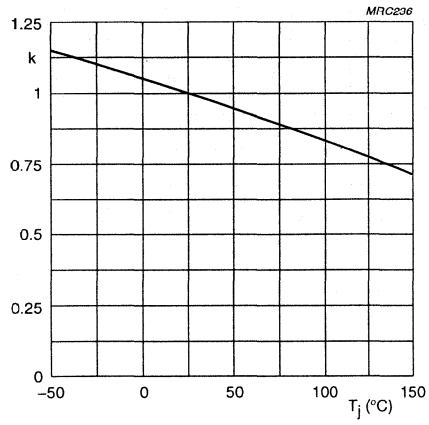
Fig.18 Drain-source on-state resistance as a function of gate-source voltage; N-channel typical values.



$V_{DS} \geq I_D \times R_{DSon}$; T_{amb} = 25 °C;
t_p = 300 µs; δ = 0.

(1) I_D = −10 mA.
(2) I_D = −20 mA.
(3) I_D = −50 mA.
(4) I_D = −100 mA.
(5) I_D = −200 mA.

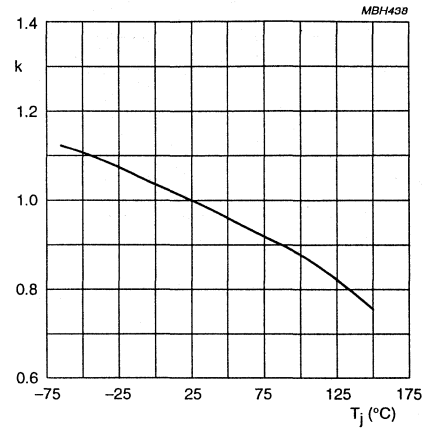
Fig.19 Drain-source on-state resistance as a function of gate-source voltage; P-channel typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

V_{GSth} at $V_{DS} = V_{GS}$; $I_D = 1$ mA.

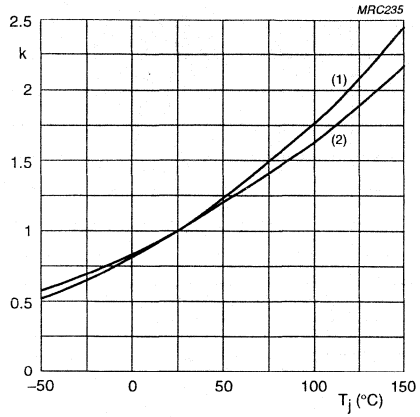
Fig.20 Temperature coefficient of gate-source threshold voltage as a function of junction temperature; N-channel, typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

V_{GSth} at $V_{DS} = V_{GS}$; $I_D = -1$ mA.

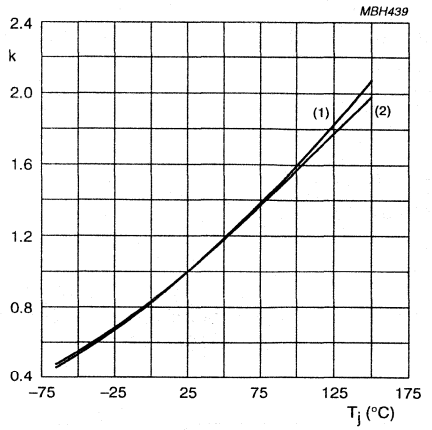
Fig.21 Temperature coefficient of gate-source threshold voltage as function of junction temperature; P-channel typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

(1) R_{DSon} at V_{GS} = 10 V; I_D = 250 mA.
(2) R_{DSon} at V_{GS} = 2.4 V; I_D = 20 mA.

Fig.22 Temperature coefficient of drain-source on-resistance as a function of junction temperature; N-channel typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

(1) R_{DSon} at V_{GS} = -4.5 V; I_D = −80 mA.
(2) R_{DSon} at V_{GS} = -2.8 V; I_D = −50 mA.

Fig.23 Temperature coefficient of drain-source on-resistance as a function of junction temperature; P-channel typical values.

Complementary enhancement mode MOS transistor

PHC20306

OBJECTIVE
Philips Semiconductors for Design-in Information
See Philips Semiconductors

FEATURES

- Very low on-state resistance
- High-speed switching
- No secondary breakdown.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

DESCRIPTION

One N-channel and one P-channel enhancement mode MOS transistor in an 8-pin SOT96-1 (SO8) plastic package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s_1	source 1
2	g_1	gate 1
3	s_2	source 2
4	g_2	gate 2
5	d_2	drain 2
6	d_2	drain 2
7	d_1	drain 1
8	d_1	drain 1

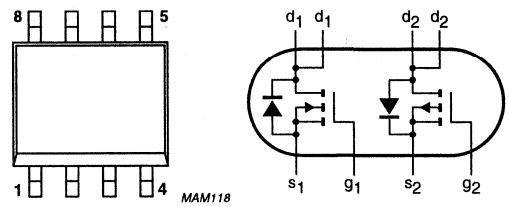


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per channel					
V_{DS}	drain-source voltage (DC)				
	N-channel		–	30	V
	P-channel		–	–30	V
V_{SD}	source-drain diode forward voltage				
	N-channel	V_{GD} = 0; I_S = 1.25 A	–	1	V
	P-channel	V_{GD} = 0; I_S = –1.25 A	–	–1.3	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage				V
	N-channel	V_{DS} = V_{GS}; I_D = 1 mA	1	–	V
	P-channel	V_{DS} = V_{GS}; I_D = –1 mA	–1	–	V
I_D	drain current (DC)	T_s = 80 °C			
	N-channel		–	8.2	A
	P-channel		–	–5.6	A
R_{DSon}	drain-source on-state resistance				
	N-channel	V_{GS} = 10 V; I_D = 4 A	–	30	mΩ
	P-channel	V_{GS} = –10 V; I_D = –2.8 A	–	65	mΩ
P_{tot}	total power dissipation	T_s = 80 °C	–	3.5	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per channel					
V_{DS}	drain-source voltage (DC)				
	N-channel		–	30	V
	P-channel		–	–30	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1			
	N-channel		–	8.2	A
	P-channel		–	–5.6	A
I_{DM}	peak drain current	note 2			
	N-channel		–	33	A
	P-channel		–	–22.5	A
P_{tot}	total power dissipation	T_s = 80 °C; note 3	–	3.5	W
		T_{amb} = 25 °C; note 4	–	2.6	W
		T_{amb} = 25 °C; note 5	–	1.1	W
		T_{amb} = 25 °C; note 6	–	1.5	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C			
	N-channel		–	3.5	A
	P-channel		–	–2.7	A
I_{SM}	peak pulsed source current	note 2			
	N-channel		–	14	A
	P-channel		–	–10.8	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Maximum permissible dissipation per MOS transistor. Both devices may be loaded up to 3.5 W at the same time.
4. Maximum permissible dissipation per MOS transistor. Device mounted on a printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
5. Maximum permissible dissipation per MOS transistor. Device mounted on a printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.
6. Maximum permissible dissipation if only one MOS transistor dissipates. Device mounted a on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	20	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per channel						
$V_{(BR)DSS}$	drain-source breakdown voltage					
	N-channel	V_{GS} = 0; I_D = 10 µA	30	–	–	V
	P-channel	V_{GS} = 0; I_D = −10 µA	−30	–	–	V
V_{GSth}	gate-source threshold voltage					
	N-channel	V_{GS} = V_{DS}; I_D = 1 mA	1	–	–	V
	P-channel	V_{GS} = V_{DS}; I_D = −1 mA	−1	–	–	V
I_{DSS}	drain-source leakage current					
	N-channel	V_{GS} = 0; V_{DS} = 24 V	–	–	100	nA
	P-channel	V_{GS} = 0; V_{DS} = −24 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0				
	N-channel		–	–	±100	nA
	P-channel		–	–	±100	nA
R_{DSon}	drain-source on-state resistance					
	N-channel	V_{GS} = 4.5 V; I_D = 2 A	–	–	45	mΩ
		V_{GS} = 10 V; I_D = 4 A	–	–	30	mΩ
	P-channel	V_{GS} = −4.5 V; I_D = −1.4 A	–	–	100	mΩ
		V_{GS} = −10 V; I_D = −2.8 A	–	–	65	mΩ
C_{iss}	input capacitance					
	N-channel	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	700	850	pF
	P-channel	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	tbf	tbf	pF
C_{oss}	output capacitance					
	N-channel	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	260	320	pF
	P-channel	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	tbf	tbf	pF
C_{rss}	reverse transfer capacitance					
	N-channel	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	110	135	pF
	P-channel	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	tbf	tbf	pF
Q_G	total gate charge					
	N-channel	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 4 A	–	16	30	nC
	P-channel	V_{GS} = −10 V; V_{DD} = −15 V; I_D = −2.8 A	–	tbf	tbf	nC
Q_{GS}	gate-source charge					
	N-channel	V_{DD} = 15 V; I_D = 4 A	–	2	–	nC
	P-channel	V_{DD} = −15 V; I_D = −2.8 A	–	tbf	–	nC

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Q_{GD}	gate-drain charge					
	N-channel	V_{DD} = 15 V; I_D = 4 A	–	6.5	–	nC
	P-channel	V_{DD} = −15 V; I_D = −2.8 A	–	tbf	–	nC
Switching times						
$t_{d(on)}$	turn-on delay time					
	N-channel	V_{GS} = 0 to 10 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	8	–	ns
	P-channel	V_{GS} = 0 to −10 V; V_{DD} = −20 V; I_D = −1 A; R_{gen} = 6 Ω	–	tbf	–	ns
t_r	rise time					
	N-channel	V_{GS} = 10 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	21	–	ns
	P-channel	V_{GS} = 0 to −10 V; V_{DD} = −20 V; I_D = −1 A; R_{gen} = 6 Ω	–	tbf	–	ns
t_{on}	turn-on switching time					
	N-channel	V_{GS} = 0 to 10 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	17	25	ns
	P-channel	V_{GS} = 0 to −10 V; V_{DD} = −20 V; I_D = −1 A; R_{gen} = 6 Ω	–	tbf	tbf	ns
$t_{d(off)}$	turn-off delay time					
	N-channel	V_{GS} = 10 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	19	–	ns
	P-channel	V_{GS} = −10 to 0 V; V_{DD} = −20 V; I_D = −1 A; R_{gen} = 6 Ω	–	tbf	–	ns
t_f	fall time					
	N-channel	V_{GS} = 0 to 10 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	9	–	ns
	P-channel	V_{GS} = −10 to 0 V; V_{DD} = −20 V; I_D = −1 A; R_{gen} = 6 Ω	–	tbf	–	ns
t_{off}	turn-off switching time					
	N-channel	V_{GS} = 10 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	40	60	ns
	P-channel	V_{GS} = −10 to 0 V; V_{DD} = −20 V; I_D = −1 A; R_{gen} = 6 Ω	–	tbf	tbf	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage					
	N-channel	V_{GD} = 0; I_S = 1.25 A	–	–	1	V
	P-channel	V_{GD} = 0; I_S = −1.25 A	–	–	−1.3	V
t_{rr}	reverse recovery time					
	N-channel	I_S = 1.25 A; di/dt = −100 A/μs	–	45	–	ns
	P-channel	I_S = −1.25 A; di/dt = 100 A/μs	–	tbf	–	ns

Complementary enhancement mode MOS transistors

PHC20512

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-state resistance.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

DESCRIPTION

One N-channel and one P-channel enhancement mode MOS transistor in an 8-pin plastic SOT96-1 (SO8) package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s_1	source 1
2	g_1	gate 1
3	s_2	source 2
4	g_2	gate 2
5	d_2	drain 2
6	d_2	drain 2
7	d_1	drain 1
8	d_1	drain 1

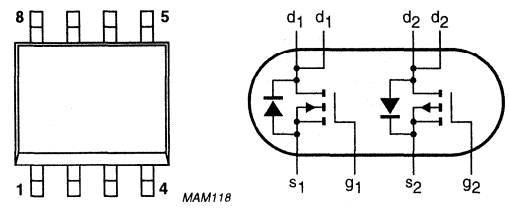


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per channel					
V_{DS}	drain-source voltage (DC)				
	N-channel		–	30	V
	P-channel		–	–30	V
V_{SD}	source-drain diode forward voltage				
	N-channel	I_S = 1.25 A	–	1	V
	P-channel	I_S = –1.25 A	–	–1.3	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage				
	N-channel	$V_{DS} = V_{GS}$; I_D = 1 mA	1	2.8	V
	P-channel	$V_{DS} = V_{GS}$; I_D = –1 mA	–1	–2.8	V
I_D	drain current (DC)	T_s = 80 °C			
	N-channel		–	6.4	A
	P-channel		–	–4	A
R_{DSon}	drain-source on-state resistance				
	N-channel	V_{GS} = 10 V; I_D = 3.2 A	–	0.05	Ω
	P-channel	V_{GS} = –10 V I_D = –2 A	–	0.12	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	3.5	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per channel					
V_{DS}	drain-source voltage (DC)				
	N-channel		–	30	V
	P-channel		–	–30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1			
	N-channel		–	6.4	A
	P-channel		–	–4	A
I_{DM}	peak drain current	note 2			
	N-channel		–	25	A
	P-channel		–	–16	A
P_{tot}	total power dissipation	T_s = 80 °C; note 3	–	3.5	W
		T_{amb} = 25 °C; note 4	–	2.6	W
		T_{amb} = 25 °C; note 5	–	1.1	W
		T_{amb} = 25 °C; note 6	–	1.5	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–65	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C			
	N-channel		–	3.5	A
	P-channel		–	–2.6	A
I_{SM}	peak pulsed source current	note 2			
	N-channel		–	14	A
	P-channel		–	–10	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Maximum permissible dissipation per MOS transistor. Both devices may be loaded up to 3.5 W at the same time.
4. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
5. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.
6. Maximum permissible dissipation if only one MOS transistor dissipates. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

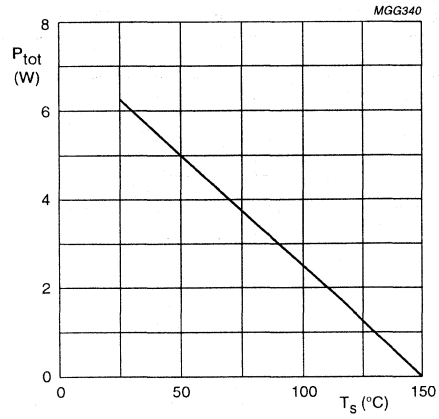
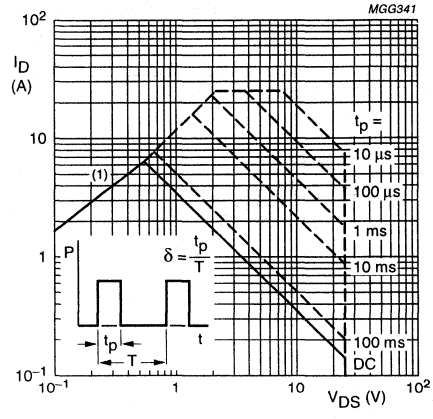
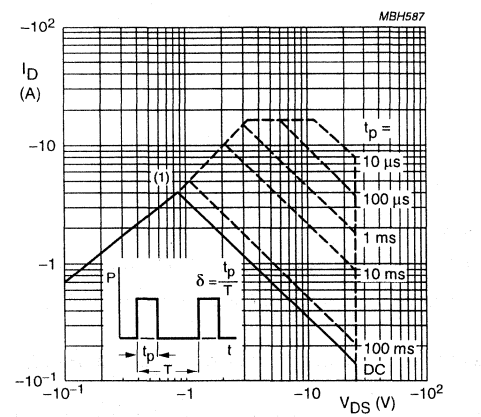


Fig.2 Power derating curve.



$\delta = 0.01$; $T_s = 80$ °C.
(1) R_{DSon} limitation.

Fig.3 SOAR; N-channel.



$\delta = 0.01$; $T_s = 80$ °C.
(1) R_{DSon} limitation.

Fig.4 SOAR; P-channel.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	20	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per channel						
$V_{(BR)DSS}$	drain-source breakdown voltage					
	N-channel	V_{GS} = 0; I_D = 10 μA	30	–	–	V
	P-channel	V_{GS} = 0; I_D = −10 μA	−30	–	–	V
V_{GSth}	gate-source threshold voltage					
	N-channel	V_{GS} = V_{DS}; I_D = 1 mA	1	–	2.8	V
	P-channel	V_{GS} = V_{DS}; I_D = −1 mA	−1	–	−2.8	V
I_{DSS}	drain-source leakage current					
	N-channel	V_{GS} = 0; V_{DS} = 24 V	–	–	100	nA
	P-channel	V_{GS} = 0; V_{DS} = −24 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0				
	N-channel		–	–	±100	nA
	P-channel		–	–	±100	nA
R_{DSon}	drain-source on-state resistance					
	N-channel	V_{GS} = 4.5 V; I_D = 1.6 A	–	–	0.1	Ω
		V_{GS} = 10 V; I_D = 3.2 A	–	–	0.05	Ω
	P-channel	V_{GS} = −4.5 V; I_D = −1 A	–	–	0.25	Ω
		V_{GS} = −10 V; I_D = −2 A	–	–	0.12	Ω
C_{iss}	input capacitance					
	N-channel	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	450	–	pF
	P-channel	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	450	–	pF
C_{oss}	output capacitance					
	N-channel	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	200	–	pF
	P-channel	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	200	–	pF
C_{rss}	reverse transfer capacitance					
	N-channel	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	100	–	pF
	P-channel	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	100	–	pF
Q_G	total gate charge					
	N-channel	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 3.2 A	–	15	–	nC
	P-channel	V_{GS} = −10 V; V_{DD} = −15 V; I_D = −2 A	–	13	–	nC
Q_{GS}	gate-source charge					
	N-channel	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 3.2 A	–	1	–	nC
	P-channel	V_{GS} = −10 V; V_{DD} = −15 V; I_D = −2 A	–	1	–	nC

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Q_{GD}	gate-drain charge					
	N-channel	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 3.2 A	–	5	–	nC
	P-channel	V_{GS} = −10 V; V_{DD} = −15 V; I_D = −2 A	–	4	–	nC
$t_{d(on)}$	turn-on delay time					
	N-channel	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω	–	7	–	ns
	P-channel	V_{GS} = 0 to −10 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω	–	6	–	ns
$t_{d(off)}$	turn-off delay time					
	N-channel	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω	–	20	–	ns
	P-channel	V_{GS} = −10 to 0 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω	–	29	–	ns
t_f	fall time					
	N-channel	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω	–	8	–	ns
	P-channel	V_{GS} = −10 to 0 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω	–	16	–	ns
t_r	rise time					
	N-channel	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω	–	12	–	ns
	P-channel	V_{GS} = 0 to −10 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω	–	4	–	ns
t_{on}	turn-on switching time					
	N-channel	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω	–	15	–	ns
	P-channel	V_{GS} = 0 to −10 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω	–	10	–	ns
t_{off}	turn-off switching time					
	N-channel	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω	–	32	–	ns
	P-channel	V_{GS} = −10 to 0 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω	–	45	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage					
	N-channel	V_{GD} = 0; I_S = 1.25 A	–	–	1	V
	P-channel	V_{GD} = 0; I_S = −1.25 A	–	–	−1.3	V
t_{rr}	reverse recovery time					
	N-channel	I_S = 1.25 A; di/dt = −100 A/μs	–	45	–	ns
	P-channel	I_S = −1.25 A; di/dt = 100 A/μs	–	75	–	ns

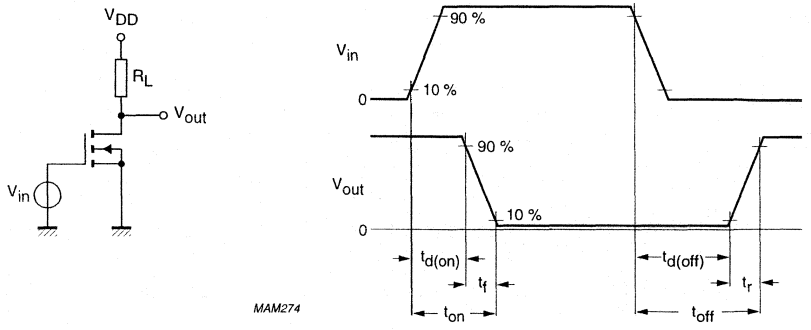


Fig.5 Switching times test circuit with input and output waveforms; N-channel.

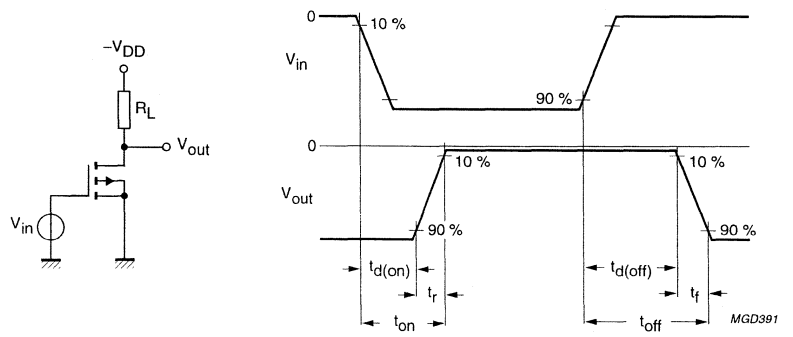
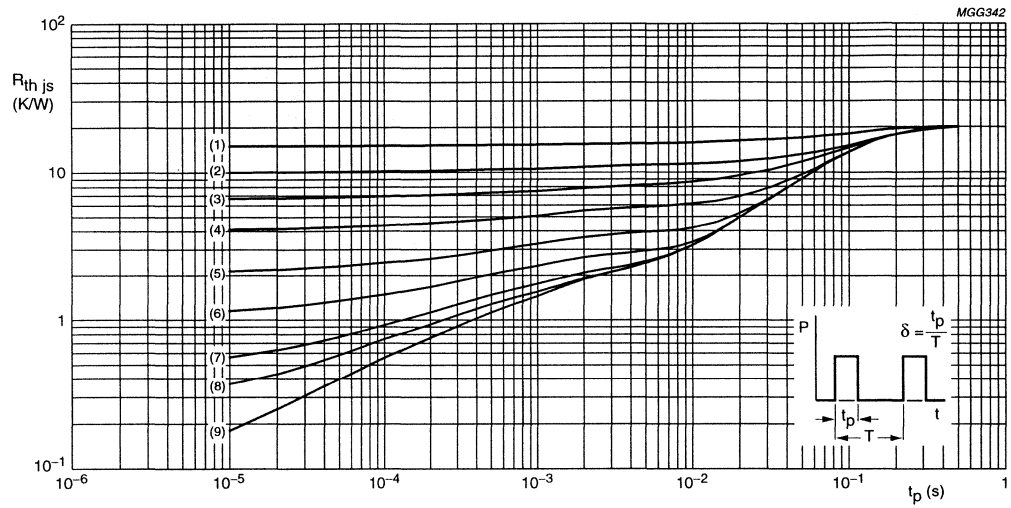


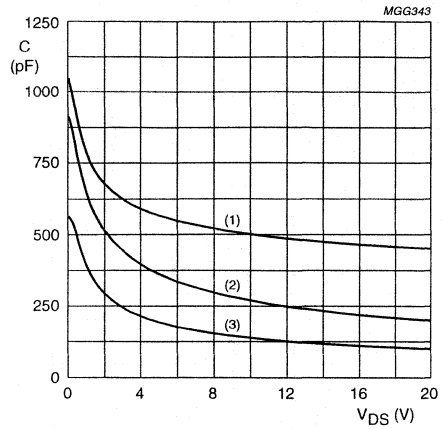
Fig.6 Switching times test circuit with input and output waveforms; P-channel.



(1) $\delta = 0.75$. (2) $\delta = 0.5$. (3) $\delta = 0.33$. (4) $\delta = 0.2$.

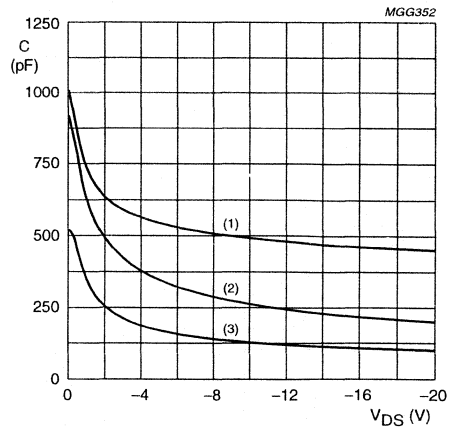
(5) $\delta = 0.1$. (6) $\delta = 0.05$. (7) $\delta = 0.02$. (8) $\delta = 0.01$. (9) $\delta = 0$.

Fig.7 Transient thermal resistance from junction to soldering point as a function of pulse time for N- and P-channels; typical values.



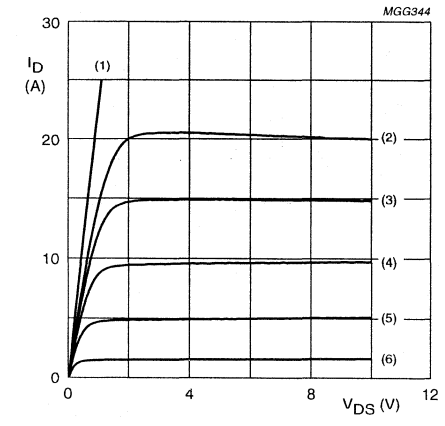
V_{GS} = 0; f = 1 MHz; T_j = 25 °C.
(1) C_{iss}.
(2) C_{oss}.
(3) C_{rss}.

Fig.8 Capacitance as a function of drain-source voltage; N-channel typical values.



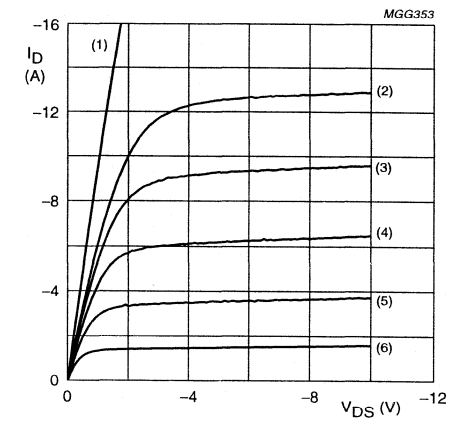
V_{GS} = 0; f = 1 MHz; T_j = 25 °C.
(1) C_{iss}.
(2) C_{oss}.
(3) C_{rss}.

Fig.9 Capacitance as a function of drain source voltage; P-channel typical values.



T_{amb} = 25 °C; t_p = 80 µs; δ = 0.
(1) V_{GS} = 10 V.
(2) V_{GS} = 5 V.
(3) V_{GS} = 4.5 V.
(4) V_{GS} = 4 V.
(5) V_{GS} = 3.5 V.
(6) V_{GS} = 3 V.

Fig.10 Output characteristics; N-channel typical values.



T_{amb} = 25 °C; t_p = 80 µs; δ = 0.
(1) V_{GS} = −10 V.
(2) V_{GS} = −5 V.
(3) V_{GS} = −4.5 V.
(4) V_{GS} = −4 V.
(5) V_{GS} = −3.5 V.
(6) V_{GS} = −3 V.

Fig.11 Output characteristics; P-channel typical values.

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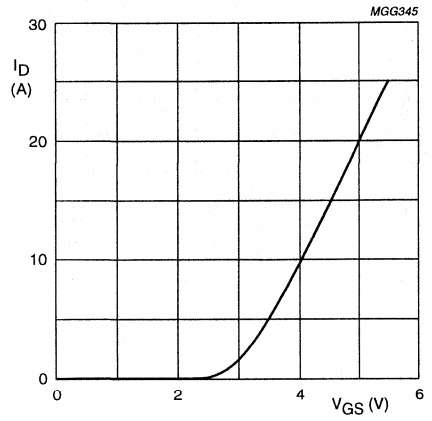
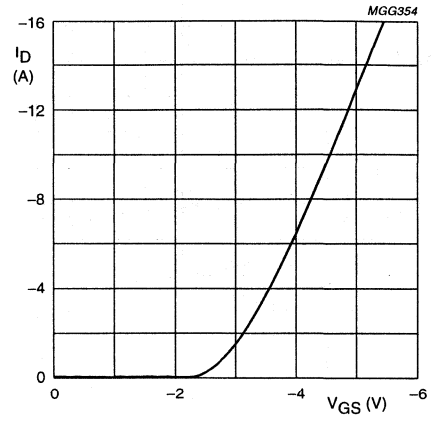


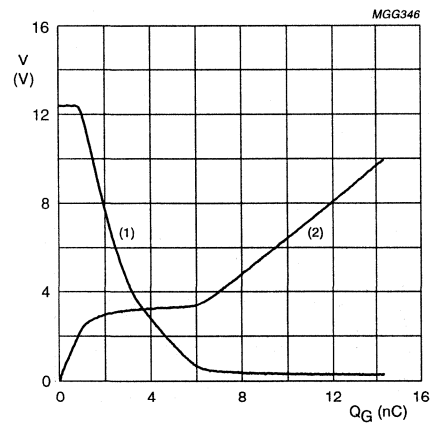
V_{DS} = 10 V; T_{amb} = 25 °C; t_p = 80 µs; δ = 0.

Fig.12 Transfer characteristic; N-channel typical values.



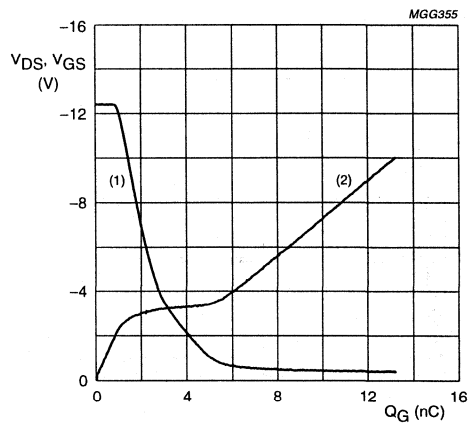
V_{DS} = −10 V; T_{amb} = 25 °C; t_p = 80 µs; δ = 0.

Fig.13 Transfer characteristic; P-channel typical values.



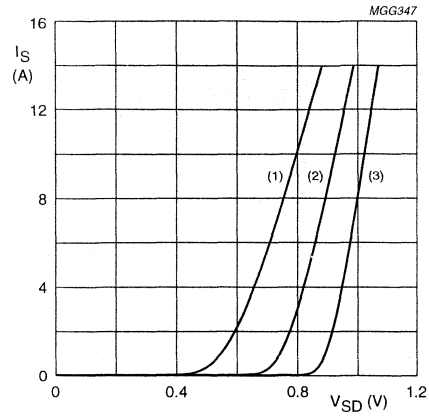
V_{DD} = 12.5 V; I_D = 3.2 A; T_{amb} = 25 °C.
(1) V_{DS}.
(2) V_{GS}.

Fig.14 Gate-source voltage and drain-source voltage as a function of total gate charge; N-channel typical values.



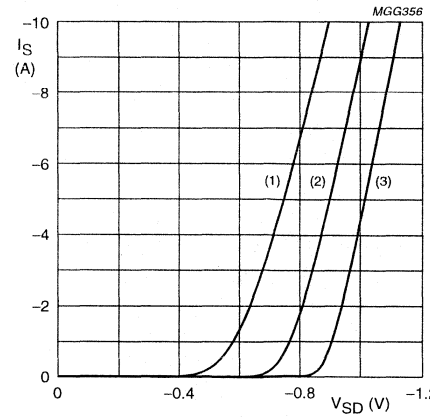
V_{DD} = −12.5 V; I_D = −2 A; T_{amb} = 25 °C.
(1) V_{DS}.
(2) V_{GS}.

Fig.15 Gate-source voltage and drain-source voltage as a function of total gate charge; P-channel typical values.



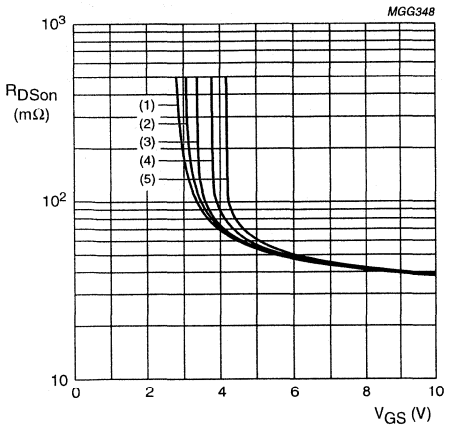
V_{GD} = 0.
(1) T_{amb} = 150 °C; t_p = 300 μs; δ = 0.
(2) T_{amb} = 25 °C; t_p = 300 μs; δ = 0.
(3) T_{amb} = −65 °C; t_p = 300 μs; δ = 0.

Fig.16 Source current as a function of source-drain diode forward voltage; N-channel typical values.



V_{GD} = 0.
(1) T_{amb} = 150 °C; t_p = 300 μs; δ = 0.
(2) T_{amb} = 25 °C; t_p = 300 μs; δ = 0.
(3) T_{amb} = −65 °C; t_p = 300 μs; δ = 0.

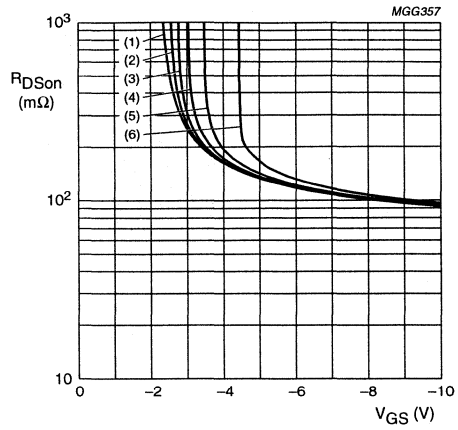
Fig.17 Source current as a function of source-drain diode forward voltage; P-channel typical values.



$V_{DS} \geq I_D \times R_{DSon}$; T_{amb} = 25 °C; t_p = 300 μs; δ = 0.

(1) I_D = 0.5 A.
(2) I_D = 1.6 A.
(3) I_D = 3.2 A.
(4) I_D = 6.4 A.
(5) I_D = 10 A.

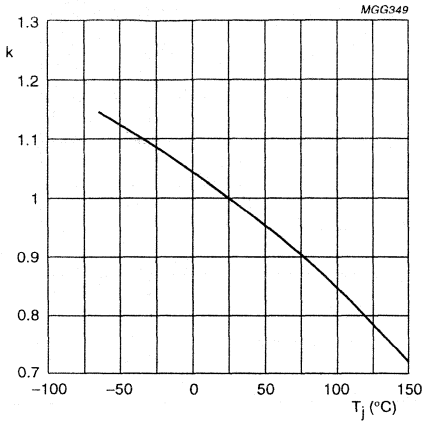
Fig.18 Drain-source on-state resistance as a function of gate-source voltage; N-channel typical values.



$V_{DS} \geq I_D \times R_{DSon}$; T_{amb} = 25 °C; t_p = 300 μs; δ = 0.

(1) I_D = 0.1 A.
(2) I_D = 0.5 A.
(3) I_D = 1 A.
(4) I_D = 2 A.
(5) I_D = 4 A.
(6) I_D = 8 A.

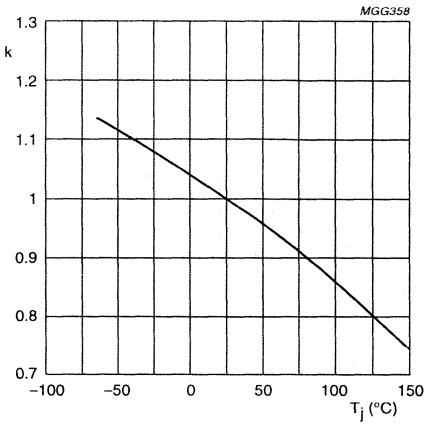
Fig.19 Drain-source on-state resistance as a function of gate-source voltage; P-channel typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

V_{GSth} at $V_{DS} = V_{GS}$; $I_D = 1$ mA.

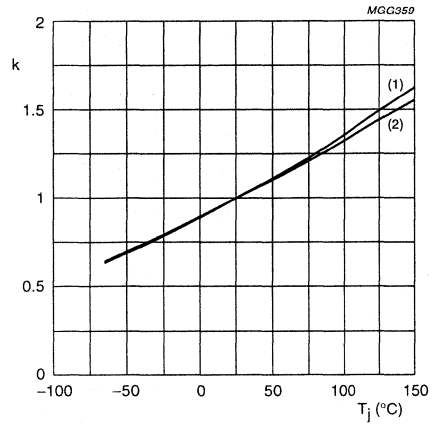
Fig.20 Temperature coefficient of gate-source threshold voltage as a function of junction temperature; N-channel typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

V_{GSth} at $V_{DS} = V_{GS}$; $I_D = -1$ mA.

Fig.21 Temperature coefficient of gate-source threshold voltage as function of junction temperature; P-channel typical values.

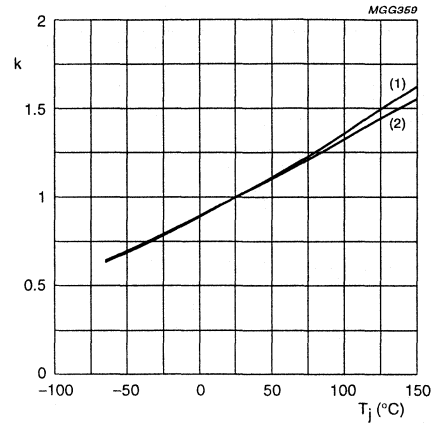


$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

(1) R_{DSon} at V_{GS} = 10 V; I_D = 3.2 A.

(2) R_{DSon} at V_{GS} = 4.5 V; I_D = 1.6 A.

Fig.22 Temperature coefficient of drain-source on-resistance as a function of junction temperature; N-channel typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

(1) R_{DSon} at V_{GS} = −10 V; I_D = −2 A.

(2) R_{DSon} at V_{GS} = −4.5 V; I_D = −1 A.

Fig.23 Temperature coefficient of drain-source on-resistance as a function of junction temperature; P-channel typical values.

Complementary enhancement mode MOS transistors

PHC21025

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

DESCRIPTION

One N-channel and one P-channel enhancement mode MOS transistor in an 8-pin plastic SOT96-1 (SO8) package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s_1	source 1
2	g_1	gate 1
3	s_2	source 2
4	g_2	gate 2
5	d_2	drain 2
6	d_2	drain 2
7	d_1	drain 1
8	d_1	drain 1

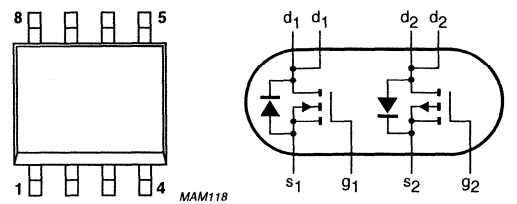


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per channel					
V_{DS}	drain-source voltage (DC)				
	N-channel		–	30	V
	P-channel		–	–30	V
V_{SD}	source-drain diode forward voltage				
	N-channel	I_S = 1.25 A	–	1.2	V
	P-channel	I_S = –1.25 A	–	–1.6	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage				V
	N-channel	$V_{DS} = V_{GS}$; I_D = 1 mA	1	2.8	V
	P-channel	$V_{DS} = V_{GS}$; I_D = –1 mA	–1	–2.8	V
I_D	drain current (DC)				
	N-channel		–	3.5	A
	P-channel		–	–2.3	A
R_{DSon}	drain-source on-state resistance				
	N-channel	V_{GS} = 10 V; I_D = 2.2 A	–	0.1	Ω
	P-channel	V_{GS} = –10 V; I_D = –1 A	–	0.25	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	2	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per channel					
V_{DS}	drain-source voltage (DC)				
	N-channel		–	30	V
	P-channel		–	–30	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)	$T_s \leq 80$ °C			
	N-channel		–	3.5	A
	P-channel		–	–2.3	A
I_{DM}	peak drain current	note 1			
	N-channel		–	14	A
	P-channel		–	–10	A
P_{tot}	total power dissipation	T_s = 80 °C; note 2	–	2	W
		T_{amb} = 25 °C; note 3	–	2	W
		T_{amb} = 25 °C; note 4	–	1	W
		T_{amb} = 25 °C; note 5	–	1.3	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C
Source-drain diode					
I_S	source current (DC)	$T_s \leq 80$ °C			
	N-channel		–	1.5	A
	P-channel		–	–1.25	A
I_{SM}	peak pulsed source current	note 1			
	N-channel		–	6	A
	P-channel		–	–5	A

Notes

1. Pulse width and duty cycle limited by maximum junction temperature.
2. Maximum permissible dissipation per MOS transistor. Both devices may be loaded up to 2 W at the same time.
3. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.
5. Maximum permissible dissipation if only one MOS transistor dissipates. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

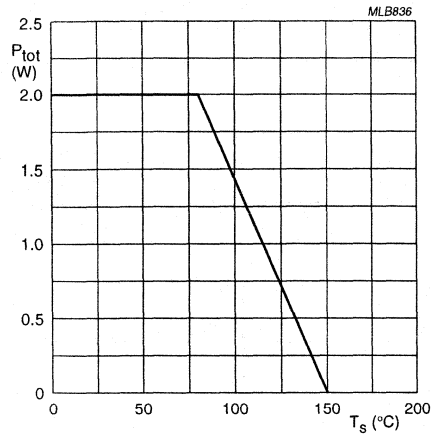
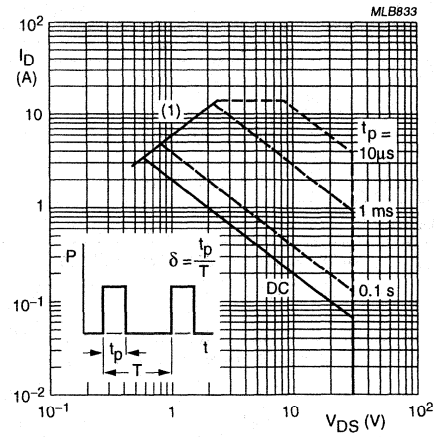
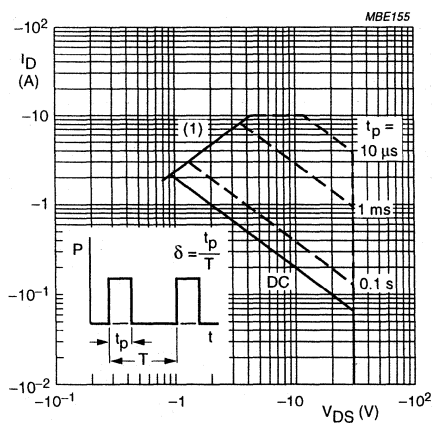


Fig.2 Power derating curve.



$\delta = 0.01$.
$T_s = 80$ °C.
(1) R_{DSon} limitation.

Fig.3 SOAR; N-channel.



$\delta = 0.01$.
$T_s = 80$ °C.
(1) R_{DSon} limitation.

Fig.4 SOAR; P-channel.

THERMAL CHARACTERISTICS

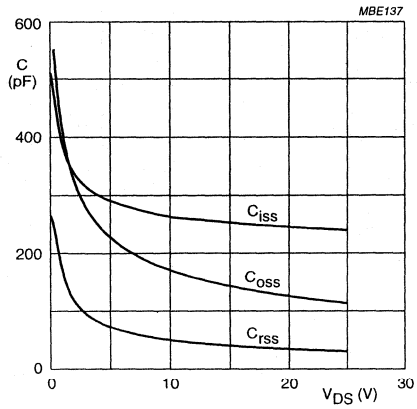
SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	35	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

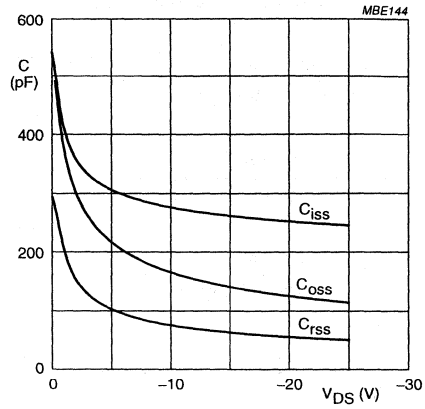
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per channel						
$V_{(BR)DSS}$	drain-source breakdown voltage					
	N-channel	V_{GS} = 0; I_D = 10 μA	30	–	–	V
	P-channel	V_{GS} = 0; I_D = −10 μA	−30	–	–	V
V_{GSth}	gate-source threshold voltage					
	N-channel	V_{GS} = V_{DS}; I_D = 1 mA	1	–	2.8	V
	P-channel	V_{GS} = V_{DS}; I_D = −1 mA	−1	–	−2.8	V
I_{DSS}	drain-source leakage current					
	N-channel	V_{GS} = 0; V_{DS} = 24 V	–	–	100	nA
	P-channel	V_{GS} = 0; V_{DS} = −24 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0				
	N-channel		–	–	±100	nA
	P-channel		–	–	±100	nA
I_{Don}	on-state drain current					
	N-channel	V_{GS} = 10 V; V_{DS} = 1 V	3.5	–	–	A
		V_{GS} = 4.5 V; V_{DS} = 5 V	2	–	–	A
	P-channel	V_{GS} = −10 V; V_{DS} = −1 V	−2.3	–	–	A
		V_{GS} = −4.5 V; V_{DS} = −5 V	−1	–	–	A
R_{DSon}	drain-source on-state resistance					
	N-channel	V_{GS} = 4.5 V; I_D = 1 A	–	0.11	0.2	Ω
		V_{GS} = 10 V; I_D = 2.2 A	–	0.08	0.1	Ω
	P-channel	V_{GS} = −4.5 V; I_D = − 0.5 A	–	0.33	0.4	Ω
		V_{GS} = −10 V; I_D = −1 A	–	0.22	0.25	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance					
	N-channel	V_{DS} = 20 V; I_D = 2.2 A	2	4.5	–	S
	P-channel	V_{DS} = −20 V; I_D = −1 A	1	2	–	S
C_{iss}	input capacitance					
	N-channel	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	–	250	–	pF
	P-channel	V_{GS} = 0; V_{DS} = −20 V; f = 1 MHz	–	250	–	pF
C_{oss}	output capacitance					
	N-channel	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	–	140	–	pF
	P-channel	V_{GS} = 0; V_{DS} = −20 V; f = 1 MHz	–	140	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{rss}	reverse transfer capacitance					
	N-channel	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	–	50	–	pF
	P-channel	V_{GS} = 0; V_{DS} = –20 V; f = 1 MHz	–	50	–	pF
Q_G	total gate charge					
	N-channel	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	–	10	30	nC
	P-channel	V_{GS} = –10 V; V_{DS} = –15 V; I_D = –2.3 A	–	10	25	nC
Q_{GS}	gate-source charge					
	N-channel	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	–	1	–	nC
	P-channel	V_{GS} = –10 V; V_{DS} = –15 V; I_D = –2.3 A	–	1	–	nC
Q_{GD}	gate-drain charge					
	N-channel	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	–	2.5	–	nC
	P-channel	V_{GS} = –10 V; V_{DS} = –15 V; I_D = –2.3 A	–	3	–	nC
Switching times						
t_{on}	turn-on time					
	N-channel	V_{GS} = 0 to 10 V; V_{DD} = 20 V; I_D = 1 A; R_L = 20 Ω	–	15	40	ns
	P-channel	V_{GS} = 0 to –10 V; V_{DD} = –20 V; I_D = –1 A; R_L = 20 Ω	–	20	80	ns
t_{off}	turn-off time					
	N-channel	V_{GS} = 10 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_L = 20 Ω	–	25	140	ns
	P-channel	V_{GS} = –10 to 0 V; V_{DD} = –20 V; I_D = –1 A; R_L = 20 Ω	–	50	140	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage					
	N-channel	V_{GD} = 0; I_S = 1.25 A	–	–	1.2	V
	P-channel	V_{GD} = 0; I_S = –1.25 A	–	–	–1.6	V
t_{rr}	reverse recovery time					
	N-channel	I_S = 1.25 A; di/dt = 100 A/μs	–	35	100	ns
	P-channel	I_S = –1.25 A; di/dt = 100 A/μs	–	150	200	ns



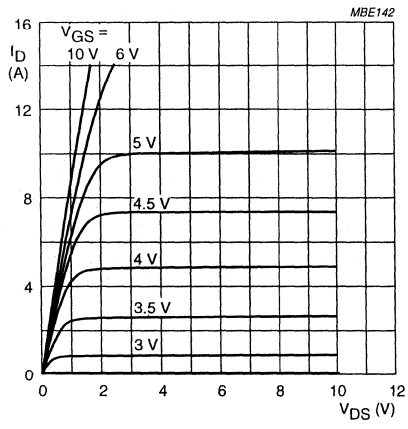
V_{GS} = 0.
T_j = 25 °C.

Fig.5 Capacitance as a function of drain-source voltage; N-channel; typical values.



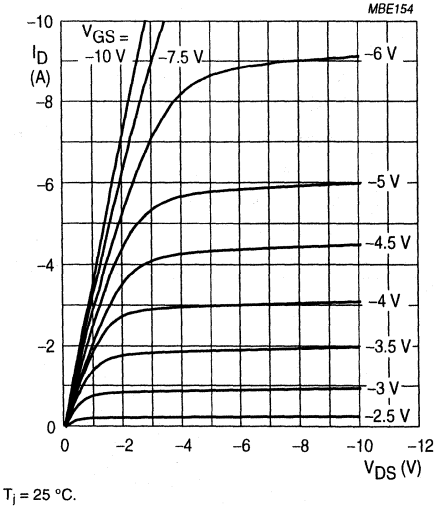
V_{GS} = 0.
T_j = 25 °C.

Fig.6 Capacitance as a function of drain source voltage; P-channel; typical values.



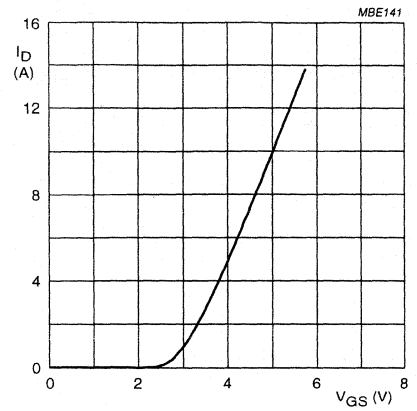
T_j = 25 °C.

Fig.7 Output characteristics; typical values; N-channel.



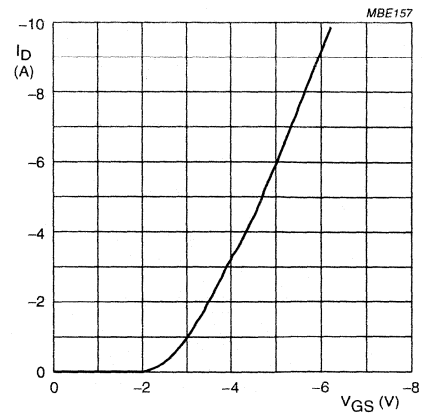
T_j = 25 °C.

Fig.8 Output characteristics; typical values; P-channel.



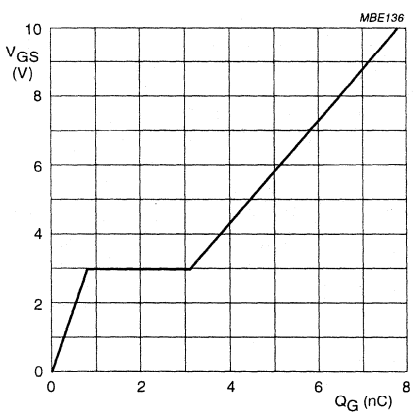
V_{DS} = 10 V.
T_j = 25 °C.

Fig.9 Transfer characteristic; typical values; N-channel.



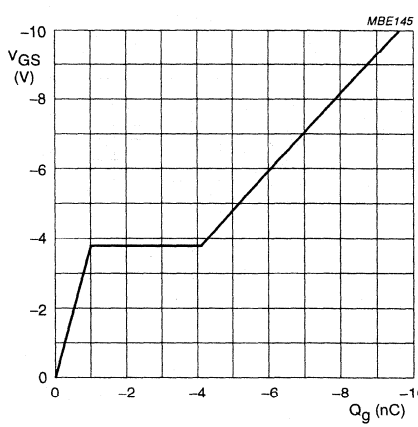
V_{DS} = −10 V.
T_j = 25 °C.

Fig.10 Transfer characteristic; typical values; P-channel.



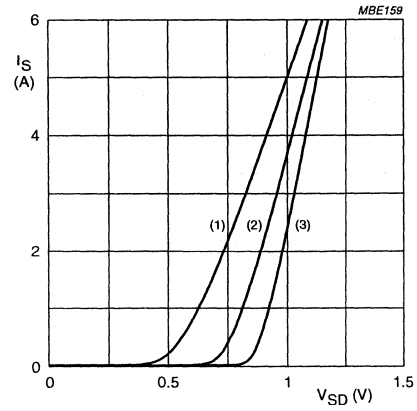
V_{DD} = 15 V.
I_D = 3.5 A.

Fig.11 Gate-source voltage as a function of total gate charge; N-channel.



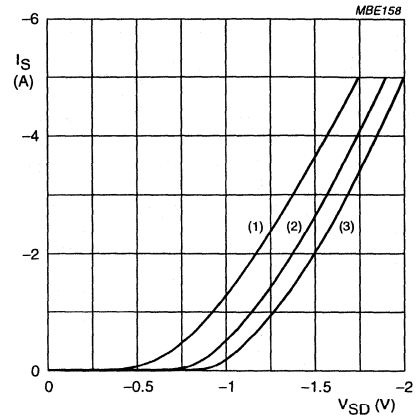
V_{DD} = −15 V.
I_D = −2.3 A.

Fig.12 Gate-source voltage as a function of total gate charge; P-channel.



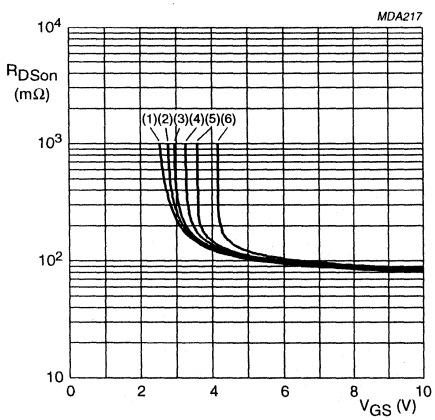
V_{GD} = 0.
(1) T_j = 150 °C.
(2) T_j = 25 °C.
(3) T_j = −55 °C.

Fig.13 Source current as a function of source-drain diode forward voltage; N-channel.



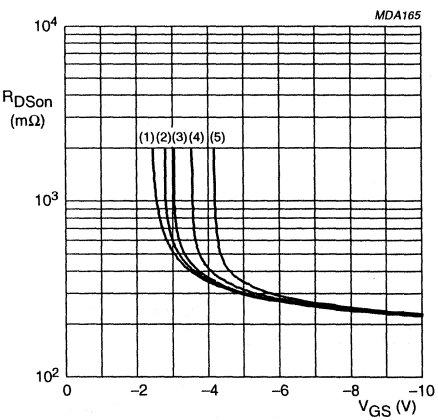
V_{GD} = 0.
(1) T_j = 150 °C.
(2) T_j = 25 °C.
(3) T_j = −55 °C.

Fig.14 Source current as a function of source-drain diode forward voltage; P-channel.



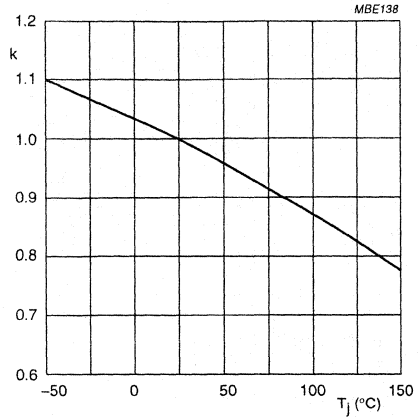
$V_{DS} \geq I_D \times R_{DSon}$; T_j = 25 °C.
(1) I_D = 0.1 A.
(2) I_D = 0.5 A.
(3) I_D = 1 A.
(4) I_D = 2.2 A.
(5) I_D = 3.5 A.
(6) I_D = 7 A.

Fig.15 Drain-source on-state resistance as a function of gate-source voltage; typical values; N-channel.



$-V_{DS} \geq -I_D \times R_{DSon}$; T_j = 25 °C.
(1) I_D = −0.1 A.
(2) I_D = −0.5 A.
(3) I_D = −1 A.
(4) I_D = −2.3 A.
(5) I_D = −4.5 A.

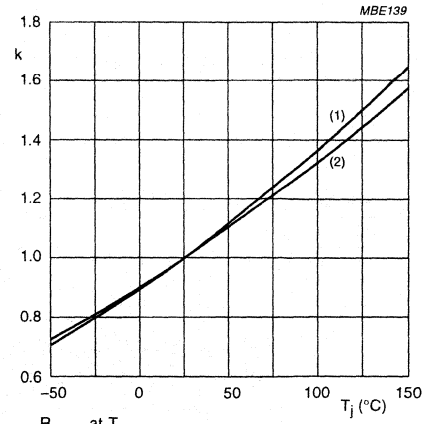
Fig.16 Drain-source on-state resistance as a function of gate-source voltage; typical values; P-channel.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

Typical V_{GSth} at I_D = 1 mA; $V_{DS} = V_{GS} = V_{GSth}$.

Fig.17 Temperature coefficient of gate-source threshold voltage; N and P-channels.



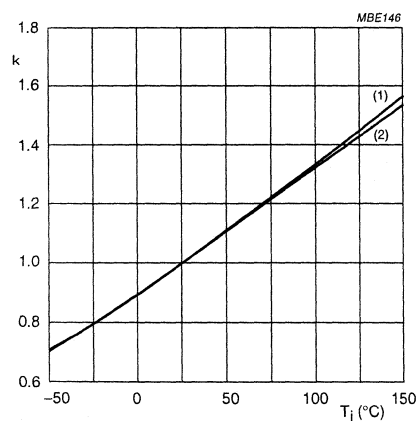
$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

Typical R_{DSon} at:

(1) I_D = 2.2 A; V_{GS} = 10 V.

(2) I_D = 1 A; V_{GS} = 4.5 V.

Fig.18 Temperature coefficient of drain-source on-resistance; N-channel.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

Typical R_{DSon} at:

(1) I_D = −1 A; V_{GS} = −10 V.

(2) I_D = −0.5 A; V_{GS} = −4.5 V.

Fig.19 Temperature coefficient of drain-source on-resistance; P-channel.

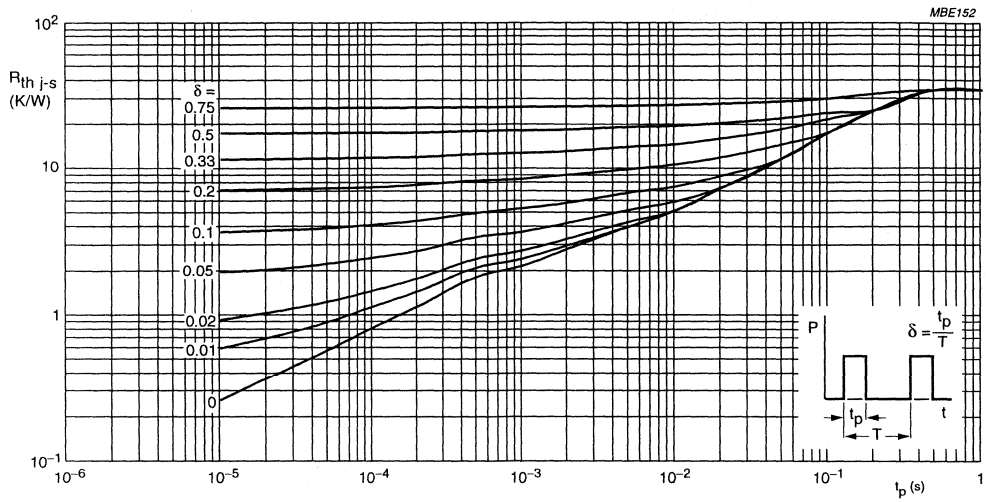


Fig.20 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

PowerMOS transistor | PHD3N20E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mounting featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

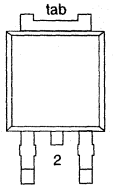
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (DC)	3.5	A
P_{tot}	Total power dissipation	50	W
$R_{DS(ON)}$	Drain-source on-state resistance	1.5	Ω

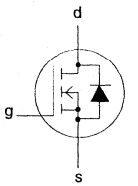
PINNING - SOT428

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	3.5	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	2.5	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	14	A
P_D	Total dissipation	T_{mb} = 25 °C	-	50	W
$\Delta P_D/\Delta T_{mb}$	Linear derating factor	T_{mb} > 25 °C	-	0.33	W/K
V_{GS}	Gate-source voltage		-	± 30	V
E_{AS}	Single pulse avalanche energy	$V_{DD} \leq 50$ V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	25	mJ
I_{AS}	Peak avalanche current	$V_{DD} \leq 50$ V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	3.5	A
T_j, T_{stg}	Operating junction and storage temperature range		- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	3	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	pcb mounted, minimum footprint	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.25	-	V/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 2 A	-	0.77	1.5	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 50 V; I_D = 2 A	0.8	3.0	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 200 V; V_{GS} = 0 V	-	0.1	25	µA
		V_{DS} = 160 V; V_{GS} = 0 V; T_j = 150 °C	-	1	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$Q_{g(tot)}$	Total gate charge	I_D = 3.3 A; V_{DD} = 160 V; V_{GS} = 10 V	-	10	12	nC
Q_{gs}	Gate-source charge		-	1.1	2	nC
Q_{gd}	Gate-drain (Miller) charge		-	4.5	6	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 100 V; I_D = 3.3 A;	-	8	-	ns
t_r	Turn-on rise time	R_G = 24 Ω; R_D = 30 Ω	-	20	-	ns
$t_{d(off)}$	Turn-off delay time		-	30	-	ns
t_f	Turn-off fall time		-	25	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_s	Internal source inductance	Measured from source lead solder point to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	200	-	pF
C_{oss}	Output capacitance		-	48	-	pF
C_{rss}	Feedback capacitance		-	20	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	3.5	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	14	A
V_{SD}	Diode forward voltage	I_S = 3.3 A; V_{GS} = 0 V	-	-	1.5	V
t_{rr}	Reverse recovery time	I_S = 3.3 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	90	-	ns
Q_{rr}	Reverse recovery charge		-	0.5	-	µC

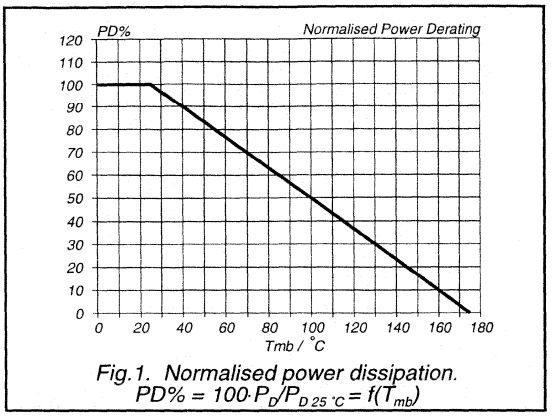


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

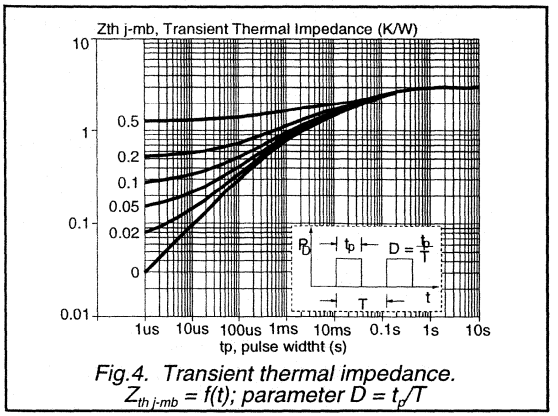


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

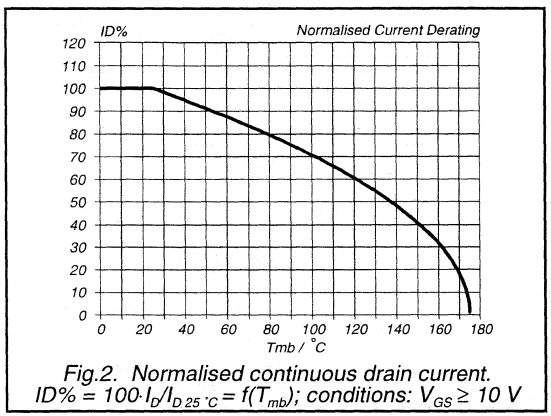


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

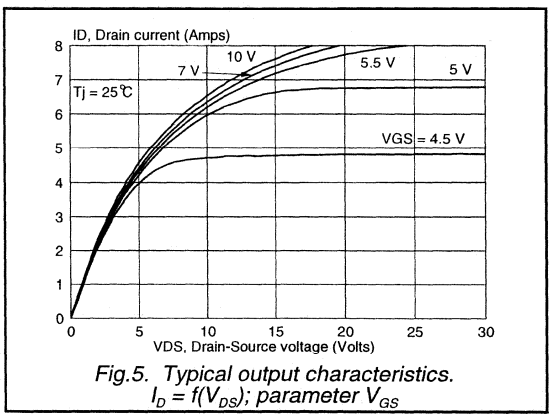


Fig.5. Typical output characteristics.
I_D = f(V_{DS}); parameter V_{GS}

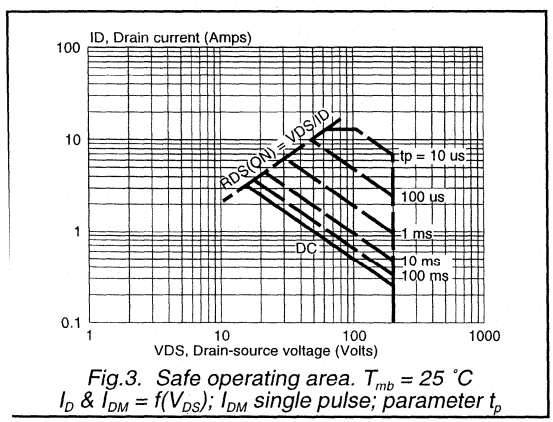


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

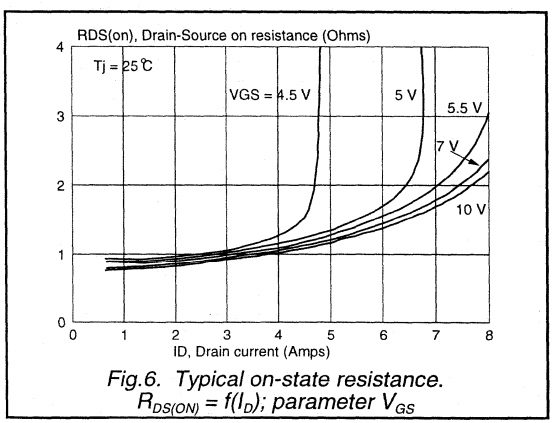


Fig.6. Typical on-state resistance.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

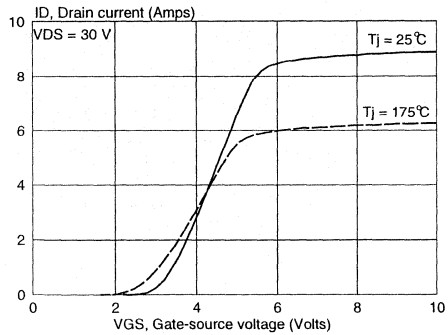


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; parameter T_j

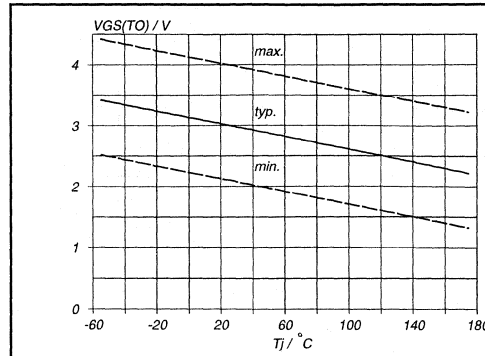


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

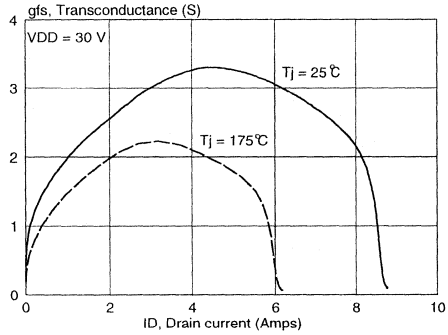


Fig.8. Typical transconductance. $g_{fs} = f(I_D)$; parameter T_j

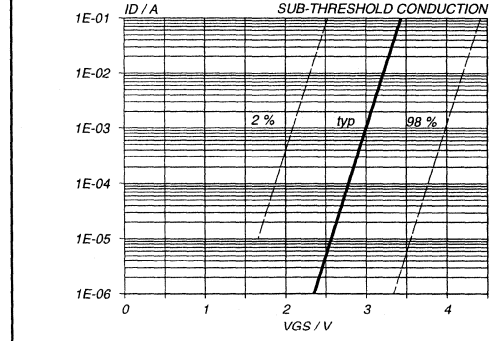


Fig.11. Sub-threshold drain current. $I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

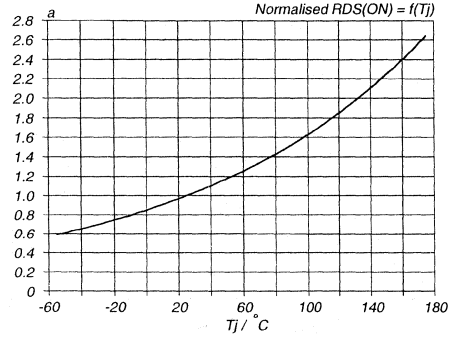


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,^{\circ}C} = f(T_j)$; I_D = 3.3 A; V_{GS} = 10 V

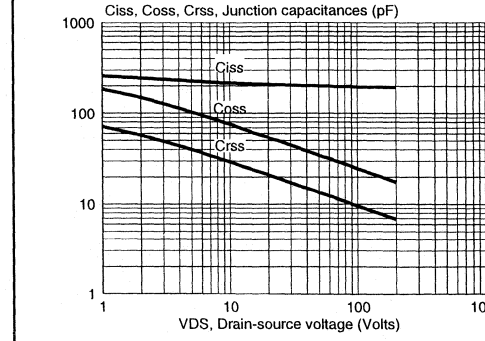


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

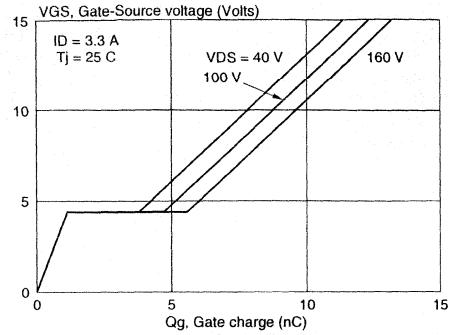


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; *parameter* V_{DS}

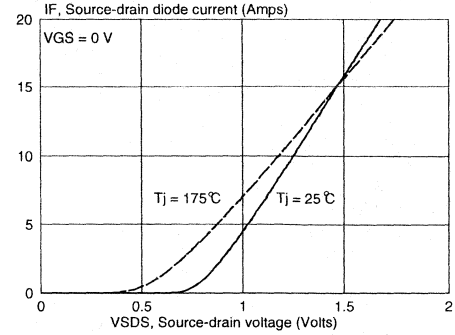


Fig.16. Source-Drain diode characteristic. $I_F = f(V_{SDS})$; *parameter* T_j

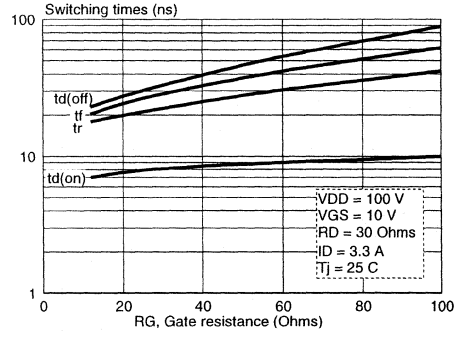


Fig.14. Typical switching times. $t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

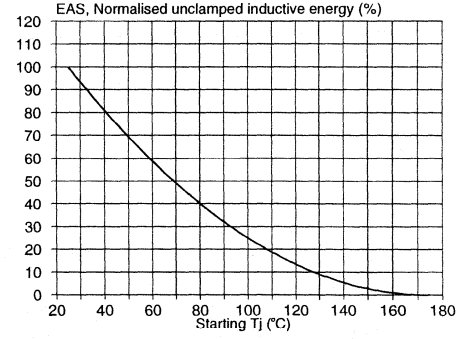


Fig.17. Normalised unclamped inductive energy. $E_{AS}\% = f(T_j)$

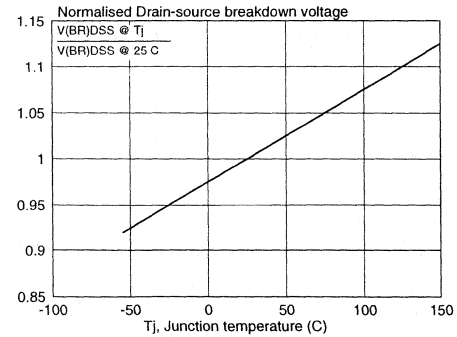


Fig.15. Normalised drain-source breakdown voltage. $V_{(BR)DSS}/V_{(BR)DSS\ 25\ ^\circ C} = f(T_j)$

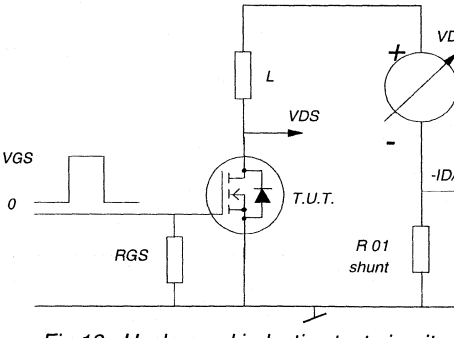


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot V_{(BR)DSS}/(V_{(BR)DSS} - V_{DD})$$

PowerMOS transistor
Logic level FET

PHD3N20L

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

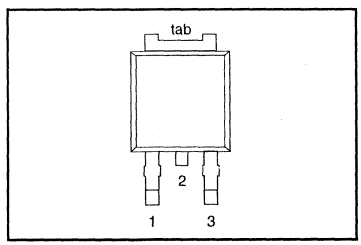
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (DC)	3.5	A
P_{tot}	Total power dissipation	50	W
$R_{DS(ON)}$	Drain-source on-state resistance	1.5	Ω

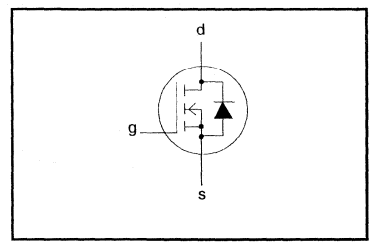
PINNING - SOT428

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	3.5	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	2.5	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	14	A
P_D	Total dissipation	T_{mb} = 25 °C	-	50	W
$\Delta P_D/\Delta T_{mb}$	Linear derating factor	T_{mb} > 25 °C	-	0.33	W/K
V_{GS}	Gate-source voltage		-	± 15	V
V_{GSM}	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	± 20	V
E_{AS}	Single pulse avalanche energy	$V_{DD} \leq 50$ V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 5 V	-	25	mJ
I_{AS}	Peak avalanche current	$V_{DD} \leq 50$ V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 5 V	-	3.5	A
T_j, T_{stg}	Operating junction and storage temperature range		- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	3	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	pcb mounted, minimum footprint	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.25	-	V/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 5 V; I_D = 2 A	-	0.77	1.5	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	1.0	1.5	2.0	V
g_{fs}	Forward transconductance	V_{DS} = 50 V; I_D = 2 A	0.8	3.0	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 200 V; V_{GS} = 0 V	-	0.1	25	µA
		V_{DS} = 160 V; V_{GS} = 0 V; T_j = 150 °C	-	1	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$Q_{g(tot)}$	Total gate charge	I_D = 3.3 A; V_{DD} = 160 V; V_{GS} = 5 V	-	7.5	9	nC
Q_{gs}	Gate-source charge		-	1	3	nC
Q_{gd}	Gate-drain (Miller) charge		-	4	6	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 100 V; I_D = 3.3 A;	-	8	-	ns
t_r	Turn-on rise time	R_G = 24 Ω; R_D = 30 Ω	-	33	-	ns
$t_{d(off)}$	Turn-off delay time		-	40	-	ns
t_f	Turn-off fall time		-	36	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_s	Internal source inductance	Measured from source lead solder point to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	270	-	pF
C_{oss}	Output capacitance		-	48	-	pF
C_{rss}	Feedback capacitance		-	17	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	3.5	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	14	A
V_{SD}	Diode forward voltage	I_S = 3.3 A; V_{GS} = 0 V	-	-	1.5	V
t_{rr}	Reverse recovery time	I_S = 3.3 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	90	-	ns
Q_{rr}	Reverse recovery charge		-	0.5	-	µC

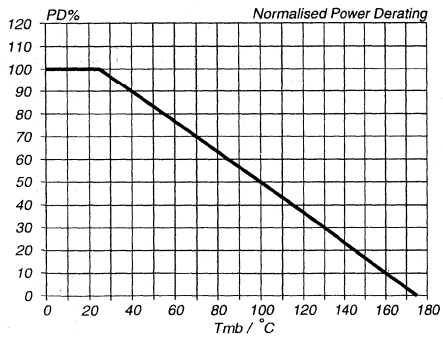


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D / P_{D\ 25\ °C} = f(T_{mb})$

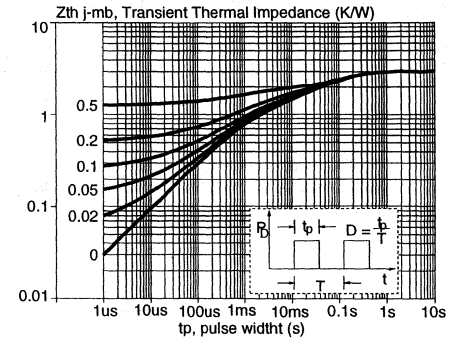


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

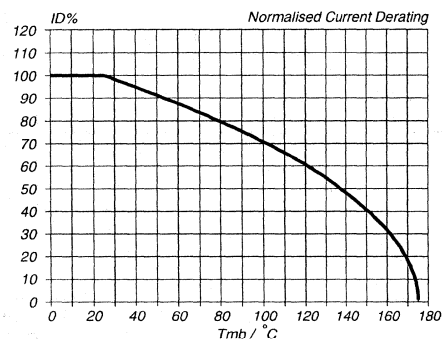


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D / I_{D\ 25\ °C} = f(T_{mb})$; conditions: $V_{GS} \geq 5$ V

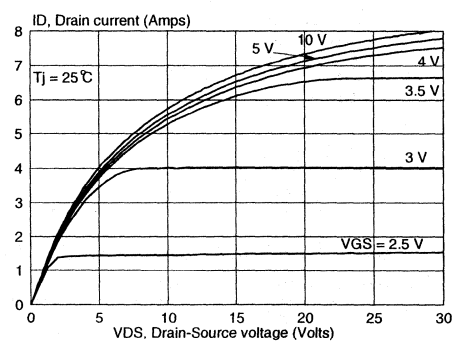


Fig.5. Typical output characteristics.
$I_D = f(V_{DS})$; parameter V_{GS}

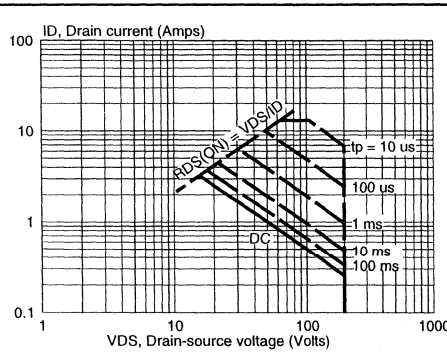


Fig.3. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

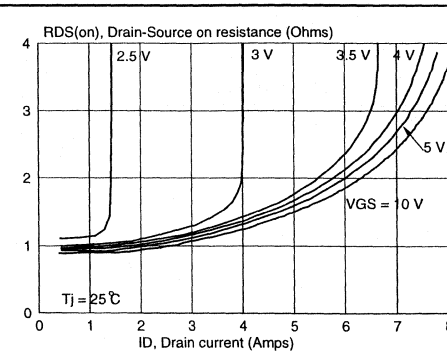


Fig.6. Typical on-state resistance.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

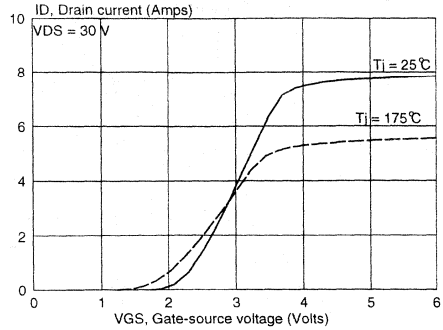


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; parameter T_j

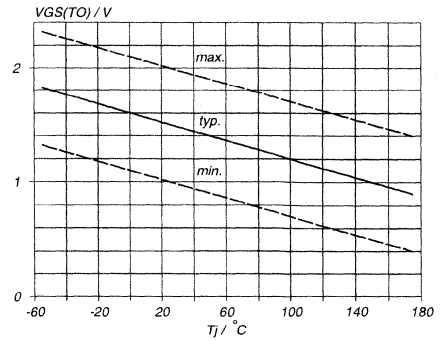


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

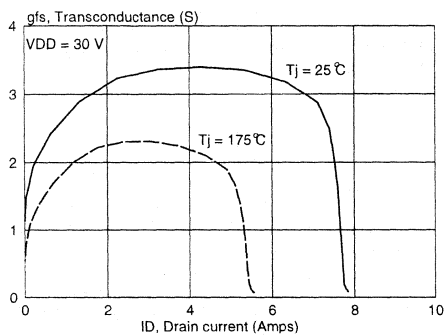


Fig.8. Typical transconductance. $g_{fs} = f(I_D)$; parameter T_j

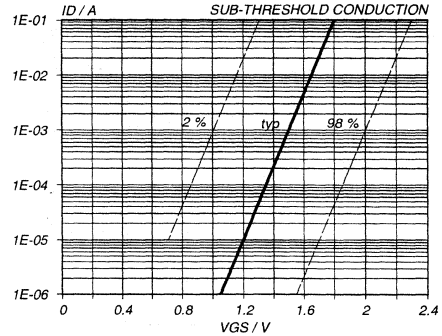


Fig.11. Sub-threshold drain current. $I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

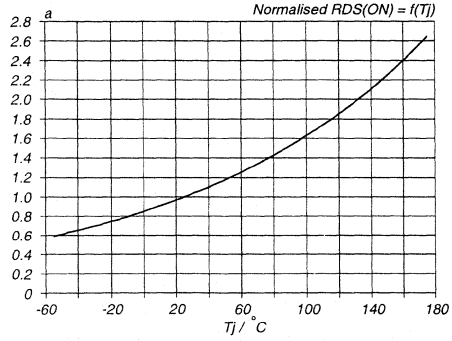


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 3.3 A; V_{GS} = 5 V

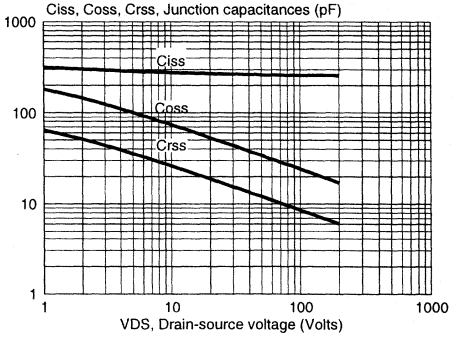


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

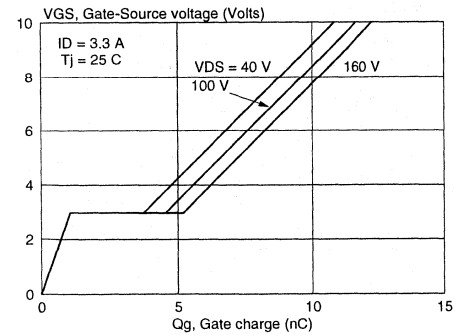


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; *parameter* V_{DS}

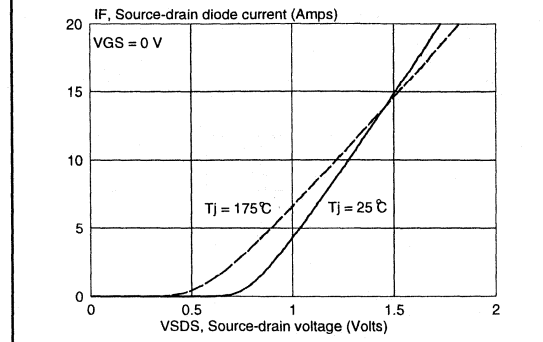


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; *parameter* T_j

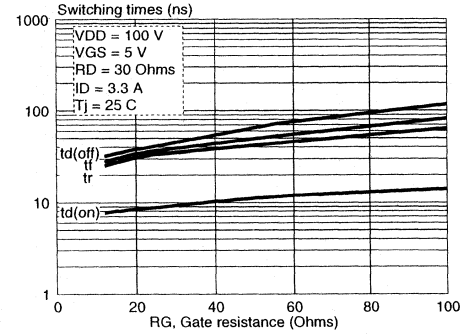


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

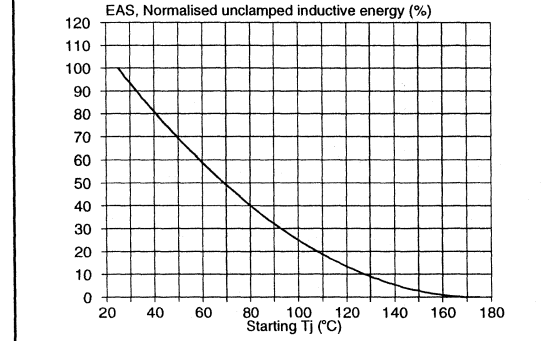


Fig.17. Normalised unclamped inductive energy.
$E_{AS}\% = f(T_j)$

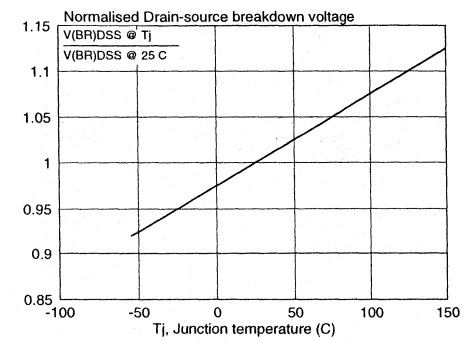


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ ^\circ C} = f(T_j)$

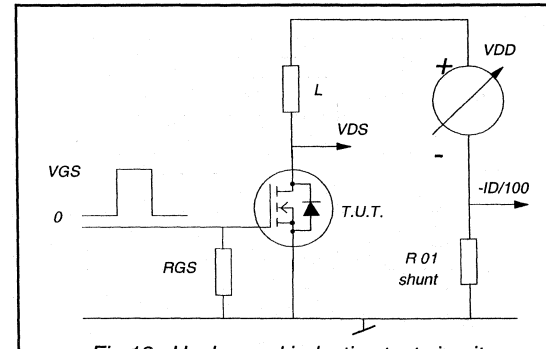


Fig.18. Unclamped inductive test circuit.
$E_{AS} = 0.5 \cdot LI_D^2 \cdot V_{(BR)DSS}/(V_{(BR)DSS} - V_{DD})$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mounting featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

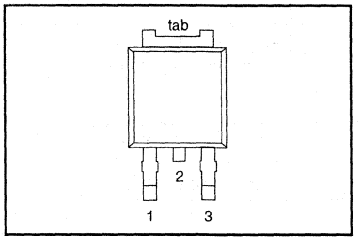
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (DC)	5.0	A
P_{tot}	Total power dissipation	60	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.9	Ω

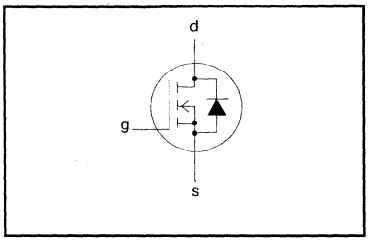
PINNING - SOT428

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	5	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	3.5	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	20	A
P_D	Total dissipation	T_{mb} = 25 °C	-	60	W
$\Delta P_D/\Delta T_{mb}$	Linear derating factor	T_{mb} > 25 °C	-	0.4	W/K
V_{GS}	Gate-source voltage		-	± 30	V
E_{AS}	Single pulse avalanche energy	$V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	40	mJ
I_{AS}	Peak avalanche current	$V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	5	A
T_j, T_{stg}	Operating junction and storage temperature range		- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	2.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	pcb mounted, minimum footprint	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.25	-	V/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 2.5 A	-	0.68	0.9	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 50 V; I_D = 2.5 A	1.5	3.5	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 200 V; V_{GS} = 0 V	-	0.1	25	µA
		V_{DS} = 160 V; V_{GS} = 0 V; T_j = 150 °C	-	1	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$Q_{g(tot)}$	Total gate charge	I_D = 4.8 A; V_{DD} = 160 V; V_{GS} = 10 V	-	11	15	nC
Q_{gs}	Gate-source charge		-	2	3	nC
Q_{gd}	Gate-drain (Miller) charge		-	5.3	7	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 100 V; I_D = 4.8 A;	-	7	-	ns
t_r	Turn-on rise time	R_G = 18 Ω; R_D = 20 Ω	-	29	-	ns
$t_{d(off)}$	Turn-off delay time		-	27	-	ns
t_f	Turn-off fall time		-	22	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_s	Internal source inductance	Measured from source lead solder point to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	300	-	pF
C_{oss}	Output capacitance		-	60	-	pF
C_{rss}	Feedback capacitance		-	20	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	5	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	20	A
V_{SD}	Diode forward voltage	I_S = 5.2 A; V_{GS} = 0 V	-	-	1.5	V
t_{rr}	Reverse recovery time	I_S = 4.8 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	114	-	ns
Q_{rr}	Reverse recovery charge		-	0.8	-	µC

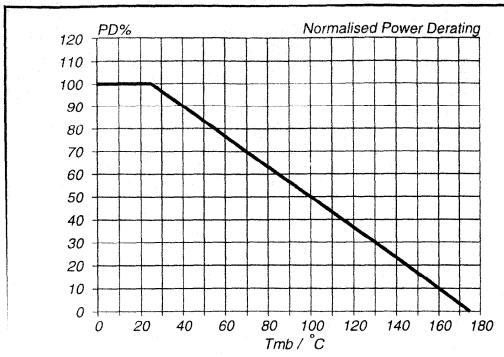


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

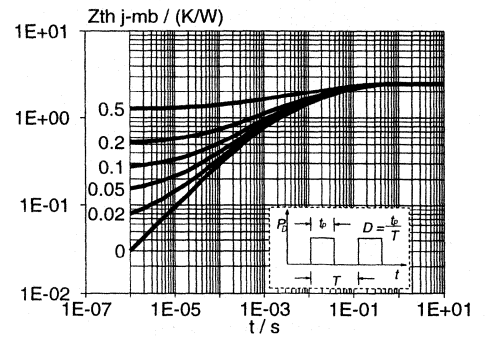


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

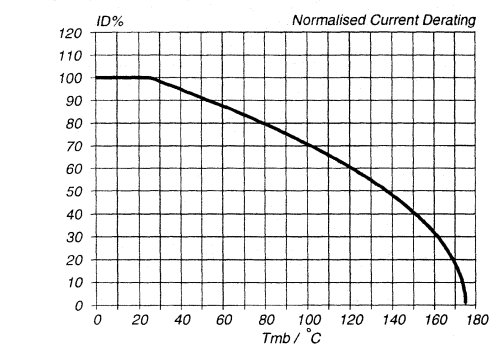


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

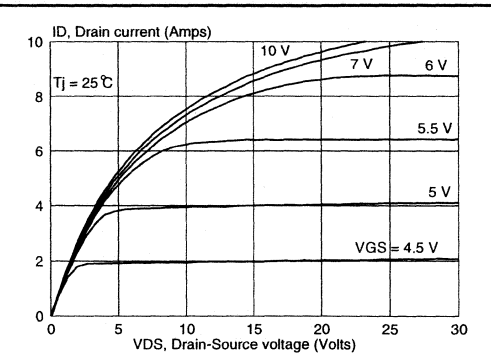


Fig.5. Typical output characteristics.
I_D = f(V_{DS}); parameter V_{GS}

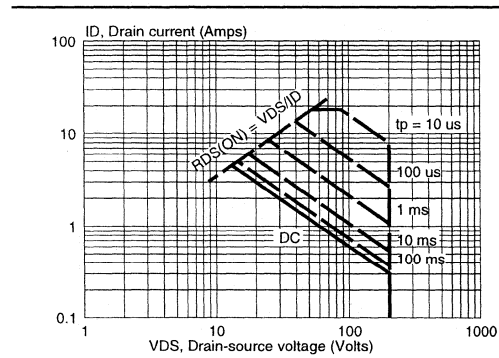


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

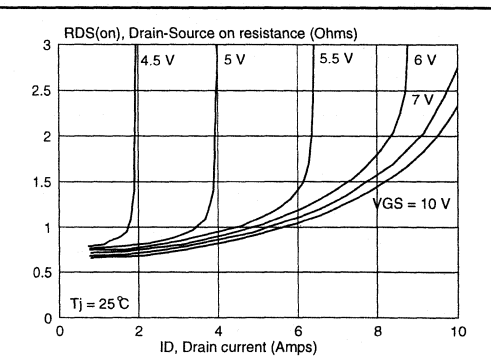


Fig.6. Typical on-state resistance.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

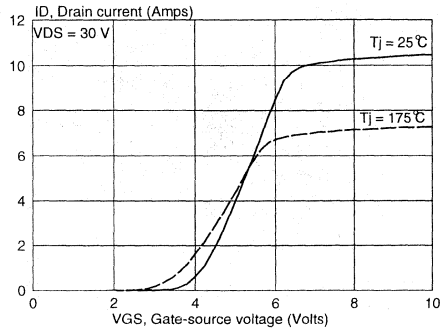


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; parameter T_j

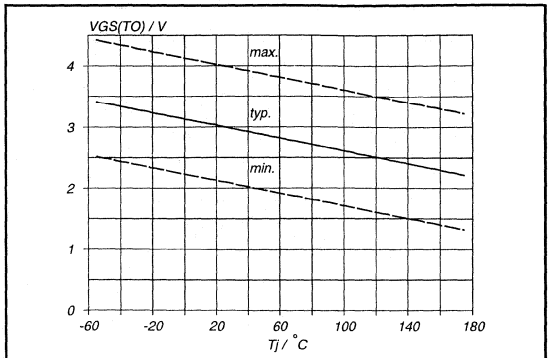


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: $I_D = 0.25$ mA; $V_{DS} = V_{GS}$

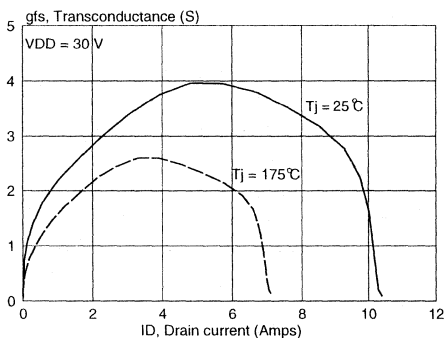


Fig.8. Typical transconductance. $g_{fs} = f(I_D)$; parameter T_j

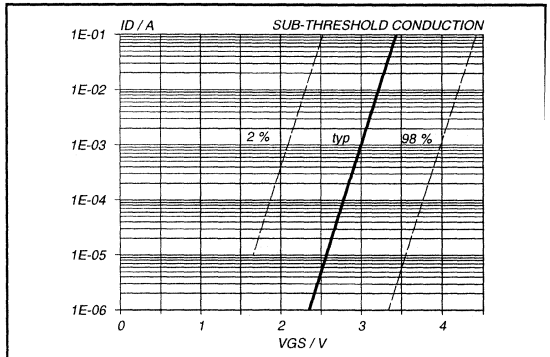


Fig.11. Sub-threshold drain current. $I_D = f(V_{GS})$; conditions: $T_j = 25$ ˚C; $V_{DS} = V_{GS}$

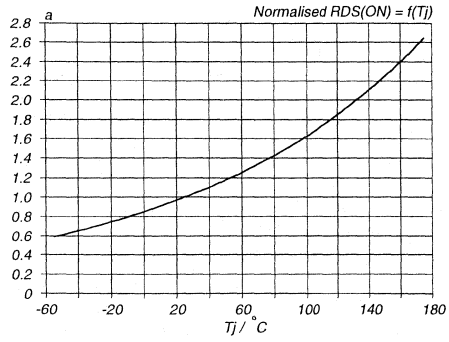


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,^{\circ}C} = f(T_j)$; $I_D = 2.5$ A; $V_{GS} = 10$ V

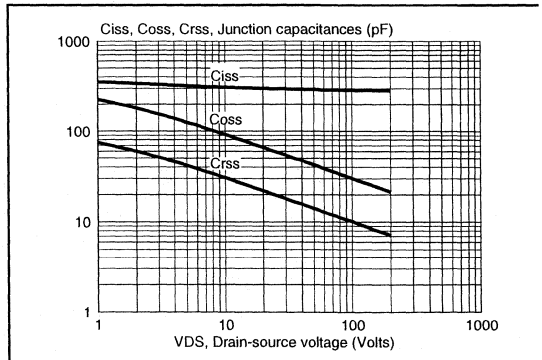


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

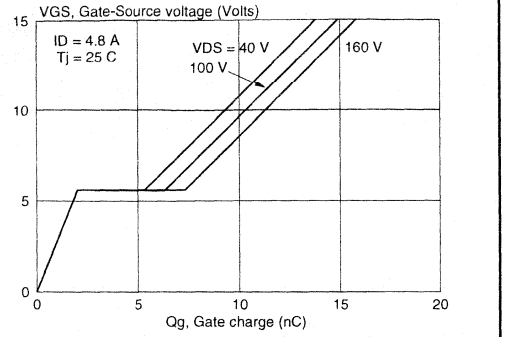


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; *parameter* V_{DS}

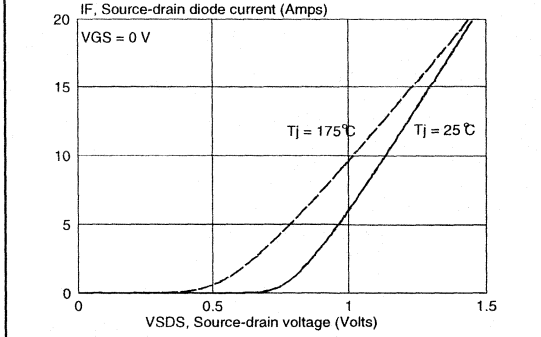


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; *parameter* T_j

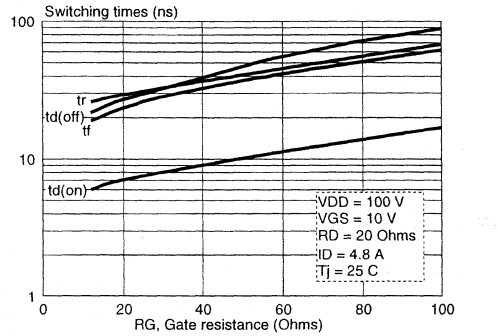


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

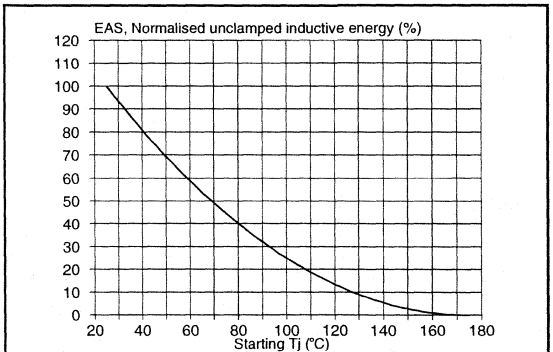


Fig.17. Normalised unclamped inductive energy.
$E_{AS}\% = f(T_j)$

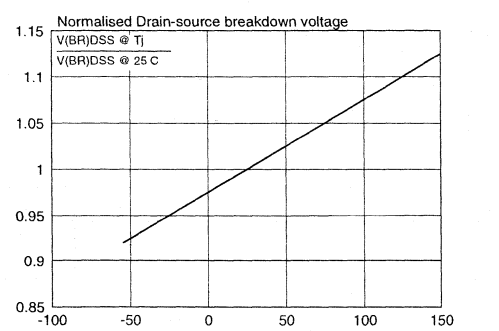


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

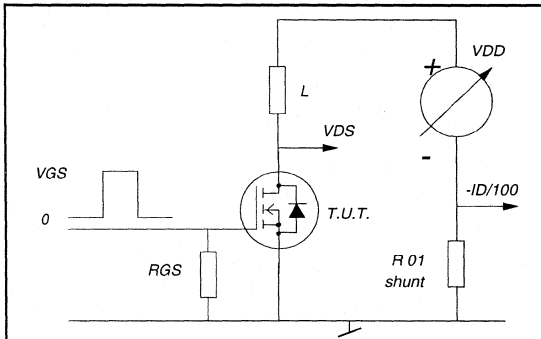


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot V_{(BR)DSS}/(V_{(BR)DSS} - V_{DD})$$

PowerMOS transistor — PHD6N10E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mounting featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

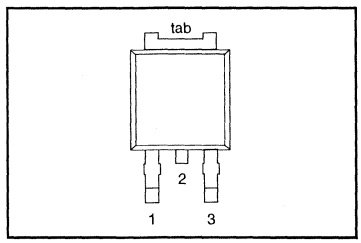
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	6.3	A
P_{tot}	Total power dissipation	50	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.54	Ω

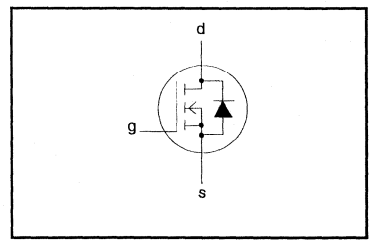
PINNING - SOT428

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	6.3	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	4.5	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	25	A
P_D	Total dissipation	T_{mb} = 25 °C	-	50	W
$\Delta P_D/\Delta T_{mb}$	Linear derating factor	T_{mb} > 25 °C	-	0.33	W/K
V_{GS}	Gate-source voltage		-	± 30	V
E_{AS}	Single pulse avalanche energy	$V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	30	mJ
I_{AS}	Peak avalanche current	$V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	6.3	A
T_j, T_{stg}	Operating junction and storage temperature range		- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	3	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	pcb mounted, minimum footprint	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.15	-	V/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 3.4 A	-	0.25	0.54	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 50 V; I_D = 3.4 A	1.3	3.0	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 100 V; V_{GS} = 0 V	-	0.1	25	μA
		V_{DS} = 80 V; V_{GS} = 0 V; T_j = 150 °C	-	1	250	μA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$Q_{g(tot)}$	Total gate charge	I_D = 5.6 A; V_{DD} = 80 V; V_{GS} = 10 V	-	9.2	12	nC
Q_{gs}	Gate-source charge		-	1.7	3	nC
Q_{gd}	Gate-drain (Miller) charge		-	4.7	6	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 50 V; I_D = 5.6 A;	-	7	-	ns
t_r	Turn-on rise time	R_G = 24 Ω; R_D = 8.4 Ω	-	40	-	ns
$t_{d(off)}$	Turn-off delay time		-	22	-	ns
t_f	Turn-off fall time		-	18	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_s	Internal source inductance	Measured from source lead solder point to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	222	-	pF
C_{oss}	Output capacitance		-	74	-	pF
C_{rss}	Feedback capacitance		-	30	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	6.3	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	25	A
V_{SD}	Diode forward voltage	I_S = 5.6 A; V_{GS} = 0 V	-	-	1.5	V
t_{rr}	Reverse recovery time	I_S = 5.6 A; V_{GS} = 0 V; dI/dt = 100 A/μs	-	70	-	ns
Q_{rr}	Reverse recovery charge		-	0.4	-	μC

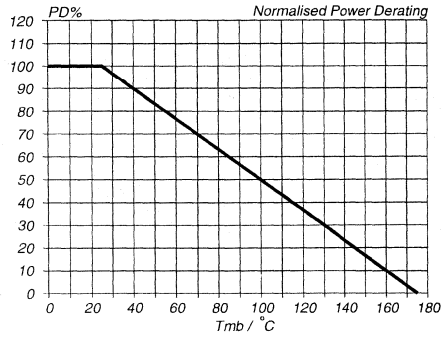


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

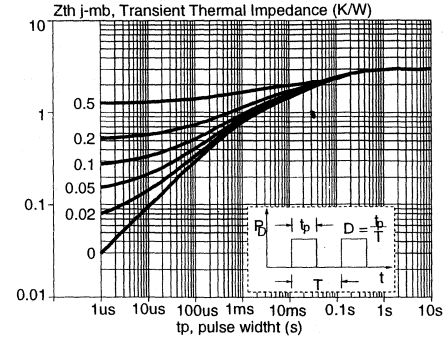


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

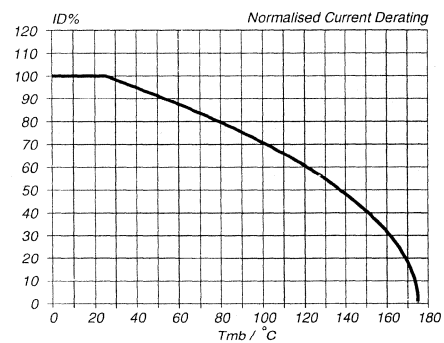


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 5 V

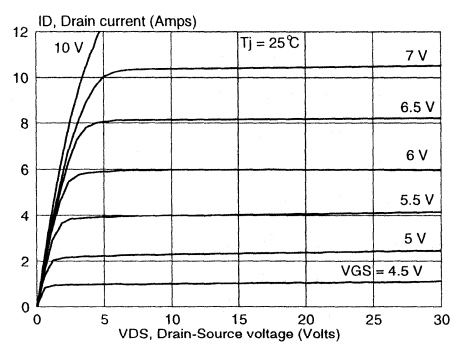


Fig.5. Typical output characteristics.
I_D = f(V_{DS}); parameter V_{GS}

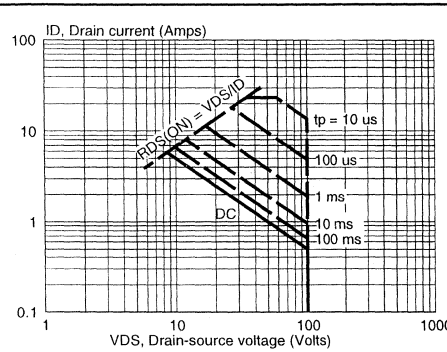


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

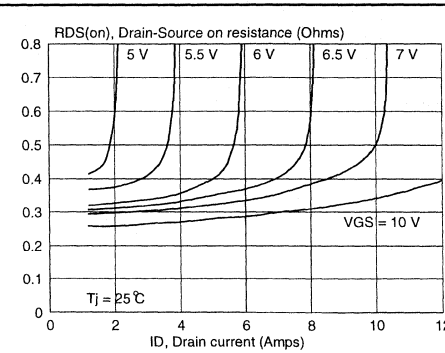


Fig.6. Typical on-state resistance.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

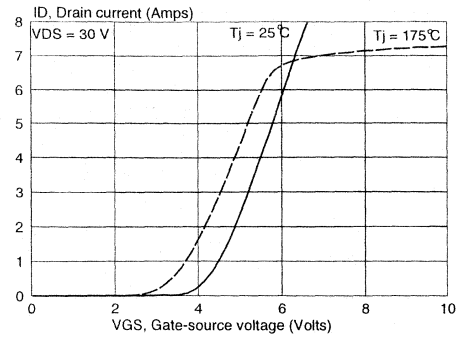


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; parameter T_j

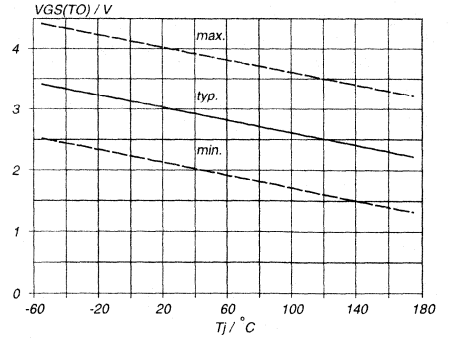


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

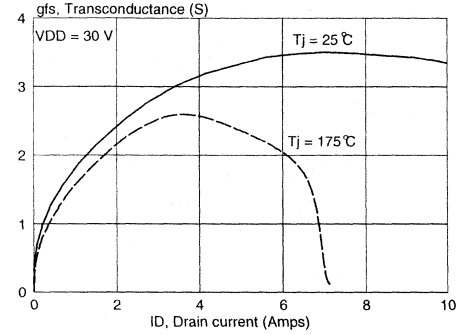


Fig.8. Typical transconductance. $g_{fs} = f(I_D)$; parameter T_j

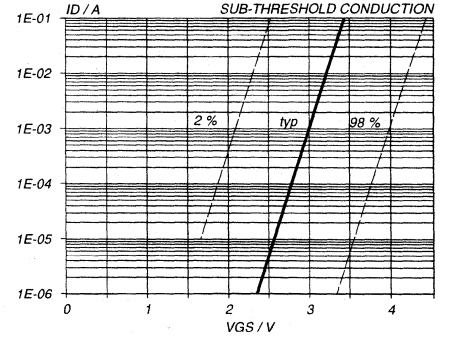


Fig.11. Sub-threshold drain current. $I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

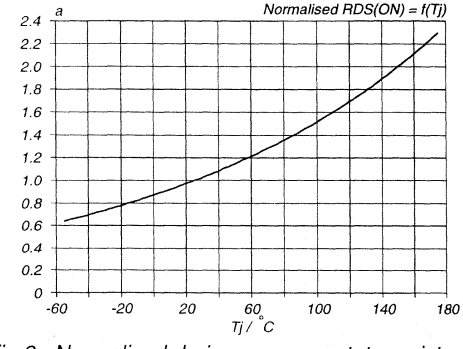


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\ ^\circ C} = f(T_j)$; I_D = 5.6 A; V_{GS} = 5 V

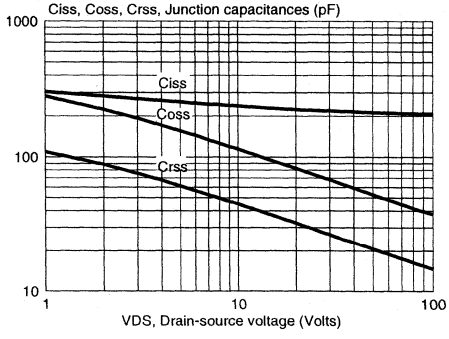


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

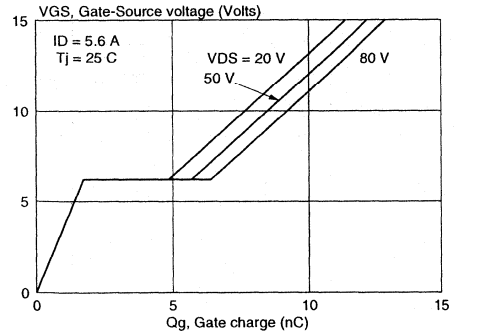


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; *parameter* V_{DS}

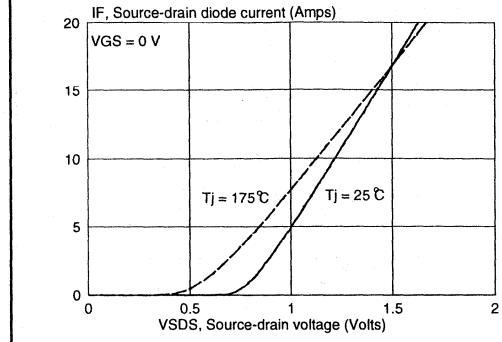


Fig.16. Source-Drain diode characteristic. $I_F = f(V_{SDS})$; *parameter* T_j

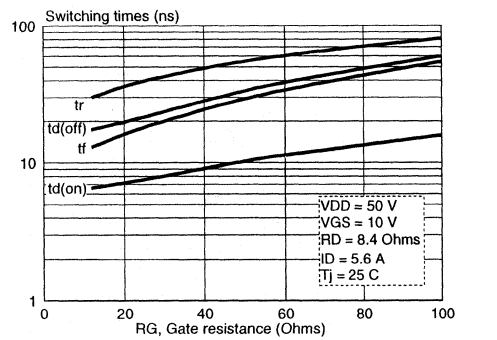


Fig.14. Normalised drain-source breakdown voltage. $V_{(BR)DSS}/V_{(BR)DSS\ 25\ ^\circ C} = f(T_j)$

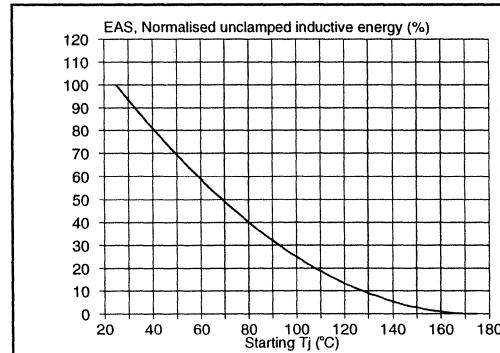


Fig.17. Normalised unclamped inductive energy. $E_{AS}\% = f(T_j)$

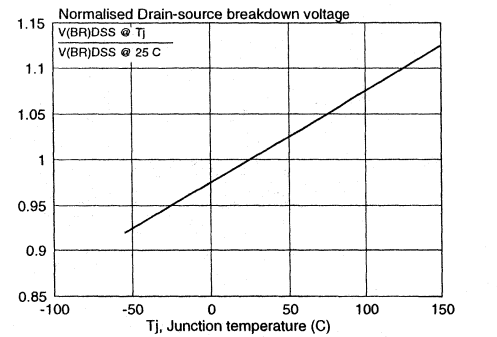


Fig.15. Normalised drain-source breakdown voltage. $V_{(BR)DSS}/V_{(BR)DSS\ 25\ ^\circ C} = f(T_j)$

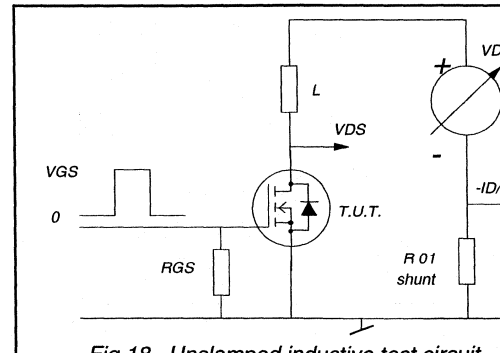


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot V_{(BR)DSS}/(V_{(BR)DSS} - V_{DD})$$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suuitable for surface mounting. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

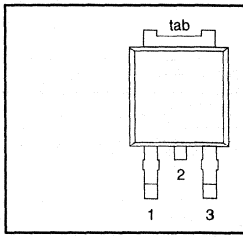
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	11	A
P_{tot}	Total power dissipation	60	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.25	Ω

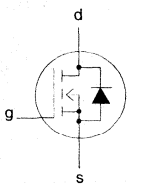
PINNING - SOT428

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	11	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	7.7	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	44	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	60	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction Temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	2.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	pcb mounted, minimum footprint	50	-	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 5.5 A	-	0.22	0.25	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5.5 A	3	4.2	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	400	500	pF
C_{oss}	Output capacitance		-	90	120	pF
C_{rss}	Feedback capacitance		-	35	50	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	9	14	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	30	45	ns
t_f	Turn-off fall time		-	20	40	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead solder point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	11	A
I_{DRM}	Pulsed reverse drain current	-	-	-	44	A
V_{SD}	Diode forward voltage	I_F = 11 A ; V_{GS} = 0 V	-	1.2	1.5	V
t_{rr}	Reverse recovery time	I_F = 11 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.35	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 11 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	35	mJ

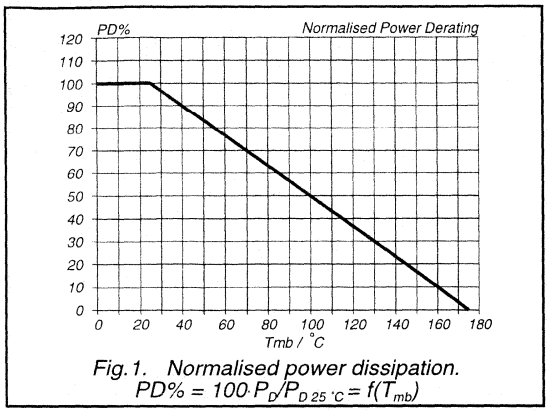


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

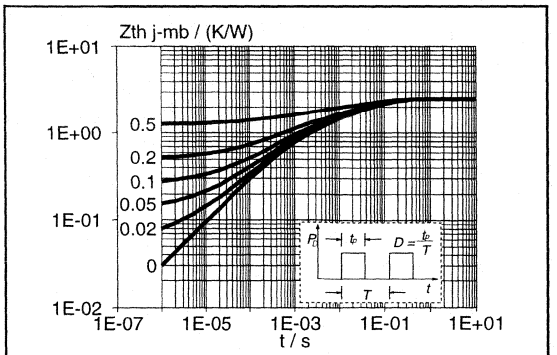


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

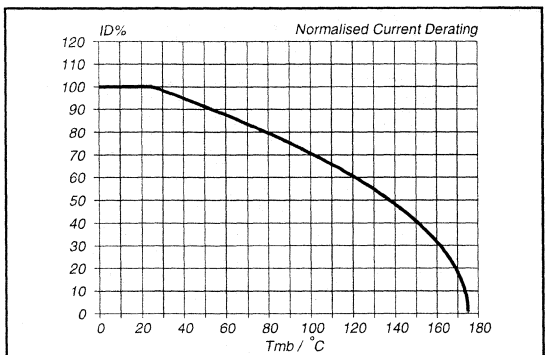


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

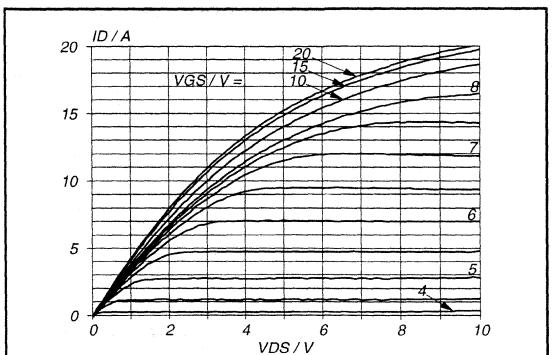


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

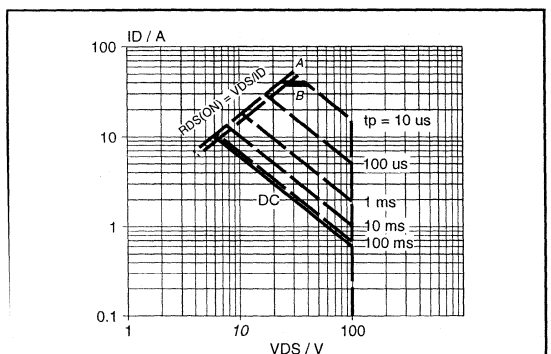


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

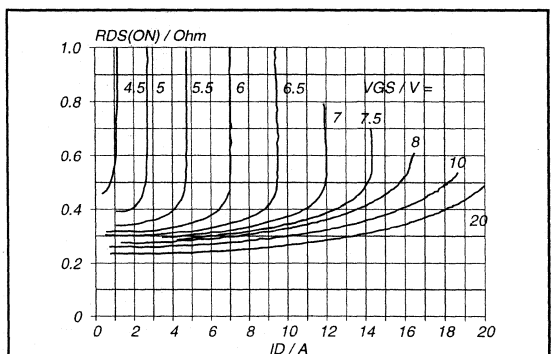


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

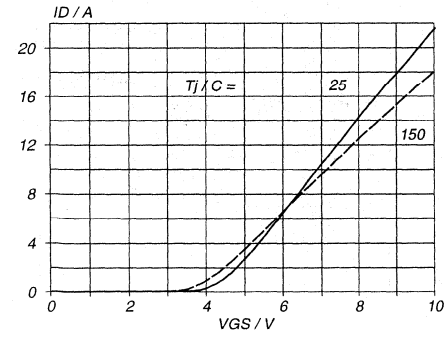


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

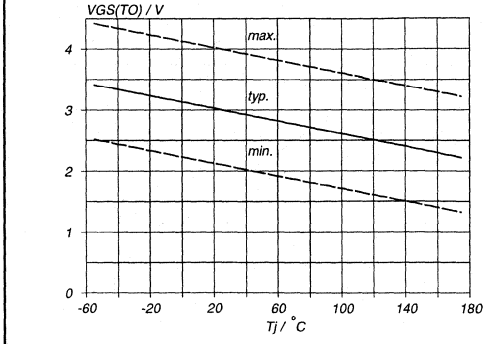


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

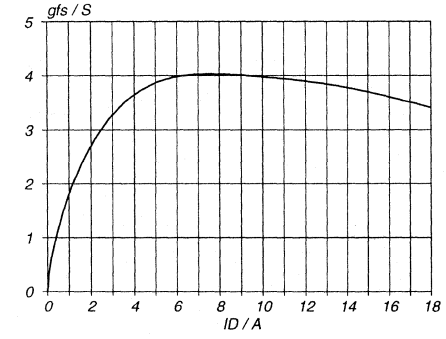


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

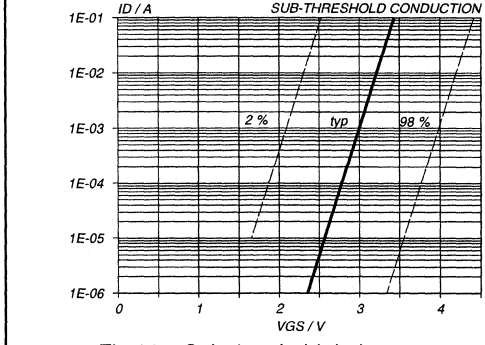


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

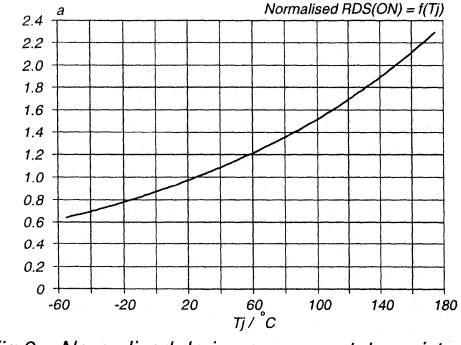


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 5.5 A; V_{GS} = 10 V

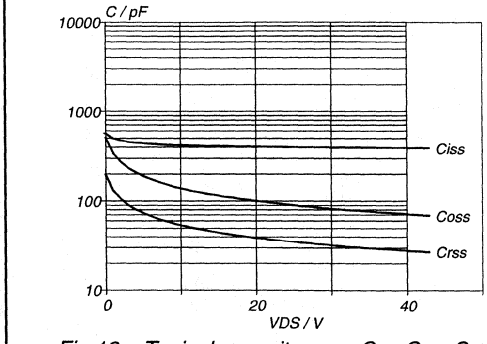


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

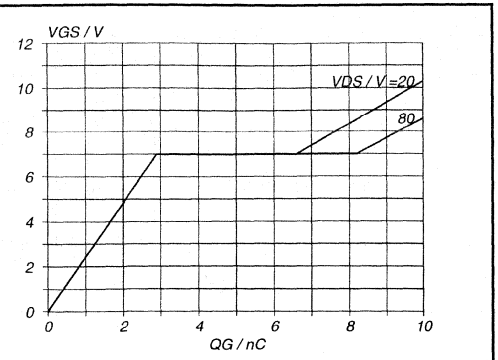


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: I_D = 11 A; parameter V_{DS}

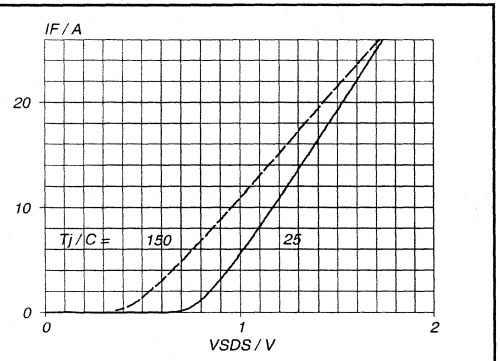


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

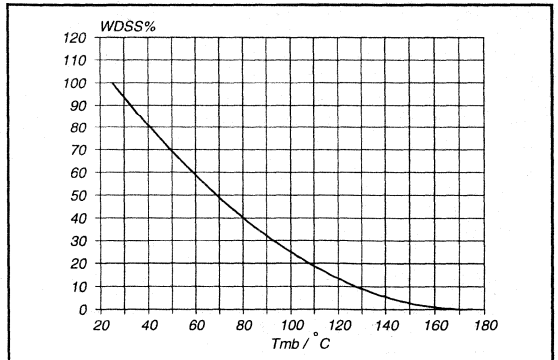


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: I_D = 11 A

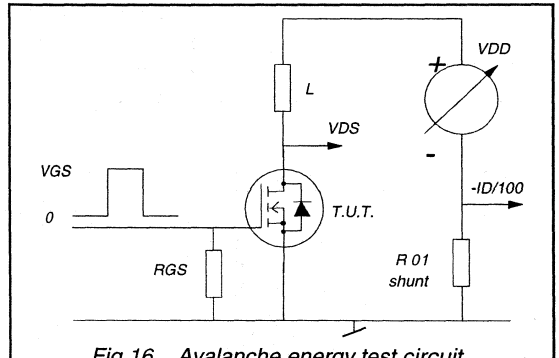


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PowerMOS transistor — PHD12N10E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mounting. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

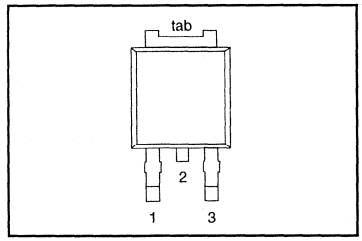
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	14	A
P_{tot}	Total power dissipation	75	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.16	Ω

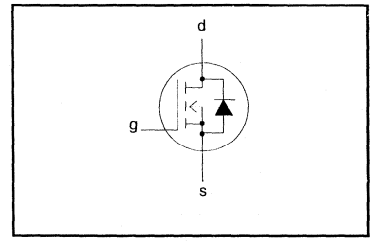
PINNING - SOT428

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	14	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	10	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	56	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	75	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction Temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	pcb mounted, minimum footprint	50	-	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A	-	0.15	0.16	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5 A	4.0	5.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	660	825	pF
C_{oss}	Output capacitance		-	140	200	pF
C_{rss}	Feedback capacitance		-	60	100	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	10	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	60	90	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_s	Internal source inductance	Measured from source lead solder point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	14	A
I_{DRM}	Pulsed reverse drain current	-	-	-	56	A
V_{SD}	Diode forward voltage	I_F = 14 A ; V_{GS} = 0 V	-	1.2	1.5	V
t_{rr}	Reverse recovery time	I_F = 14 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.6	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 14 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50Ω	-	-	70	mJ

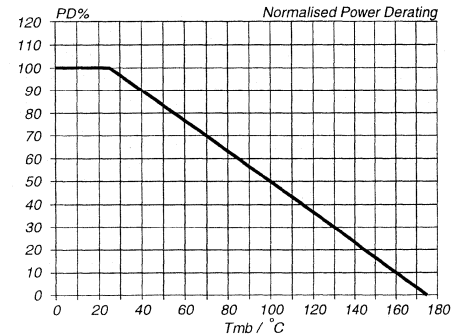


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

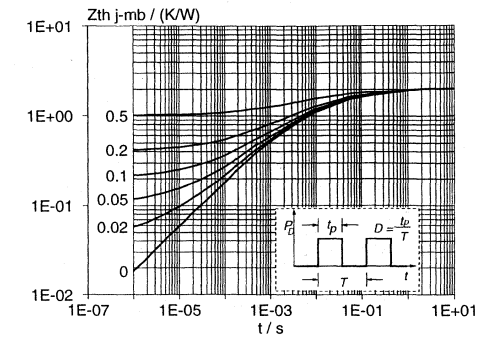


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

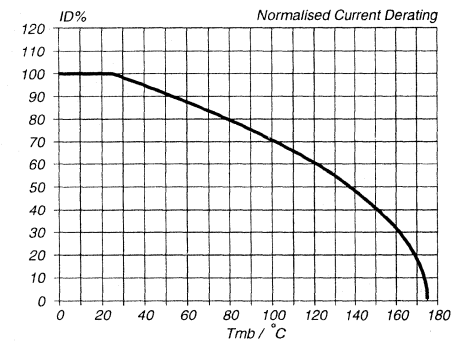


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

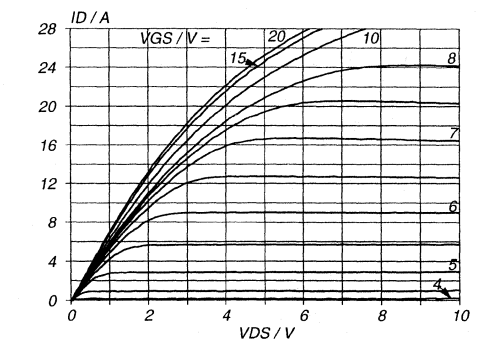


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

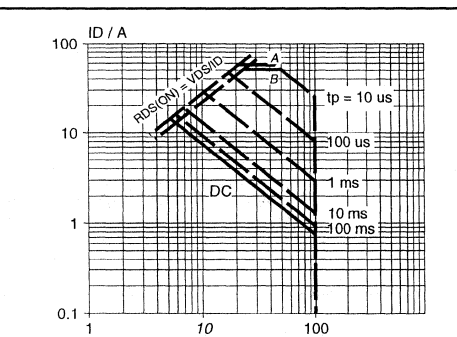


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

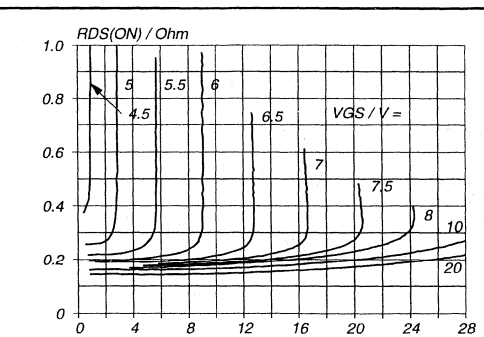


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

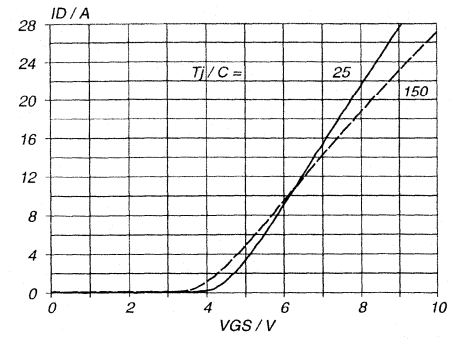


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

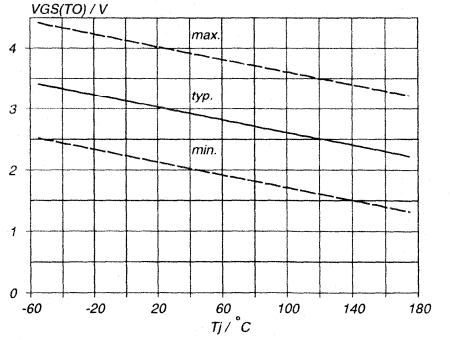


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

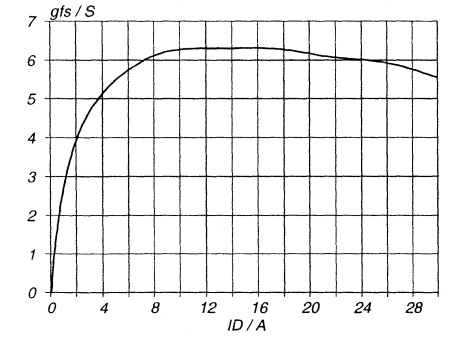


Fig.8. Typical transconductance, $T_j = 25$ °C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

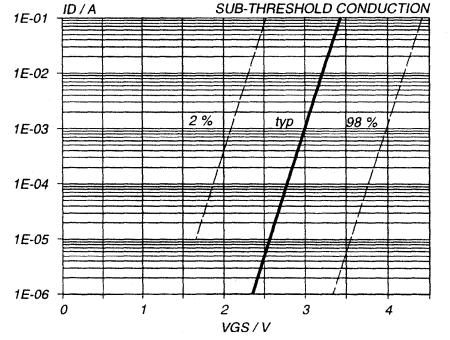


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

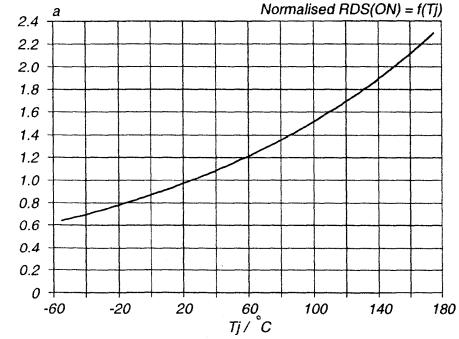


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 5$ A; $V_{GS} = 10$ V

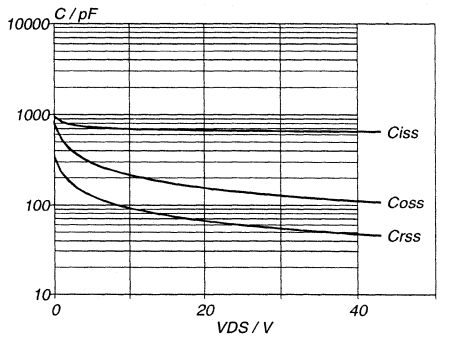


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

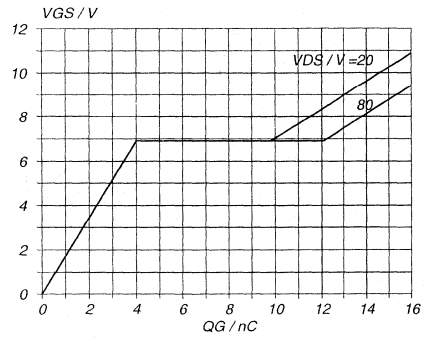


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 14 A; parameter V_{DS}

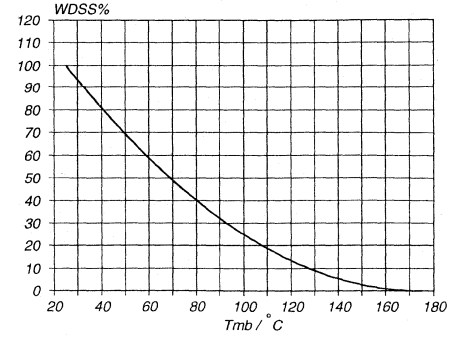


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: I_D = 14 A

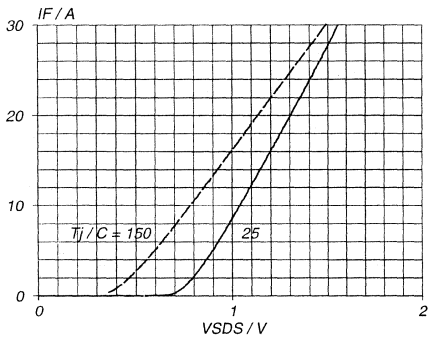


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

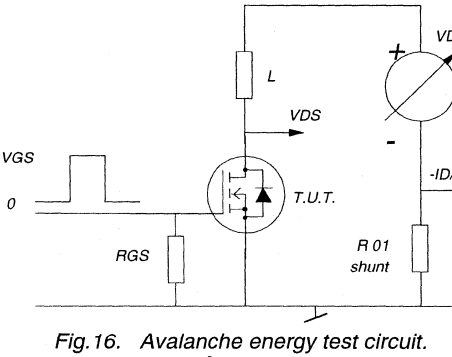


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mounting featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

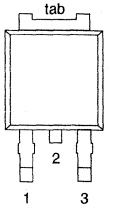
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	12	A
P_{tot}	Total power dissipation	50	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.15	Ω

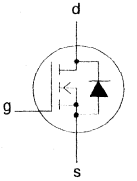
PINNING - SOT428

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	12	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	9	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	48	A
P_D	Total dissipation	T_{mb} = 25 °C	-	50	W
$\Delta P_D/\Delta T_{mb}$	Linear derating factor	T_{mb} > 25 °C	-	0.33	W/K
V_{GS}	Gate-source voltage		-	± 30	V
E_{AS}	Single pulse avalanche energy	$V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	25	mJ
I_{AS}	Peak avalanche current	$V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	6	A
T_j, T_{stg}	Operating junction and storage temperature range		- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	3	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	pcb mounted, minimum footprint	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.08	-	V/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 6 A	-	0.1	0.15	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 50 V; I_D = 6 A	2.4	4.0	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 60 V; V_{GS} = 0 V	-	0.1	25	µA
		V_{DS} = 48 V; V_{GS} = 0 V; T_j = 150 °C	-	1	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$Q_{g(tot)}$	Total gate charge	I_D = 10 A; V_{DD} = 48 V; V_{GS} = 10 V	-	10	12	nC
Q_{gs}	Gate-source charge		-	2	3	nC
Q_{gd}	Gate-drain (Miller) charge		-	5.6	7	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 30 V; I_D = 10 A;	-	8	-	ns
t_r	Turn-on rise time	R_G = 24 Ω; R_D = 2.7 Ω	-	55	-	ns
$t_{d(off)}$	Turn-off delay time		-	25	-	ns
t_f	Turn-off fall time		-	22	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_s	Internal source inductance	Measured from source lead solder point to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	220	-	pF
C_{oss}	Output capacitance		-	108	-	pF
C_{rss}	Feedback capacitance		-	48	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	12	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	48	A
V_{SD}	Diode forward voltage	I_S = 10 A; V_{GS} = 0 V	-	-	1.5	V
t_{rr}	Reverse recovery time	I_S = 10 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	38	-	ns
Q_{rr}	Reverse recovery charge		-	0.1	-	µC

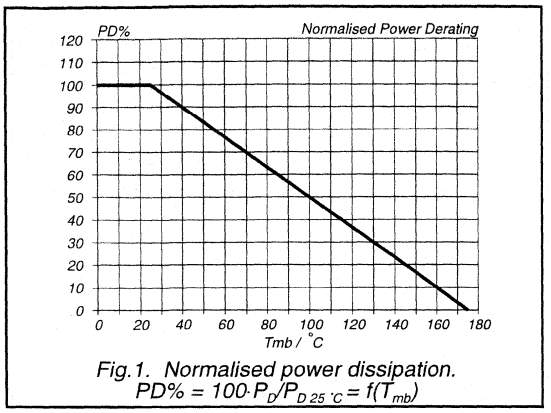


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

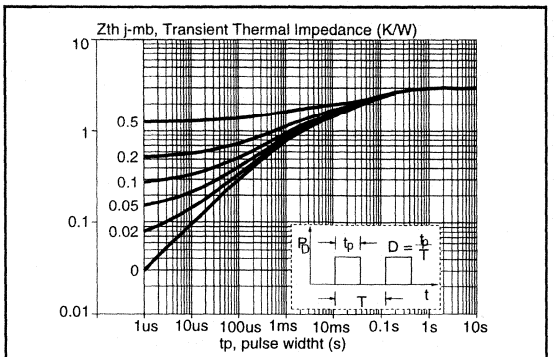


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

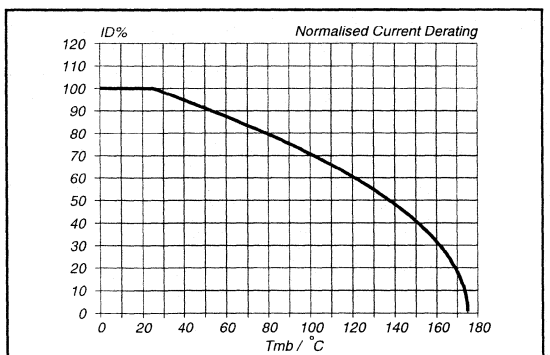


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

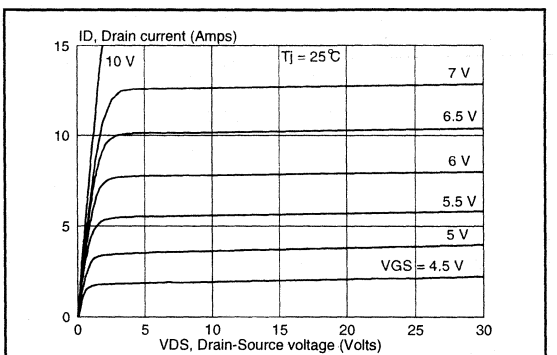


Fig.5. Typical output characteristics.
I_D = f(V_{DS}); parameter V_{GS}

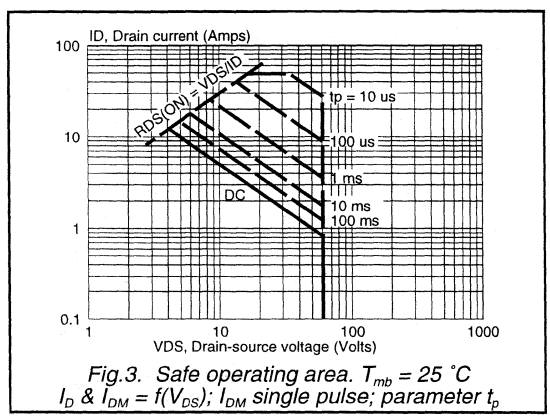


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

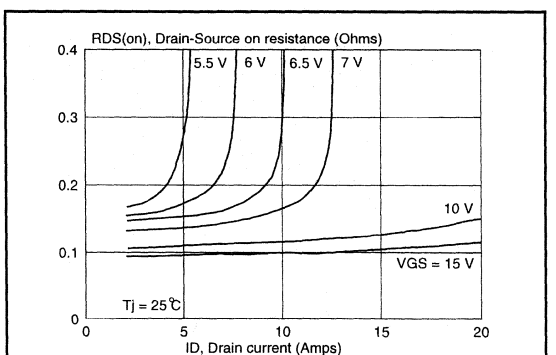


Fig.6. Typical on-state resistance.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

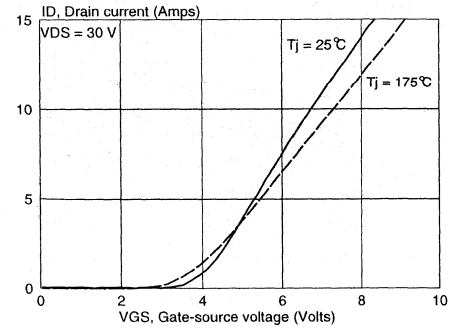


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; parameter T_j

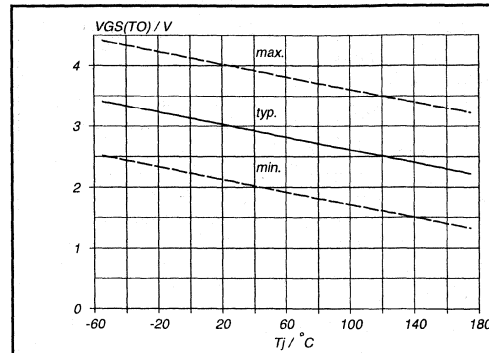


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

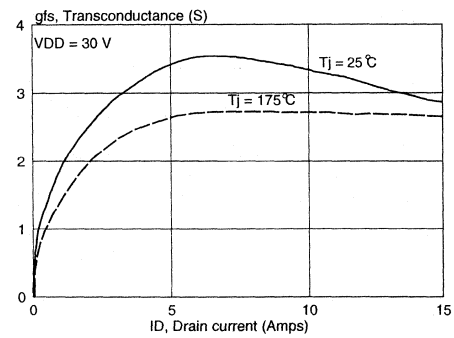


Fig.8. Typical transconductance. $g_{fs} = f(I_D)$; parameter T_j

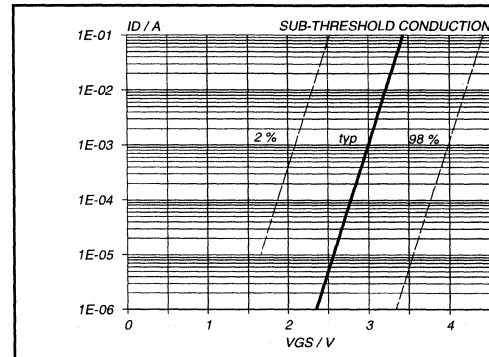


Fig.11. Sub-threshold drain current. $I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

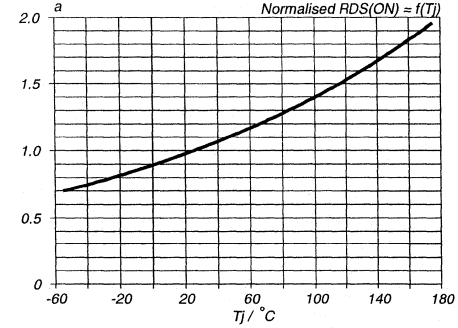


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,^{\circ}C} = f(T_j)$; I_D = 10 A; V_{GS} = 10 V

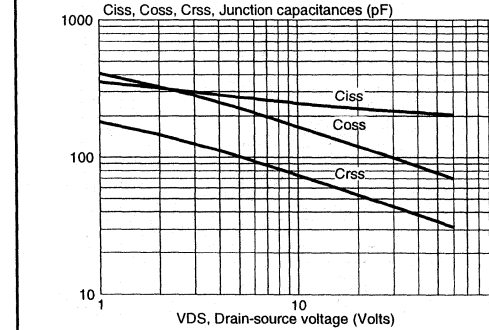


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

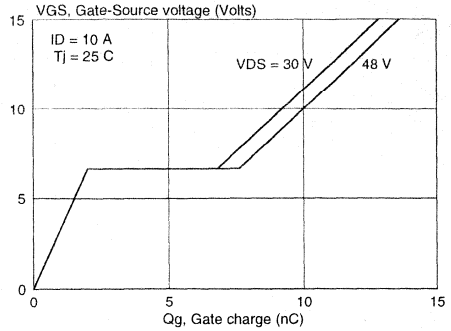


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

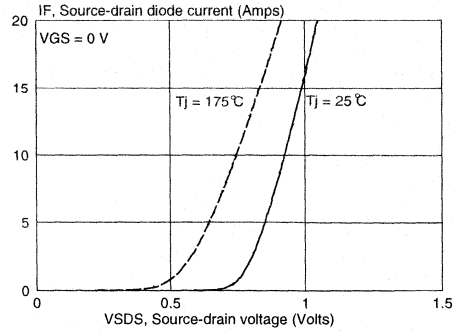


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

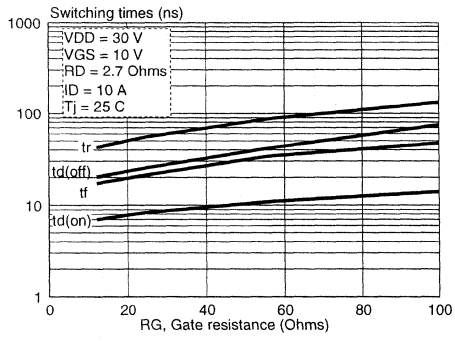


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

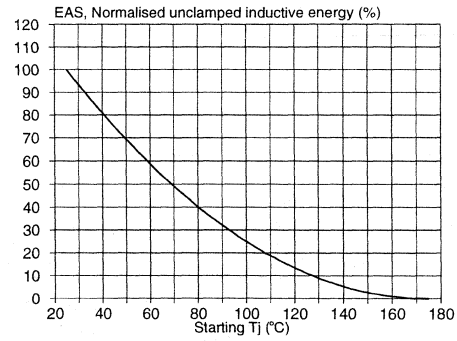


Fig.17. Normalised unclamped inductive energy.
$E_{AS}\% = f(T_j)$

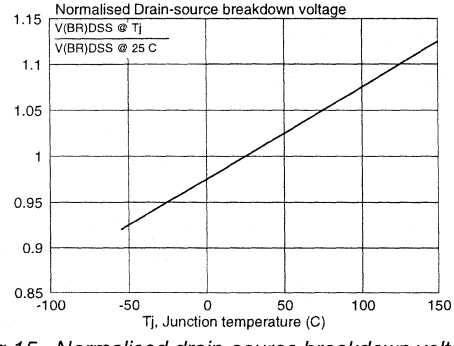


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

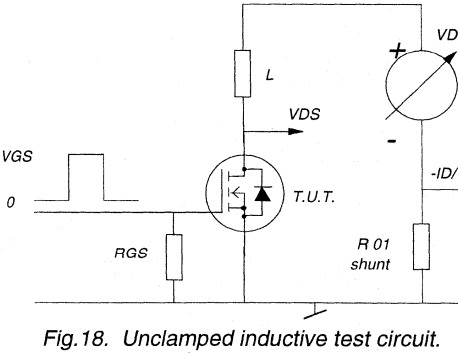


Fig.18. Unclamped inductive test circuit.
$E_{AS} = 0.5 \cdot LI_D^2 \cdot V_{(BR)DSS}/(V_{(BR)DSS} - V_{DD})$

PowerMOS transistor Logic level FET

PHD3055L

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

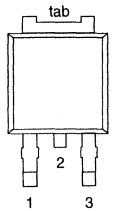
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	12	A
P_{tot}	Total power dissipation	50	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.18	Ω

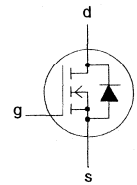
PINNING - SOT428

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	12	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	9	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	48	A
P_D	Total dissipation	T_{mb} = 25 °C	-	50	W
$\Delta P_D/\Delta T_{mb}$	Linear derating factor	T_{mb} > 25 °C	-	0.33	W/K
V_{GS}	Gate-source voltage		-	± 15	V
V_{GSM}	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	± 20	V
E_{AS}	Single pulse avalanche energy	$V_{DD} \leq 50$ V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 5 V	-	25	mJ
I_{AS}	Peak avalanche current	$V_{DD} \leq 50$ V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 5 V	-	6	A
T_j, T_{stg}	Operating junction and storage temperature range		- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	3	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	pcb mounted, minimum footprint	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.08	-	V/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 5 V; I_D = 6 A	-	0.13	0.18	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	1.0	1.5	2.0	V
g_{fs}	Forward transconductance	V_{DS} = 50 V; I_D = 6 A	3.5	5.5	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 60 V; V_{GS} = 0 V	-	0.1	25	µA
		V_{DS} = 48 V; V_{GS} = 0 V; T_j = 150 °C	-	1	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$Q_{g(tot)}$	Total gate charge	I_D = 10 A; V_{DD} = 48 V; V_{GS} = 5 V	-	7.5	10	nC
Q_{gs}	Gate-source charge		-	1.9	3	nC
Q_{gd}	Gate-drain (Miller) charge		-	5.5	7	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 30 V; I_D = 10 A;	-	12	-	ns
t_r	Turn-on rise time	R_G = 24 Ω; R_D = 2.7 Ω	-	105	-	ns
$t_{d(off)}$	Turn-off delay time		-	26	-	ns
t_f	Turn-off fall time		-	35	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_s	Internal source inductance	Measured from source lead solder point to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	290	-	pF
C_{oss}	Output capacitance		-	103	-	pF
C_{rss}	Feedback capacitance		-	40	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	12	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	48	A
V_{SD}	Diode forward voltage	I_S = 10 A; V_{GS} = 0 V	-	-	1.5	V
t_{rr}	Reverse recovery time	I_S = 10 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	40	-	ns
Q_{rr}	Reverse recovery charge		-	0.1	-	µC

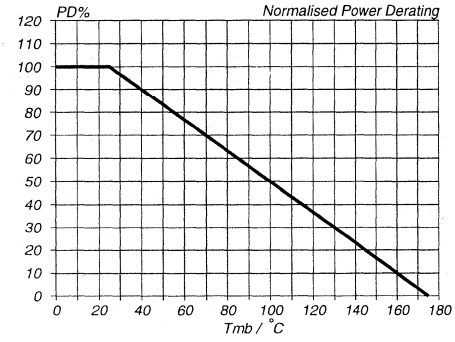


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

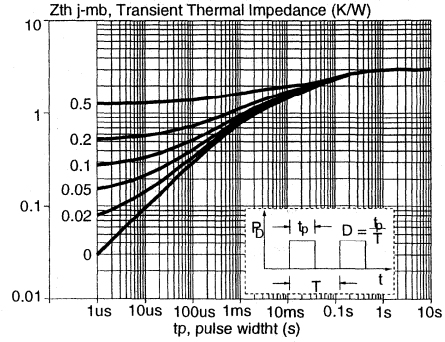


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

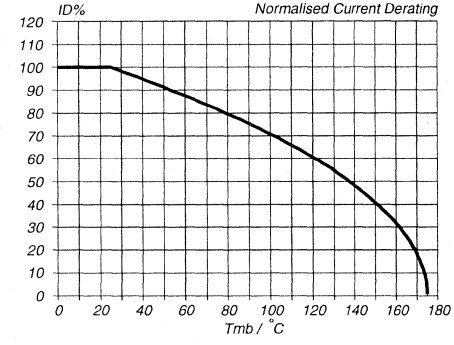


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

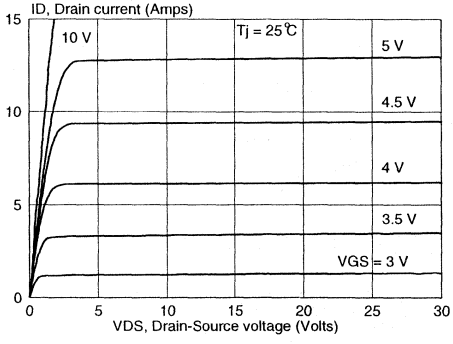


Fig.5. Typical output characteristics.
I_D = f(V_{DS}); parameter V_{GS}

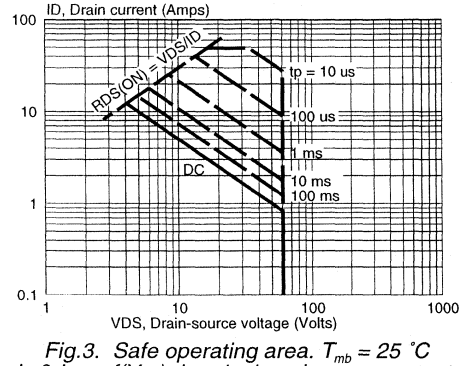


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

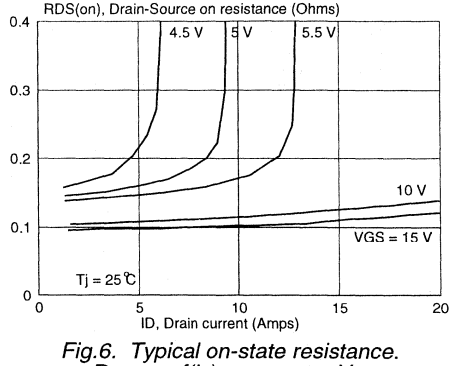


Fig.6. Typical on-state resistance.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

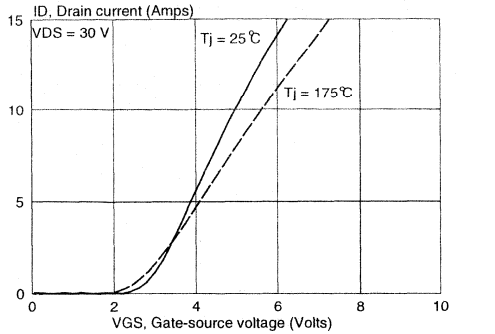


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; parameter T_j

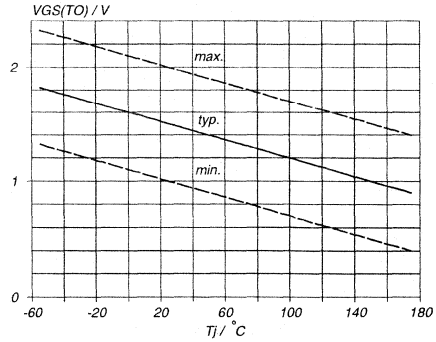


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

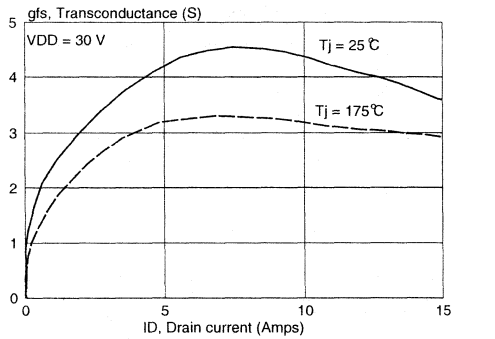


Fig.8. Typical transconductance. $g_{fs} = f(I_D)$; parameter T_j

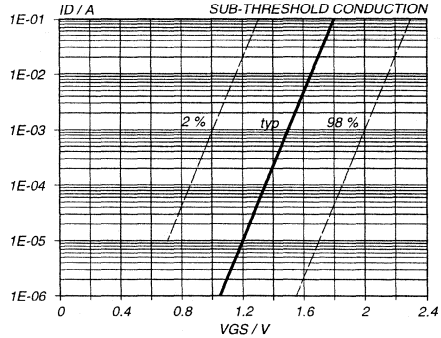


Fig.11. Sub-threshold drain current. $I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

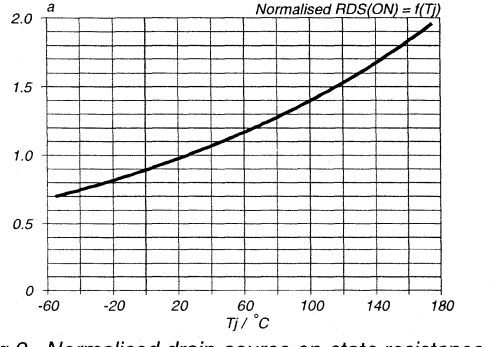


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,^{\circ}C} = f(T_j)$; I_D = 10 A; V_{GS} = 10 V

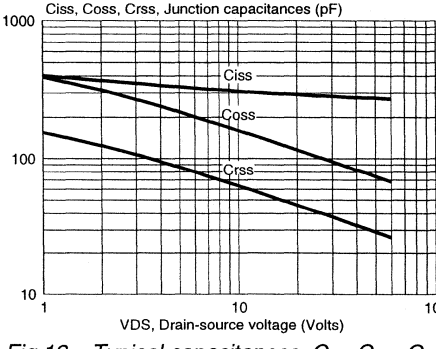


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

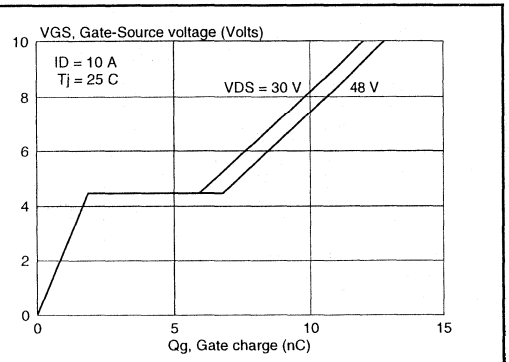


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; *parameter* V_{DS}

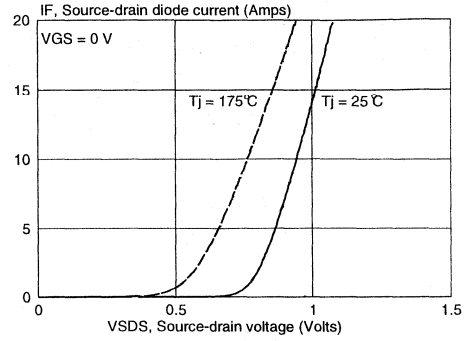


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; *parameter* T_j

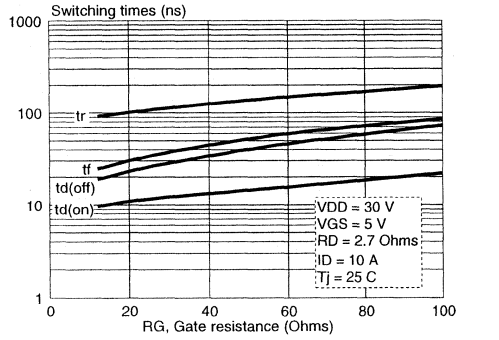


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

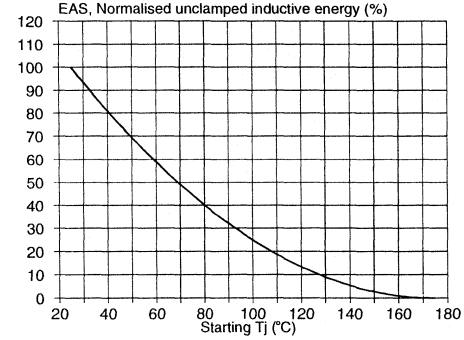


Fig.17. Normalised unclamped inductive energy.
$E_{AS}\% = f(T_j)$

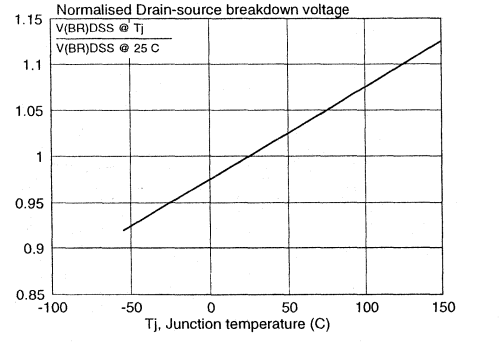


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ ^\circ C} = f(T_j)$

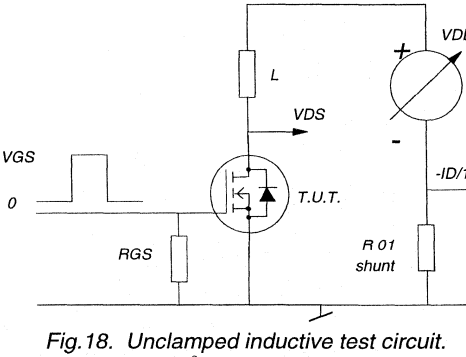


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot V_{(BR)DSS}/(V_{(BR)DSS} - V_{DD})$$

N-channel enhancement mode MOS transistor

PHN103

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-state resistance.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

DESCRIPTION

N-channel enhancement mode MOS transistor in an 8-pin plastic SOT96-1 (SO8) package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	n.c	not connected
2	s	source
3	s	source
4	g	gate
5	d	drain
6	d	drain
7	d	drain
8	d	drain

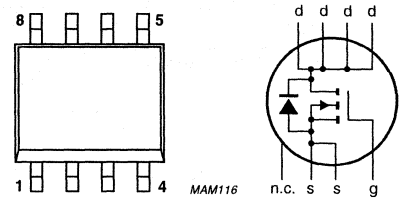


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{SD}	source-drain diode forward voltage	I_S = 1.25 A	–	1	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; $V_{DS} = V_{GS}$	1	2.8	V
I_D	drain current (DC)	T_s = 80 °C	–	8.5	A
R_{DSon}	drain-source on-state resistance	I_D = 5.5 A; V_{GS} = 10 V	–	0.03	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	4	W

N-channel enhancement mode MOS transistor

PHN103

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	8.5	A
I_{DM}	peak drain current	note 2	–	35	A
P_{tot}	total power dissipation	T_s = 80 °C	–	4	W
		T_{amb} = 25 °C; note 3	–	2.7	W
		T_{amb} = 25 °C; note 4	–	1.15	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–65	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	5	A
I_{SM}	peak pulsed source current	note 2	–	20	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	17.5	K/W

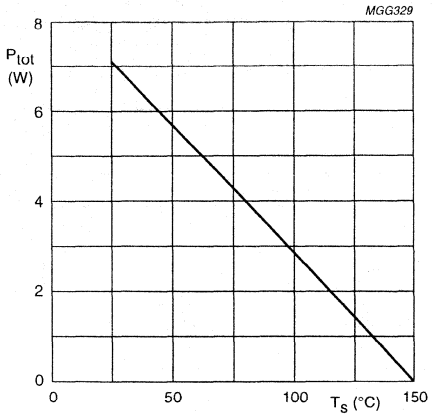
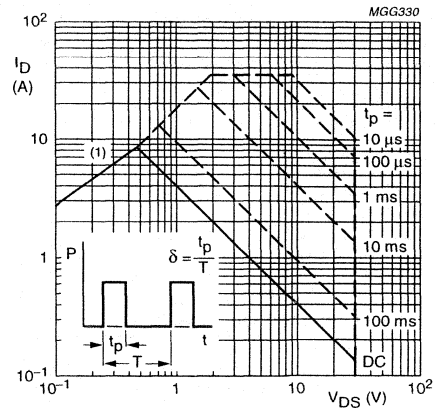


Fig.2 Power derating curve.



$\delta = 0.01$; $T_s = 80$ °C.
(1) R_{DSon} limitation.

Fig.3 SOAR.

N-channel enhancement mode MOS transistor

PHN103

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 µA	30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	1	–	2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 24 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 2.75 A	–	–	0.05	Ω
		V_{GS} = 10 V; I_D = 5.5 A	–	–	0.03	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	750	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	520	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	200	–	pF
Q_G	total gate charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 4 A	–	25	40	nC
Q_{GS}	gate-source charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 4 A	–	3	–	nC
Q_{GD}	gate-drain charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 4 A	–	7.5	–	nC
Switching times (see Fig.4)						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	7	–	ns
t_r	rise time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	10	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	17	35	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	35	–	ns
t_f	fall time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	40	–	ns
t_{off}	turn-off switching time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	75	150	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 1.25 A	–	–	1	V
t_{rr}	reverse recovery time	I_S = 1.25 A; di/dt = 100 A/µs	–	70	–	ns

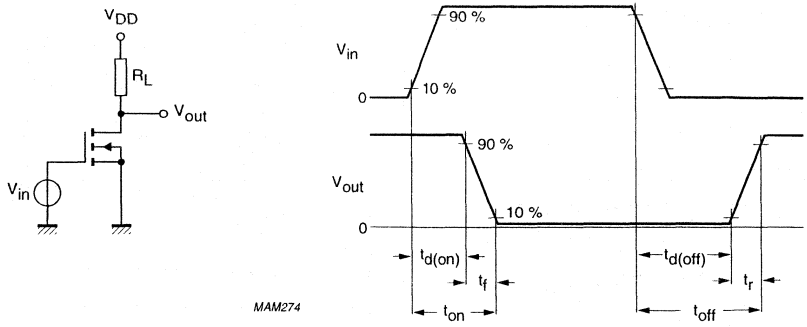
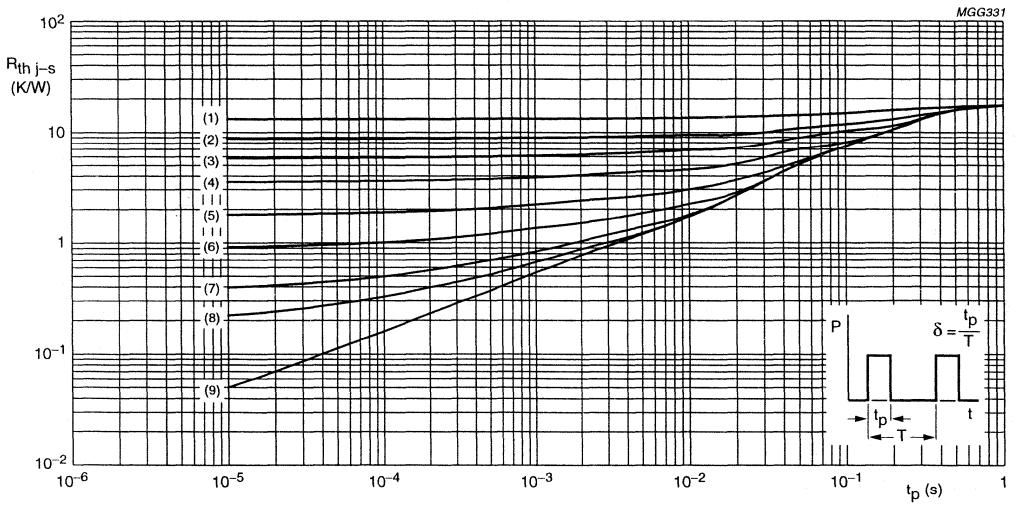
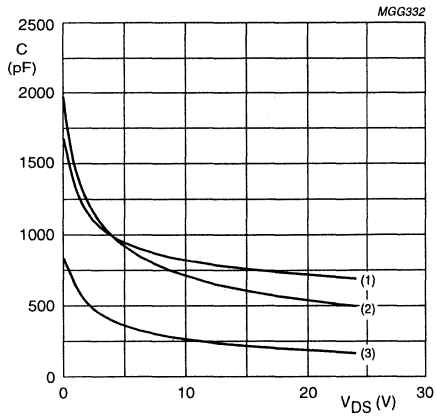


Fig.4 Switching times test circuit; input and output waveforms.



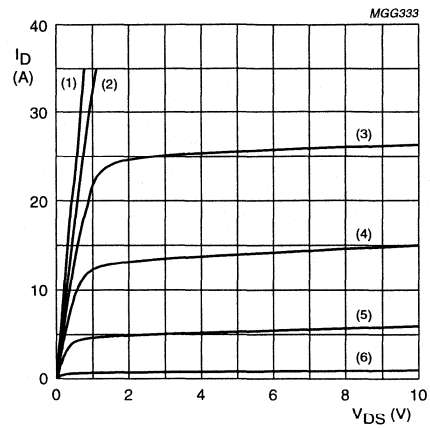
(1) $\delta = 0.75$. (2) $\delta = 0.5$. (3) $\delta = 0.33$. (4) $\delta = 0.2$.
(5) $\delta = 0.1$. (6) $\delta = 0.05$. (7) $\delta = 0.02$. (8) $\delta = 0.01$. (9) $\delta = 0$.

Fig.5 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.



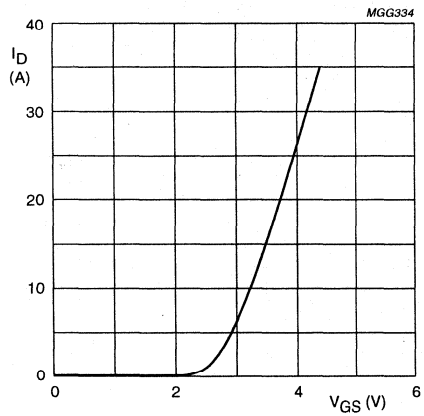
V_{GS} = 0; f = 1 MHz; T_j = 25 °C.
(1) C_{iss}.
(2) C_{oss}.
(3) C_{rss}.

Fig.6 Capacitance as a function of drain-source voltage; typical values.



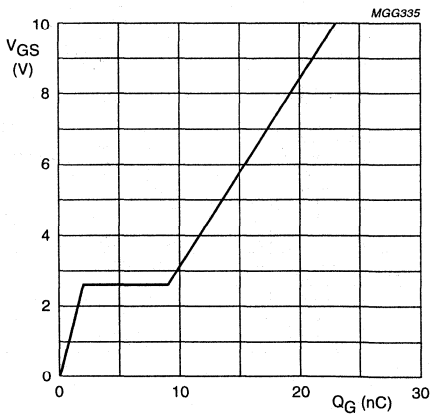
T_j = 25 °C.
(1) V_{GS} = 10 V.
(2) V_{GS} = 5 V.
(3) V_{GS} = 4 V.
(4) V_{GS} = 3.5 V.
(5) V_{GS} = 3 V.
(6) V_{GS} = 2.5 V.

Fig.7 Output characteristics; typical values.



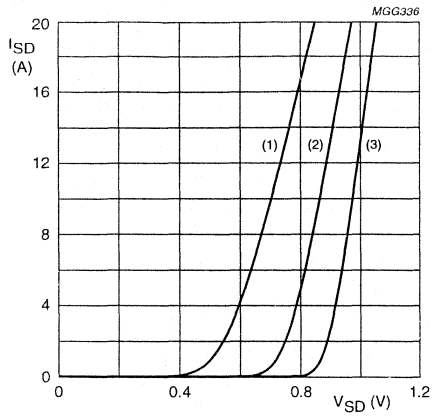
V_{DS} = 10 V; T_j = 25 °C.

Fig.8 Transfer characteristic; typical value.



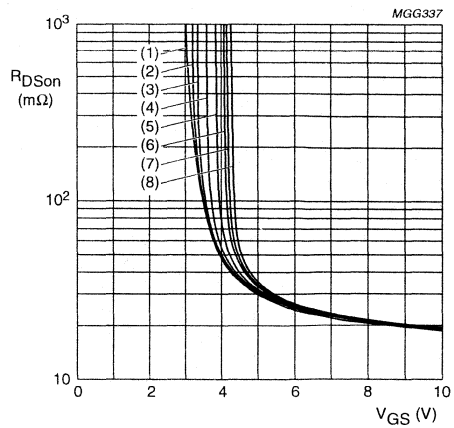
V_{DD} = 15 V; I_D = 4 A.

Fig.9 Gate-source voltage as a function of total gate charge; typical values.



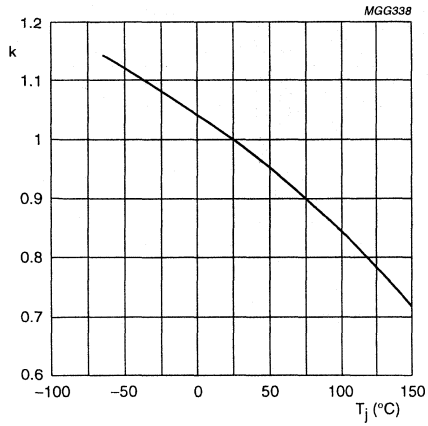
$V_{GD} = 0$.
(1) $T_j = 150$ °C.
(2) $T_j = 25$ °C.
(3) $T_j = -65$ °C.

Fig.10 Source current as a function of source-drain diode forward voltage; typical values.



$V_{DS} \geq I_D \times R_{DSon}$; $T_j = 25$ °C.
(1) $I_D = 0.1$ A.
(2) $I_D = 0.5$ A.
(3) $I_D = 1.0$ A.
(4) $I_D = 2.75$ A.
(5) $I_D = 5.5$ A.
(6) $I_D = 8.5$ A.
(7) $I_D = 10$ A.
(8) $I_D = 12$ A.

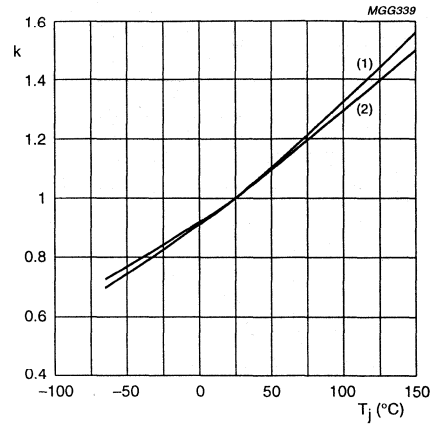
Fig.11 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

V_{GSth} at $V_{DS} = V_{GS}$; I_D = 1 mA.

Fig.12 Temperature coefficient of gate-source threshold voltage; typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

(1) R_{DSon} at V_{GS} = 10 V; I_D = 5.5 A.
(2) R_{DSon} at V_{GS} = 4.5 V; I_D = 2.75 A.

Fig.13 Temperature coefficient of drain-source on-state resistance; typical values.

N-channel enhancement mode MOS transistor

PHN110

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	n.c	not connected
2	s	source
3	s	source
4	g	gate
5	d	drain
6	d	drain
7	d	drain
8	d	drain

DESCRIPTION

N-channel enhancement mode MOS transistor in an 8-pin plastic SOT96-1 (SO8) package.

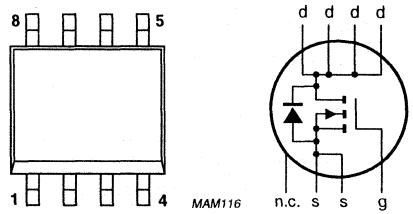


Fig.1 Simplified outline and symbol.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{SD}	source-drain diode forward voltage	I_S = 1.25 A	–	1.2	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}	1	2.8	V
I_D	drain current (DC)	T_s = 80 °C	–	4	A
R_{DSon}	drain-source on-state resistance	I_D = 2.2 A; V_{GS} = 10 V	–	0.1	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	2.8	W

N-channel enhancement mode MOS transistor

PHN110

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	4	A
I_{DM}	peak drain current	note 2	–	16	A
P_{tot}	total power dissipation	T_s = 80 °C	–	2.8	W
		T_{amb} = 25 °C; note 3	–	2.4	W
		T_{amb} = 25 °C; note 4	–	1.1	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–65	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	3.5	A
I_{SM}	peak pulsed source current	note 2	–	14	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Value based on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Value based on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

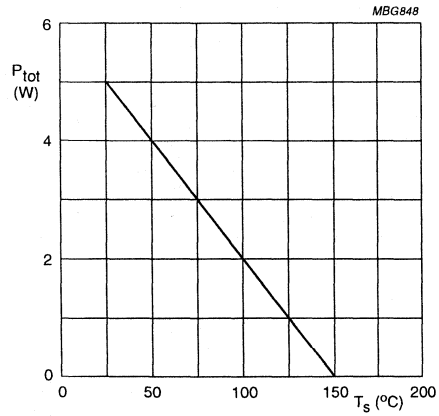
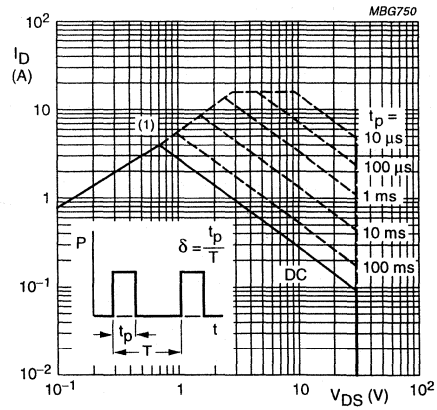


Fig.2 Power derating curve.



δ = 0.01; T_S = 80 °C.
(1) R_{DSon} limitation.

Fig.3 SOAR.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	25	K/W

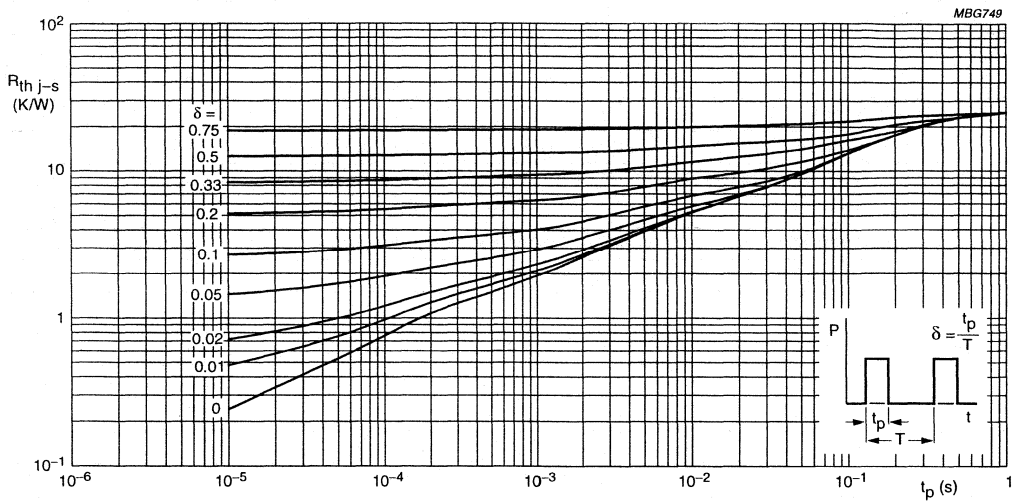


Fig.4 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

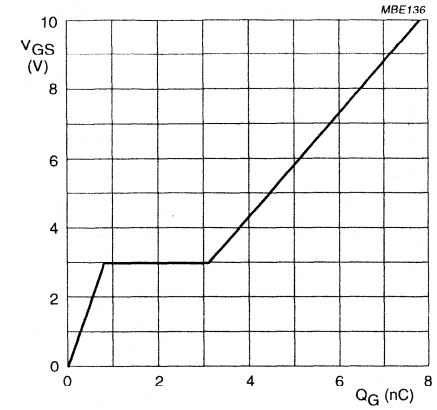
N-channel enhancement mode MOS transistor

PHN110

CHARACTERISTICS

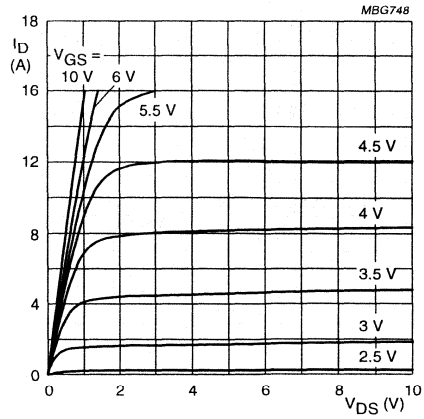
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 µA	30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	1	–	2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 24 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 1 A	–	0.11	0.2	Ω
		V_{GS} = 10 V; I_D = 2 A	–	0.08	0.1	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	250	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	140	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	50	–	pF
Q_g	total gate charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 2 A	–	10	30	nC
Q_{gs}	gate-source charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 2 A	–	1	–	nC
Q_{gd}	gate-drain charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 2 A	–	2.5	–	nC
Switching times (see Fig.11)						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	4.5	–	ns
t_f	fall time		–	3.5	–	ns
t_{on}	turn-on switching time		–	8	16	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	15	–	ns
t_r	rise time		–	10	–	ns
t_{off}	turn-off switching time		–	25	50	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 1.25 A	–	–	1.2	V
t_{rr}	reverse recovery time	I_S = 1.25 A; di/dt = –100 A/µs	–	35	100	ns



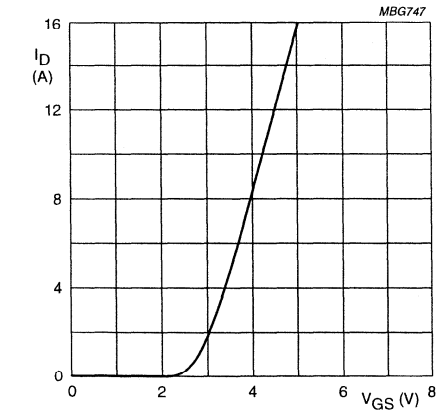
V_{DD} = 15 V: I_D = 2 A.

Fig.5 Gate-source voltage as a function of total gate charge; typical values.



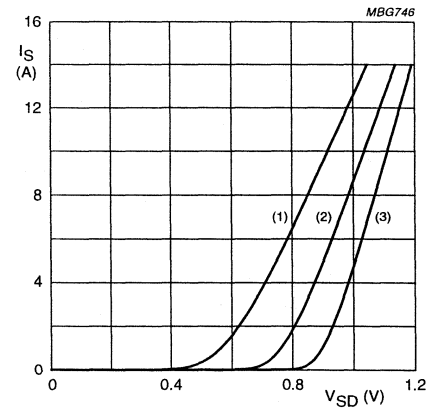
T_j = 25 °C.

Fig.6 Output characteristics; typical values.



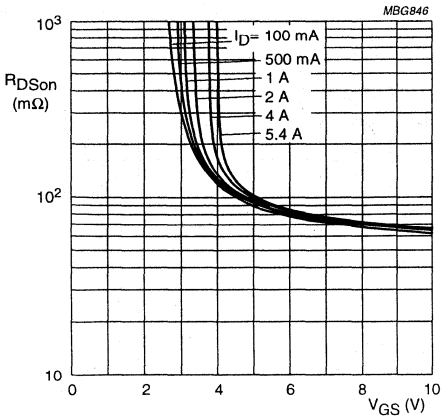
V_{DS} = 10 V; T_j = 25 °C.

Fig.7 Transfer characteristics; typical values.



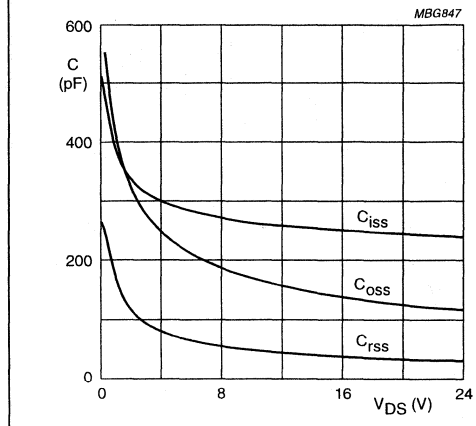
V_{GD} = 0.
(1) T_j = 150 °C.
(2) T_j = 25 °C.
(3) T_j = −65 °C.

Fig.8 Source current as a function of source-drain diode forward voltage; typical values.



$V_{DS} \geq I_D \times R_{DSon}$; T_j = 25 °C.

Fig.9 Drain-source on-resistance as a function of gate-source voltage; typical values.



V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

Fig.10 Capacitance as a function of drain-source voltage; typical values.

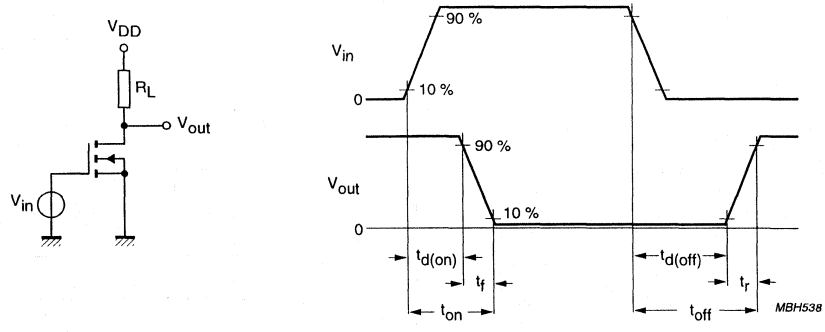
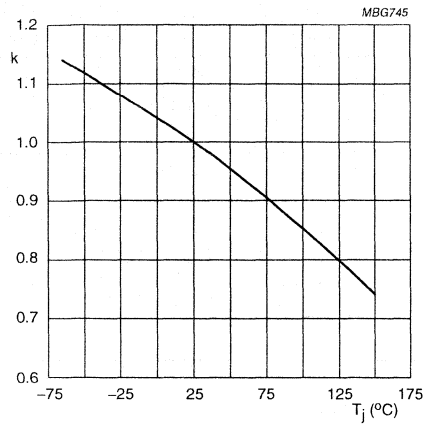


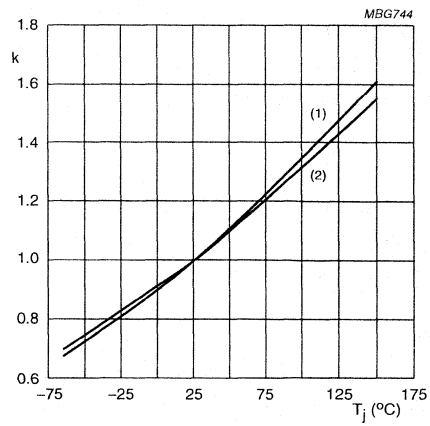
Fig.11 Switching time test circuit and input and output waveforms.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

Typical V_{GSth} at $V_{DS} = {}_{GS}$; I_D = 1 mA.

Fig.12 Temperature coefficient of gate-source threshold voltage; typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$ Typical R_{DSon} at:

(1) I_D = 2 A; V_{GS} = 10 V.

(2) I_D = 1 A; V_{GS} = 4.5 V.

Fig.13 Temperature coefficient of drain-source on-resistance; typical values.

Dual N-channel enhancement mode MOS transistor

PHN203

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-state resistance.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

DESCRIPTION

Two N-channel enhancement mode MOS transistors in an 8-pin plastic SOT96-1 (SO8) package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s_1	source 1
2	g_1	gate 1
3	s_2	source 2
4	g_2	gate 2
5	d_2	drain 2
6	d_2	drain 2
7	d_1	drain 1
8	d_1	drain 1

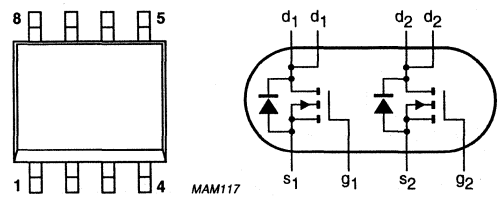


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per N-channel					
V_{DS}	drain-source voltage (DC)		–	30	V
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 1.25 A	–	1	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	–	V
I_D	drain current (DC)	T_s = 80 °C	–	8.2	A
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 4 A	–	30	mΩ
P_{tot}	total power dissipation	T_s = 80 °C	–	3.5	W

OBJECTIVE
See Philips Semiconductors for Design-in information

Dual N-channel enhancement mode MOS transistor

PHN203

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per N-channel					
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	8.2	A
I_{DM}	peak drain current	note 2	–	33	A
P_{tot}	total power dissipation	T_s = 80 °C; note 3	–	3.5	W
		T_{amb} = 25 °C; note 4	–	2.6	W
		T_{amb} = 25 °C; note 5	–	1.1	W
		T_{amb} = 25 °C; note 6	–	1.5	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	3.5	A
I_{SM}	peak pulsed source current	note 2	–	14	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Maximum permissible dissipation per transistor. Both devices may be loaded up to 3.5 Watt at the same time.
4. Maximum permissible dissipation per transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
5. Maximum permissible dissipation per transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.
6. Maximum permissible dissipation if only one MOS transistor dissipates. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	20	K/W

Dual N-channel enhancement mode MOS transistor

PHN203

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per N-channel						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	1	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 24 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 2 A	–	–	45	mΩ
		V_{GS} = 10 V; I_D = 4 A	–	–	30	mΩ
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	700	850	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	260	320	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	110	135	pF
Q_G	total gate charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 4 A	–	16	30	nC
Q_{GS}	gate-source charge	V_{DD} = 15 V; I_D = 4 A	–	2	–	nC
Q_{GD}	gate-drain charge	V_{DD} = 15 V; I_D = 4 A	–	6.5	–	nC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to 10 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	8	–	ns
t_f	fall time	V_{GS} = 0 to 10 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	9	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to 10 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	17	25	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = 10 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	19	–	ns
t_r	rise time	V_{GS} = 10 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	21	–	ns
t_{off}	turn-off switching time	V_{GS} = 10 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	40	60	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 1.25 A	–	–	1	V
t_{rr}	reverse recovery time	I_S = 1.25 A; di/dt = –100 A/μs	–	45	–	ns

Dual N-channel enhancement mode MOS transistor

PHN205

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-state resistance.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

DESCRIPTION

Two N-channel enhancement mode MOS transistors in an 8-pin plastic SOT96-1 (SO8) package.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s_1	source 1
2	g_1	gate 1
3	s_2	source 2
4	g_2	gate 2
5	d_2	drain 2
6	d_2	drain 2
7	d_1	drain 1
8	d_1	drain 1

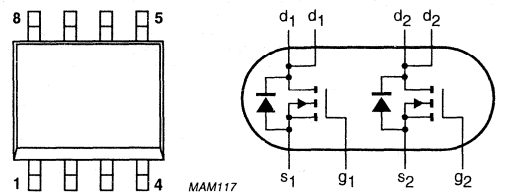


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per N-channel					
V_{DS}	drain-source voltage (DC)		–	30	V
V_{SD}	source-drain diode forward voltage	I_S = 1.25 A	–	1	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}	1	2.8	V
I_D	drain current (DC)	T_s = 80 °C	–	6.4	A
R_{DSon}	drain-source on-state resistance	I_D = 3.2 A; V_{GS} = 10 V	–	50	mΩ
P_{tot}	total power dissipation	T_s = 80 °C	–	3.5	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per N-channel					
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	6.4	A
I_{DM}	peak drain current	note 2	–	25	A
P_{tot}	total power dissipation	T_s = 80 °C; note 3	–	3.5	W
		T_{amb} = 25 °C; note 4	–	2.6	W
		T_{amb} = 25 °C; note 5	–	1.1	W
		T_{amb} = 25 °C; note 6	–	1.5	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–65	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	3.5	A
I_{SM}	peak pulsed source current	note 2	–	14	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Maximum permissible dissipation per MOS transistor. Both devices may be loaded up to 3.5 W at the same time.
4. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
5. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.
6. Maximum permissible dissipation if only one MOS transistor dissipates. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	20	K/W

Dual N-channel enhancement mode MOS transistor

PHN205

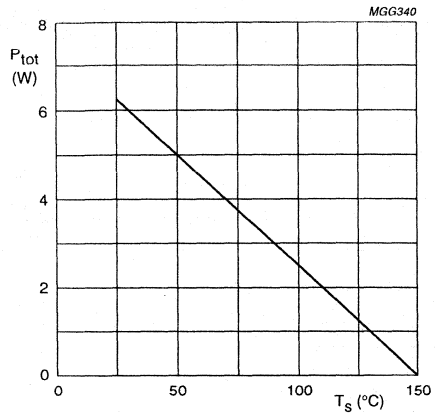
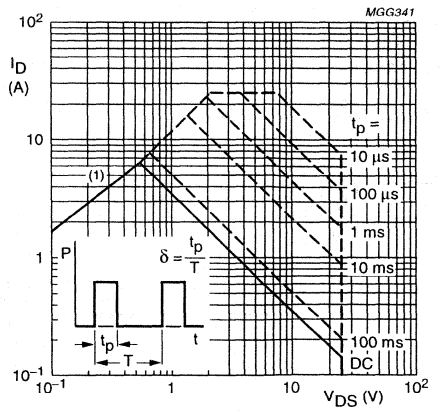


Fig.2 Power derating curve.



$\delta = 0.01$; $T_s = 80$ °C.
(1) R_{DSon} limitation.

Fig.3 SOAR.

Dual N-channel enhancement mode MOS transistor

PHN205

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per N-channel						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	1	–	2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 24 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 1.6 A	–	–	0.1	Ω
		V_{GS} = 10 V; I_D = 3.2 A	–	–	0.05	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	450	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	200	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	100	–	pF
Q_G	total gate charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 3.2 A	–	15	–	nC
Q_{GS}	gate-source charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 3.2 A	–	1	–	nC
Q_{GD}	gate-drain charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 3.2 A	–	5	–	nC
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω; see Fig.4	–	7	–	ns
t_f	fall time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω; see Fig.4	–	8	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω; see Fig.4	–	15	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω; see Fig.4	–	20	–	ns
t_r	rise time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω; see Fig.4	–	12	–	ns
t_{off}	turn-off switching time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω; see Fig.4	–	32	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 1.25 A	–	–	1	V
t_{rr}	reverse recovery time	I_S = 1.25 A; di/dt = –100 A/μs	–	45	–	ns

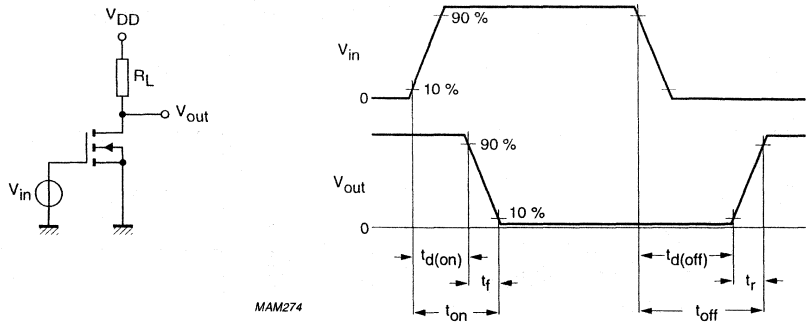
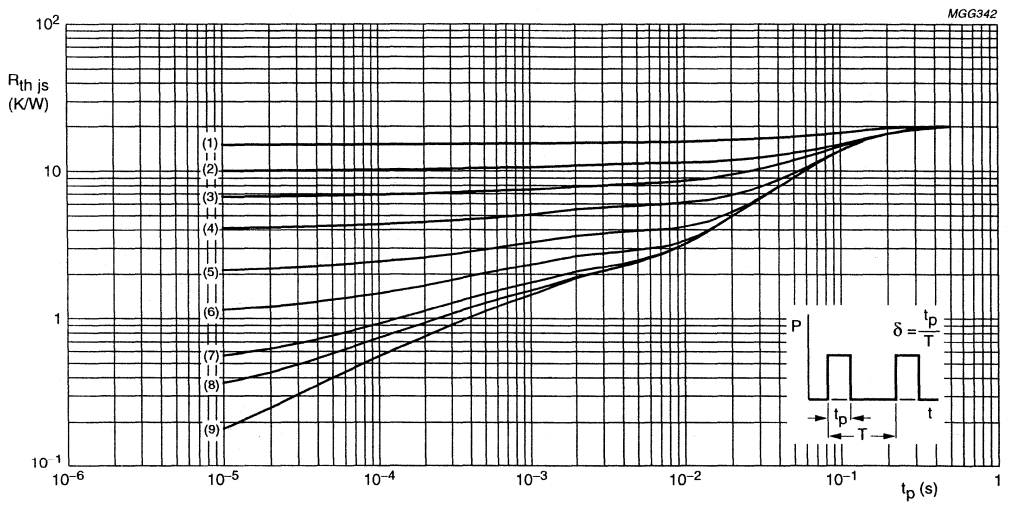
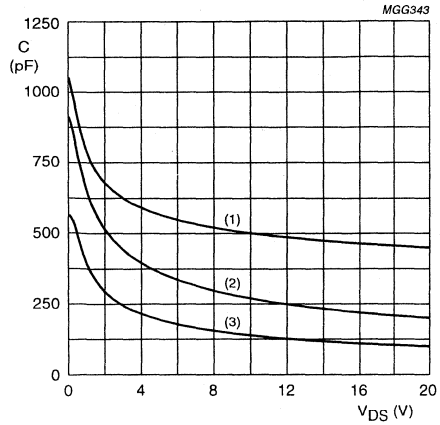


Fig.4 Switching time test circuit; input and output waveforms.



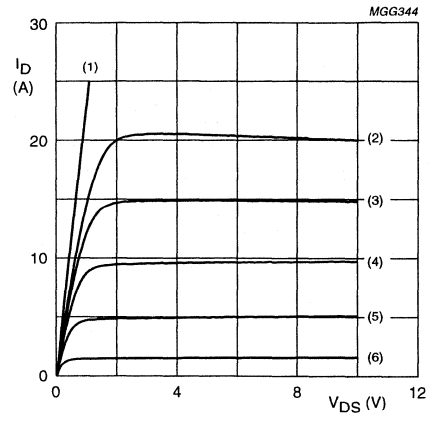
(1) δ = 0.75. (2) δ = 0.5. (3) δ = 0.33. (4) δ = 0.2.
(5) δ = 0.1. (6) δ = 0.05. (7) δ = 0.02. (8) δ = 0.01. (9) δ = 0.

Fig.5 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.



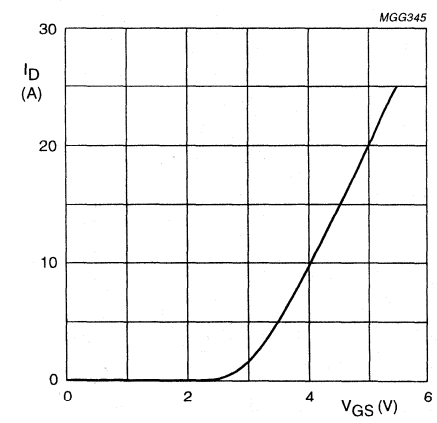
V_{GS} = 0; f = 1 MHz; T_j = 25 °C.
(1) C_{iss}.
(2) C_{oss}.
(3) C_{rss}.

Fig.6 Capacitance as a function of drain-source voltage; typical values.



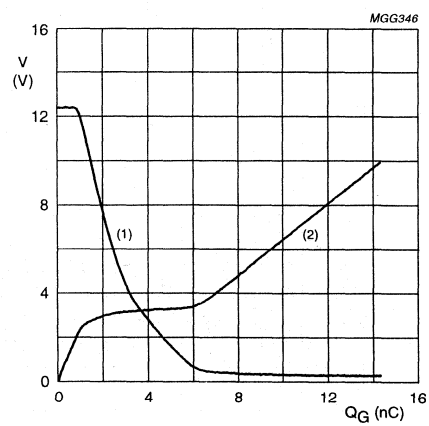
T_{amb} = 25 °C; t_p = 80 µs; δ = 0.
(1) V_{GS} = 10 V.
(2) V_{GS} = 5 V.
(3) V_{GS} = 4.5 V.
(4) V_{GS} = 4 V.
(5) V_{GS} = 3.5 V.
(6) V_{GS} = 3 V.

Fig.7 Output characteristics; typical values.



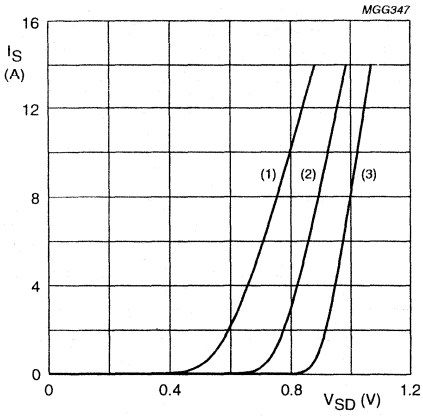
V_{DS} = 10 V; T_{amb} = 25 °C; t_p = 80 µs; δ = 0.

Fig.8 Transfer characteristics; typical values.



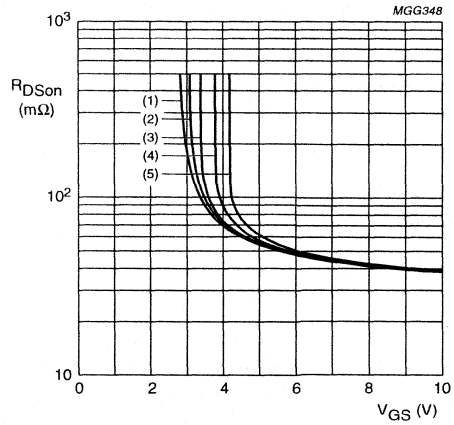
V_{DD} = 12.5 V; I_D = 3.2 A; T_{amb} = 25 °C.
(1) V_{DS}.
(2) V_{GS}.

Fig.9 Gate-source voltage and drain-source voltage as a function of total gate charge; typical values.



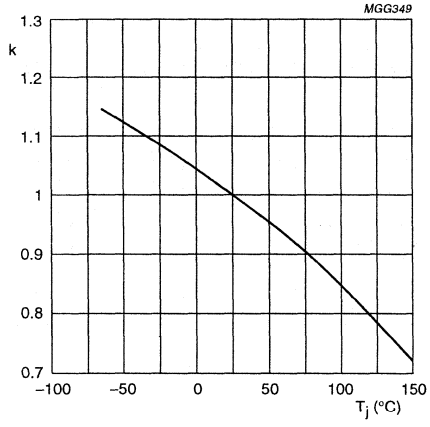
$V_{GD} = 0$.
(1) $T_{amb} = 150$ °C; $t_p = 300$ µs; $\delta = 0$.
(2) $T_{amb} = 25$ °C; $t_p = 300$ µs; $\delta = 0$.
(3) $T_{amb} = -65$ °C; $t_p = 300$ µs; $\delta = 0$.

Fig.10 Source current as a function of source-drain diode forward voltage; typical values.



$T_{amb} = 25$ °C; $t_p = 300$ µs; $\delta = 0$.
$V_{DS} \geq I_D \times R_{DSon}$.
(1) $I_D = 0.5$ A.
(2) $I_D = 1.6$ A.
(3) $I_D = 3.2$A.
(4) $I_D = 6.4$ A.
(5) $I_D = 10$ A.

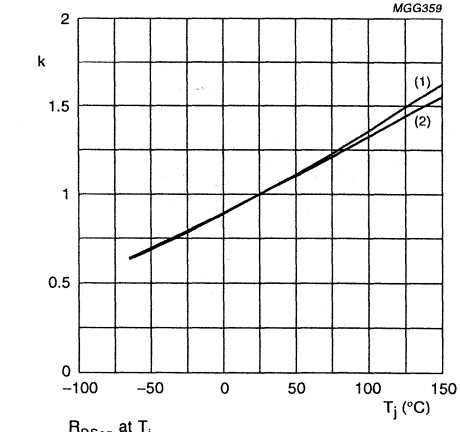
Fig.11 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

V_{GSth} at $V_{DS} = V_{GS}$; $I_D = 1$ mA.

Fig.12 Temperature coefficient of gate-source threshold voltage as a function of junction temperature; typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

(1) R_{DSon} at $V_{GS} = 10$ V; $I_D = 3.2$ A.
(2) R_{DSon} at $V_{GS} = 4.5$ V; $I_D = 1.6$ A.

Fig.13 Temperature coefficient of drain-source on-resistance as a function of junction temperature; typical values.

Dual N-channel enhancement mode MOS transistor

PHN210

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

DESCRIPTION

Two N-channel enhancement mode MOS transistors in an 8-pin plastic SOT96-1 (SO8) package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s_1	source 1
2	g_1	gate 1
3	s_2	source 2
4	g_2	gate 2
5	d_2	drain 2
6	d_2	drain 2
7	d_1	drain 1
8	d_1	drain 1

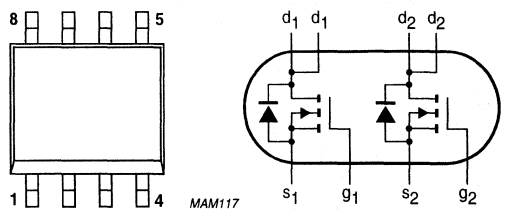


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per N-channel					
V_{DS}	drain-source voltage (DC)		–	30	V
V_{SD}	source-drain diode forward voltage	I_S = 1.25 A	–	1.2	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; $V_{DS} = V_{GS}$	1	2.8	V
I_D	drain current (DC)		–	3.5	A
R_{DSon}	drain-source on-state resistance	I_D = 2.2 A; V_{GS} = 10 V	–	0.1	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	2	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per N-channel					
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)	$T_s \leq 80°$ C	–	3.5	A
I_{DM}	peak drain current	note 1	–	14	A
P_{tot}	total power dissipation	T_s = 80 °C; note 2	–	2	W
		T_{amb} = 25 °C; note 3	–	2	W
		T_{amb} = 25 °C; note 4	–	1	W
		T_{amb} = 25 °C; note 5	–	1.3	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C
Source-drain diode					
I_S	source current (DC)	$T_s \leq 80$ °C	–	1.5	A
I_{SM}	peak pulsed source current	note 1	–	6	A

Notes

1. Pulse width and duty cycle limited by maximum junction temperature.
2. Maximum permissible dissipation per MOS transistor. Both devices may be loaded up to 2 W at the same time.
3. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.
5. Maximum permissible dissipation if only one MOS transistor dissipates. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

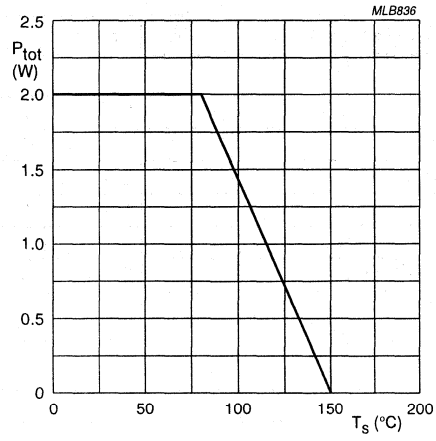
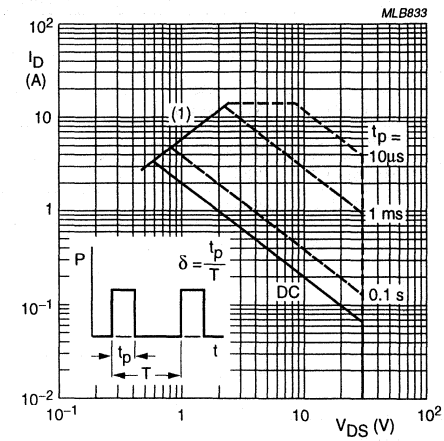


Fig.2 Power derating curve.



δ = 0.01.
T_s = 80 °C.
(1) R_{DSon} limitation.

Fig.3 SOAR.

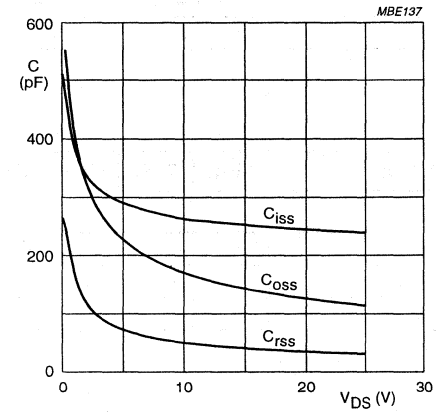
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	35	K/W

CHARACTERISTICS

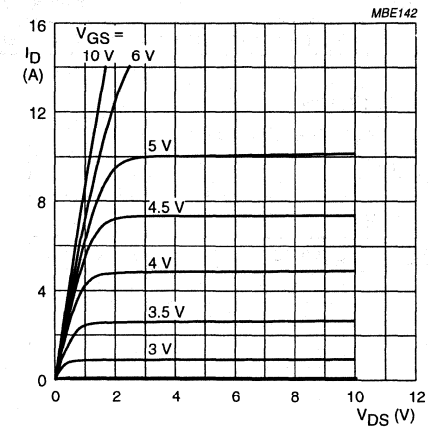
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per N-channel						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	1	–	2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 24 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
I_{Don}	on-state drain current	V_{GS} = 10 V; V_{DS} = 1 V	3.5	–	–	A
		V_{GS} = 4.5 V; V_{DS} = 5 V	2	–	–	A
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 1 A	–	0.11	0.2	Ω
		V_{GS} = 10 V; I_D = 2.2 A	–	0.08	0.1	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = 20 V; I_D = 2.2 A	2	4.5	–	S
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	–	250	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	–	140	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	–	50	–	pF
Q_G	total gate charge	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	–	10	30	nC
Q_{GS}	gate-source charge	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	–	1	–	nC
Q_{GD}	gate-drain charge	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	–	2.5	–	nC
Switching times						
t_{on}	turn-on time	V_{GS} = 0 to 10 V; V_{DD} = 20 V; I_D = 1 A; R_L = 20 Ω	–	15	40	ns
t_{off}	turn-off time	V_{GS} = 10 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_L = 20 Ω	–	25	140	ns
Source-drain diode						
V_{SD}	source drain diode forward voltage	V_{GD} = 0; I_S = 1.25 A	–	–	1.2	V
t_{rr}	reverse recovery time	I_S = 1.25 A; di/dt = 100 A/μs	–	35	100	ns



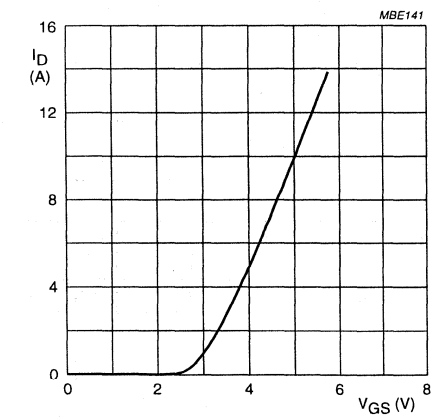
V_{GS} = 0.
T_j = 25 °C.

Fig.4 Capacitance as a function of drain-source voltage; typical values.



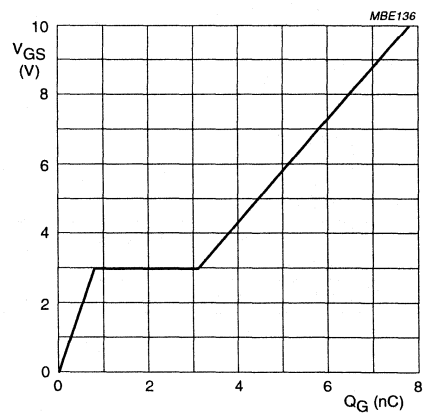
T_j = 25 °C.

Fig.5 Output characteristics; typical values.



V_{DS} = 10 V.
T_j = 25 °C.

Fig.6 Transfer characteristic; typical values.

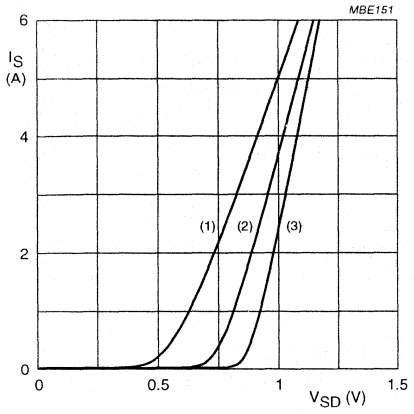


V_{DD} = 15 V.
I_D = 3.5 A.

Fig.7 Gate-source voltage as a function of total gate charge.

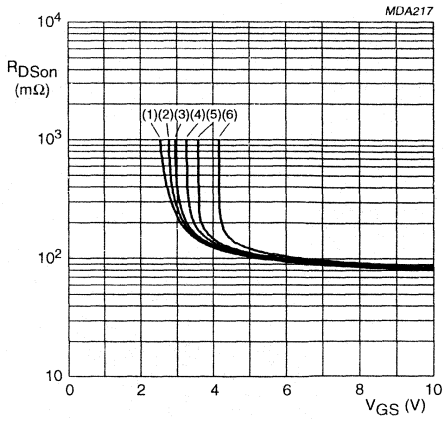
Dual N-channel enhancement mode MOS transistor

PHN210



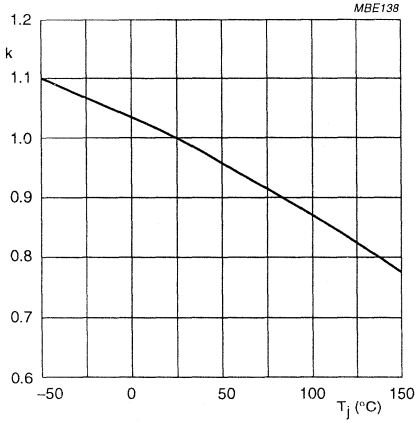
$V_{GD} = 0$.
(1) $T_j = 150$ °C.
(2) $T_j = 25$ °C.
(3) $T_j = -55$ °C.

Fig.8 Source current as a function of source-drain diode forward voltage.



$V_{DS} \geq I_D \times R_{DSon}$; $T_j = 25$ °C.
(1) $I_D = 0.1$ A.
(2) $I_D = 0.5$ A.
(3) $I_D = 1$ A.
(4) $I_D = 2.2$ A.
(5) $I_D = 3.5$ A.
(6) $I_D = 7$ A.

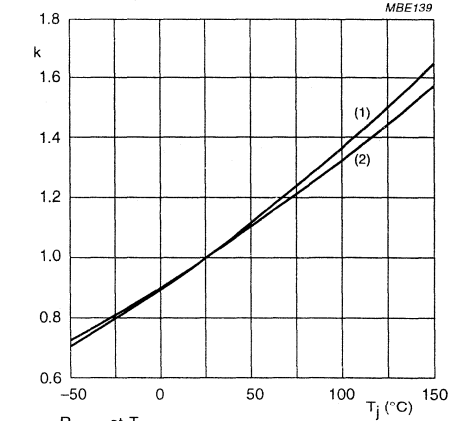
Fig.9 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

Typical V_{GSth} at $I_D = 1$ mA; $V_{DS} = V_{GS} = V_{GSth}$.

Fig.10 Temperature coefficient of gate-source threshold voltage.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

Typical R_{DSon} at:
(1) $I_D = 2.2$ A; $V_{GS} = 10$ V.
(2) $I_D = 1$ A; $V_{GS} = 4.5$ V.

Fig.11 Temperature coefficient of drain-source on-resistance.

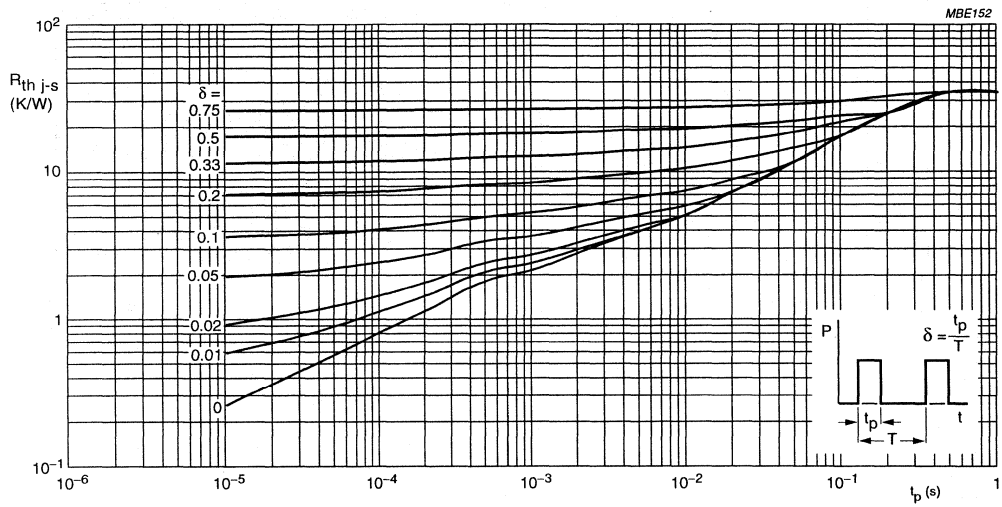


Fig.12 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

4 N-channel 60 mΩ FET array enhancement mode MOS transistors

PHN405

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-state resistance
- Current monitoring.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

DESCRIPTION

Four enhancement mode MOS transistors in a 16-pin plastic SOT338-1 (SSOP16) package. Two transistors feature current monitoring (sense FETs).

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT338-1 (SSOP16)

PIN	SYMBOL	DESCRIPTION
1 and 4	d_1	drain 1
2	s_1	source 1
3	g_1	gate 1
5 and 8	d_2	drain 2
6	s_2	source 2
7	g_2	gate 2
9	g_3	gate 3
10	s_3	source 3
11 and 15	d_3	drain 3
12	m_3	current monitor 3
13	g_4	gate 4
14	s_4	source 4
16	m_4	current monitor 4

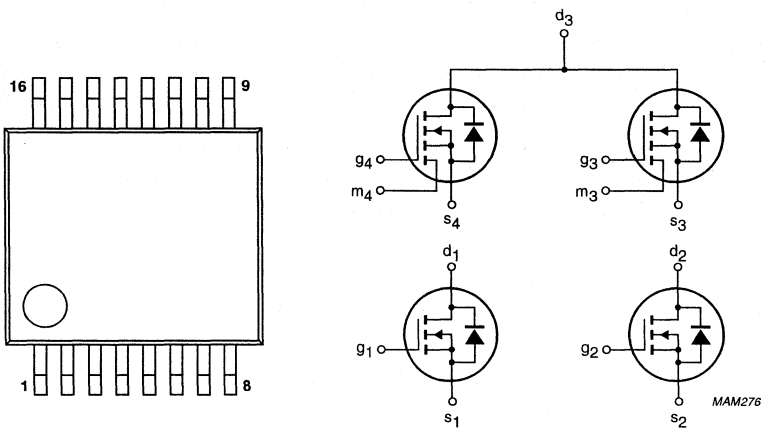


Fig.1 Simplified outline and symbol.

4 N-channel 60 mΩ FET array enhancement mode MOS transistors

PHN405

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}	1	2.8	V
I_D	drain current (DC)	T_s = 80 °C	–	3.7	A
R_{DSon}	drain-source on-state resistance	I_D = 2 A; V_{GS} = 10 V	–	60	mΩ
P_{tot}	total power dissipation	T_s = 80 °C	–	1.4	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per FET					
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	3.7	A
I_{DM}	peak drain current	note 2	–	14.8	A
P_{tot}	total power dissipation	T_s = 80 °C; note 3	–	1.4	W
		T_s = 80 °C; note 4	–	1.25	W
		T_s = 80 °C; note 5	–	1.09	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Current monitor					
I_M	monitor current (DC)	T_s = 80 °C	–	50	mA
I_{MM}	peak monitor current	note 2	–	220	mA
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	1.4	A
I_{SM}	peak source current	note 2	–	5.6	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. When only one FET dissipates.
4. When either FETs 1 and 3 or 2 and 4 dissipate an equal amount of power.
5. When all four FETs dissipate an equal amount of power.

4 N-channel 60 mΩ FET array enhancement mode MOS transistors

PHN405

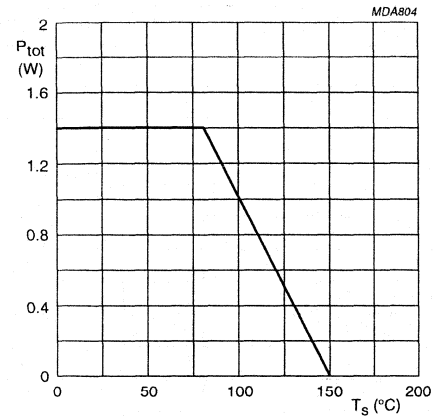
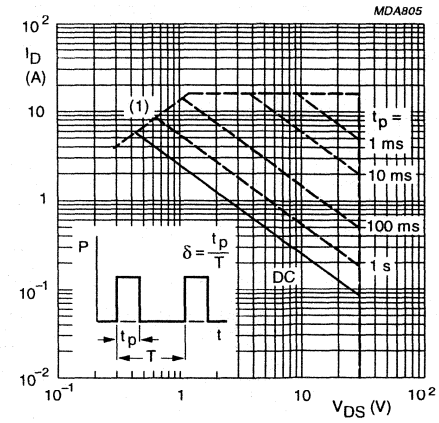


Fig.2 Power derating curve.



$\delta = 0.01$; $T_s = 80$ °C.
(1) R_{DSon} limitation.

Fig.3 SOAR.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
Per FET				
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	note 1	50	K/W
		note 2	56	K/W
		note 3	64	K/W

Notes

1. When only one FET dissipates.
2. When either FETs 1 and 3 or 2 and 4 dissipate an equal amount of power.
3. When all four FETs dissipate an equal amount of power.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per FET						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	1	–	2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 24 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 1 A	–	–	120	mΩ
		V_{GS} = 10 V; I_D = 2 A	–	–	60	mΩ
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	230	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	90	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	50	–	pF
Q_G	total gate charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 1 A	–	7.1	10	nC
Q_{GS}	gate-source charge	V_{DD} = 15 V; I_D = 1 A;	–	0.5	–	nC
Q_{GD}	gate-drain charge	V_{DD} = 15 V; I_D = 1 A;	–	2.4	–	nC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to 10 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	3.5	–	ns
t_f	fall time	V_{GS} = 0 to 10 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	3.5	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to 10 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	7	10	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = 10 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	12	–	ns
t_r	rise time	V_{GS} = 10 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	8	–	ns
t_{off}	turn-off switching time	V_{GS} = 10 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	20	30	ns
Current monitor						
R_{DMon}	on-state drain-monitor resistance	V_{GM} = 10 V; I_D = 25 mA; I_S = 0	–	–	4	Ω
		V_{GM} = 4.5 V; I_D = 12 mA; I_S = 0	–	–	8	Ω
I_S/I_M	source to monitor current ratio	V_{GS} = 10 V; I_D = 2 A; V_{MS} = 0	–	66.7	–	
C_{Moss}	output capacitance of monitor cells	V_{GM} = V_{MS} = 0; V_{DS} = 24 V; f = 1 MHz	–	1.35	–	pF
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 1.25 A	–	–	1	V
t_{rr}	reverse recovery time	I_S = 1.25 A; di/dt = –100 A/μs	–	25	–	ns

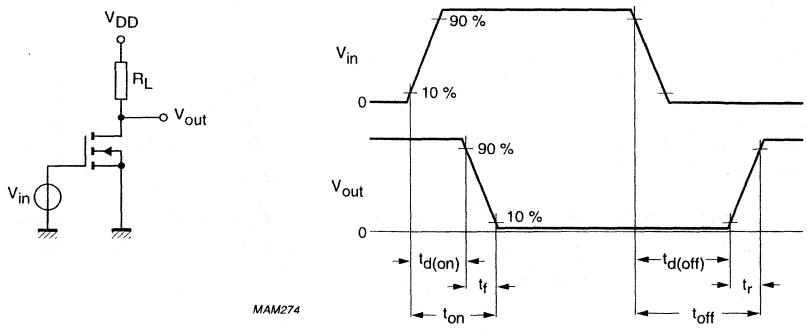


Fig.4 Switching times test circuit with input and output waveforms.

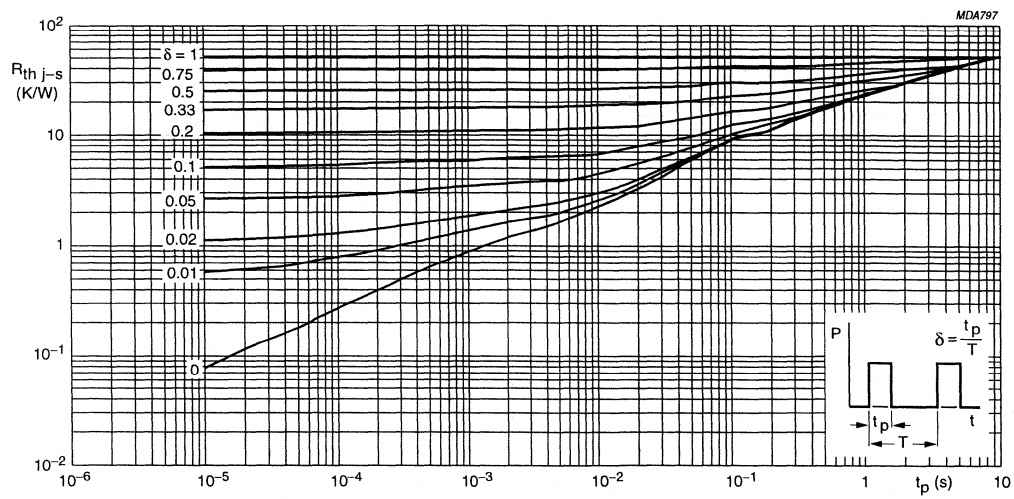
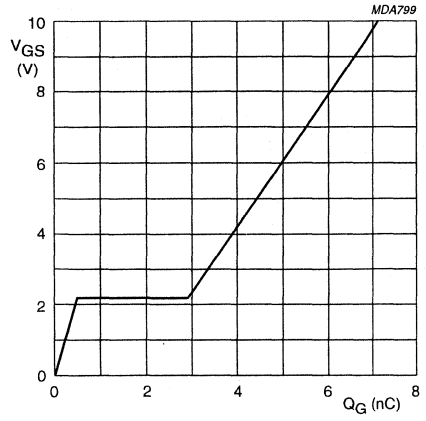
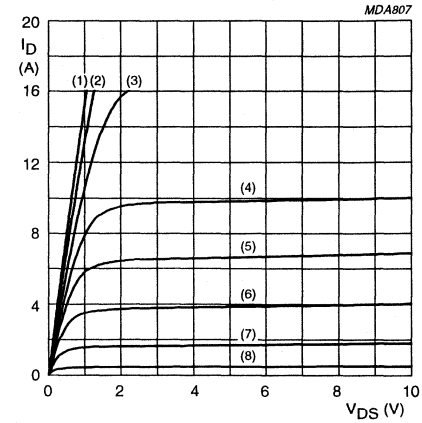


Fig.5 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.



V_{DD} = 15 V; I_D = 1 A; T_{amb} = 25 °C.

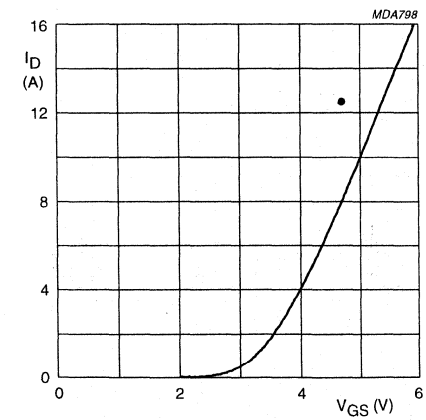
Fig.6 Gate-source voltage as a function of total gate charge; typical values.



T_{amb} = 25 °C; t_p = 80 µs; δ = 0.

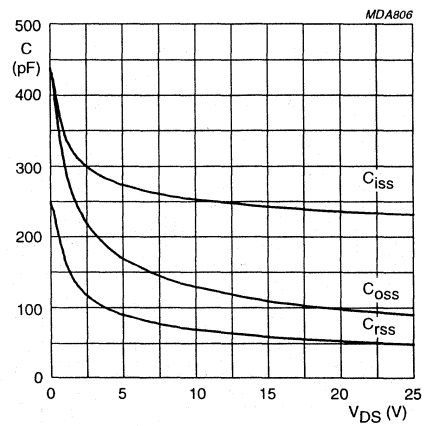
(1) V_{GS} = 10 V.
(2) V_{GS} = 7.5 V.
(3) V_{GS} = 6 V.
(4) V_{GS} = 5 V.
(5) V_{GS} = 4.5 V.
(6) V_{GS} = 4 V.
(7) V_{GS} = 3.5 V.
(8) V_{GS} = 3 V.

Fig.7 Output characteristics; typical values.



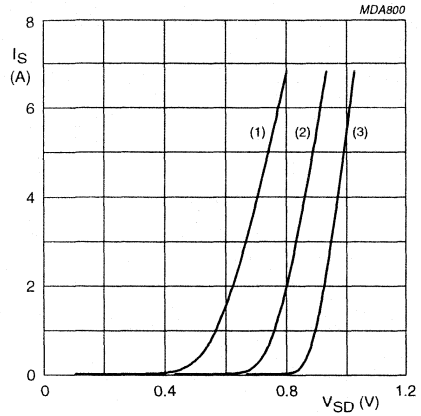
V_{DS} = 10 V; T_{amb} = 25 °C; t_p = 80 µs; δ = 0.

Fig.8 Transfer characteristic; typical values.



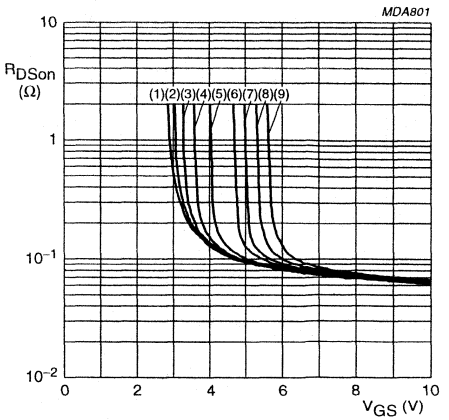
V_{GS} = 0 ; f = 1 MHz; T_j = 25 °C.

Fig.9 Capacitance as a function of drain-source voltage; typical values.



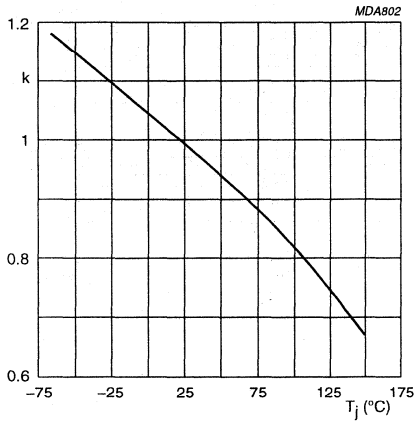
t_p = 300 μs; δ = 0.
(1) T_{amb} = 150 °C.
(2) T_{amb} = 25 °C.
(3) T_{amb} = −65 °C.

Fig.10 Source current as a function of source-drain diode forward voltage; typical values.



T_{amb} = 25 °C; t_p = 300 μs; δ = 0.
(1) I_D = 0.25 A.
(2) I_D = 0.5 A.
(3) I_D = 1 A.
(4) I_D = 2 A.
(5) I_D = 4 A.
(6) I_D = 8 A.
(7) I_D = 10 A.
(8) I_D = 13 A.
(9) I_D = 16 A.

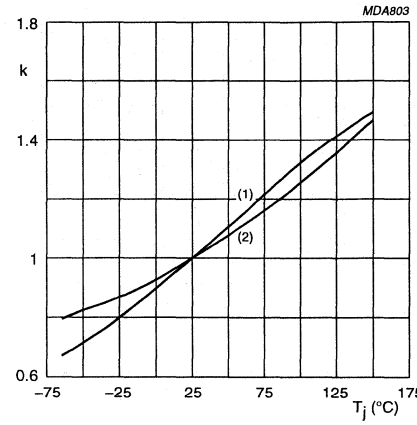
Fig.11 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

V_{GSth} at $V_{DS} = V_{GS}$; I_D = 1 mA.

Fig.12 Temperature coefficient of gate-source threshold voltage as a function of junction temperature; typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

R_{DSon} at:

(1) V_{GS} = 10 V; I_D = 2 A.

(2) V_{GS} = 4.5 V; I_D = 1 A.

Fig.13 Temperature coefficient of drain-source on-resistance as a function of junction temperature; typical values.

6 N-channel 30 mΩ FET/Schottky barrier diode array

PHN603S

FEATURES

- 30 mΩ on-state resistance
- On board Schottky diodes for back-emf clamping.

APPLICATIONS

- Driving high performance three phase brushless DC motors.

DESCRIPTION

Six enhancement mode MOS transistors and six Schottky barrier diodes in a 24-pin SOT137-1 (SO24) plastic package, in three half-bridge configuration.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

PINNING - SOT137-1 (SO24)

PIN	SYMBOL	DESCRIPTION
1 and 4	d_1	drain 1
2	s_1	source 1
3	g_1	gate 1
5 and 8	d_2	drain 2
6	s_2	source 2
7	g_2	gate 2
9 and 12	d_3	drain 3
10	s_3	source 3
11	g_3	gate 3
13	g_4	gate 4
14, 15, 16, 18, 19, 20, 22, 23, 24	d_4	drain 4
17	g_5	gate 5
21	g_6	gate 6

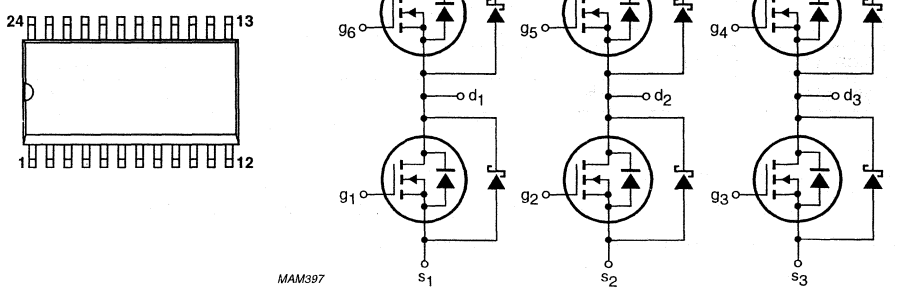


Fig.1 Simplified outline and symbol.

6 N-channel 30 mΩ FET/Schottky barrier diode array

PHN603S

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per N-channel					
V_{DS}	drain-source voltage (DC)		–	30	V
V_F	forward voltage (Schottky barrier diode)	V_{GD} = 0; I_F = 2.5 A	–	0.8	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	–	V
I_D	drain current (DC)	T_s = 80 °C	–	5	A
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A	–	30	mΩ
P_{tot}	total power dissipation	T_s = 80 °C	–	2	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per N-channel					
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	5	A
I_{DM}	peak drain current	note 3	–	20	A
Schottky barrier diode					
I_F	forward current (DC)	T_s = 80 °C	–	2.5	A
I_{FRM}	repetitive peak forward current	note 3	–	10	A
Total device					
P_{tot}	total power dissipation	T_s = 80 °C	–	2	W
		T_{amb} = 25 °C; note 2	–	1.5	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 50 K/W.
3. Pulse width and duty cycle limited by maximum junction temperature.

6 N-channel 30 mΩ FET/Schottky barrier diode array

PHN603S

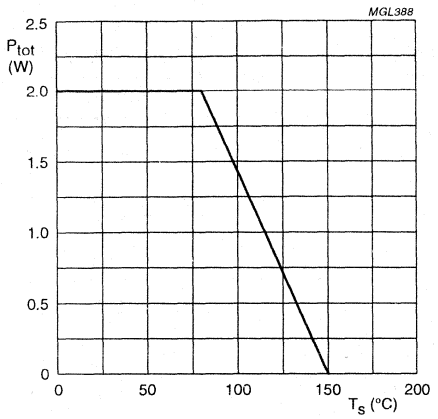


Fig.2 Power derating curve.

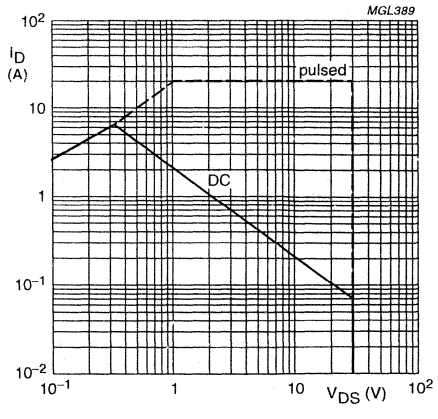


Fig.3 SOAR.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
Per N-channel			
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	35	K/W

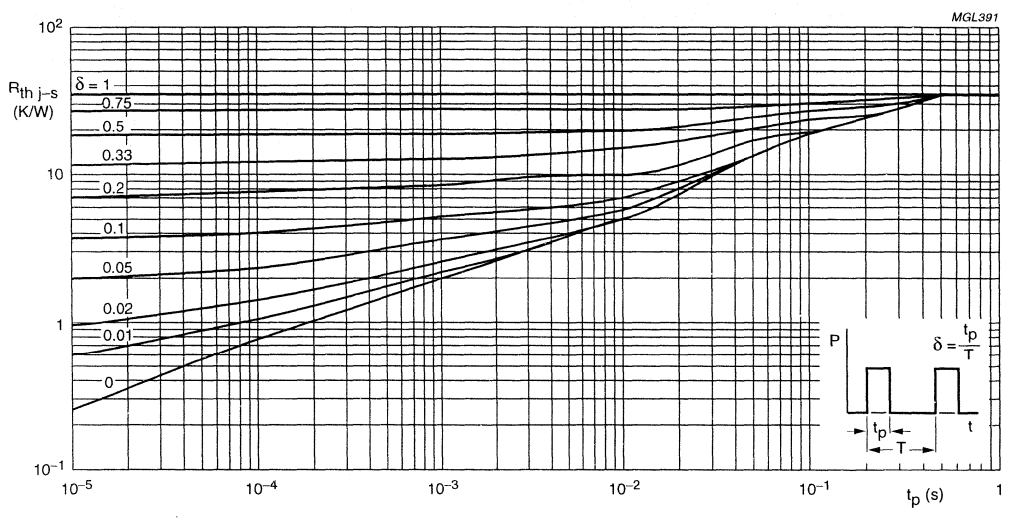
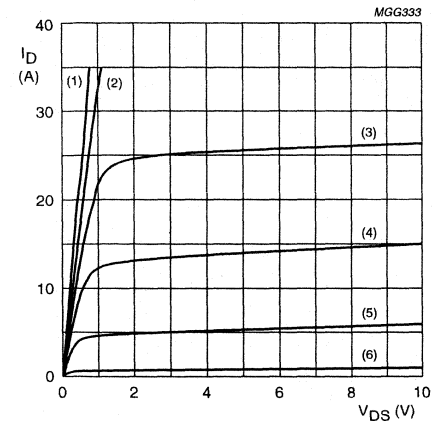


Fig.4 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

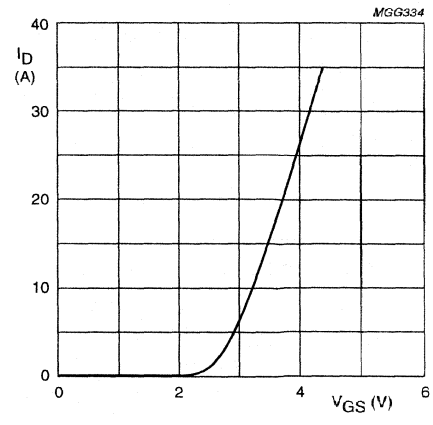
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per N-channel						
V_{GSth}	gate-source threshold voltage	$V_{GS} = V_{DS}$; I_D = 1 mA	1	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 25 V	–	1	–	μA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 2.5 A	–	–	50	mΩ
		V_{GS} = 10 V; I_D = 5 A	–	–	30	mΩ
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 25 V; f = 1 MHz	–	700	850	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 25 V; f = 1 MHz	–	260	320	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 25 V; f = 1 MHz	–	110	135	pF
Q_G	total gate charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 5 A	–	16	30	nC
Q_{GS}	gate-source charge	V_{DD} = 15 V; I_D = 5 A	–	2	–	nC
Q_{GD}	gate-drain charge	V_{DD} = 15 V; I_D = 5 A	–	6.5	–	nC
Switching times (see Fig.14)						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to 10 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	8	–	ns
t_f	fall time		–	9	–	ns
t_{on}	turn-on switching time		–	17	25	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = 10 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	19	–	ns
t_r	rise time		–	21	–	ns
t_{off}	turn-off switching time		–	40	60	ns
Schottky barrier diode						
V_{RRM}	repetitive peak reverse voltage	V_{GS} = 0	–	–	30	V
V_{RWM}	crest working reverse voltage	V_{GS} = 0	–	–	30	V
V_F	forward voltage	V_{GD} = 0; I_F = 2.5 A	–	–	0.8	V
		V_{GD} = 0; I_F = 2.5 A; T_j = 150 °C	–	–	0.7	V
I_R	reverse current	V_{GS} = 0; V_R = 25 V	–	1	–	μA
		V_{GS} = 0; V_R = 25 V; T_j = 150 °C	–	1.5	–	mA



T_j = 25 °C.

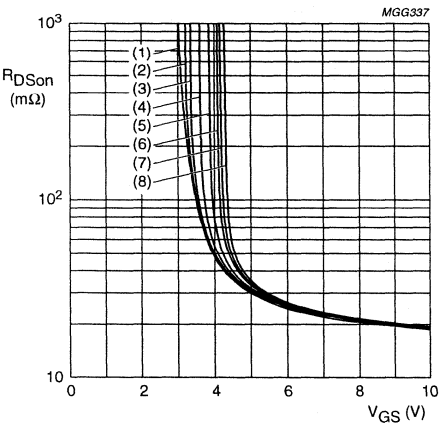
(1) V_{GS} = 10 V.
(2) V_{GS} = 5 V.
(3) V_{GS} = 4 V.
(4) V_{GS} = 3.5 V.
(5) V_{GS} = 3 V.
(6) V_{GS} = 2.5 V.

Fig.5 Output characteristics; typical values.



V_{DS} = 10 V; T_j = 25 °C.

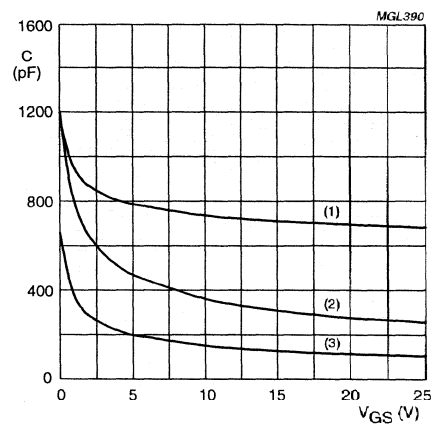
Fig.6 Transfer characteristic; typical values.



$V_{DS} \geq I_D \times R_{DSon}$; T_j = 25 °C.

(1) I_D = 0.1 A.
(2) I_D = 0.5 A.
(3) I_D = 1 A.
(4) I_D = 2.75 A.
(5) I_D = 5.5 A.
(6) I_D = 8.5 A.
(7) I_D = 10 A.
(8) I_D = 12 A.

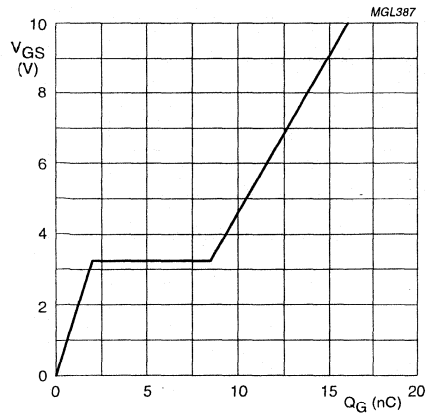
Fig.7 Drain-source on-state resistance as a function of gate-source voltage; typical values.



V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

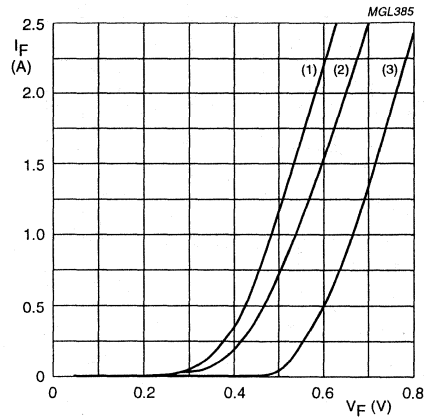
(1) C_{iss}.
(2) C_{oss}.
(3) C_{rss}.

Fig.8 Capacitance as a function of drain-source voltage; typical values.



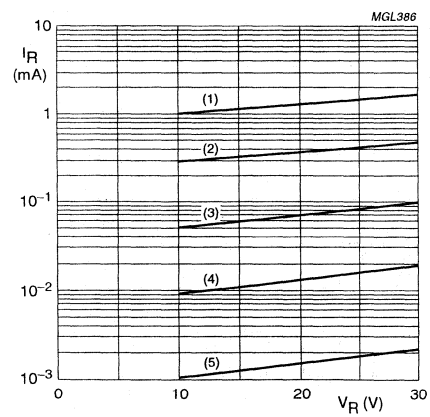
V_{DD} = 15 V; I_D = 5 A; T_j = 25 °C.

Fig.9 Gate-source voltage as a function of total gate charge; typical values.



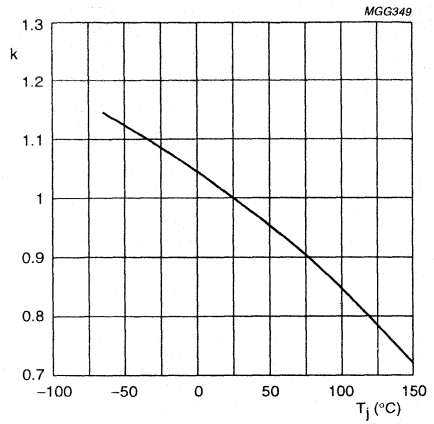
V_{GD} = 0.
(1) T_j = 150 °C; typical values. (3) T_j = 25 °C; maximum values.
(2) T_j = 150 °C; maximum values.

Fig.10 Forward current (Schottky barrier diode) as a function of forward voltage; typical values.



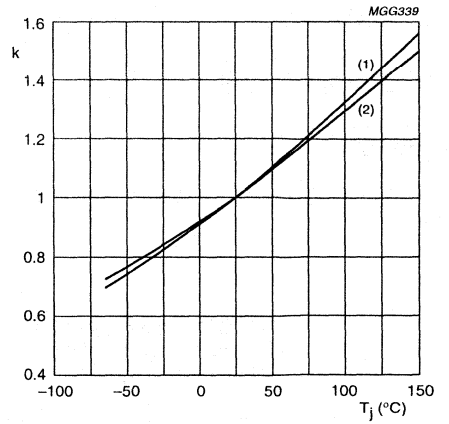
V_{GS} = 0.
(1) T_j = 150 °C. (3) T_j = 100 °C. (5) T_j = 50 °C.
(2) T_j = 125 °C. (4) T_j = 75 °C.

Fig.11 Reverse current (Schottky barrier diode) as a function of reverse voltage; typical values.



$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$ V_{GSth} at $V_{DS} = V_{GS}$; I_D = 1 mA.

Fig.12 Temperature coefficient of gate-source threshold voltage as a function of junction temperature; typical values.



$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$

(1) R_{DSon} at V_{GS} = 10 V; I_D = 5.5 A.
(2) R_{DSon} at V_{GS} = 4.5 V; I_D = 2.75 A.

Fig.13 Temperature coefficient of drain-source on-resistance as a function of junction temperature; typical values.

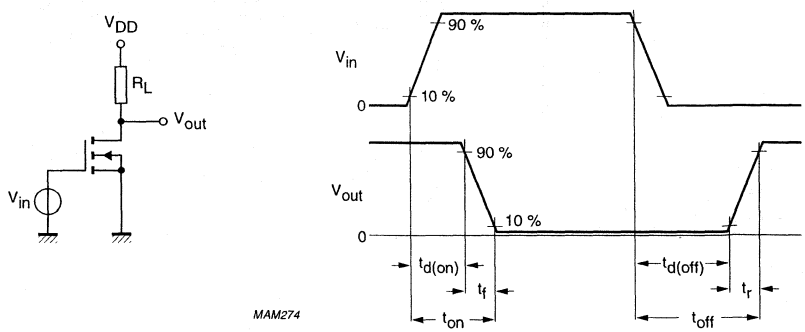


Fig.14 Switching times test circuit; input and output waveforms.

7 N-channel 80 mΩ FET array enhancement mode MOS transistors

PHN708

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-state resistance.

APPLICATIONS

- Driving high performance three phase brushless DC motors.

DESCRIPTION

Seven enhancement mode MOS transistors in a 24-pin plastic SOT340-1 (SSOP24) package. Six of the transistors are in three half-bridge configurations.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT340-1 (SSOP24)

PIN	SYMBOL	DESCRIPTION
1 and 4	d_1	drain 1
2	s_1	source 1
3	g_1	gate 1
5 and 8	d_2	drain 2
6	s_2	source 2
7	g_2	gate 2
9 and 12	d_3	drain 3
10	s_3	source 3
11	g_3	gate 3
13	g_4	gate 4
14	s_4	source 4
15, 17, 18, 20, 21, 23, 24	d_4	drain 4
16	g_5	gate 5
19	g_6	gate 6
22	g_7	gate 7

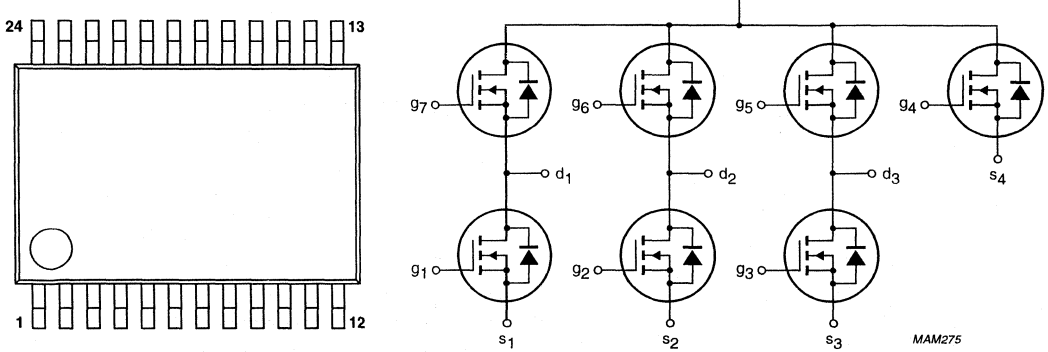


Fig.1 Simplified outline and symbol.

7 N-channel 80 mΩ FET array enhancement mode MOS transistors

PHN708

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}	1	2.8	V
I_D	drain current (DC)	T_s = 80 °C	–	3.1	A
R_{DSon}	drain-source on-state resistance	I_D = 1.5 A; V_{GS} = 10 V	–	80	mΩ
P_{tot}	total power dissipation	T_s = 80 °C	–	1.3	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per FET					
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	3.1	A
I_{DM}	peak drain current	note 2	–	12.4	A
P_{tot}	total power dissipation	T_s = 80 °C; note 3	–	1.3	W
		T_s = 80 °C; note 4	–	1.13	W
		T_s = 80 °C; note 5	–	0.92	W
		T_s = 80 °C; note 6	–	0.77	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	1.3	A
I_{SM}	peak source current	note 2	–	5.2	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. When only one FET dissipates.
4. When either combination of FETs 1-5, 1-6, 2-5, 2-7, 3-6 or 3-7 dissipate an equal amount of power.
5. When FET four plus either combination of FETs 1-5, 1-6, 2-5, 2-7, 3-6 or 3-7 dissipate an equal amount of power.
6. When all seven FETs dissipate an equal amount of power.

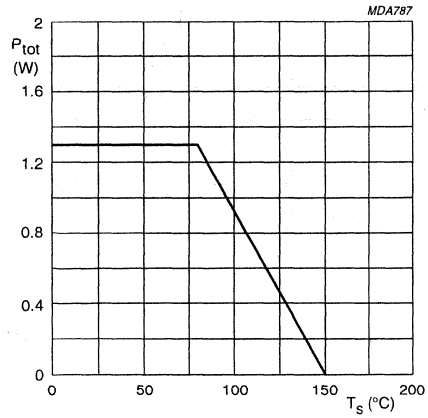
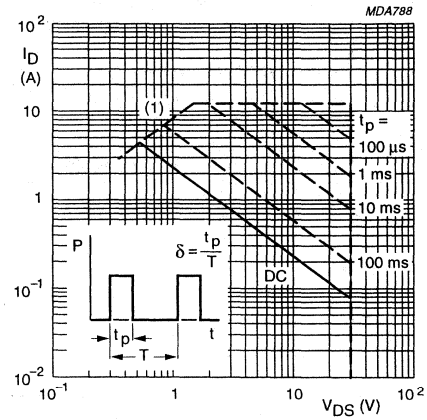


Fig.2 Power derating curve.



δ = 0.01; T_s = 80 °C.
(1) R_{DSon} limitation.

Fig.3 SOAR.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
Per FET				
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	note 1	53	K/W
		note 2	62	K/W
		note 3	76	K/W
		note 4	91	K/W

Notes

1. When only one FET dissipates.
2. When either combination of FETs 1-5, 1-6, 2-5, 2-7, 3-6 or 3-7 dissipate an equal amount of power.
3. When FET four plus either combination of FETs 1-5, 1-6, 2-5, 2-7, 3-6 or 3-7 dissipate an equal amount of power.
4. When all seven FETs dissipate an equal amount of power.

7 N-channel 80 mΩ FET array enhancement mode MOS transistors

PHN708

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per FET						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	1	–	2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 24 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 0.75 A	–	–	130	mΩ
		V_{GS} = 10 V; I_D = 1.5 A	–	–	80	mΩ
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	180	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	70	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	36	–	pF
Q_G	total gate charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 1 A	–	5.4	8	nC
Q_{GS}	gate-source charge	V_{DD} = 15 V; I_D = 1 A	–	0.4	–	nC
Q_{GD}	gate-drain charge	V_{DD} = 15 V; I_D = 1 A	–	1.6	–	nC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to 10 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	3	–	ns
t_f	fall time	V_{GS} = 0 to 10 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	2.5	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to 10 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	5.5	10	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = 10 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	10	–	ns
t_r	rise time	V_{GS} = 10 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	6	–	ns
t_{off}	turn-off switching time	V_{GS} = 10 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	16	25	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 1.25 A	–	–	1	V
t_{rr}	reverse recovery time	I_S = 1.25 A; di/dt = –100 A/μs	–	25	–	ns

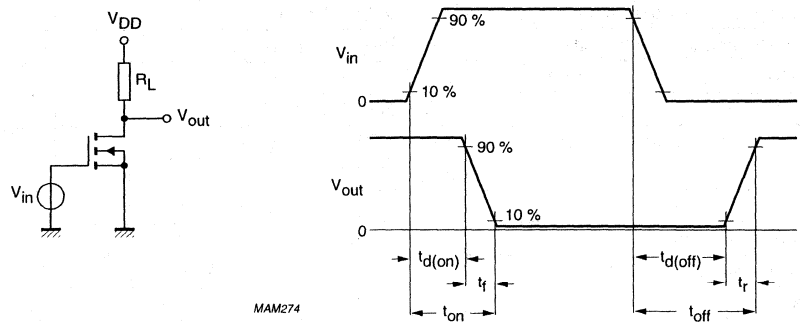


Fig.4 Switching times test circuit with input and output waveforms.

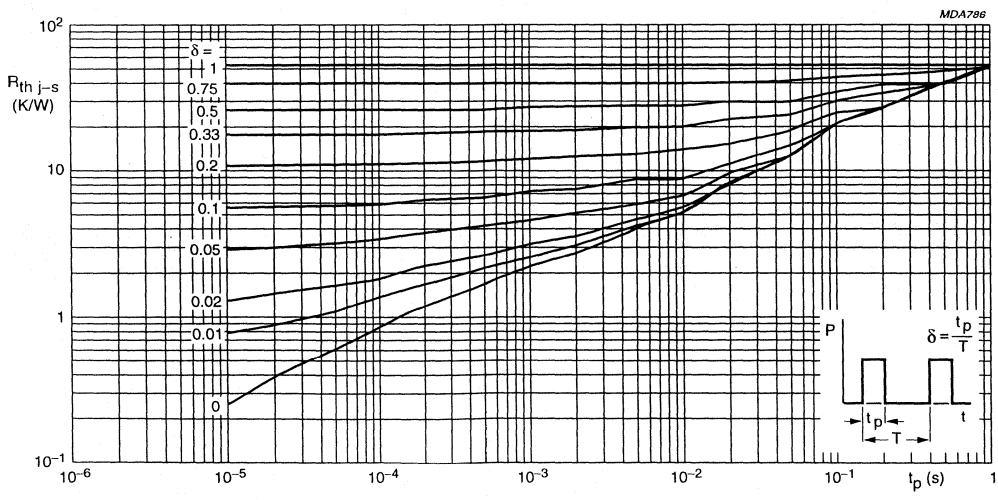
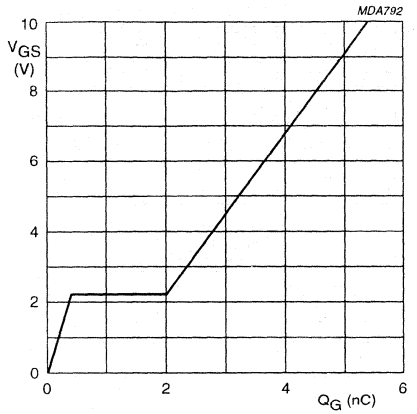


Fig.5 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

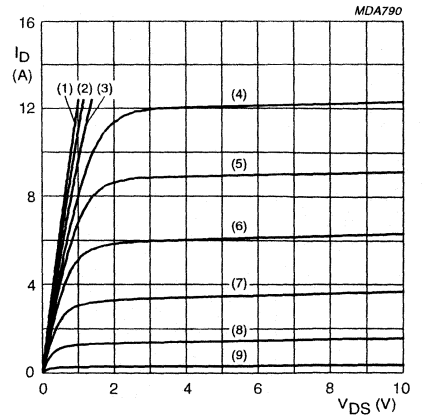
7 N-channel 80 mΩ FET array enhancement mode MOS transistors

PHN708



V_{DD} = 15 V; I_D = 1 A; T_{amb} = 25 °C.

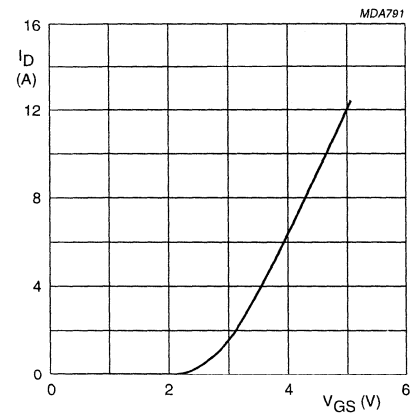
Fig.6 Gate-source voltage as a function of total gate charge; typical values.



T_{amb} = 25 °C; t_p = 80 µs; δ = 0.

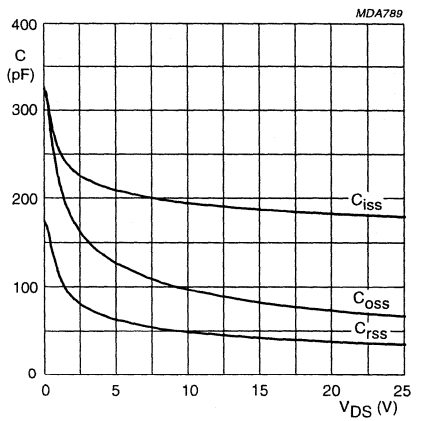
(1) V_{GS} = 10 V.
(2) V_{GS} = 7.5 V.
(3) V_{GS} = 6 V.
(4) V_{GS} = 5 V.
(5) V_{GS} = 4.5 V.
(6) V_{GS} = 4 V.
(7) V_{GS} = 3.5 V.
(8) V_{GS} = 3 V.
(9) V_{GS} = 2.5 V.

Fig.7 Output characteristics; typical values.



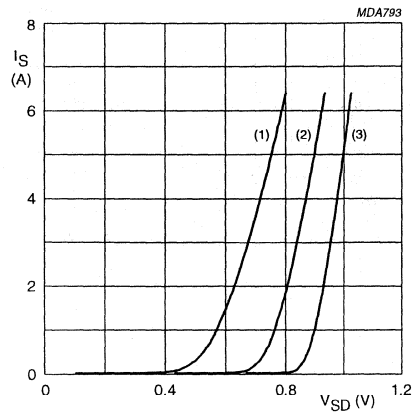
V_{DS} = 10 V; T_{amb} = 25 °C; t_p = 80 µs; δ = 0.

Fig.8 Transfer characteristic; typical values.



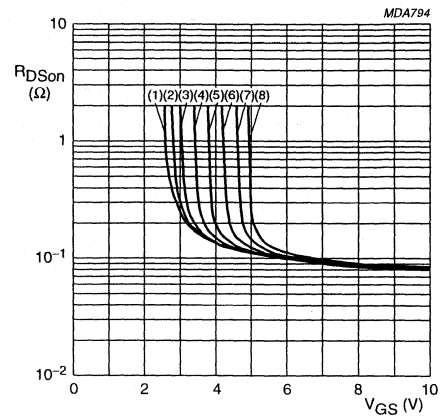
V_{GS} = 0 ; f = 1 MHz; T_j = 25 °C.

Fig.9 Capacitance as a function of drain-source voltage; typical values.



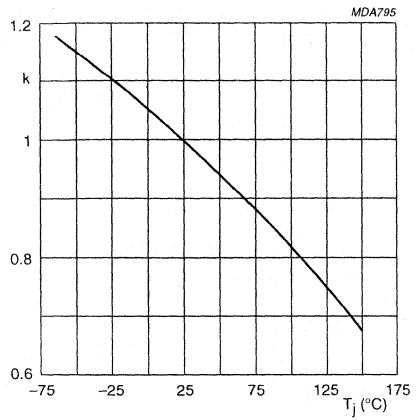
t_p = 300 µs; δ = 0.
(1) T_{amb} = 150 °C.
(2) T_{amb} = 25 °C.
(3) T_{amb} = −65 °C.

Fig.10 Source current as a function of source-drain diode forward voltage; typical values.



T_{amb} = 25 °C; t_p = 300 µs; δ = 0.
(1) I_D = 0.3 A.
(2) I_D = 0.75 A.
(3) I_D = 1.5 A.
(4) I_D = 3.1 A.
(5) I_D = 5 A.
(6) I_D = 7.5 A.
(7) I_D = 10 A.
(8) I_D = 12.4 A.

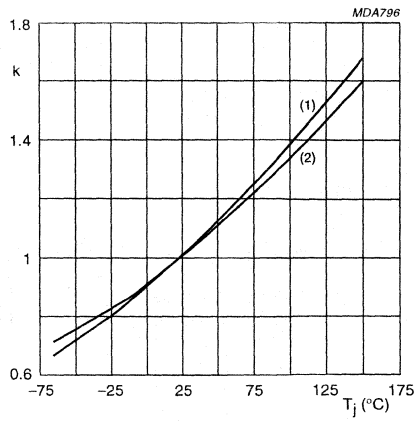
Fig.11 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

V_{GSth} at $V_{DS} = V_{GS}$; I_D = 1 mA.

Fig.12 Temperature coefficient of gate-source threshold voltage as a function of junction temperature; typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

R_{DSon} at:
(1) V_{GS} = 10 V; I_D = 1.5 A.
(2) V_{GS} = 4.5 V; I_D = 0.75 A.

Fig.13 Temperature coefficient of drain-source on-resistance as a function of junction temperature; typical values.

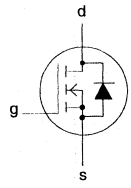
TrenchMOS™ transistor Logic level FET

PHN1011

FEATURES

- 'Trench' technology
- Low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low-profile surface mount package
- Logic level gate drive

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 25 V

I_D = 11 A

$R_{DS(ON)} \leq$ 11 mΩ

GENERAL DESCRIPTION

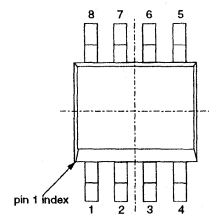
N-channel, enhancement mode, logic level, field-effect power transistor, using **'trench'** technology to achieve very low on-resistance in a low-profile, surface mount package. This device is intended for use in computer motherboard d.c. to d.c. converters and general purpose switching applications.

The PHN1011 is supplied in the SOT96 (SO8) 8-leaded, low profile, surface mounting package.

PINNING

PIN	DESCRIPTION
1-3	source
4	gate
5-8	drain

SOT96 (SO8)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	25	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	25	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
I_D	Drain current (DC)	T_a = 25 °C, $t_p \leq$ 10 s	-	11	A
		T_a = 70 °C, $t_p \leq$ 10 s	-	9	A
I_{DM}	Drain current (pulse peak value)	T_a = 25 °C	-	44	A
P_{tot}	Total power dissipation	T_a = 25 °C	-	2.5	W
		T_a = 70 °C	-	1.6	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	FR4 board, minimum footprint, $t_p \leq$ 10 s.	-	50	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 250 µA;	25	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 250 µA	1	1.5	2	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 25 V; V_{GS} = 0 V;	-	0.05	1	µA
		T_j = 55˚C	-	-	25	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 10 A	-	9	11	mΩ
		V_{GS} = 5 V; I_D = 5 A	-	-	13.5	mΩ

DYNAMIC CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 10 A	-	32	-	S
$Q_{g(tot)}$	Total gate charge	I_D = 10 A; V_{DD} = 25 V; V_{GS} = 5 V	-	40	-	nC
Q_{gs}	Gate-source charge		-	6.6	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	19	-	nC
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	2000	2300	pF
C_{oss}	Output capacitance		-	460	530	pF
C_{rss}	Feedback capacitance		-	200	230	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 25 V; I_D = 10 A;	-	15	-	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 10 Ω	-	67	-	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	140	-	ns
t_f	Turn-off fall time		-	90	-	ns

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_a = 25 ˚C, $t_p \leq$ 10 s	-	-	11	A
I_{DRM}	Pulsed reverse drain current		-	-	44	A
V_{SD}	Diode forward voltage	I_F = 10 A; V_{GS} = 0 V	-	0.8	1.2	V
		I_F = 40 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 10 A; -dI_F/dt = 100 A/µs;	-	50	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_{DS} = 25 V	-	0.1	-	µC

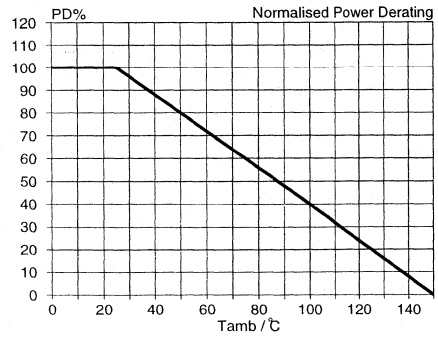


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ ^\circ C}$ = f(T_a)

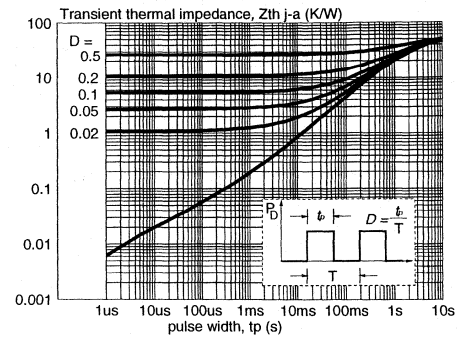


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}a}$ = f(t); parameter D = t_p/T

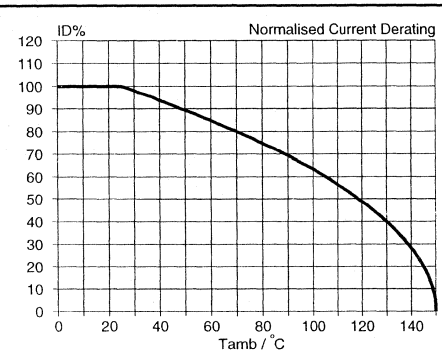


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ ^\circ C}$ = f(T_a); conditions: $V_{GS} \geq$ 10 V

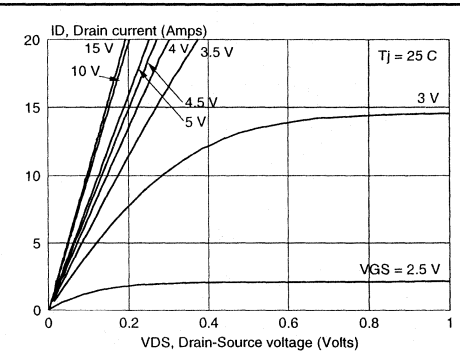


Fig.5. Typical output characteristics, T_j = 25 ˚C.
I_D = f(V_{DS}); parameter V_{GS}

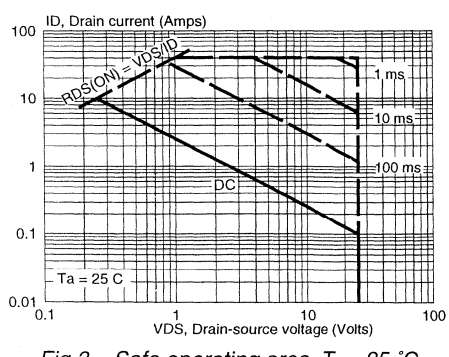


Fig.3. Safe operating area. T_a = 25 ˚C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

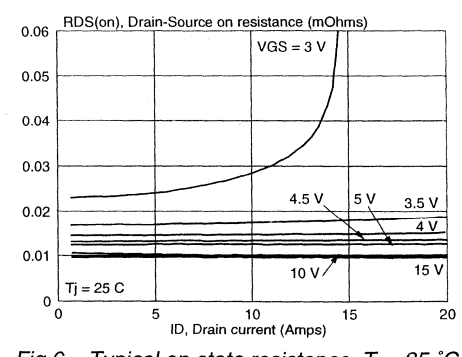


Fig.6. Typical on-state resistance, T_j = 25 ˚C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

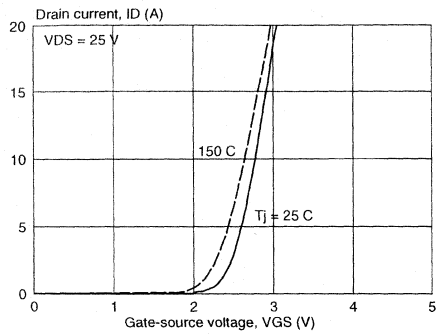


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

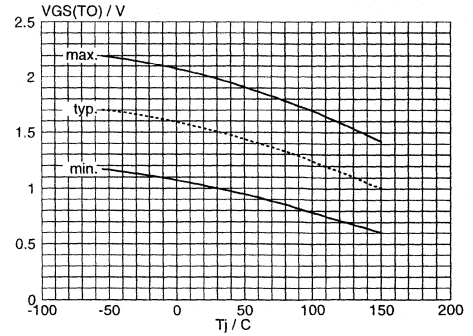


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

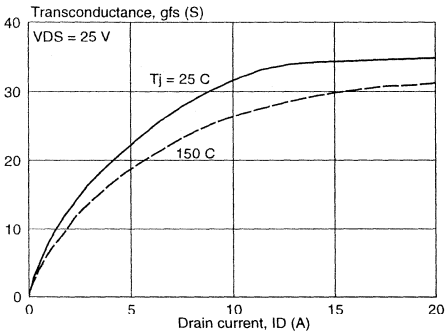


Fig.8. Typical transconductance, T_j = 25 ˚C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

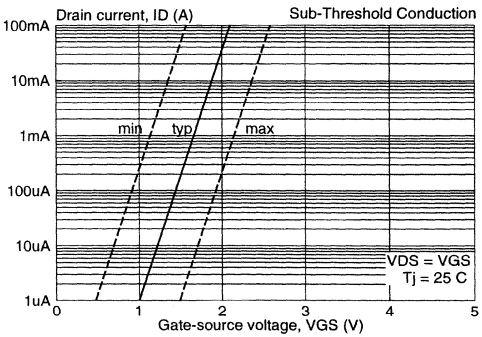


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

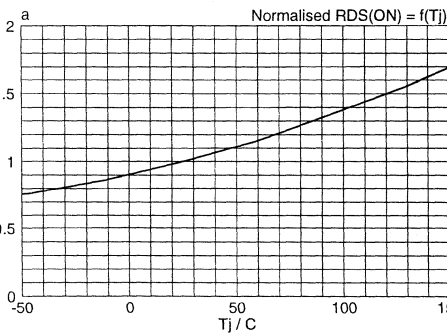


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ ^\circ C} = f(T_j)$; I_D = 10 A; V_{GS} = 10 V

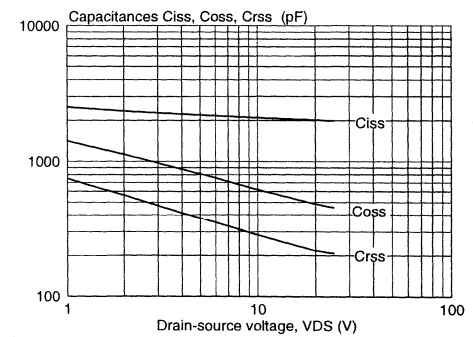


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

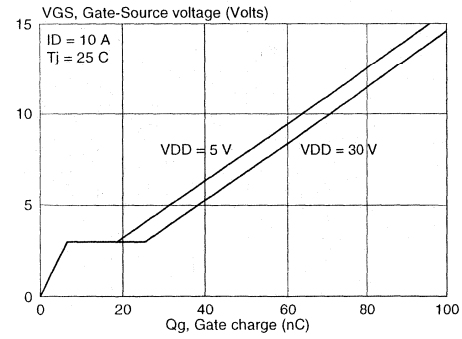


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 10$ A; parameter V_{DS}

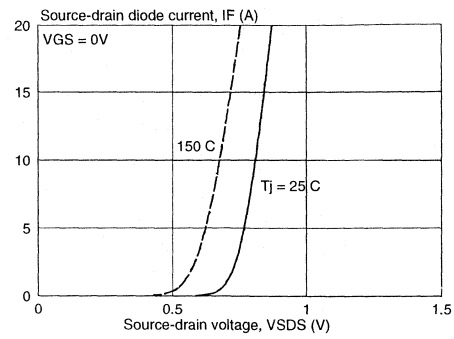


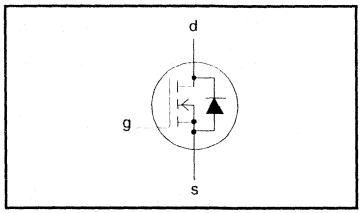
Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

TrenchMOS™ transistor — PHN1013

FEATURES

- 'Trench' technology
- Low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low-profile surface mount package

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 30 V

I_D = 10 A

$R_{DS(ON)} \leq$ 13.5 mΩ

GENERAL DESCRIPTION

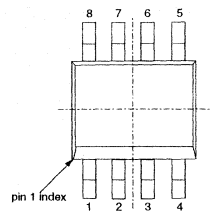
N-channel, enhancement mode field-effect power transistor, using '**trench**' technology to achieve very low on-resistance in a low-profile, surface mount package. This device is intended for use in computer motherboard d.c. to d.c. converters and general purpose switching applications.

The PHN1013 is supplied in the SOT96 (SO8) 8-leaded, low profile, surface mounting package.

PINNING

PIN	DESCRIPTION
1-3	source
4	gate
5-8	drain

SOT96 (SO8)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	30	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	30	V
$\pm V_{GS}$	Gate-source voltage	-	-	20	V
I_D	Drain current (DC)	T_a = 25 °C, $t_p \leq$ 10 s	-	10	A
		T_a = 70 °C, $t_p \leq$ 10 s	-	8	A
I_{DM}	Drain current (pulse peak value)	T_a = 25 °C	-	40	A
P_{tot}	Total power dissipation	T_a = 25 °C	-	2.5	W
		T_a = 70 °C	-	1.6	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	FR4 board, minimum footprint, $t_p \leq$ 10 s.	-	50	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 250 µA;	30	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 250 µA	1	2.1	-	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 30 V; V_{GS} = 0 V;	-	0.05	1	µA
		T_j = 55˚C	-	-	25	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 10 A	-	11	13.5	mΩ
		V_{GS} = 5 V; I_D = 5 A	-	-	20	mΩ

DYNAMIC CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 10 A	-	18	-	S
$Q_{g(tot)}$	Total gate charge	I_D = 10 A; V_{DD} = 30 V; V_{GS} = 10 V	-	49	-	nC
Q_{gs}	Gate-source charge		-	6.6	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	19	-	nC
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1400	1700	pF
C_{oss}	Output capacitance		-	514	620	pF
C_{rss}	Feedback capacitance		-	218	260	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 10 A;	-	15	-	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 10 Ω	-	67	-	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	77	-	ns
t_f	Turn-off fall time		-	71	-	ns

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_a = 25 ˚C, $t_p \leq$ 10 s	-	-	10	A
I_{DRM}	Pulsed reverse drain current		-	-	40	A
V_{SD}	Diode forward voltage	I_F = 10 A; V_{GS} = 0 V	-	0.8	1.2	V
		I_F = 40 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 10 A; -dI_F/dt = 100 A/µs;	-	50	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.1	-	µC

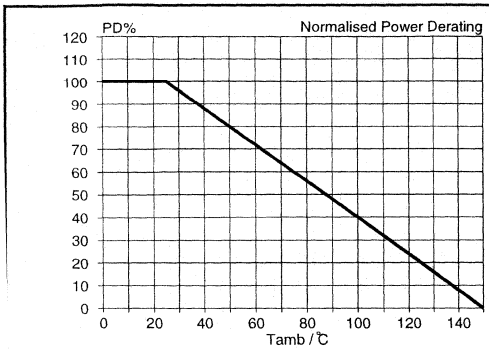


Fig.1. Normalised power dissipation.
PD% = 100·$P_D/P_{D\ 25\ °C}$ = f(T_a)

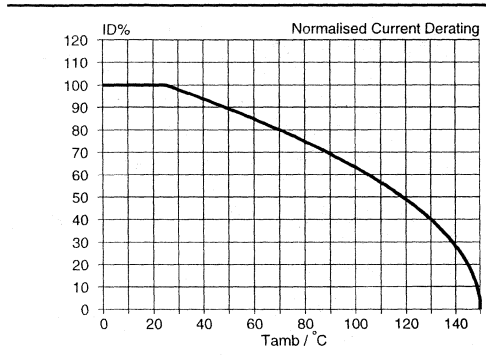


Fig.2. Normalised continuous drain current.
ID% = 100·$I_D/I_{D\ 25\ °C}$ = f(T_a); conditions: $V_{GS} \geq 10$ V

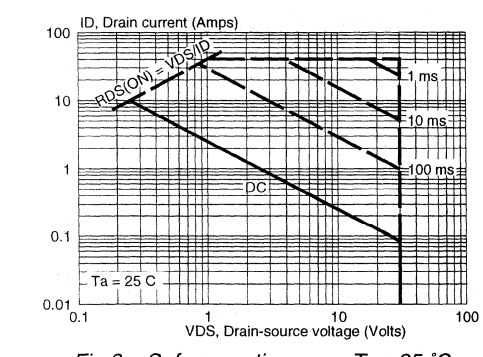


Fig.3. Safe operating area. T_a = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

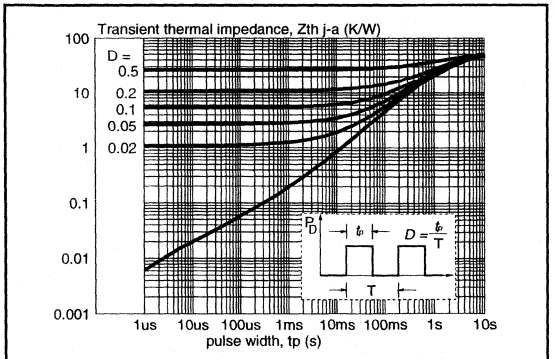


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}a}$ = f(t); parameter D = t_p/T

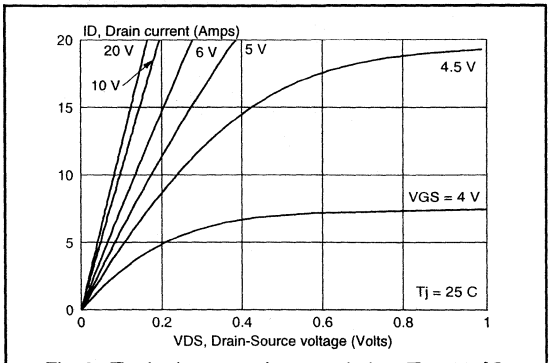


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

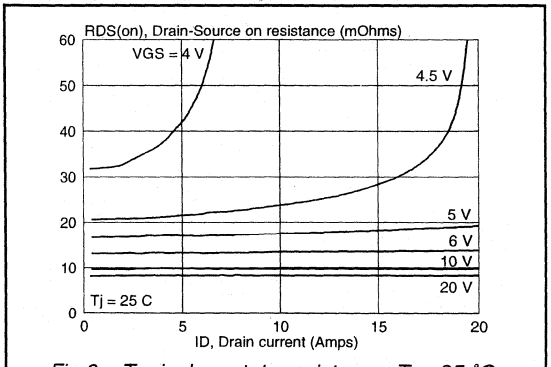


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

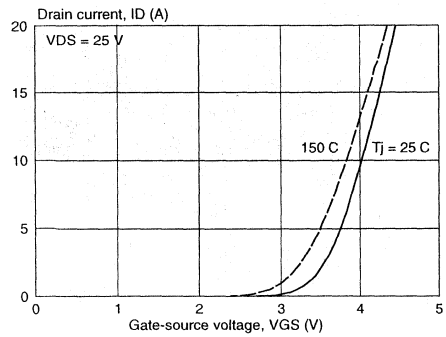


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

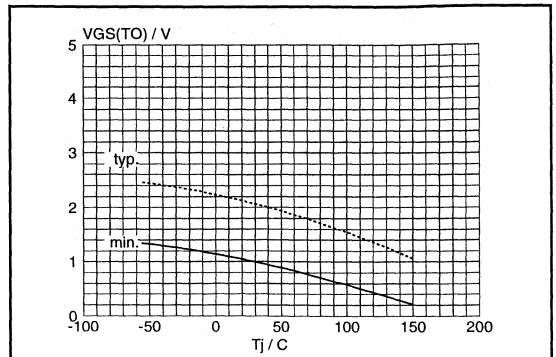


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

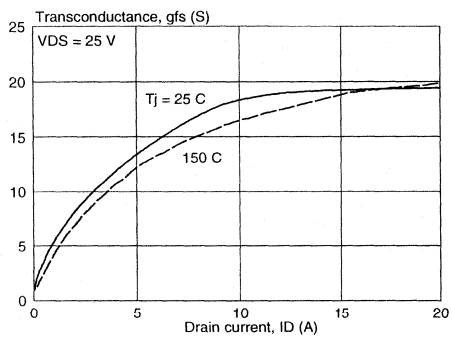


Fig.8. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

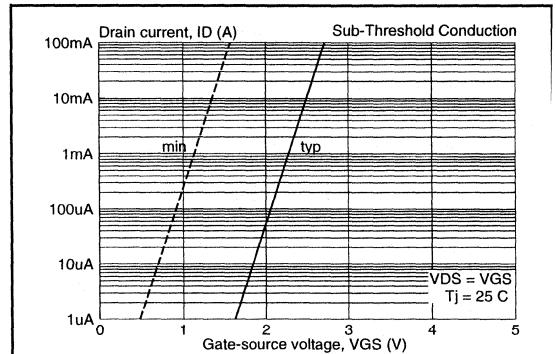


Fig.11. Sub-threshold drain current. $I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

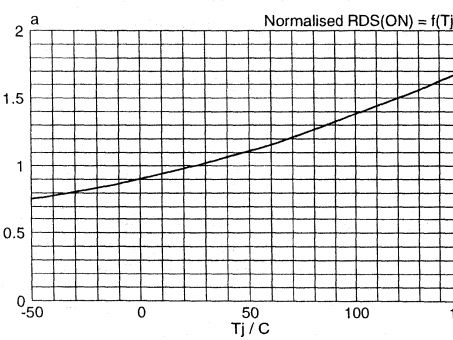


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\ °C} = f(T_j)$; I_D = 10 A; V_{GS} = 10 V

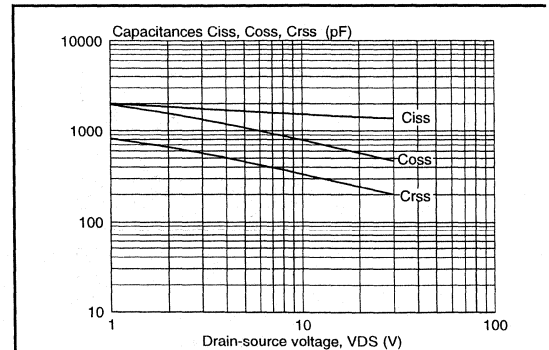


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

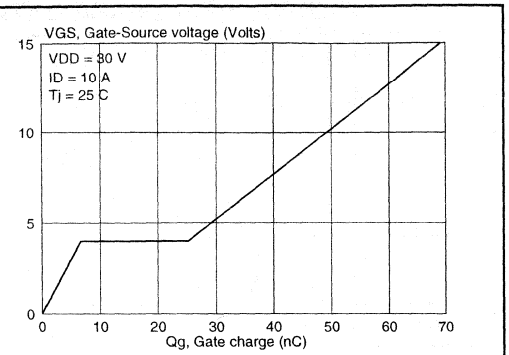


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 10$ A; parameter V_{DS}

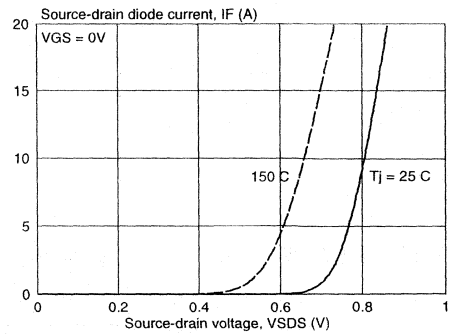


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

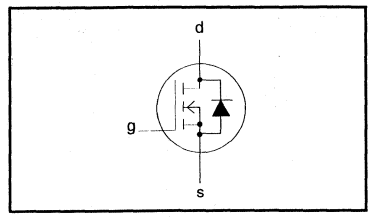
TrenchMOS™ transistor Logic level FET

PHN1015

FEATURES

- 'Trench' technology
- Low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low-profile surface mount package

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 25 V

I_D = 9 A

$R_{DS(ON)} \leq 18\ m\Omega$

$R_{DS(ON)} \leq 14\ m\Omega$

GENERAL DESCRIPTION

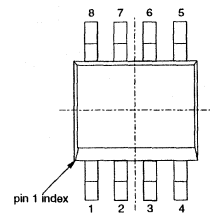
N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using **'trench'** technology. The combination of very low on-state resistance and low switching losses make this device the optimum choice in high speed computer motherboard d.c. to d.c. converters.

The PHN1015 is supplied in the SOT96 (SO8) 8-leaded, low profile, surface mounting package.

PINNING

PIN	DESCRIPTION
1-3	source
4	gate
5-8	drain

SOT96 (SO8)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	25	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	25	V
V_{GS}	Gate-source voltage	-	-	± 15	V
V_{GSM}	Pulsed gate-source voltage	$T_j \leq 150°C$	-	± 20	V
I_D	Drain current (DC)	T_a = 25 °C, $t_p \leq 10$ s	-	9	A
		T_a = 100 °C, $t_p \leq 10$ s	-	5.7	A
I_{DM}	Drain current (pulse peak value)	T_a = 25 °C	-	36	A
P_{tot}	Total power dissipation	T_a = 25 °C	-	2.5	W
		T_a = 70 °C	-	1.6	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	FR4 board, minimum footprint, $t_p \leq 10$ s.	-	50	K/W

ELECTRICAL CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	25	-	-	V
		T_j = -55˚C	22	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	1.5	2	V
		T_j = 150˚C	0.6	-	-	V
		T_j = -55˚C	-	-	2.3	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 10 A	-	9	14	mΩ
		V_{GS} = 5 V; I_D = 10 A	-	13	18	mΩ
		V_{GS} = 5 V; I_D = 10 A; T_j = 150˚C	-	-	31	mΩ
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 10 A	8	20	-	S
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	10	100	nA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 25 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 150˚C	-	-	500	µA
$Q_{g(tot)}$	Total gate charge	I_D = 20 A; V_{DD} = 24 V; V_{GS} = 10 V	-	52	-	nC
Q_{gs}	Gate-source charge		-	5.6	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	14	-	nC
$t_{d\,on}$	Turn-on delay time	V_{DD} = 15 V; I_D = 25 A;	-	8.4	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 5 Ω	-	63	100	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	60	100	ns
t_f	Turn-off fall time		-	66	100	ns
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1300	-	pF
C_{oss}	Output capacitance		-	430	-	pF
C_{rss}	Feedback capacitance		-	228	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_a = 25 ˚C, $t_p \leq$ 10 s	-	-	9.2	A
I_{DRM}	Pulsed reverse drain current		-	-	37	A
V_{SD}	Diode forward voltage	I_F = 10 A; V_{GS} = 0 V	-	0.8	1.2	V
t_{rr}	Reverse recovery time	I_F = 10 A; -dI_F/dt = 100 A/µs;	-	70	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 25 V	-	0.1	-	µC

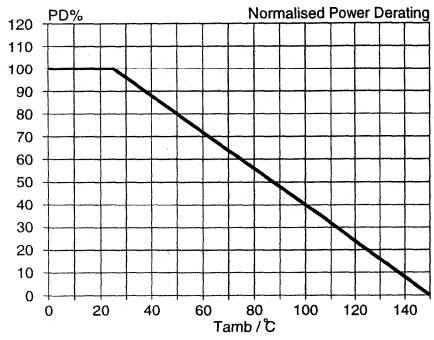


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ ^\circ C}$ = f(T_a)

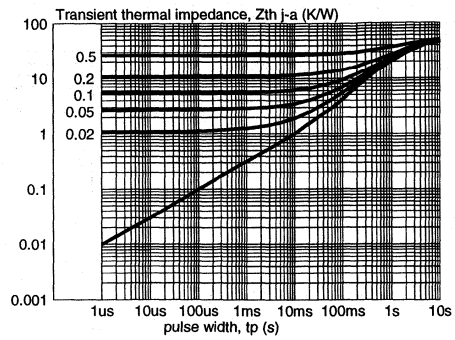


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}a}$ = f(t); parameter D = t_p/T

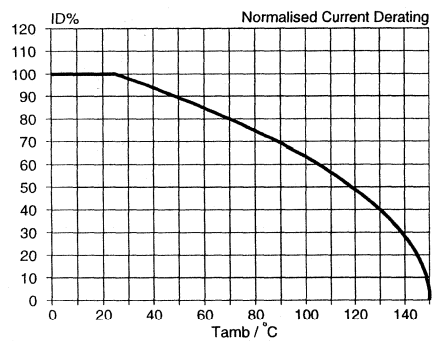


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ ^\circ C}$ = f(T_a); conditions: $V_{GS} \geq 5$ V

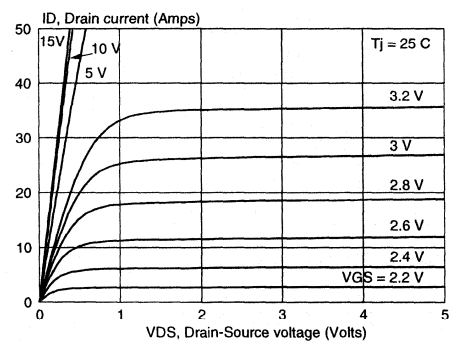


Fig.5. Typical output characteristics, T_j = 25 ˚C.
I_D = f(V_{DS}); parameter V_{GS}

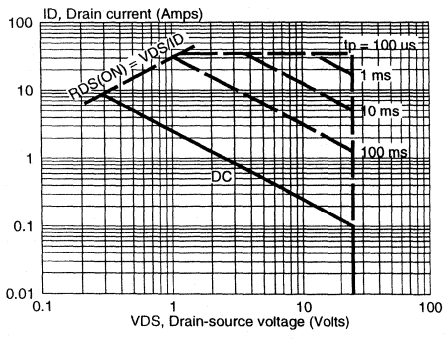


Fig.3. Safe operating area. T_a = 25 ˚C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

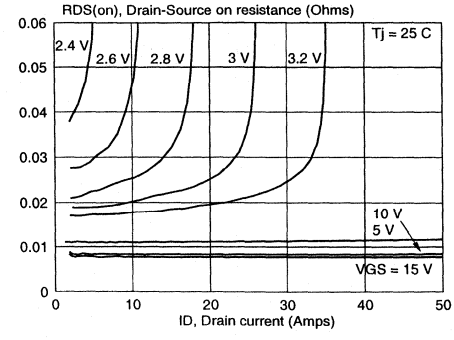


Fig.6. Typical on-state resistance, T_j = 25 ˚C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

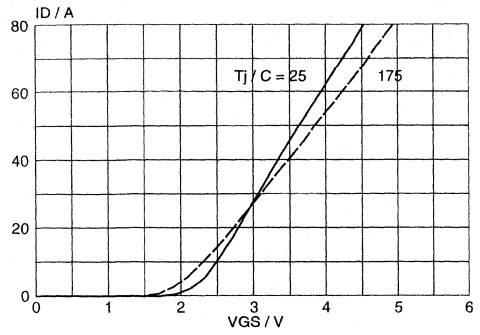


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$

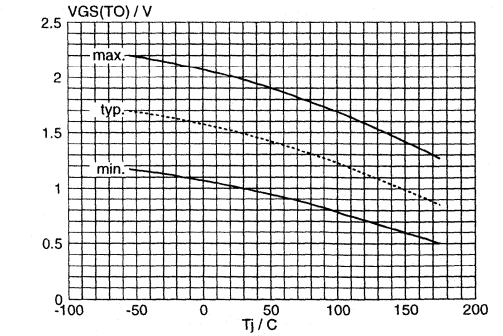


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

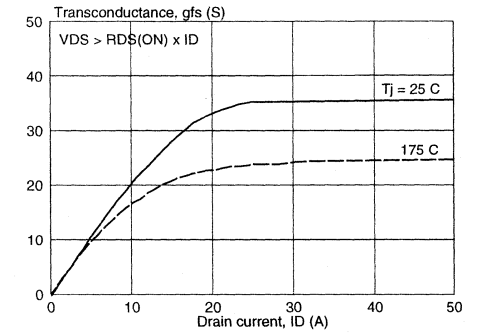


Fig.8. Typical transconductance, T_j = 25 ˚C.
$g_{fs} = f(I_D)$

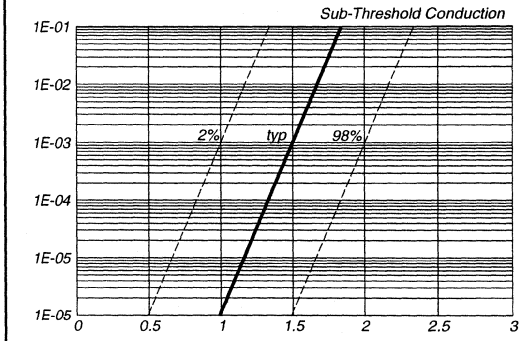


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

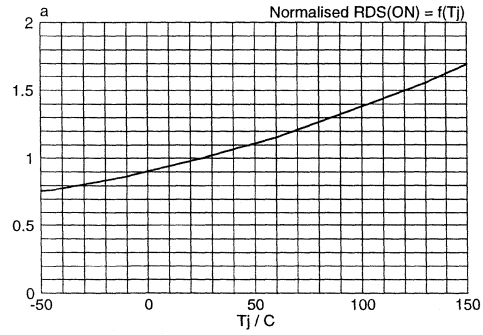


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ ^{\circ}C} = f(T_j)$

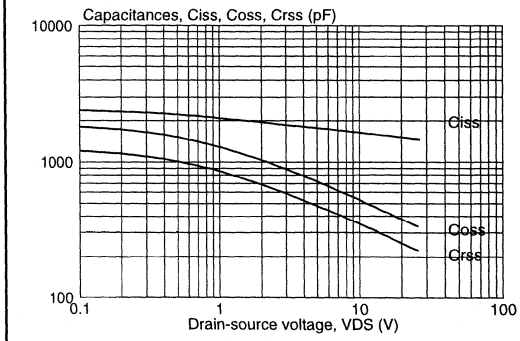


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

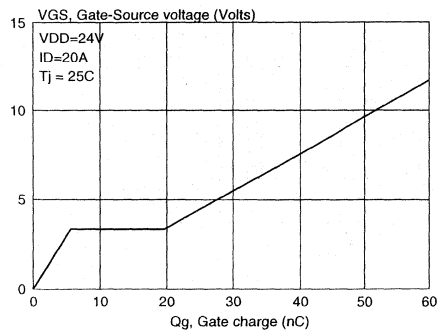


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$

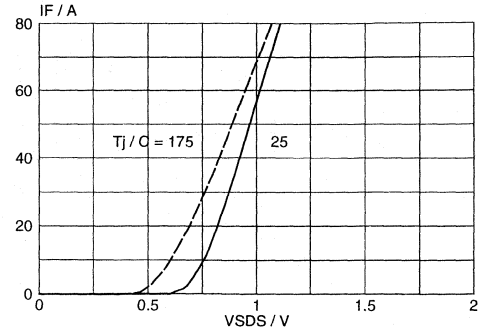


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

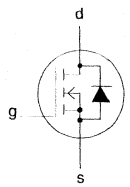
TrenchMOS™ transistor
Logic level FET

PHN1018

FEATURES

- 'Trench' technology
- Low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low-profile surface mount package

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 25 V

I_D = 8.7 A

$R_{DS(ON)} \leq 21$ mΩ

$R_{DS(ON)} \leq 16$ mΩ

GENERAL DESCRIPTION

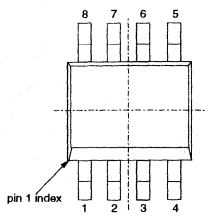
N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using '**trench**' technology. The combination of very low on-state resistance and low switching losses make this device the optimum choice in high speed computer motherboard d.c. to d.c. converters.

The PHN1018 is supplied in the SOT96 (SO8) 8-leaded, low profile, surface mounting package.

PINNING

PIN	DESCRIPTION
1-3	source
4	gate
5-8	drain

SOT96 (SO8)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	25	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	25	V
V_{GS}	Gate-source voltage	-	-	± 15	V
V_{GSM}	Pulsed gate-source voltage	$T_j \leq 150$°C	-	± 20	V
I_D	Drain current (DC)	T_a = 25 °C, $t_p \leq 10$ s	-	8.7	A
		T_a = 100 °C, $t_p \leq 10$ s	-	5.5	A
I_{DM}	Drain current (pulse peak value)	T_a = 25 °C	-	35	A
P_{tot}	Total power dissipation	T_a = 25 °C	-	2.5	W
		T_a = 70 °C	-	1.6	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	FR4 board, minimum footprint, $t_p \leq 10$ s.	-	50	K/W

ELECTRICAL CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	25	-	-	V
		T_j = -55˚C	22	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	1.5	2	V
		T_j = 150˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 10 A	-	13	16	mΩ
		V_{GS} = 5 V; I_D = 5 A	-	18	21	mΩ
		V_{GS} = 5 V; I_D = 5 A; T_j = 150˚C	-	-	36	mΩ
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	8	27	-	S
I_{DSS}	Zero gate voltage drain current	V_{DS} = 25 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 150˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	10	100	nA
$Q_{g(tot)}$	Total gate charge	I_D = 20 A; V_{DD} = 24 V; V_{GS} = 10 V	-	40	-	nC
Q_{gs}	Gate-source charge		-	7	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	10	-	nC
$t_{d\,on}$	Turn-on delay time	V_{DD} = 15 V; I_D = 25 A;	-	10	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 5 Ω	-	50	75	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	50	75	ns
t_f	Turn-off fall time		-	30	45	ns
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1050	-	pF
C_{oss}	Output capacitance		-	270	-	pF
C_{rss}	Feedback capacitance		-	140	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_a = 25 ˚C, $t_p \leq$ 10 s	-	-	8.7	A
I_{DRM}	Pulsed reverse drain current		-	-	35	A
V_{SD}	Diode forward voltage	I_F = 10 A; V_{GS} = 0 V	-	0.8	1.2	V
t_{rr}	Reverse recovery time	I_F = 10 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 25 V	-	0.1	-	µC

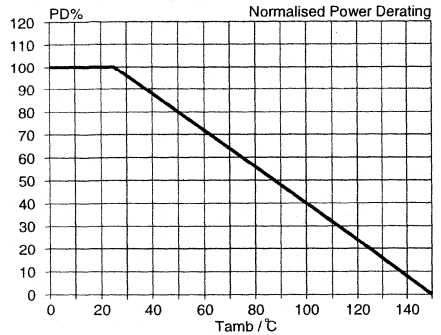


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D / P_{D\ 25\ ^\circ C} = f(T_a)$

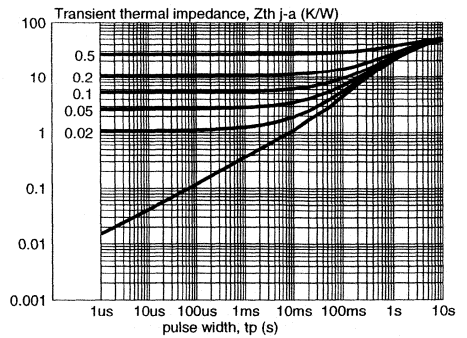


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}a} = f(t)$; parameter $D = t_p/T$

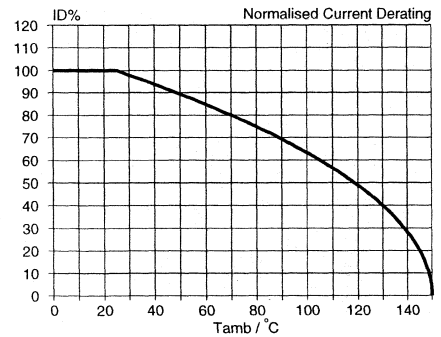


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D / I_{D\ 25\ ^\circ C} = f(T_a)$; conditions: $V_{GS} \geq 5$ V

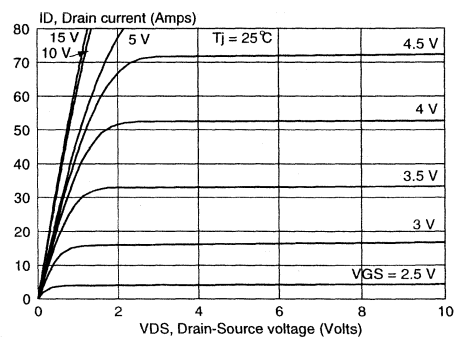


Fig.5. Typical output characteristics, T_j = 25 ˚C.
$I_D = f(V_{DS})$; parameter V_{GS}

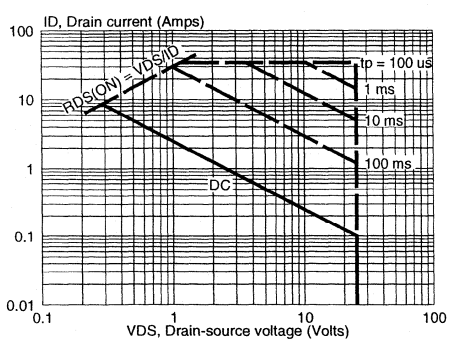


Fig.3. Safe operating area. T_a = 25 ˚C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

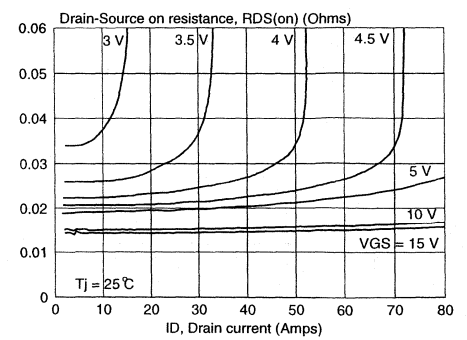


Fig.6. Typical on-state resistance, T_j = 25 ˚C.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

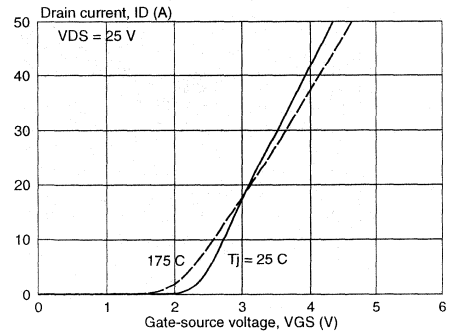


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$

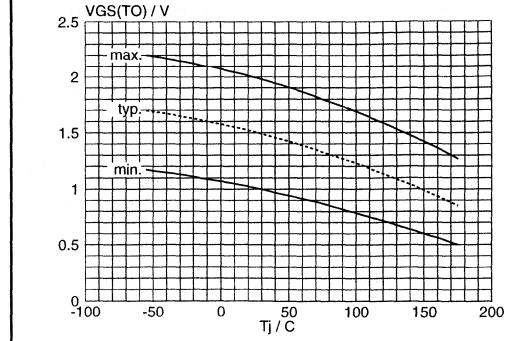


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

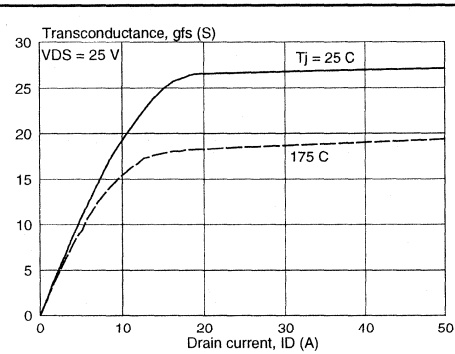


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$

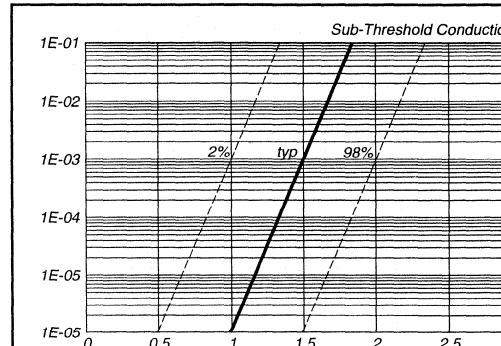


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

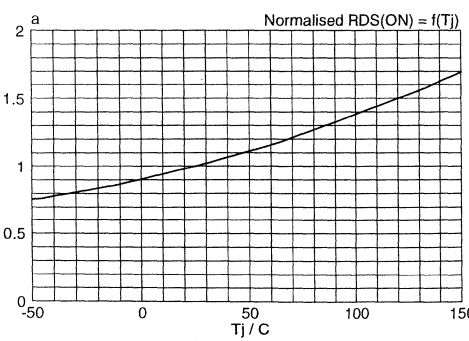


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$

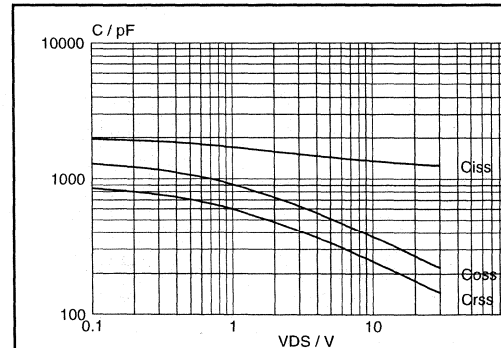


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; V_{GS} = 0 V; f = 1 MHz

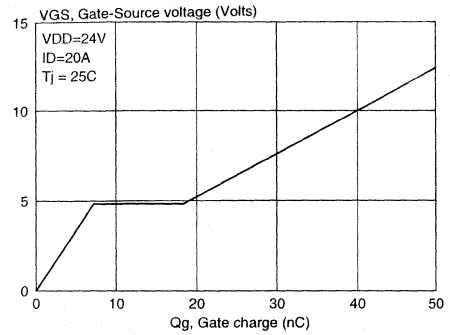


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$

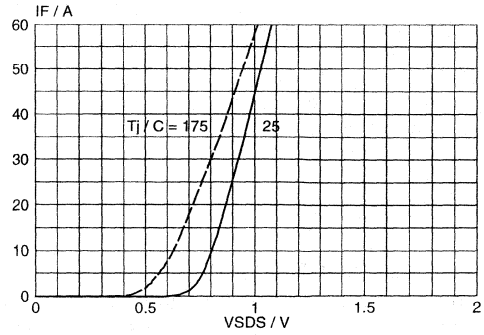


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

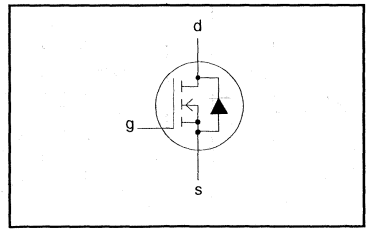
PowerMOS transistors Avalanche energy rated

PHP2N50E, PHB2N50E, PHD2N50E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 500 V

I_D = 2 A

$R_{DS(ON)} \leq 5\ \Omega$

GENERAL DESCRIPTION

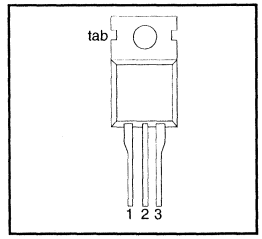
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHP2N50E is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHB2N50E is supplied in the SOT404 surface mounting package.
The PHD2N50E is supplied in the SOT428 surface mounting package.

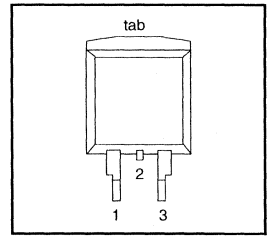
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

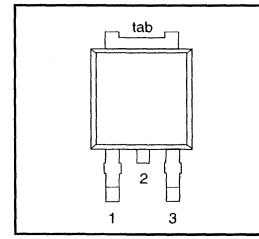
SOT78 (TO220AB)



SOT404



SOT428



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	500	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	500	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	2	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	1.3	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	8	A
P_D	Total dissipation	T_{mb} = 25 °C	-	50	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

1 It is not possible to make connection to pin 2 of the SOT428 or SOT404 packages.

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 2 A; $V_{DD} \leq 50$ V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	130	mJ
E_{AR}	Repetitive avalanche energy[2]		-	3.6	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	2	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	SOT78 package, in free air	-	60	-	K/W
		SOT404 and SOT428 packages, pcb mounted, minimum footprint	-	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	500	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 1 A	-	3.1	5	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 1 A	0.5	1.3	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 500 V; V_{GS} = 0 V	-	1	25	µA
		V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 °C	-	30	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 2 A; V_{DD} = 400 V; V_{GS} = 10 V	-	20	25	nC
Q_{gs}	Gate-source charge		-	2	3	nC
Q_{gd}	Gate-drain (Miller) charge		-	12	15	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 250 V; R_D = 120 Ω;	-	10	-	ns
t_r	Turn-on rise time	R_G = 24 Ω	-	20	-	ns
$t_{d(off)}$	Turn-off delay time		-	60	-	ns
t_f	Turn-off fall time		-	20	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	236	-	pF
C_{oss}	Output capacitance		-	40	-	pF
C_{rss}	Feedback capacitance		-	22	-	pF

[2] pulse width and repetition rate limited by T_j max.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	2	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	8	A
V_{SD}	Diode forward voltage	I_S = 2 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 2 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	300	-	ns
Q_{rr}	Reverse recovery charge		-	2.1	-	µC

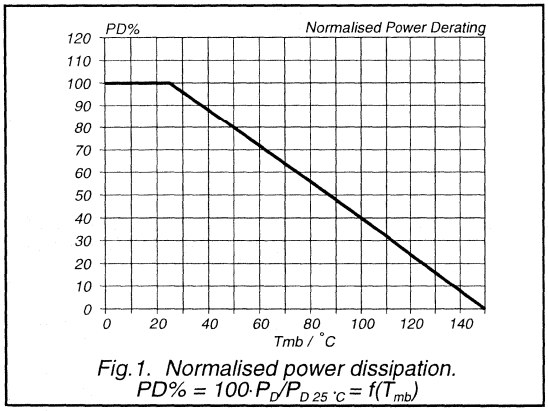


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

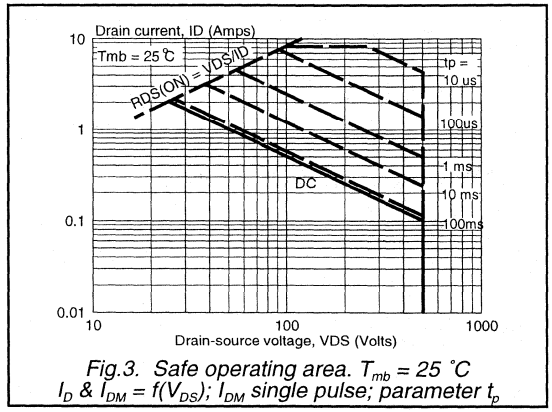


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

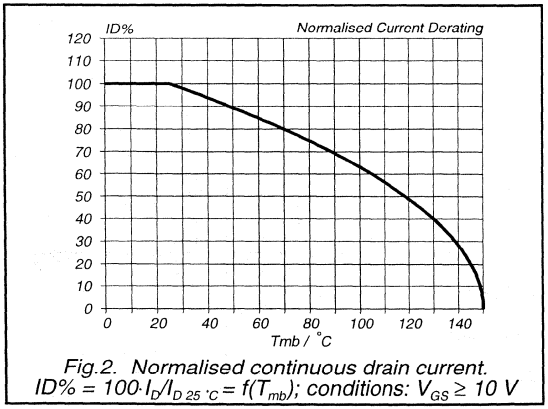


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

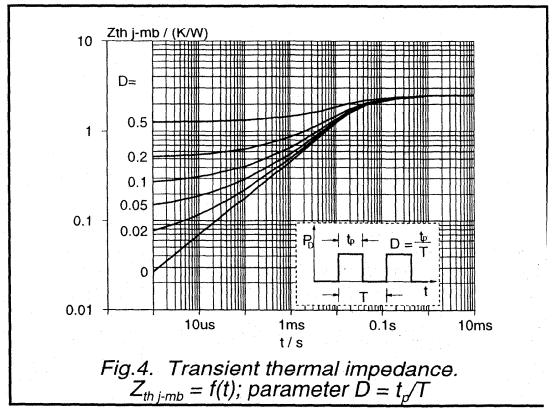


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

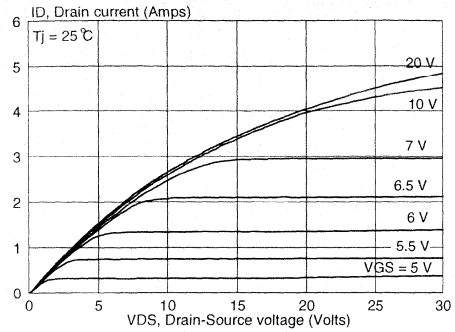


Fig.5. Typical output characteristics. $I_D = f(V_{DS})$; parameter V_{GS}

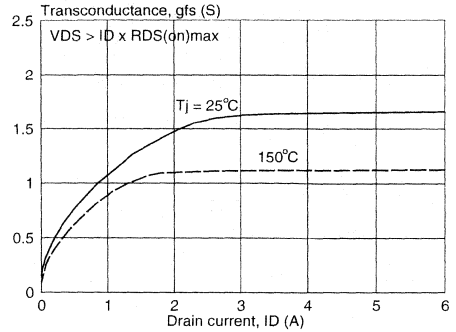


Fig.8. Typical transconductance. $g_{fs} = f(I_D)$; parameter T_j

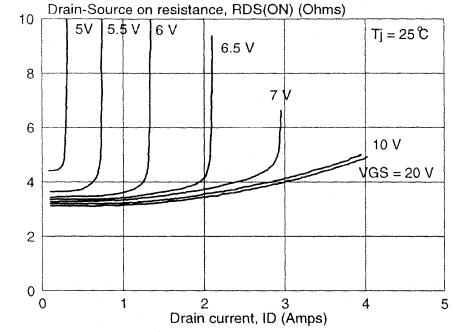


Fig.6. Typical on-state resistance. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

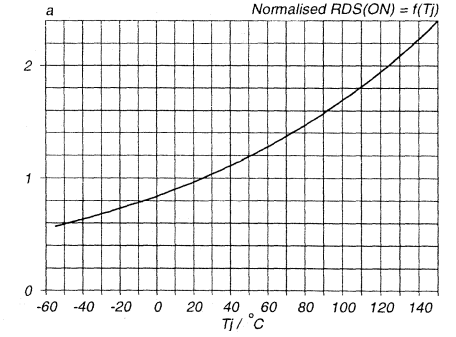


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 1 A; V_{GS} = 10 V

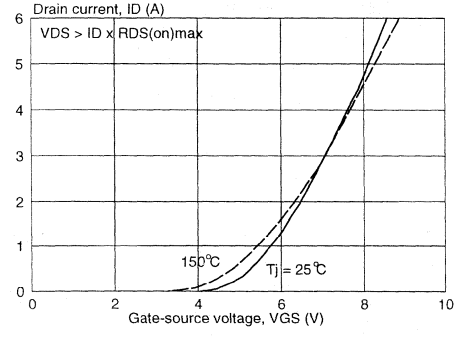


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; parameter T_j

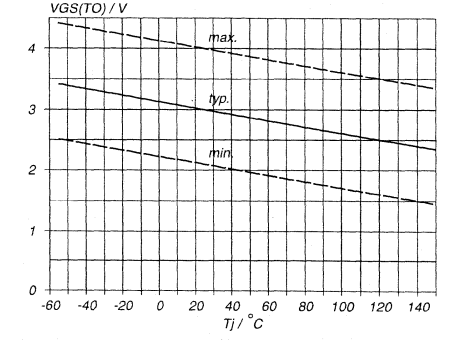


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

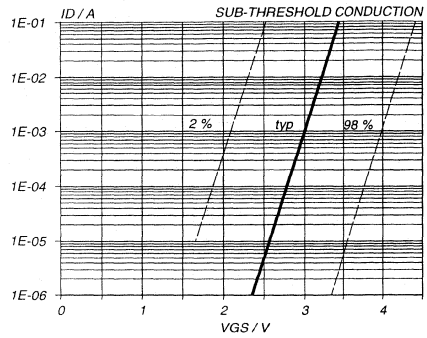


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

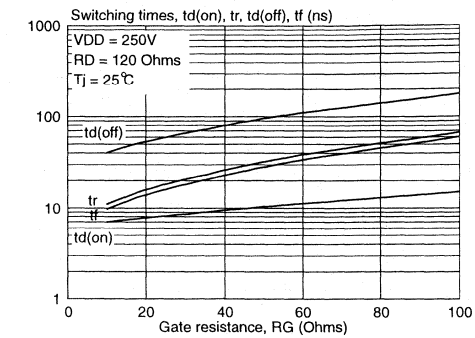


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

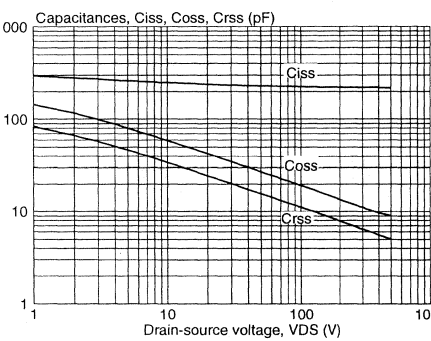


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

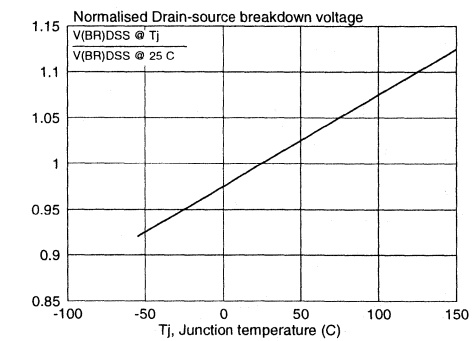


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

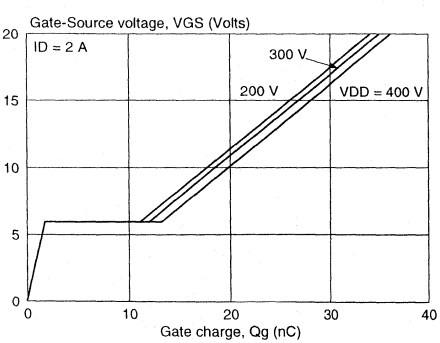


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

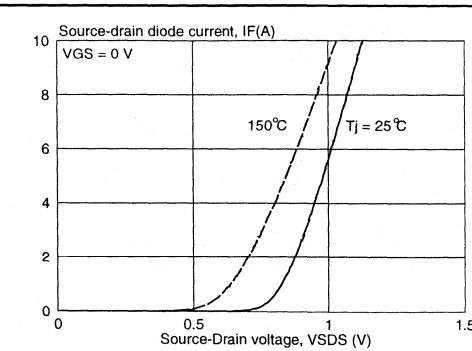


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

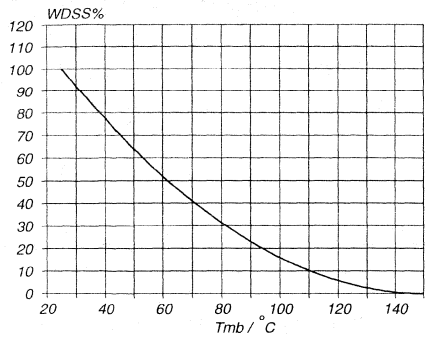


Fig.17. Normalised non-repetitive avalanche energy rating.
$E_{AS}\% = f(T_{mb})$

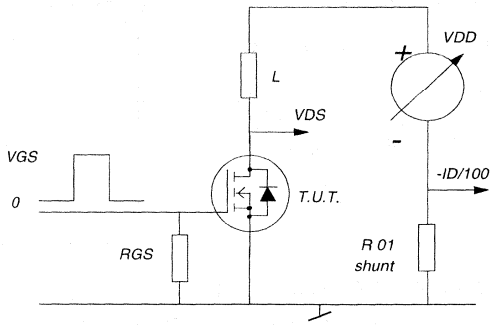


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot \frac{V_{(BR)DSS}}{(V_{(BR)DSS} - V_{DD})}$$

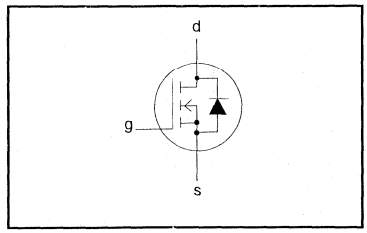
PowerMOS transistors Avalanche energy rated

PHP2N60E, PHB2N60E, PHD2N60E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 600 V

I_D = 1.9 A

$R_{DS(ON)} \leq 6\ \Omega$

GENERAL DESCRIPTION

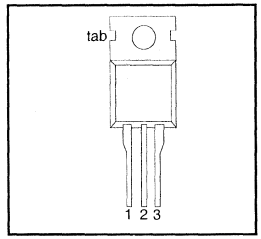
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHP2N60E is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHB2N60E is supplied in the SOT404 surface mounting package.
The PHD2N60E is supplied in the SOT428 surface mounting package.

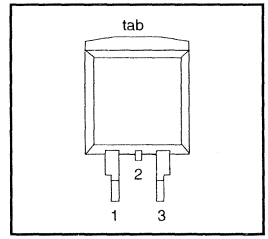
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

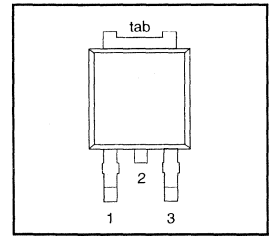
SOT78 (TO220AB)



SOT404



SOT428



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	600	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	600	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	1.9	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	1.2	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	7.6	A
P_D	Total dissipation	T_{mb} = 25 °C	-	50	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

1 It is not possible to make connection to pin 2 of the SOT428 or SOT404 packages.

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 1.9 A; $V_{DD} \leq 50$ V; starting T_j = 25˚C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	144	mJ
E_{AR}	Repetitive avalanche energy[2]		-	3.6	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	1.9	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.5	K/W
$R_{th\ j\text{-}a$	Thermal resistance junction to ambient	SOT78 package, in free air	-	60	-	K/W
		SOT404 and SOT428 packages, pcb mounted, minimum footprint	-	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	600	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 1 A	-	4.6	6	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 1 A	0.5	1.4	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 600 V; V_{GS} = 0 V	-	1	100	µA
		V_{DS} = 480 V; V_{GS} = 0 V; T_j = 125 ˚C	-	50	500	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 2 A; V_{DD} = 480 V; V_{GS} = 10 V	-	20	25	nC
Q_{gs}	Gate-source charge		-	2	3	nC
Q_{gd}	Gate-drain (Miller) charge		-	9	15	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V; R_D = 150 Ω;	-	10	-	ns
t_r	Turn-on rise time	R_G = 24 Ω	-	20	-	ns
$t_{d(off)}$	Turn-off delay time		-	60	-	ns
t_f	Turn-off fall time		-	20	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	236	-	pF
C_{oss}	Output capacitance		-	34	-	pF
C_{rss}	Feedback capacitance		-	20	-	pF

! pulse width and repetition rate limited by T_j max.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	1.9	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	7.6	A
V_{SD}	Diode forward voltage	I_S = 2 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 2 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	360	-	ns
Q_{rr}	Reverse recovery charge		-	2.4	-	µC

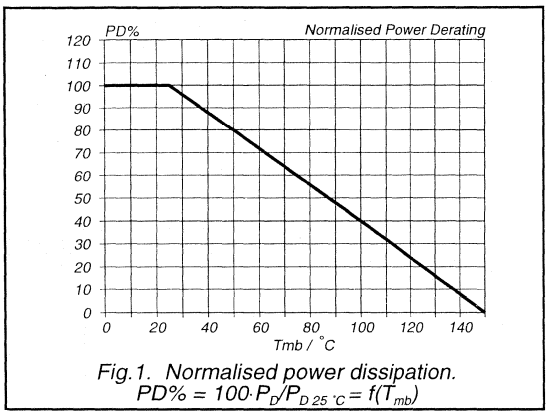


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

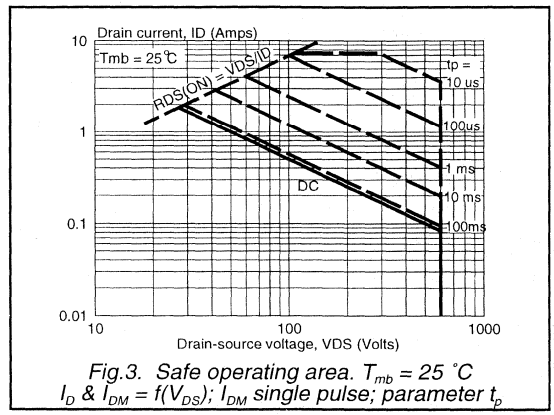


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

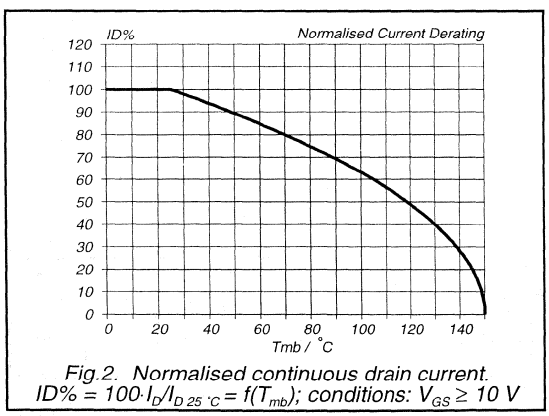


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

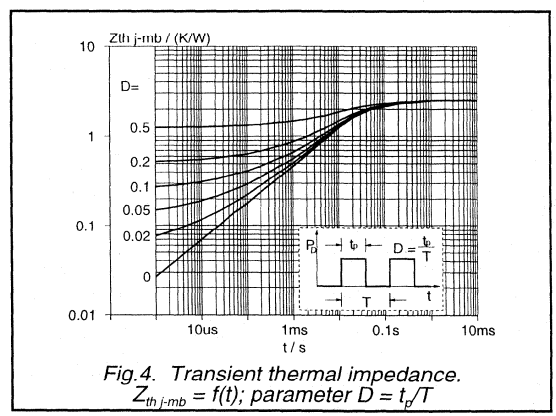


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

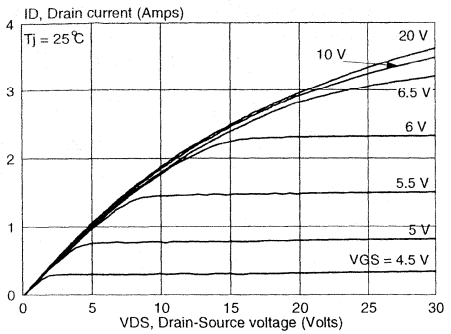


Fig.5. Typical output characteristics.
$I_D = f(V_{DS})$; parameter V_{GS}

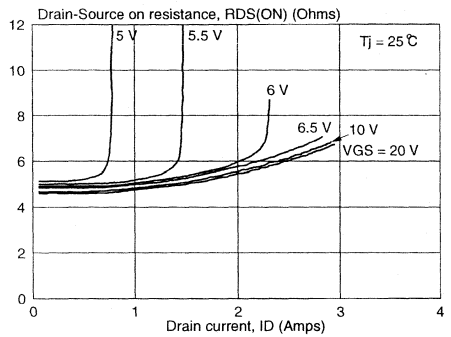


Fig.6. Typical on-state resistance.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

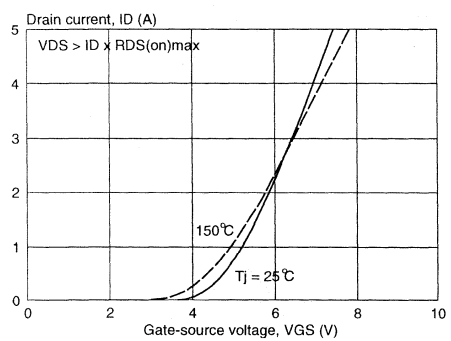


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

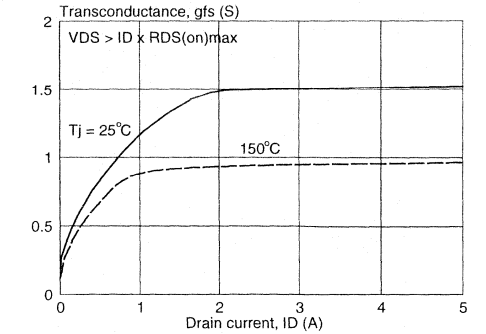


Fig.8. Typical transconductance.
$g_{fs} = f(I_D)$; parameter T_j

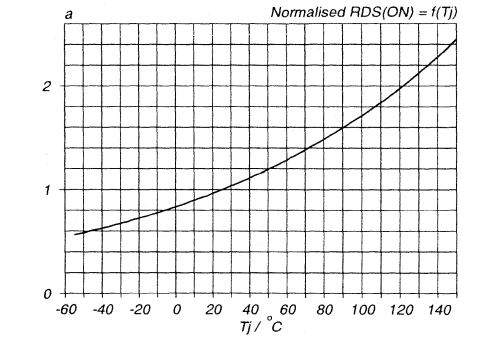


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 1 A; V_{GS} = 10 V

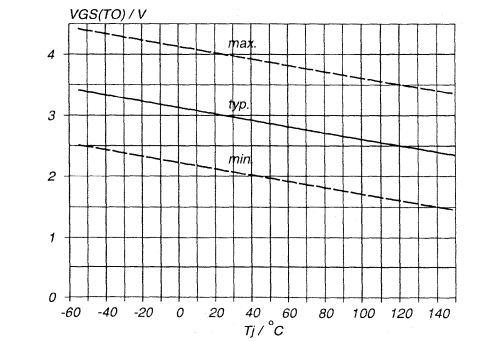


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

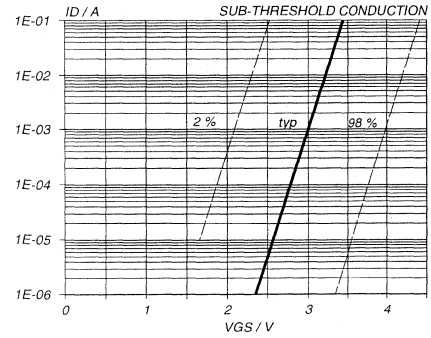


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

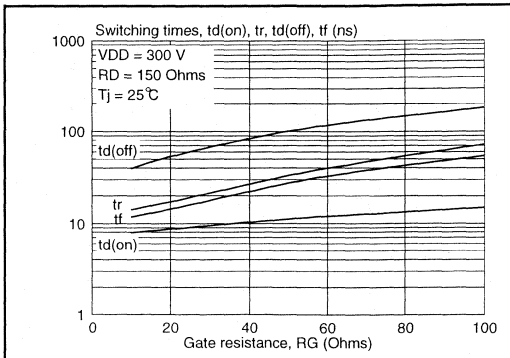


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

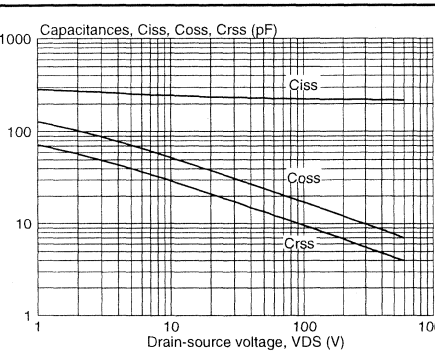


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

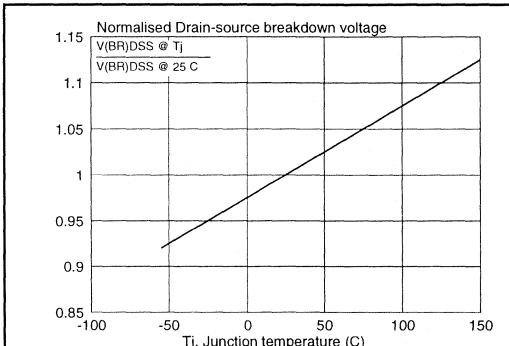


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

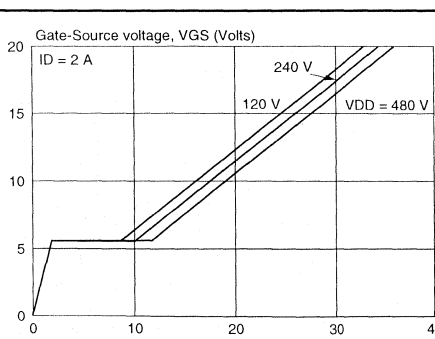


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

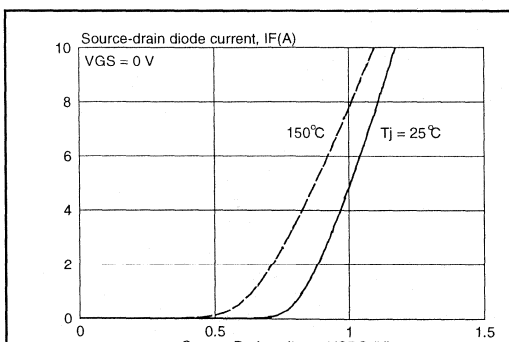


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

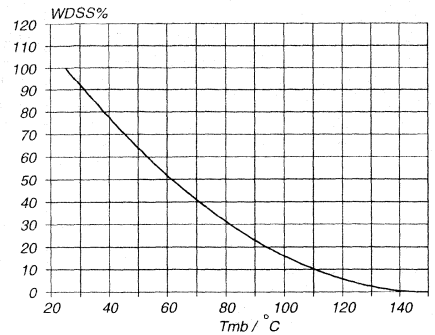


Fig.17. Normalised non-repetitive avalanche energy rating.
$E_{AS}\% = f(T_{mb})$

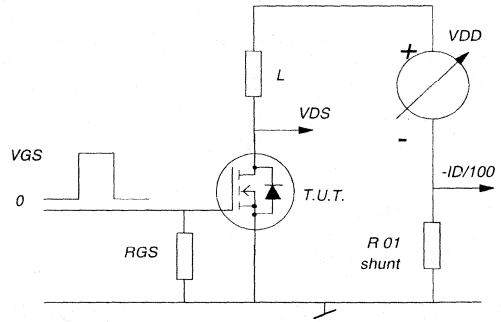


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot \frac{V_{(BR)DSS}}{(V_{(BR)DSS} - V_{DD})}$$

PowerMOS transistor — PHP3N20E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

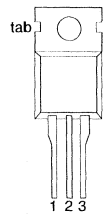
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (DC)	3.5	A
P_{tot}	Total power dissipation	50	W
$R_{DS(ON)}$	Drain-source on-state resistance	1.5	Ω

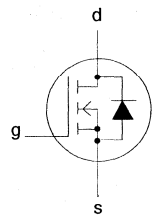
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	3.5	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	2.5	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	14	A
P_D	Total dissipation	T_{mb} = 25 °C	-	50	W
$\Delta P_D/\Delta T_{mb}$	Linear derating factor	T_{mb} > 25 °C	-	0.33	W/K
V_{GS}	Gate-source voltage		-	± 30	V
E_{AS}	Single pulse avalanche energy	$V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	25	mJ
I_{AS}	Peak avalanche current	$V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	3.5	A
T_j, T_{stg}	Operating junction and storage temperature range		- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	3	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.25	-	V/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 2 A	-	0.77	1.5	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 50 V; I_D = 2 A	0.8	3.0	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 200 V; V_{GS} = 0 V	-	0.1	25	µA
		V_{DS} = 160 V; V_{GS} = 0 V; T_j = 150 °C	-	1	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$Q_{g(tot)}$	Total gate charge	I_D = 3.3 A; V_{DD} = 160 V; V_{GS} = 10 V	-	10	12	nC
Q_{gs}	Gate-source charge		-	1.1	2	nC
Q_{gd}	Gate-drain (Miller) charge		-	4.5	6	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 100 V; I_D = 3.3 A;	-	8	-	ns
t_r	Turn-on rise time	R_G = 24 Ω; R_D = 30 Ω	-	20	-	ns
$t_{d(off)}$	Turn-off delay time		-	30	-	ns
t_f	Turn-off fall time		-	25	-	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	200	-	pF
C_{oss}	Output capacitance		-	48	-	pF
C_{rss}	Feedback capacitance		-	20	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	3.5	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	14	A
V_{SD}	Diode forward voltage	I_S = 3.3 A; V_{GS} = 0 V	-	-	1.5	V
t_{rr}	Reverse recovery time	I_S = 3.3 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	90	-	ns
Q_{rr}	Reverse recovery charge		-	0.5	-	µC

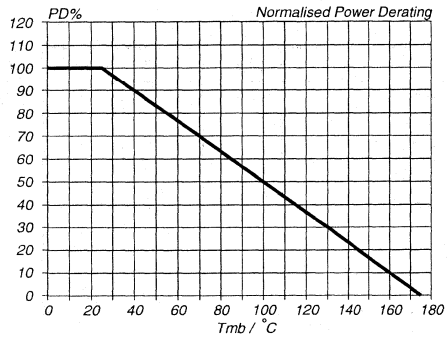


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

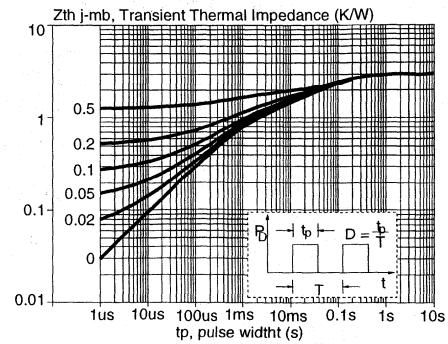


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

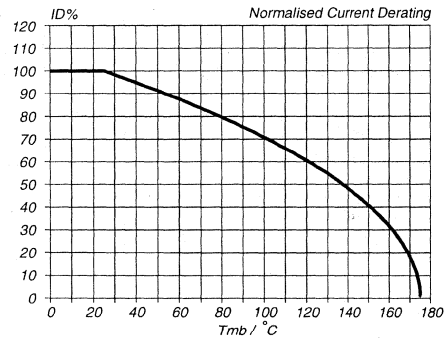


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

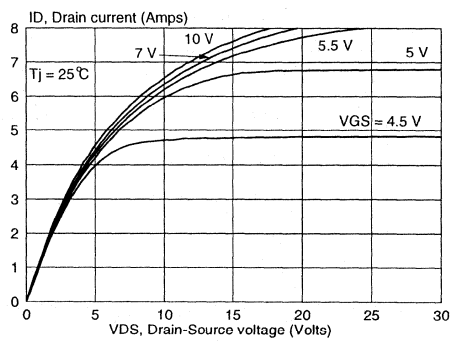


Fig.5. Typical output characteristics.
I_D = f(V_{DS}); parameter V_{GS}

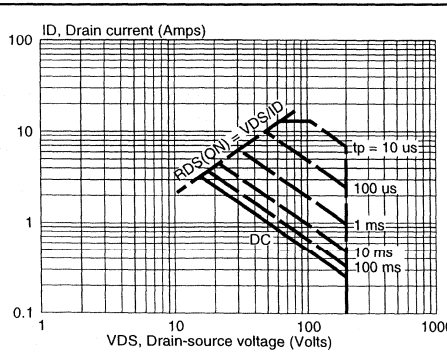


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

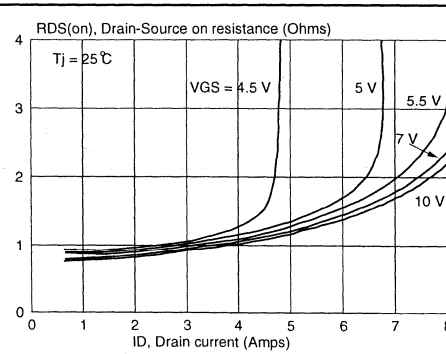


Fig.6. Typical on-state resistance.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

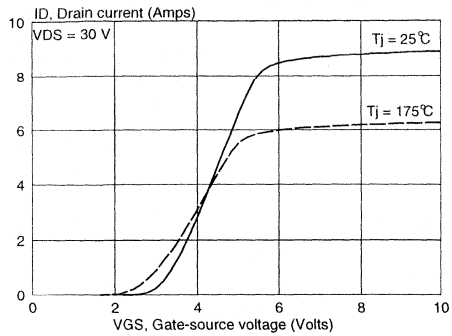


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; parameter T_j

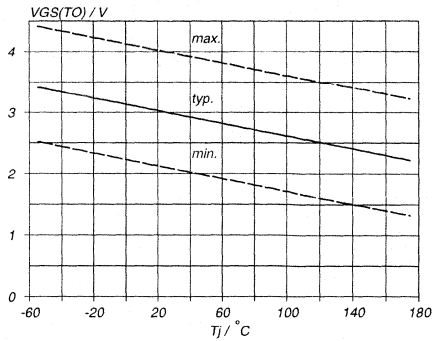


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: $I_D = 0.25$ mA; $V_{DS} = V_{GS}$

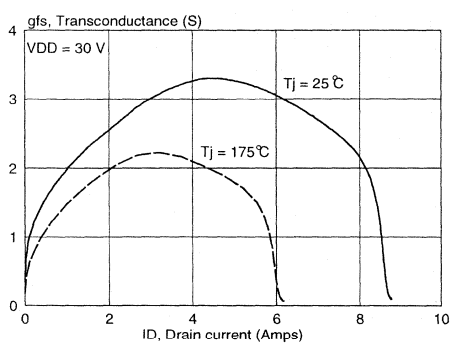


Fig.8. Typical transconductance. $g_{fs} = f(I_D)$; parameter T_j

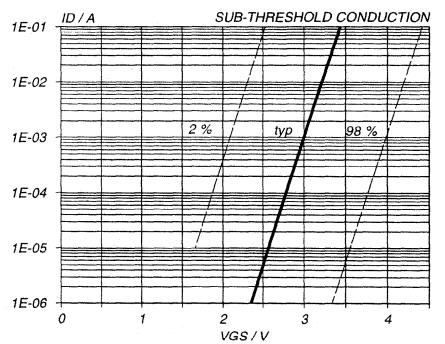


Fig.11. Sub-threshold drain current. $I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

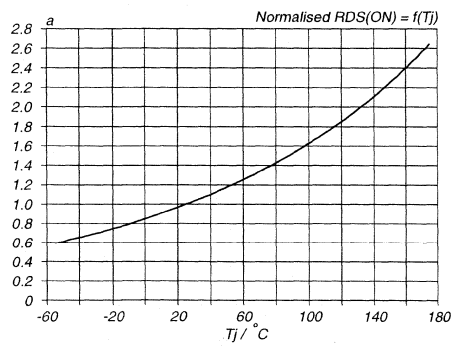


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 3.3$ A; $V_{GS} = 10$ V

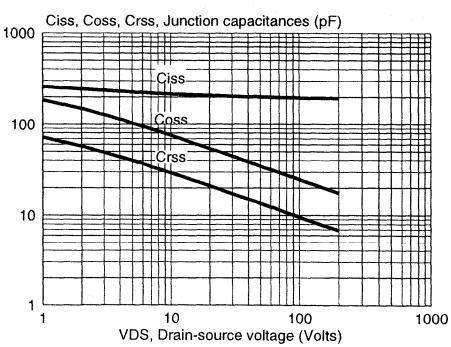


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

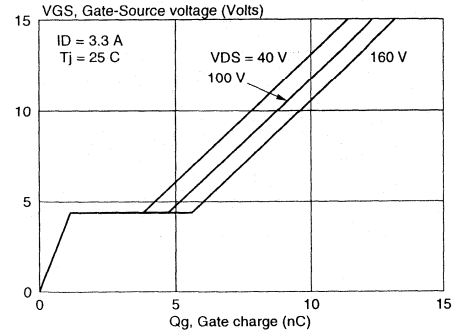


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; *parameter* V_{DS}

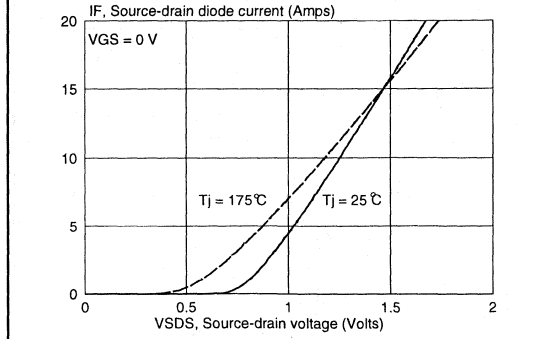


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; *parameter* T_j

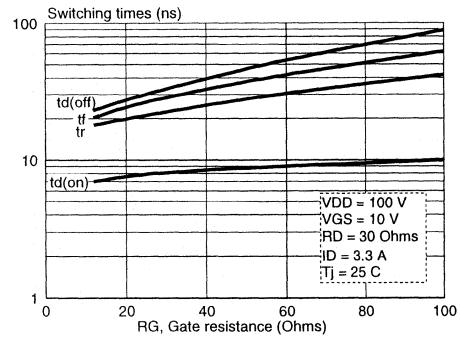


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

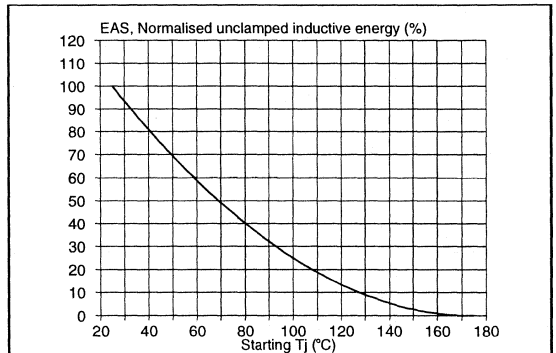


Fig.17. Normalised unclamped inductive energy.
$E_{AS}\% = f(T_j)$

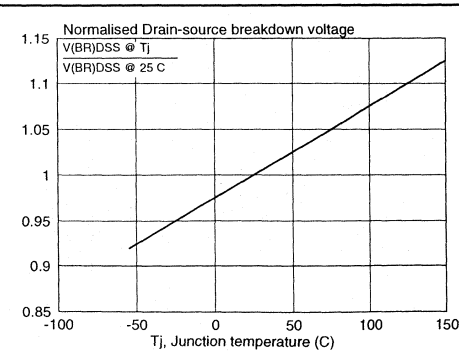


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

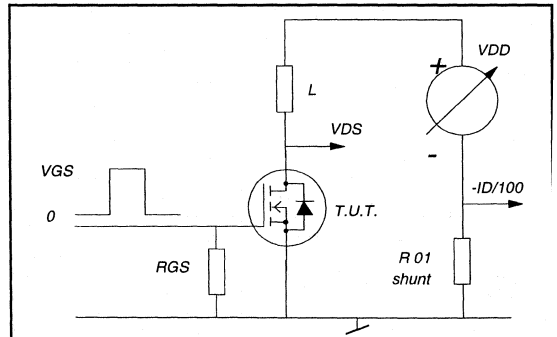


Fig.18. Unclamped inductive test circuit.
$E_{AS} = 0.5 \cdot LI_D^2 \cdot V_{(BR)DSS}/(V_{(BR)DSS} - V_{DD})$

PowerMOS transistor Logic level FET

PHP3N20L

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

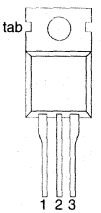
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (DC)	3.5	A
P_{tot}	Total power dissipation	50	W
$R_{DS(ON)}$	Drain-source on-state resistance	1.5	Ω

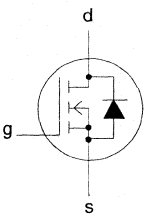
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	3.5	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	2.5	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	14	A
P_D	Total dissipation	T_{mb} = 25 °C	-	50	W
$\Delta P_D/\Delta T_{mb}$	Linear derating factor	T_{mb} > 25 °C	-	0.33	W/K
V_{GS}	Gate-source voltage		-	± 15	V
V_{GSM}	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	± 20	V
E_{AS}	Single pulse avalanche energy	$V_{DD} \leq 50$ V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 5 V	-	25	mJ
I_{AS}	Peak avalanche current	$V_{DD} \leq 50$ V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 5 V	-	3.5	A
T_j, T_{stg}	Operating junction and storage temperature range		- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	3	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		60	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.25	-	V/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 5 V; I_D = 2 A	-	0.77	1.5	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	1.0	1.5	2.0	V
g_{fs}	Forward transconductance	V_{DS} = 50 V; I_D = 2 A	0.8	3.0	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 200 V; V_{GS} = 0 V	-	0.1	25	µA
		V_{DS} = 160 V; V_{GS} = 0 V; T_j = 150 °C	-	1	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$Q_{g(tot)}$	Total gate charge	I_D = 3.3 A; V_{DD} = 160 V; V_{GS} = 5 V	-	7.5	9	nC
Q_{gs}	Gate-source charge		-	1	3	nC
Q_{gd}	Gate-drain (Miller) charge		-	4	6	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 100 V; I_D = 3.3 A;	-	8	-	ns
t_r	Turn-on rise time	R_G = 24 Ω; R_D = 30 Ω	-	33	-	ns
$t_{d(off)}$	Turn-off delay time		-	40	-	ns
t_f	Turn-off fall time		-	36	-	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	270	-	pF
C_{oss}	Output capacitance		-	48	-	pF
C_{rss}	Feedback capacitance		-	17	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	3.5	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	14	A
V_{SD}	Diode forward voltage	I_S = 3.3 A; V_{GS} = 0 V	-	-	1.5	V
t_{rr}	Reverse recovery time	I_S = 3.3 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	90	-	ns
Q_{rr}	Reverse recovery charge		-	0.5	-	µC

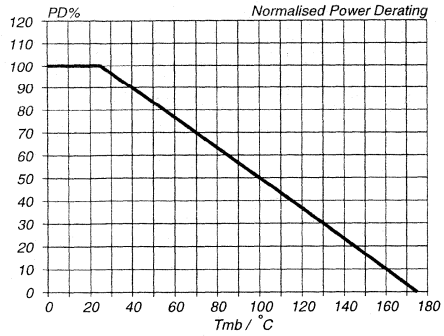


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

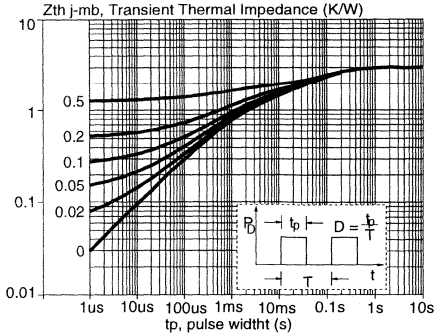


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

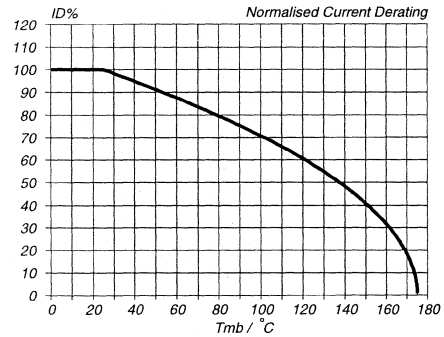


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq 5$ V

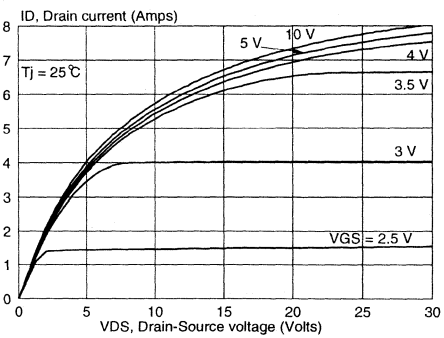


Fig.5. Typical output characteristics.
I_D = f(V_{DS}); parameter V_{GS}

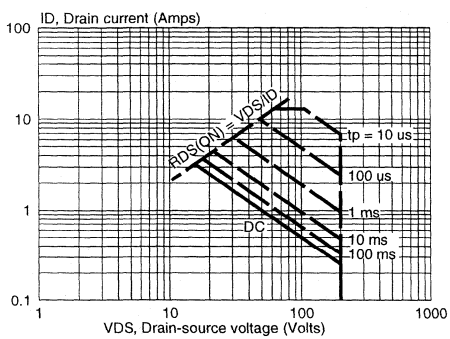


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

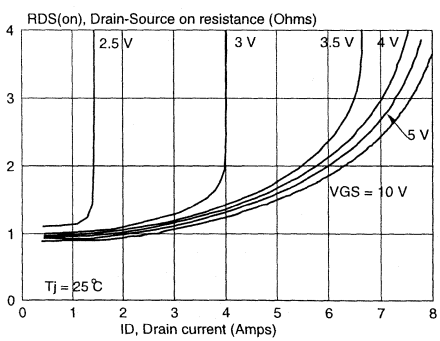


Fig.6. Typical on-state resistance.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

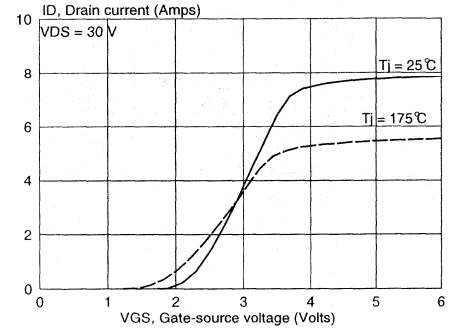


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; parameter T_j

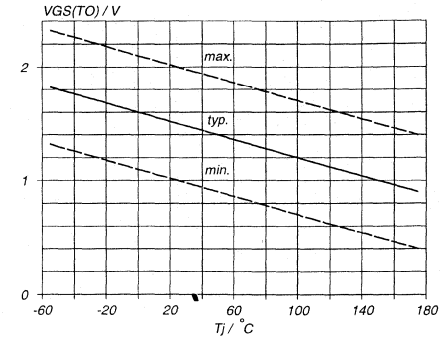


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: $I_D = 0.25$ mA; $V_{DS} = V_{GS}$

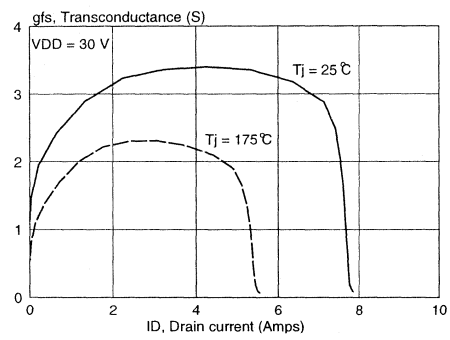


Fig.8. Typical transconductance. $g_{fs} = f(I_D)$; parameter T_j

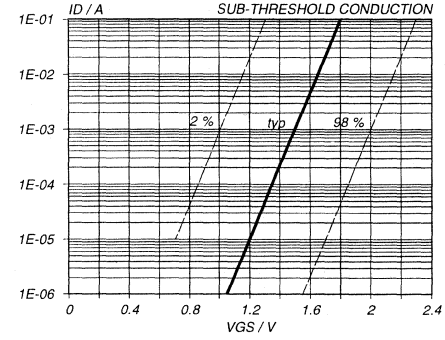


Fig.11. Sub-threshold drain current. $I_D = f(V_{GS})$; conditions: $T_j = 25$ ˚C; $V_{DS} = V_{GS}$

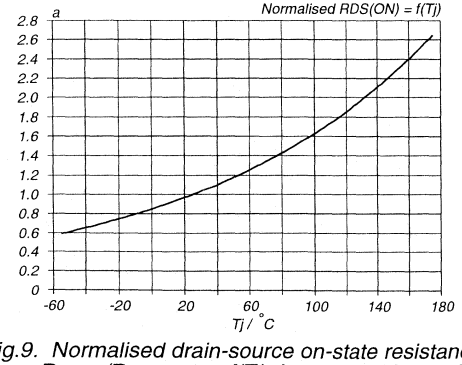


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,^{\circ}C} = f(T_j)$; $I_D = 3.3$ A; $V_{GS} = 5$ V

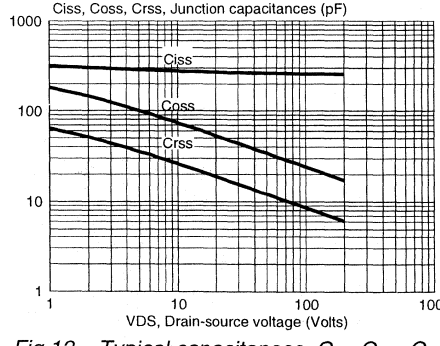


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

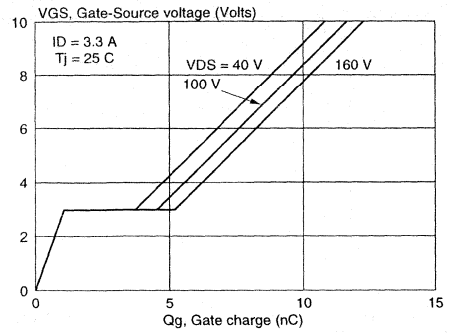


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; *parameter* V_{DS}

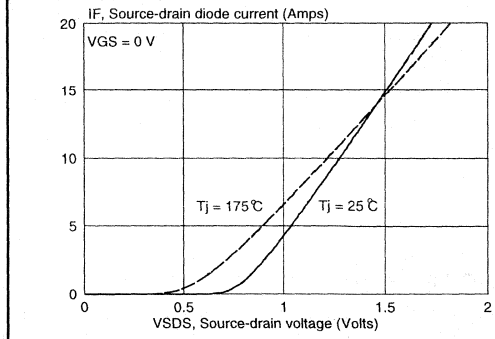


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; *parameter* T_j

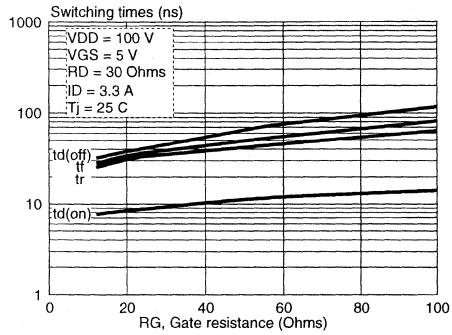


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

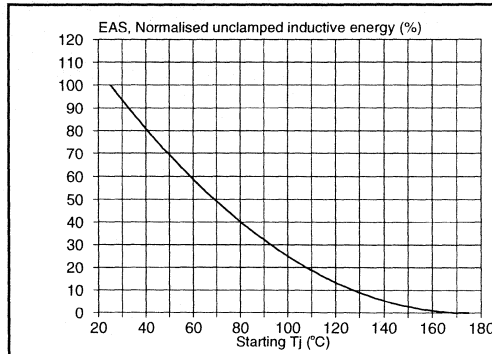


Fig.17. Normalised unclamped inductive energy.
$E_{AS}\% = f(T_j)$

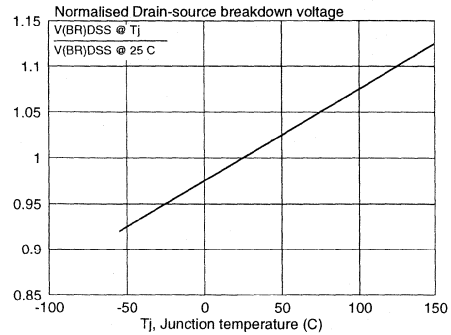


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ ^\circ C} = f(T_j)$

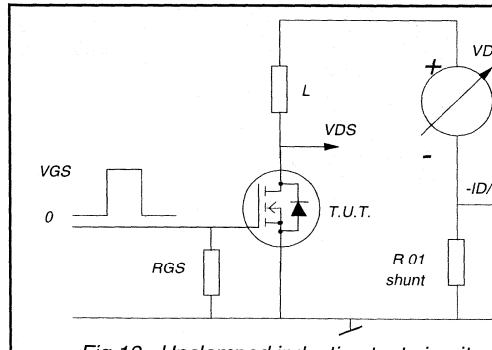


Fig.18. Unclamped inductive test circuit.
$E_{AS} = 0.5 \cdot LI_D^2 \cdot V_{(BR)DSS}/(V_{(BR)DSS} - V_{DD})$

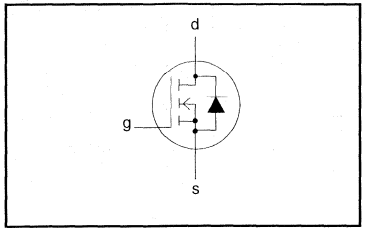
PowerMOS transistors Avalanche energy rated

PHP3N40E, PHB3N40E, PHD3N40E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 400 V

I_D = 2.5 A

$R_{DS(ON)} \leq 3.5\ \Omega$

GENERAL DESCRIPTION

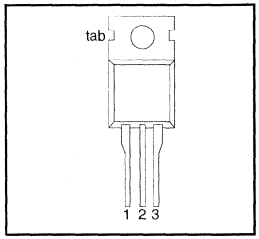
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHP3N40E is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHB3N40E is supplied in the SOT404 surface mounting package.
The PHD3N40E is supplied in the SOT428 surface mounting package.

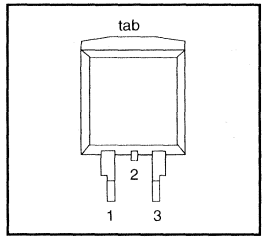
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

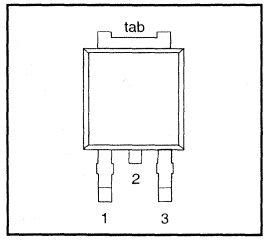
SOT78 (TO220AB)



SOT404



SOT428



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	400	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	400	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	2.5	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	1.5	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	10	A
P_D	Total dissipation	T_{mb} = 25 °C	-	50	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

1 It is not possible to make connection to pin 2 of the SOT428 or SOT404 packages.

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 2 A; $V_{DD} \leq 50$ V; starting $T_j = 25^{\circ}C$; $R_{GS} = 50\ \Omega$; $V_{GS} = 10$ V	-	120	mJ
E_{AR}	Repetitive avalanche energy[2]		-	3.6	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	2	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	SOT78 package, in free air	-	60	-	K/W
		SOT404 and SOT428 packages, pcb mounted, minimum footprint	-	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	400	-	-	V
$\Delta V_{(BR)DSS} / \Delta T_j$	Drain-source breakdown voltage temperature coefficient	$V_{DS} = V_{GS}$; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 1.25 A	-	2	3.5	Ω
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 1.25 A	0.5	1.5	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 400 V; V_{GS} = 0 V	-	1	25	µA
		V_{DS} = 320 V; V_{GS} = 0 V; T_j = 125 °C	-	30	250	µA
I_{GSS}	Gate-source leakage current	$V_{GS} = \pm 30$ V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 2.5 A; V_{DD} = 320 V; V_{GS} = 10 V	-	20	25	nC
Q_{gs}	Gate-source charge		-	2	3	nC
Q_{gd}	Gate-drain (Miller) charge		-	8	12	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 200 V; $R_D = 82\ \Omega$;	-	10	-	ns
t_r	Turn-on rise time	$R_G = 24\ \Omega$	-	25	-	ns
$t_{d(off)}$	Turn-off delay time		-	46	-	ns
t_f	Turn-off fall time		-	25	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	240	-	pF
C_{oss}	Output capacitance		-	44	-	pF
C_{rss}	Feedback capacitance		-	26	-	pF

2 pulse width and repetition rate limited by T_j max.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	2.5	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	10	A
V_{SD}	Diode forward voltage	I_S = 2.5 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 2.5 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	200	-	ns
Q_{rr}	Reverse recovery charge		-	2	-	µC

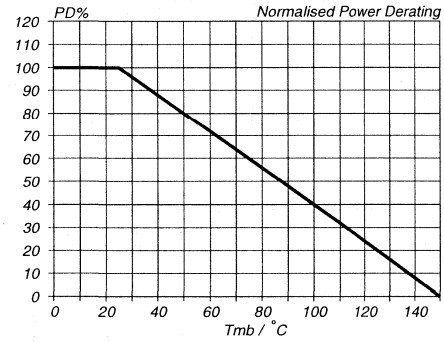


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

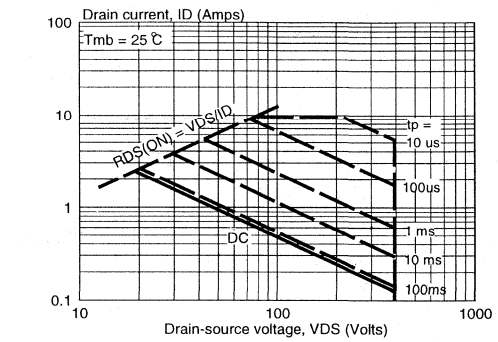


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

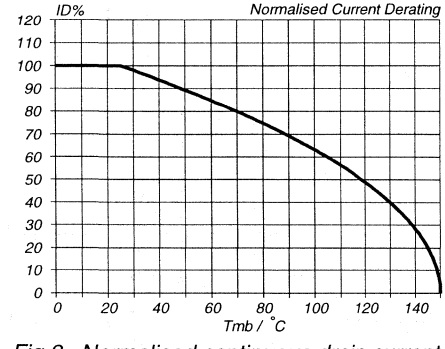


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

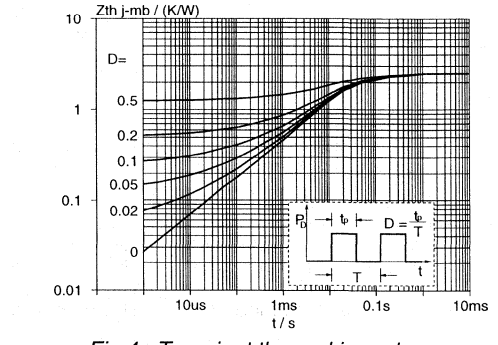


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

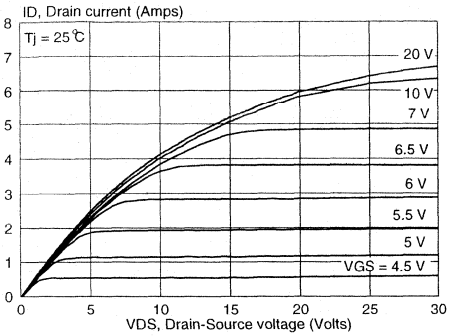


Fig.5. Typical output characteristics.
$I_D = f(V_{DS})$; parameter V_{GS}

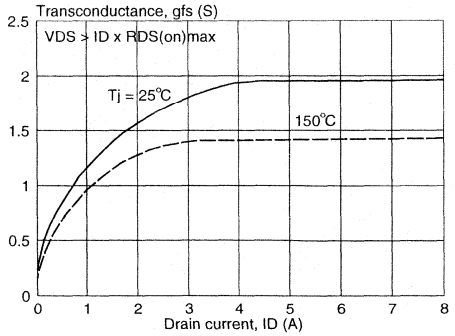


Fig.8. Typical transconductance.
$g_{fs} = f(I_D)$; parameter T_j

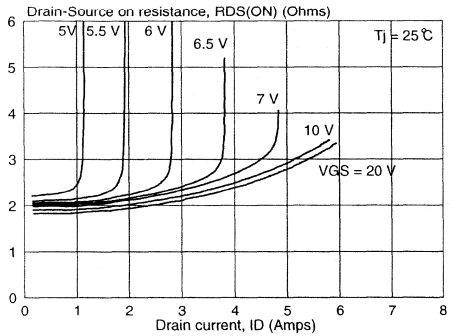


Fig.6. Typical on-state resistance.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

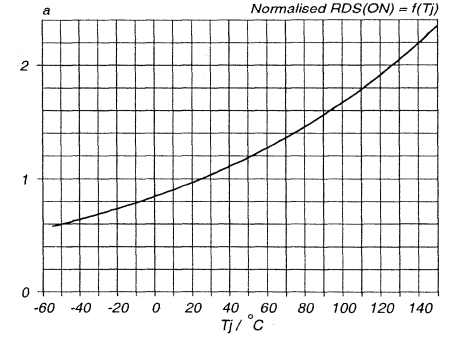


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 1.25 A; V_{GS} = 10 V

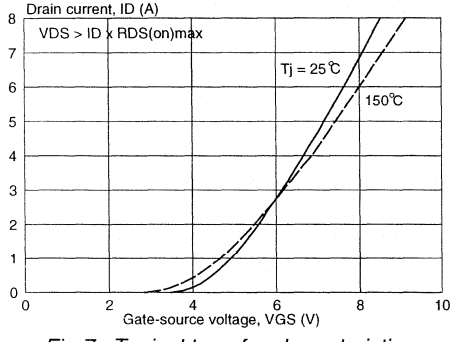


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

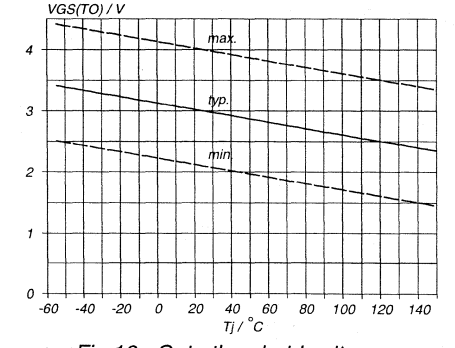


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

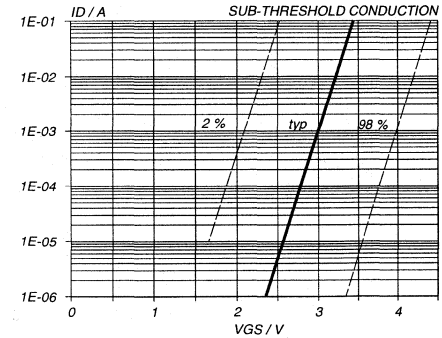


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ ˚C; $V_{DS} = V_{GS}$

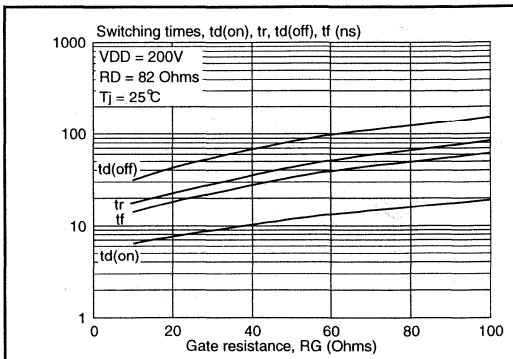


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

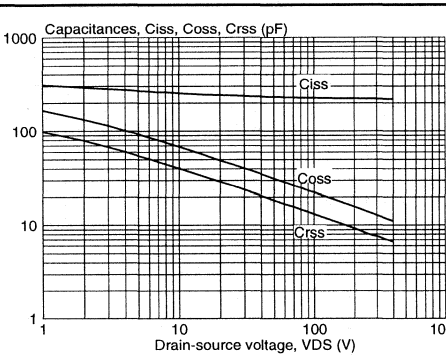


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

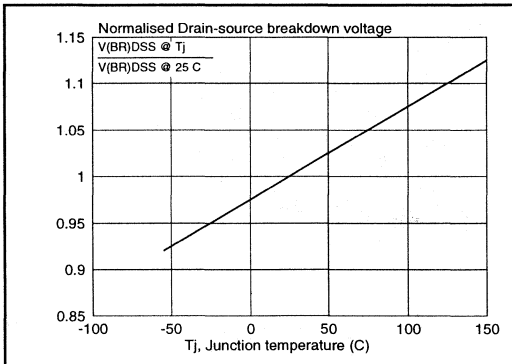


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ ^\circ C} = f(T_j)$

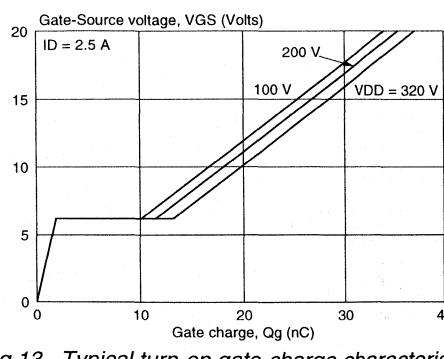


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

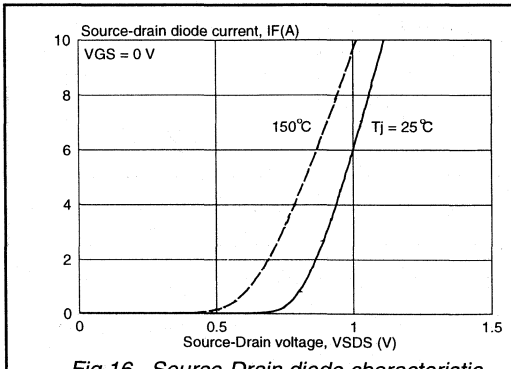


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

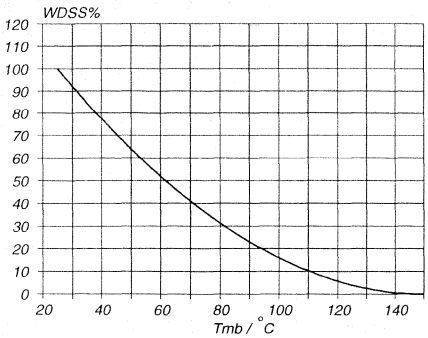


Fig.17. Normalised non-repetitive avalanche energy rating.
$E_{AS}\% = f(T_{mb})$

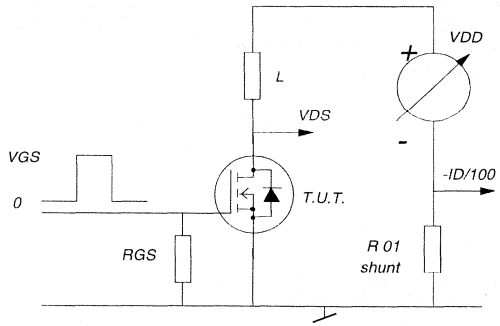


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot \frac{V_{(BR)DSS}}{(V_{(BR)DSS} - V_{DD})}$$

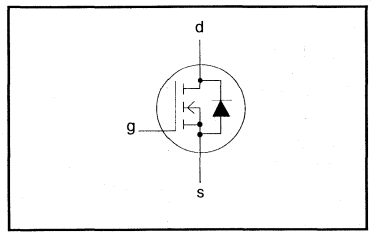
PowerMOS transistors Avalanche energy rated

PHP3N50E, PHB3N50E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 500 V

I_D = 3.4 A

$R_{DS(ON)} \leq 3\ \Omega$

GENERAL DESCRIPTION

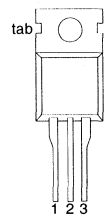
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHP3N50E is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHB3N50E is supplied in the SOT404 surface mounting package.

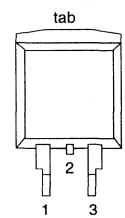
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

SOT78 (TO220AB)



SOT404



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	500	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	500	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	3.4	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	2.2	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	14	A
P_D	Total dissipation	T_{mb} = 25 °C	-	83	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

1 It is not possible to make connection to pin 2 of the SOT404 package.

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 2.5 A; $V_{DD} \leq 50$ V; starting T_j = 25 °C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	210	mJ
E_{AR}	Repetitive avalanche energy[2]		-	5	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	2.5	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	SOT78 package, in free air	-	60	-	K/W
		SOT404 package, pcb mounted, minimum footprint	-	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	500	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 1.7 A	-	2.5	3	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 1.7 A	1	2	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 500 V; V_{GS} = 0 V	-	1	25	µA
		V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 °C	-	30	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 3.4 A; V_{DD} = 400 V; V_{GS} = 10 V	-	26	30	nC
Q_{gs}	Gate-source charge		-	2	3	nC
Q_{gd}	Gate-drain (Miller) charge		-	13	17	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 250 V; R_D = 68 Ω;	-	10	-	ns
t_r	Turn-on rise time	R_G = 18 Ω	-	29	-	ns
$t_{d(off)}$	Turn-off delay time		-	66	-	ns
t_f	Turn-off fall time		-	32	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	310	-	pF
C_{oss}	Output capacitance		-	50	-	pF
C_{rss}	Feedback capacitance		-	28	-	pF

2 pulse width and repetition rate limited by T_j max.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	3.4	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	14	A
V_{SD}	Diode forward voltage	I_S = 3.4 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 3.4 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	370	-	ns
Q_{rr}	Reverse recovery charge		-	2.7	-	µC

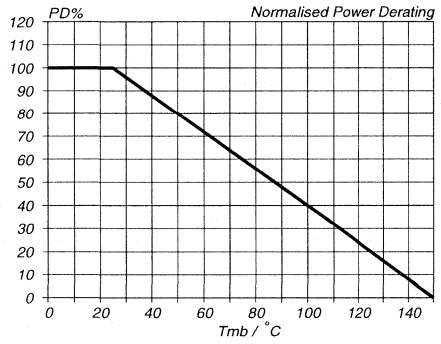


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

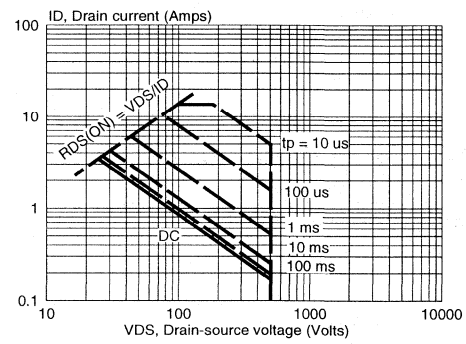


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

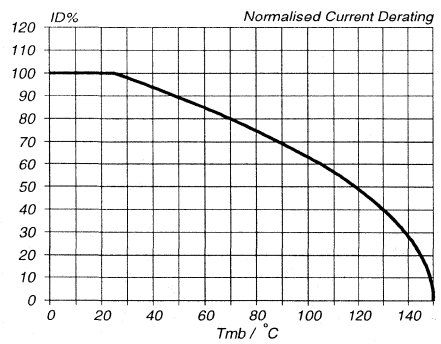


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

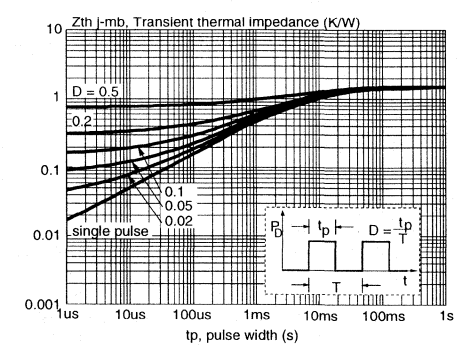


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

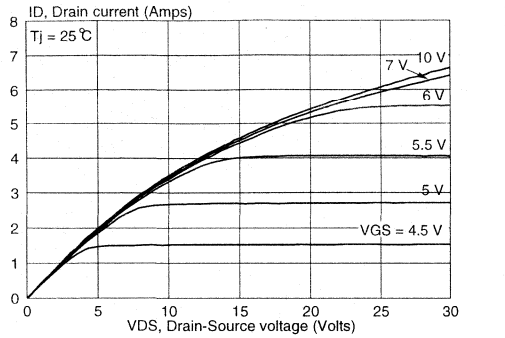


Fig.5. Typical output characteristics.
$I_D = f(V_{DS})$; parameter V_{GS}

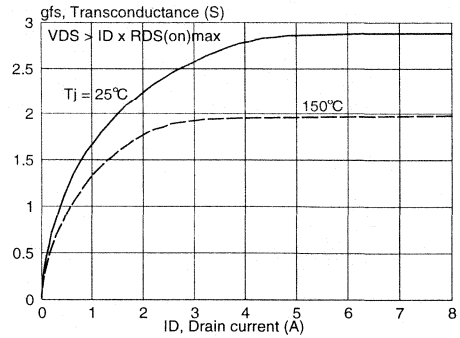


Fig.8. Typical transconductance.
$g_{fs} = f(I_D)$; parameter T_j

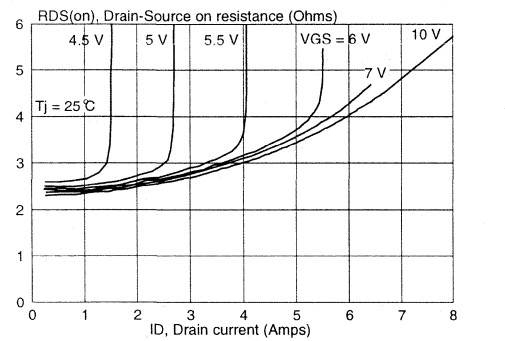


Fig.6. Typical on-state resistance.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

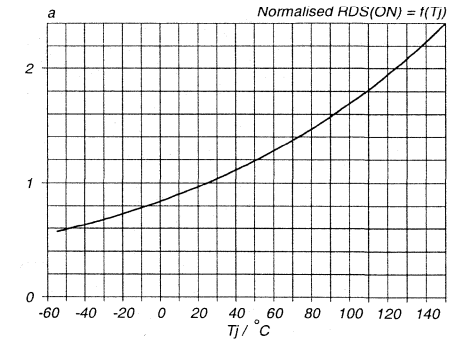


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 1.7 A; V_{GS} = 10 V

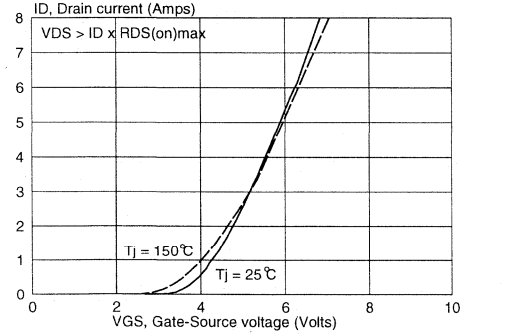


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

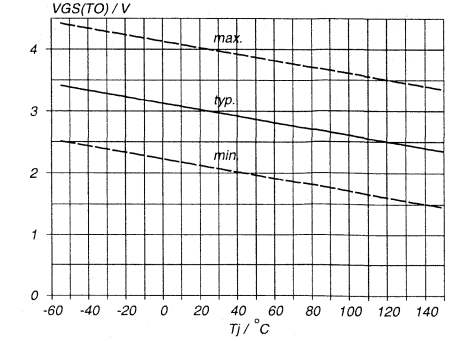


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

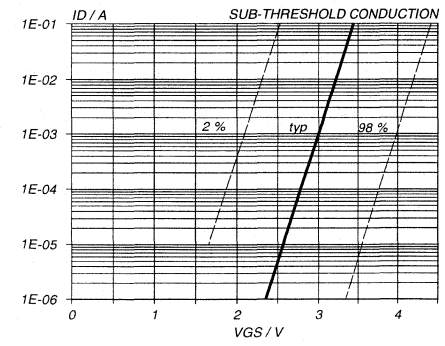


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

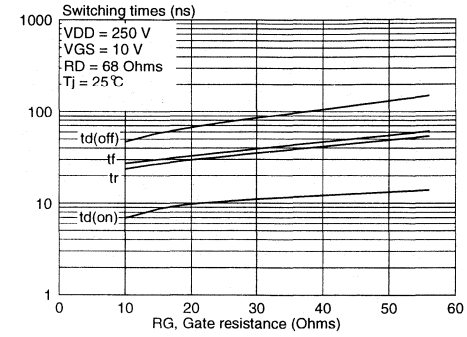


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

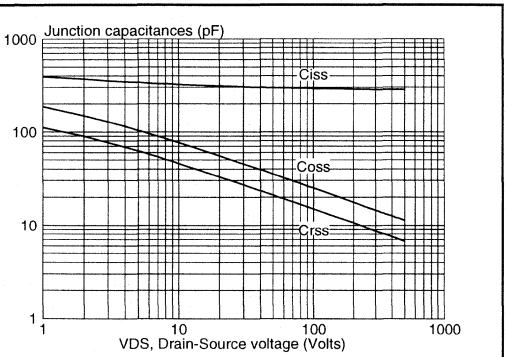


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

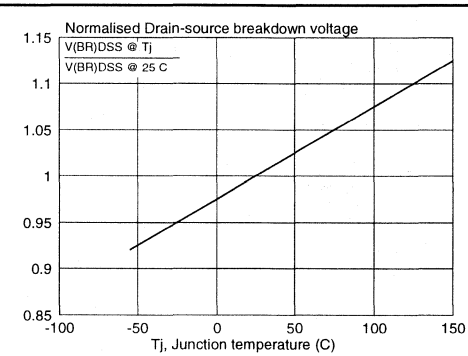


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

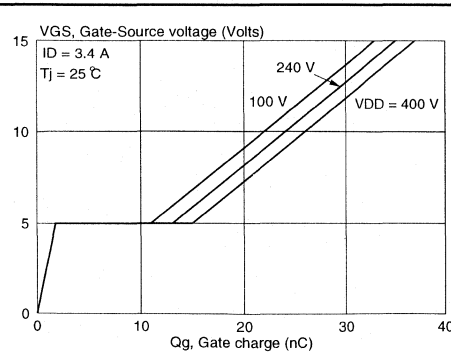


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

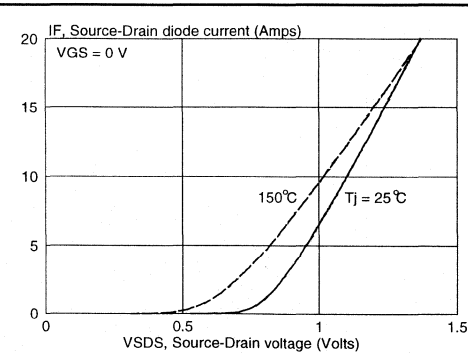


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

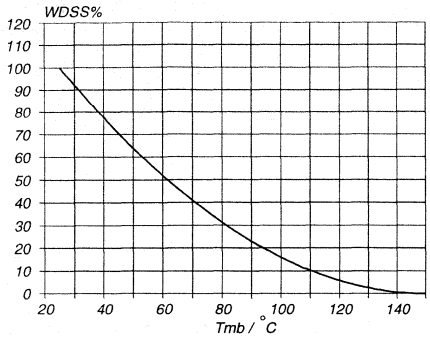


Fig.17. Normalised non-repetitive avalanche energy rating.
$E_{AS}\% = f(T_{mb})$

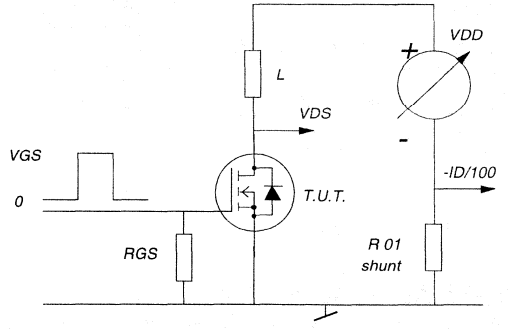


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot \frac{V_{(BR)DSS}}{(V_{(BR)DSS} - V_{DD})}$$

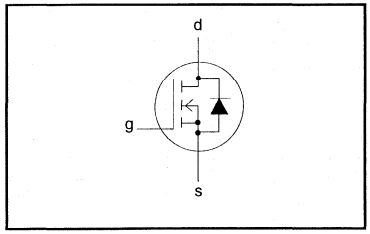
PowerMOS transistors Avalanche energy rated

PHP3N60E, PHB3N60E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 600 V

I_D = 2.8 A

$R_{DS(ON)} \leq 4.4\ \Omega$

GENERAL DESCRIPTION

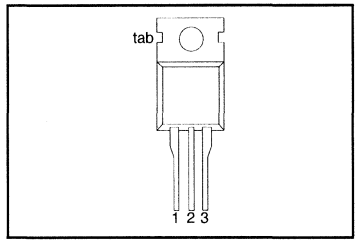
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHP3N60E is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHB3N60E is supplied in the SOT404 surface mounting package.

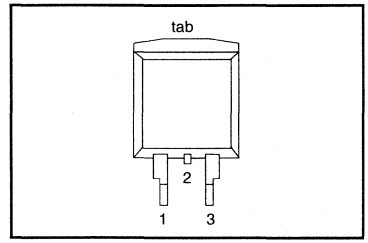
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

SOT78 (TO220AB)



SOT404



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	600	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	600	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	2.8	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	1.8	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	11	A
P_D	Total dissipation	T_{mb} = 25 °C	-	83	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

1 It is not possible to make connection to pin 2 of the SOT404 package.

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 2.2 A; $V_{DD} \leq 50$ V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	171	mJ
E_{AR}	Repetitive avalanche energy[2]		-	5	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	2.2	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.5	K/W
$R_{th\ j\text{-}a$	Thermal resistance junction to ambient	SOT78 package, in free air	-	60	-	K/W
		SOT404 package, pcb mounted, minimum footprint	-	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	600	-	-	V
$\Delta V_{(BR)DSS} / \Delta T_j$	Drain-source breakdown voltage temperature coefficient	$V_{DS} = V_{GS}$; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 1.4 A	-	4	4.4	Ω
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 1.4 A	0.7	1.7	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 600 V; V_{GS} = 0 V	-	1	100	µA
		V_{DS} = 480 V; V_{GS} = 0 V; T_j = 125 °C	-	50	500	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 2.8 A; V_{DD} = 480 V; V_{GS} = 10 V	-	25	30	nC
Q_{gs}	Gate-source charge		-	2	3	nC
Q_{gd}	Gate-drain (Miller) charge		-	12	15	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V; R_D = 100 Ω;	-	10	-	ns
t_r	Turn-on rise time	R_G = 18 Ω	-	26	-	ns
$t_{d(off)}$	Turn-off delay time		-	66	-	ns
t_f	Turn-off fall time		-	30	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	300	-	pF
C_{oss}	Output capacitance		-	43	-	pF
C_{rss}	Feedback capacitance		-	25	-	pF

2 pulse width and repetition rate limited by T_j max.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	2.8	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	11	A
V_{SD}	Diode forward voltage	I_S = 2.8 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 2.8 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	500	-	ns
Q_{rr}	Reverse recovery charge		-	3	-	µC

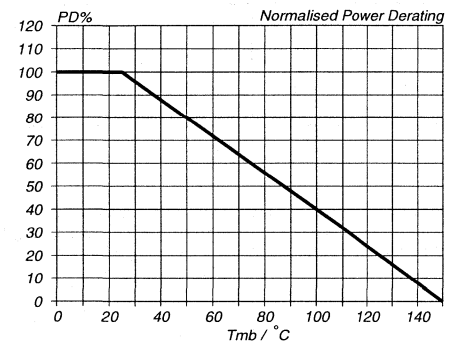


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

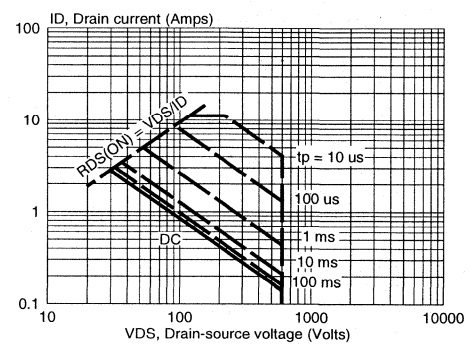


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

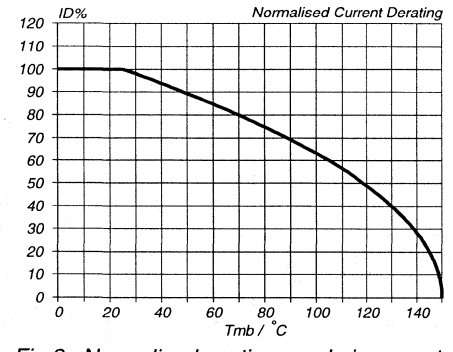


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

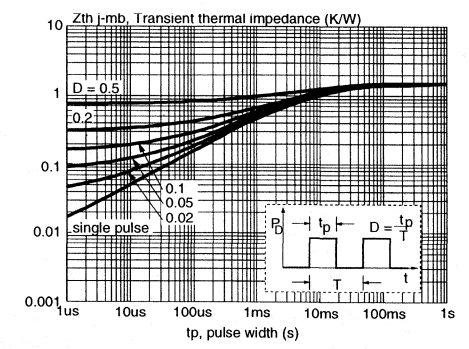


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

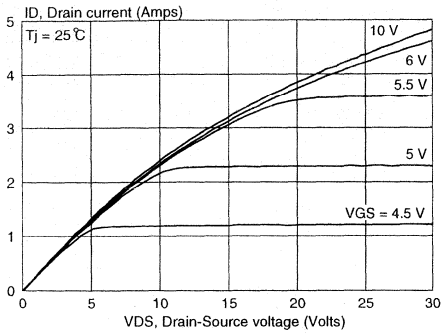


Fig.5. Typical output characteristics.
$I_D = f(V_{DS})$; parameter V_{GS}

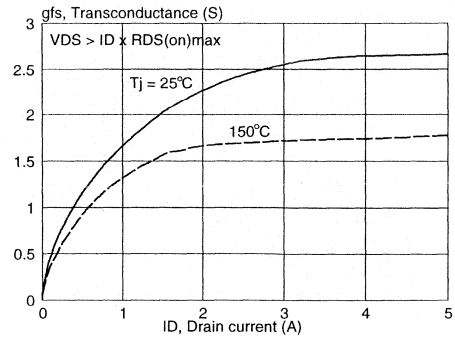


Fig.8. Typical transconductance.
$g_{fs} = f(I_D)$; parameter T_j

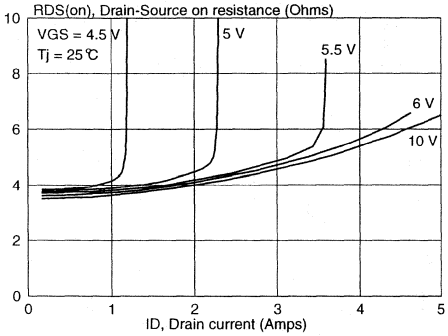


Fig.6. Typical on-state resistance.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

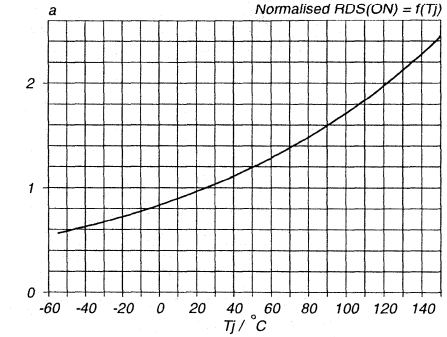


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 1.4 A; V_{GS} = 10 V

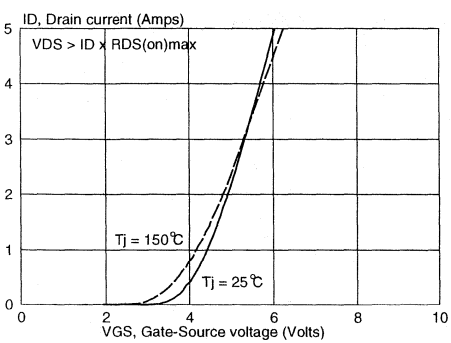


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

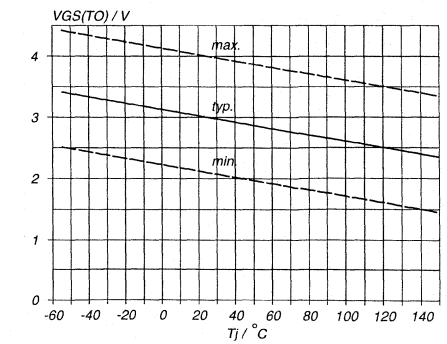


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

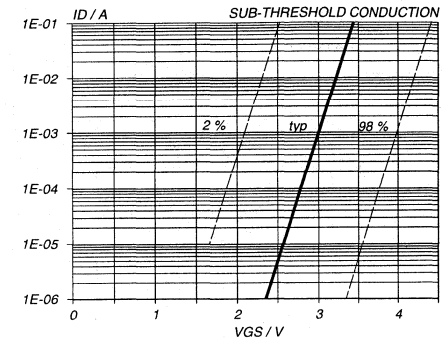


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; *conditions:* $T_j = 25$ °C; $V_{DS} = V_{GS}$

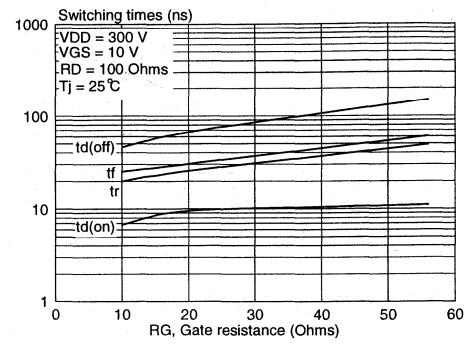


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

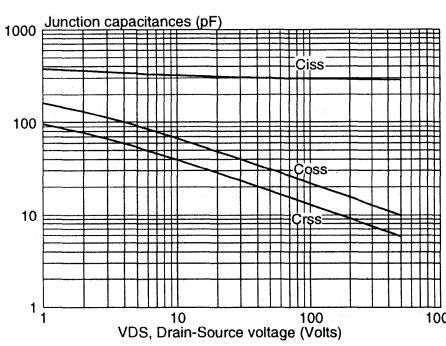


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; *conditions:* $V_{GS} = 0$ V; $f = 1$ MHz

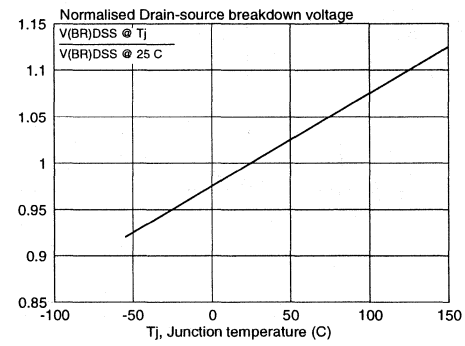


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

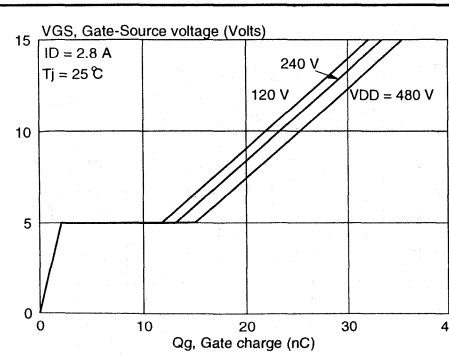


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; *parameter* V_{DS}

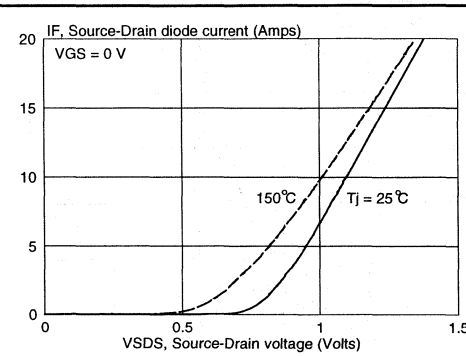


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; *parameter* T_j

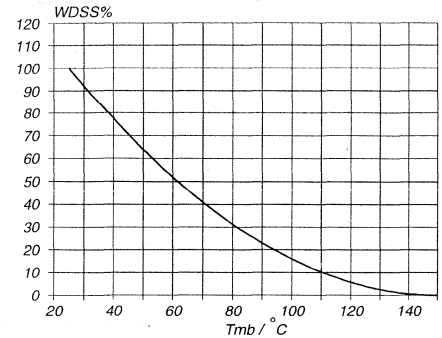


Fig.17. Normalised non-repetitive avalanche energy rating.
$E_{AS}\% = f(T_{mb})$

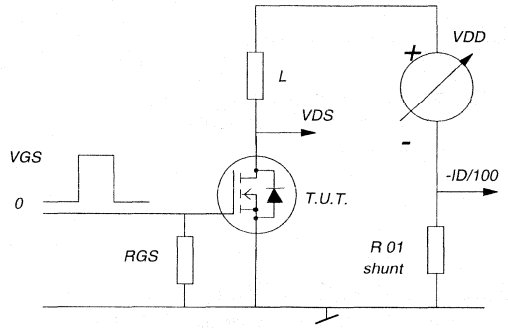


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot \frac{V_{(BR)DSS}}{(V_{(BR)DSS} - V_{DD})}$$

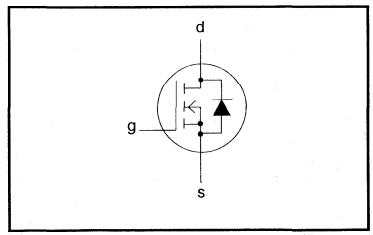
PowerMOS transistors Avalanche energy rated

PHP4N40E, PHB4N40E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 400 V

I_D = 4.4 A

$R_{DS(ON)} \leq 1.8\ \Omega$

GENERAL DESCRIPTION

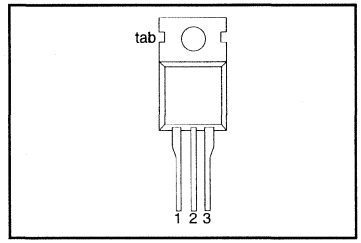
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHP4N40E is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHB4N40E is supplied in the SOT404 surface mounting package.

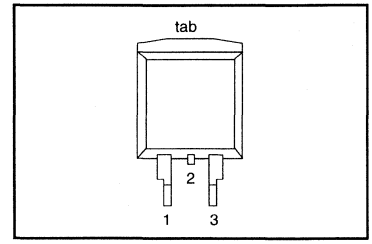
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

SOT78 (TO220AB)



SOT404



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	400	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	400	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	4.4	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	2.7	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	18	A
P_D	Total dissipation	T_{mb} = 25 °C	-	83	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

1 It is not possible to make connection to pin 2 of the SOT404 package.

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 3.3 A; $V_{DD} \leq 50$ V; starting T_j = 25˚C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	190	mJ
E_{AR}	Repetitive avalanche energy[2]		-	5	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	3.3	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.5	K/W
$R_{th\ j\text{-}a$	Thermal resistance junction to ambient	SOT78 package, in free air	-	60	-	K/W
		SOT404 package, pcb mounted, minimum footprint	-	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	400	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 2.2 A	-	1.3	1.8	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 2.2 A	1.3	2.2	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 400 V; V_{GS} = 0 V	-	1	25	µA
		V_{DS} = 320 V; V_{GS} = 0 V; T_j = 125 ˚C	-	30	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 4.4 A; V_{DD} = 320 V; V_{GS} = 10 V	-	26	30	nC
Q_{gs}	Gate-source charge		-	2	4	nC
Q_{gd}	Gate-drain (Miller) charge		-	14	17	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 200 V; R_D = 47 Ω;	-	10	-	ns
t_r	Turn-on rise time	R_G = 18 Ω	-	30	-	ns
$t_{d(off)}$	Turn-off delay time		-	55	-	ns
t_f	Turn-off fall time		-	38	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	310	-	pF
C_{oss}	Output capacitance		-	60	-	pF
C_{rss}	Feedback capacitance		-	36	-	pF

2 pulse width and repetition rate limited by T_j max.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	4.4	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	18	A
V_{SD}	Diode forward voltage	I_S = 4.4 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 4.4 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	250	-	ns
Q_{rr}	Reverse recovery charge		-	2.2	-	µC

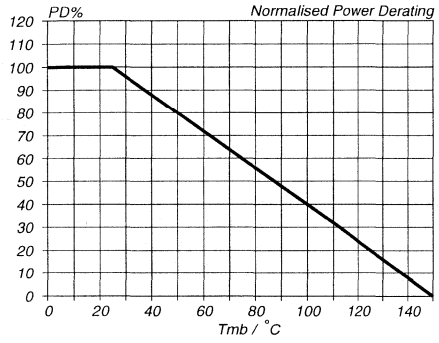


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

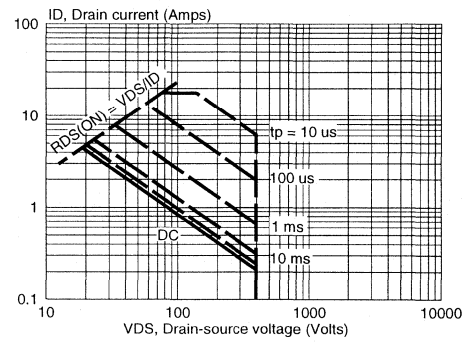


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

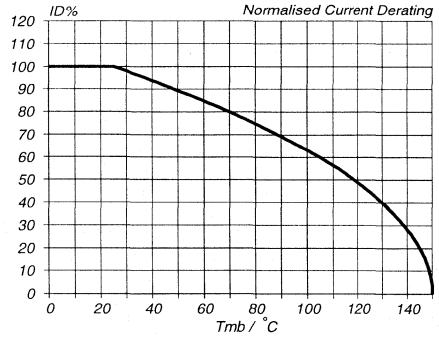


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

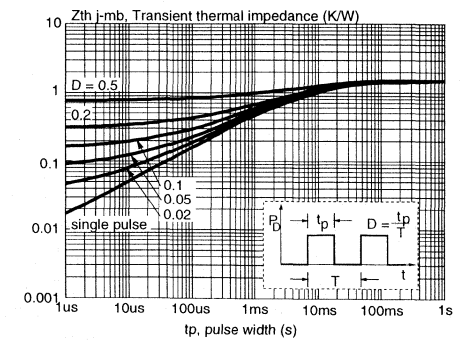


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

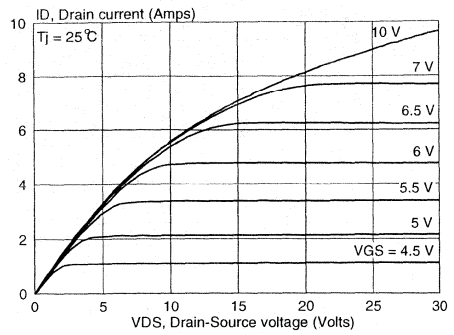


Fig.5. Typical output characteristics. $I_D = f(V_{DS})$; parameter V_{GS}

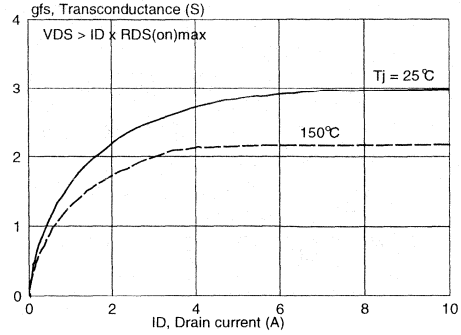


Fig.8. Typical transconductance. $g_{fs} = f(I_D)$; parameter T_j

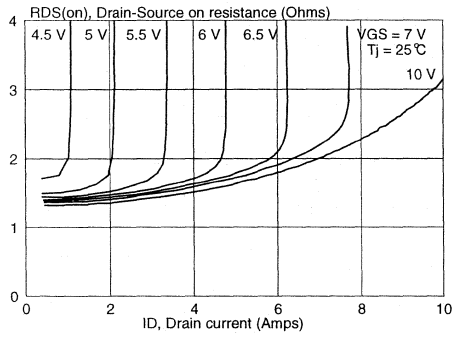


Fig.6. Typical on-state resistance. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

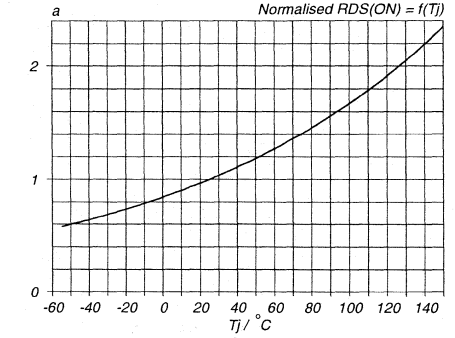


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 2.2 A; V_{GS} = 10 V

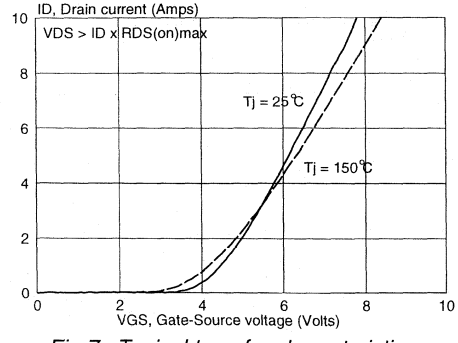


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; parameter T_j

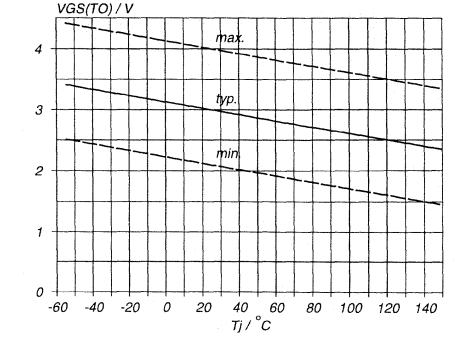


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

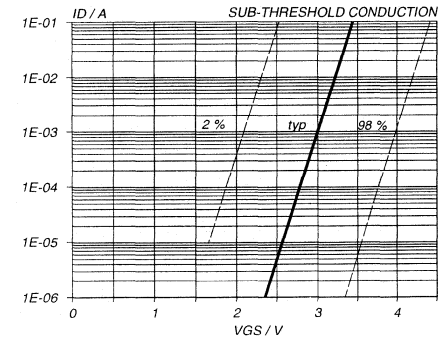


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

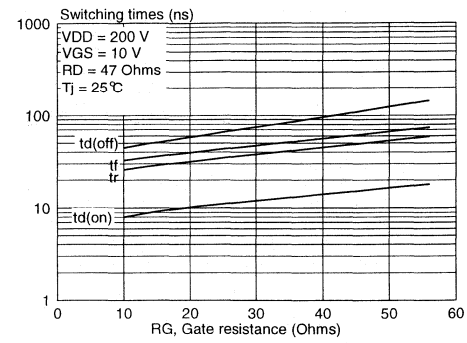


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

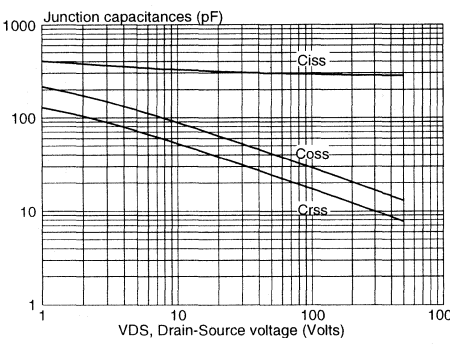


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

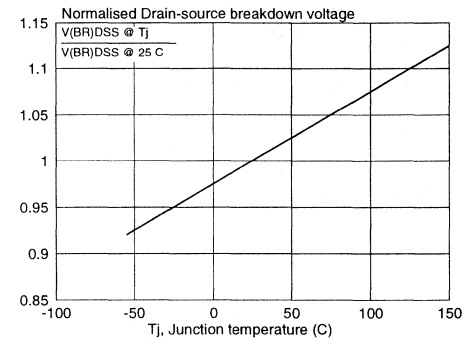


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

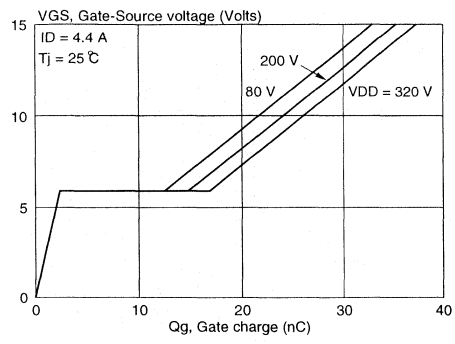


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

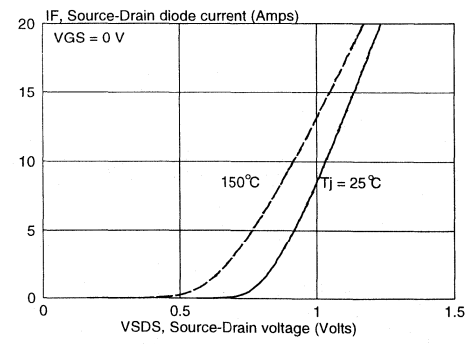


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

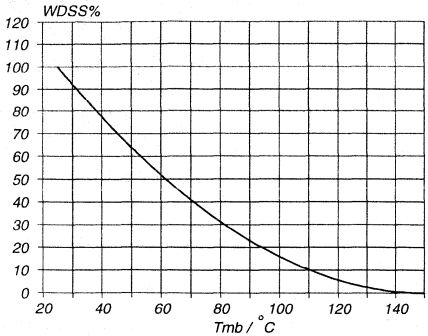


Fig.17. Normalised non-repetitive avalanche energy rating.
$E_{AS}\% = f(T_{mb})$

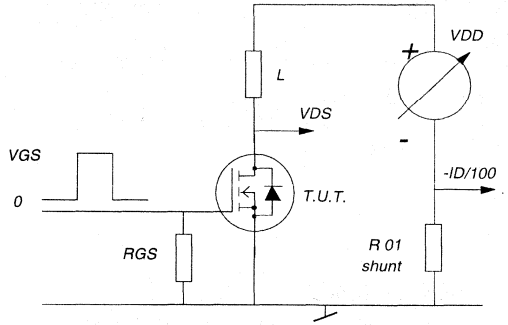


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot \frac{V_{(BR)DSS}}{(V_{(BR)DSS} - V_{DD})}$$

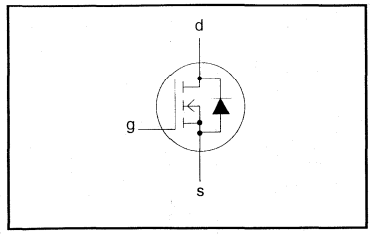
PowerMOS transistors Avalanche energy rated

PHP4N60E, PHB4N60E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 600 V

I_D = 4.5 A

$R_{DS(ON)} \leq 2.5\ \Omega$

GENERAL DESCRIPTION

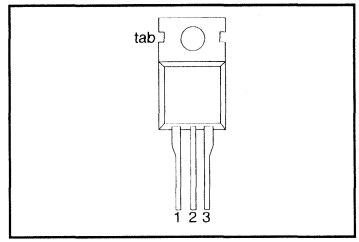
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHP4N60E is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHB4N60E is supplied in the SOT404 surface mounting package.

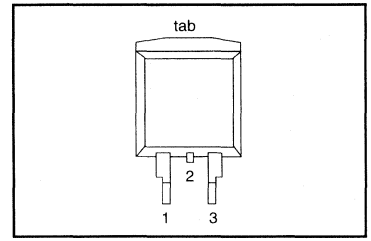
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

SOT78 (TO220AB)



SOT404



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	600	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	600	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	4.5	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	2.9	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	18	A
P_D	Total dissipation	T_{mb} = 25 °C	-	125	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

1 It is not possible to make connection to pin 2 of the SOT404 package.

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 3.6 A; $V_{DD} \leq 50$ V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	290	mJ
E_{AR}	Repetitive avalanche energy[2]		-	7.4	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	3.6	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	SOT78 package, in free air	-	60	-	K/W
		SOT404 package, pcb mounted, minimum footprint	-	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	600	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 2.25 A	-	2.1	2.5	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 2.25 A	2	3.4	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 600 V; V_{GS} = 0 V	-	2	100	µA
		V_{DS} = 480 V; V_{GS} = 0 V; T_j = 125 °C	-	50	500	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 4.5 A; V_{DD} = 480 V; V_{GS} = 10 V	-	48	60	nC
Q_{gs}	Gate-source charge		-	4	6	nC
Q_{gd}	Gate-drain (Miller) charge		-	24	30	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V; R_D = 68 Ω;	-	12	-	ns
t_r	Turn-on rise time	R_G = 12 Ω	-	33	-	ns
$t_{d(off)}$	Turn-off delay time		-	82	-	ns
t_f	Turn-off fall time		-	36	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	600	-	pF
C_{oss}	Output capacitance		-	80	-	pF
C_{rss}	Feedback capacitance		-	46	-	pF

2 pulse width and repetition rate limited by T_j max.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	4.5	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	18	A
V_{SD}	Diode forward voltage	I_S = 4.5 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 4.5 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	480	-	ns
Q_{rr}	Reverse recovery charge		-	4	-	µC

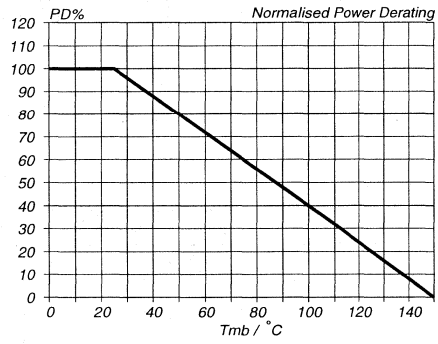


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

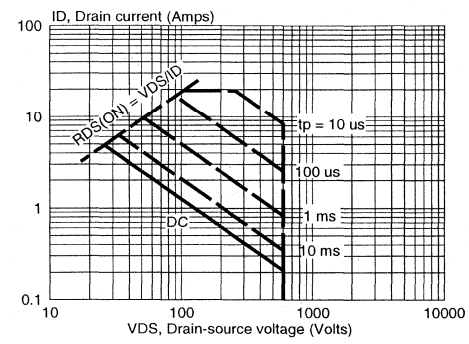


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

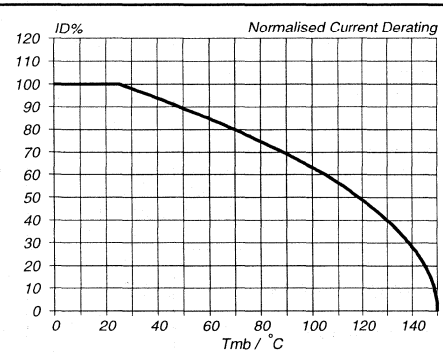


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

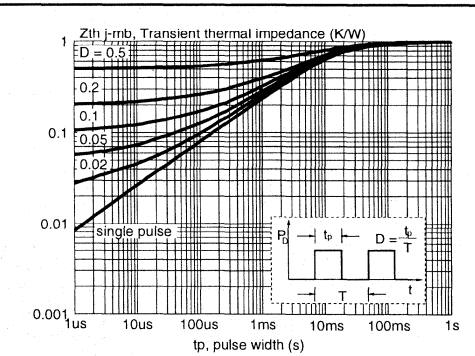


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

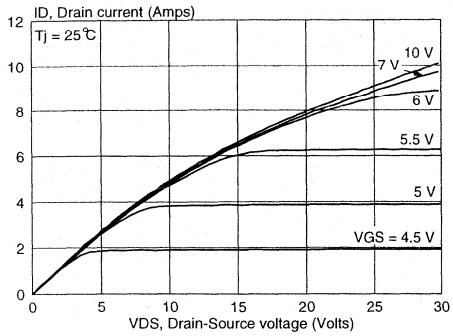


Fig.5. Typical output characteristics. $I_D = f(V_{DS})$; parameter V_{GS}

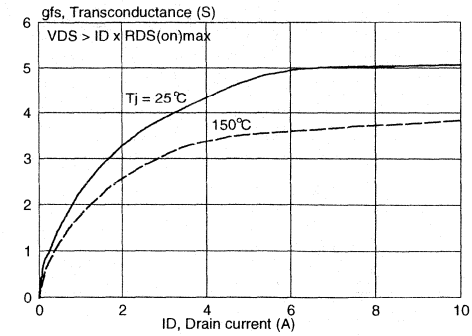


Fig.8. Typical transconductance. $g_{fs} = f(I_D)$; parameter T_j

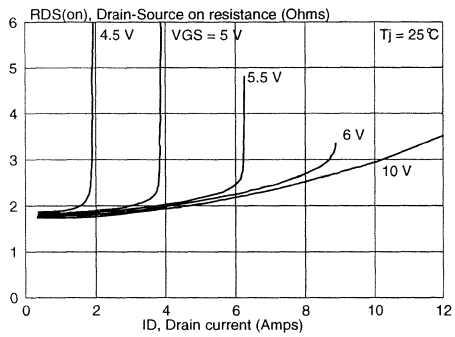


Fig.6. Typical on-state resistance. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

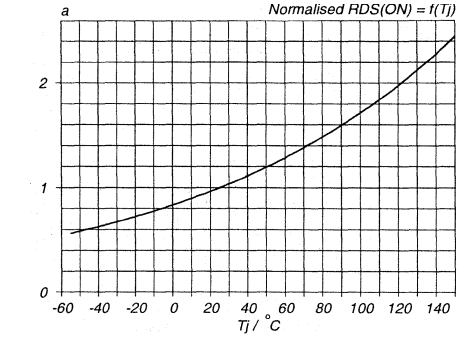


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 2.25$ A; $V_{GS} = 10$ V

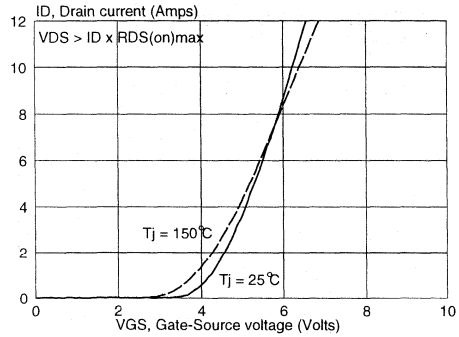


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; parameter T_j

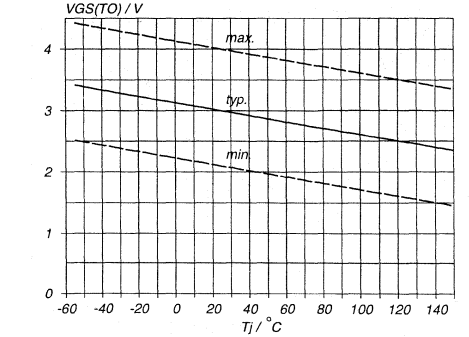


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: $I_D = 0.25$ mA; $V_{DS} = V_{GS}$

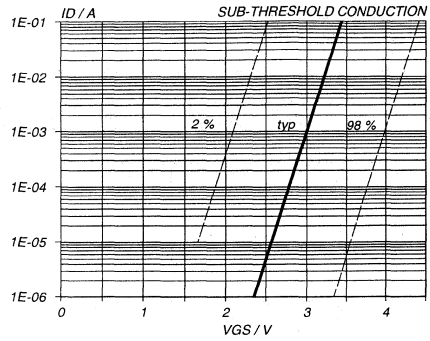


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

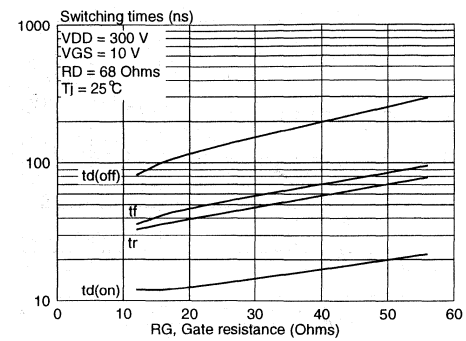


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

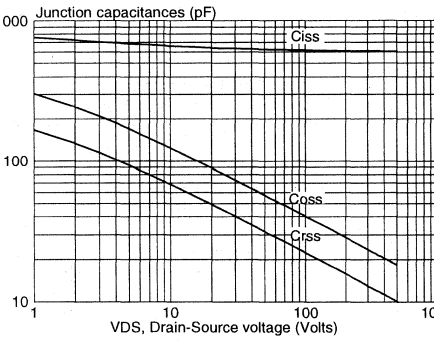


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

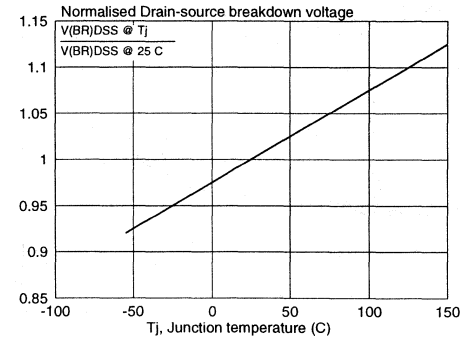


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

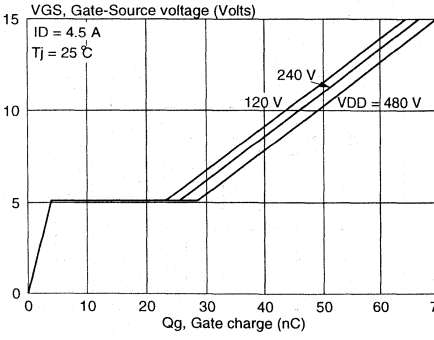


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

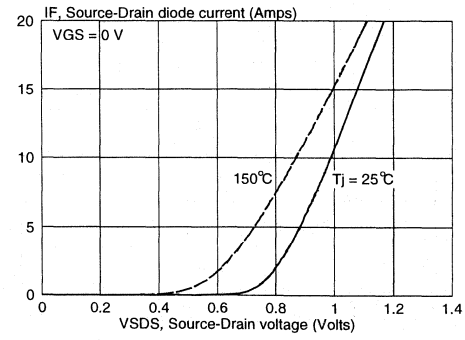


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

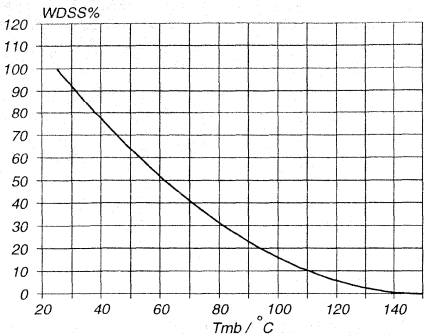


Fig.17. Normalised non-repetitive avalanche energy rating.
$E_{AS}\% = f(T_{mb})$

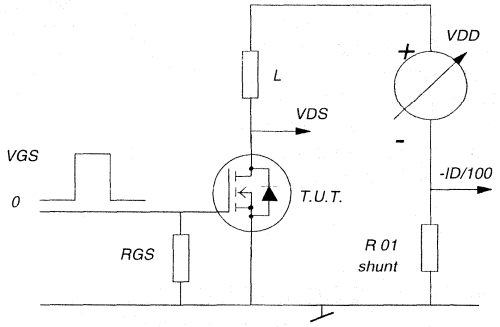


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot \frac{V_{(BR)DSS}}{(V_{(BR)DSS} - V_{DD})}$$

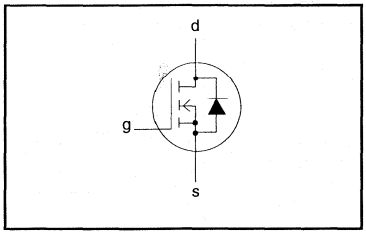
PowerMOS transistors FREDFET, Avalanche energy rated

PHP4ND40E, PHB4ND40E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance
- Fast reverse recovery diode

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 400 V

I_D = 4.4 A

$R_{DS(ON)} \leq 1.8\ \Omega$

t_{rr} = 180 ns

GENERAL DESCRIPTION

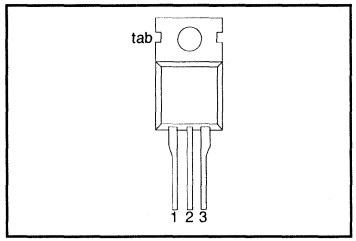
N-channel, enhancement mode field-effect power transistor, incorporating a **F**ast **R**ecovery **E**pitaxial **D**iode (FRED). This gives improved switching performance in half bridge ansd full bridge converters making this device particularly suitable for inverters, lighting ballasts and motor control circuits.

The PHP4ND40E is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHB4ND40E is supplied in the SOT404 surface mounting package.

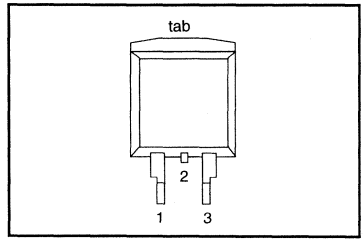
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

SOT78 (TO220AB)



SOT404



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	400	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	400	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	4.4	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	2.7	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	18	A
P_D	Total dissipation	T_{mb} = 25 °C	-	83	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

1 It is not possible to make connection to pin 2 of the SOT404 package.

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 3.3 A; $V_{DD} \leq 50$ V; starting T_j = 25˚C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	190	mJ
E_{AR}	Repetitive avalanche energy[2]		-	5	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	3.3	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.5	K/W
$R_{th\ j\text{-}a$	Thermal resistance junction to ambient	SOT78 package, in free air	-	60	-	K/W
		SOT404 package, pcb mounted, minimum footprint	-	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	400	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 2.2 A	-	1.3	1.8	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 2.2 A	1.3	2.2	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 400 V; V_{GS} = 0 V	-	1	25	µA
		V_{DS} = 320 V; V_{GS} = 0 V; T_j = 125 ˚C	-	30	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 4.4 A; V_{DD} = 320 V; V_{GS} = 10 V	-	26	30	nC
Q_{gs}	Gate-source charge		-	2	4	nC
Q_{gd}	Gate-drain (Miller) charge		-	14	17	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 200 V; R_D = 47 Ω;	-	10	-	ns
t_r	Turn-on rise time	R_G = 18 Ω	-	30	-	ns
$t_{d(off)}$	Turn-off delay time		-	55	-	ns
t_f	Turn-off fall time		-	38	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	310	-	pF
C_{oss}	Output capacitance		-	60	-	pF
C_{rss}	Feedback capacitance		-	36	-	pF

2 pulse width and repetition rate limited by T_j max.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	4.4	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	18	A
V_{SD}	Diode forward voltage	I_S = 4.4 A; V_{GS} = 0 V	-	-	1.5	V
t_{rr}	Reverse recovery time	I_S = 4.4 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	180	-	ns
		I_S = 4.4 A; V_{GS} = 0 V; dI/dt = 100 A/µs; 125°C	-	220	-	ns
Q_{rr}	Reverse recovery charge	I_S = 4.4 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	0.65	-	µC
		I_S = 4.4 A; V_{GS} = 0 V; dI/dt = 100 A/µs; 125°C	-	2.6	-	µC
I_{rrm}	Peak reverse recovery current	I_S = 4.4 A; V_{GS} = 0 V; dI/dt = 100 A/µs; 125°C	-	15	-	A

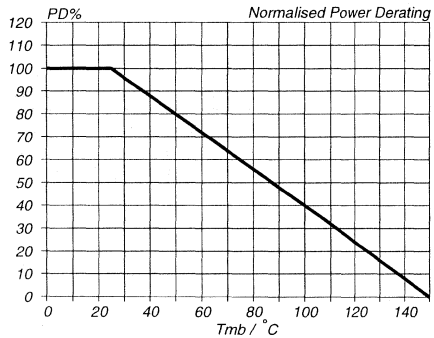


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

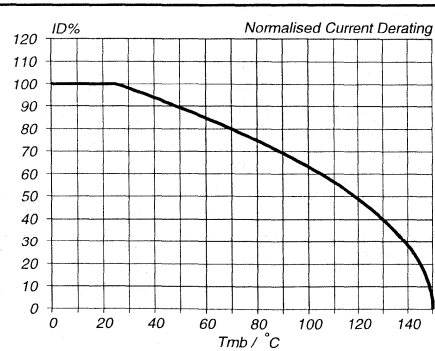


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

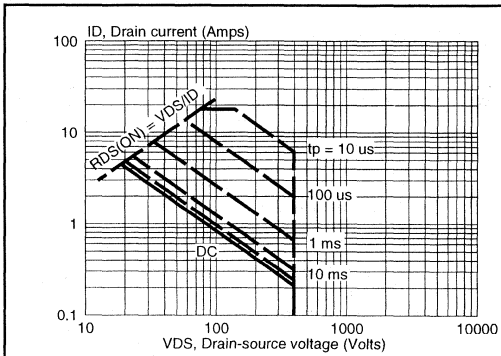


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

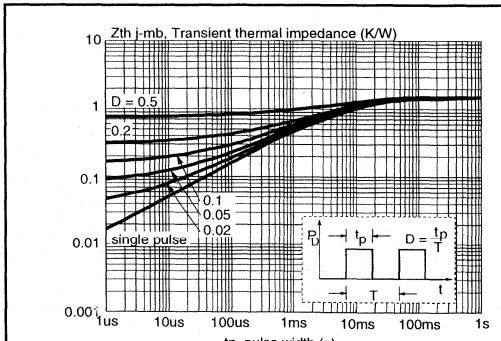


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

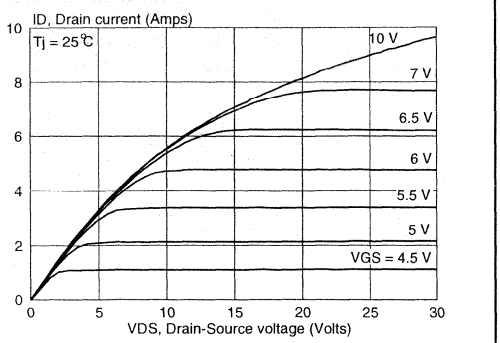


Fig.5. Typical output characteristics.
$I_D = f(V_{DS})$; parameter V_{GS}

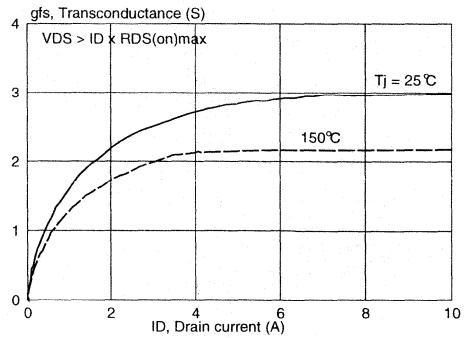


Fig.8. Typical transconductance.
$g_{fs} = f(I_D)$; parameter T_j

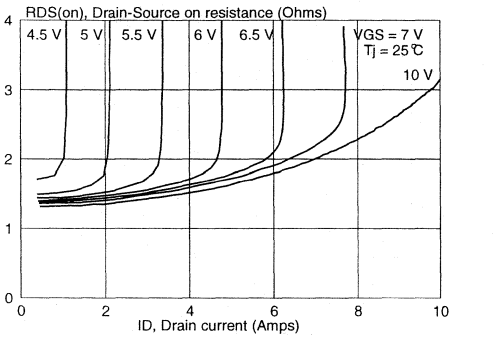


Fig.6. Typical on-state resistance.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

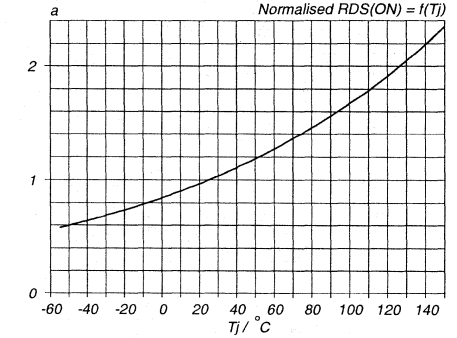


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 2.2 A; V_{GS} = 10 V

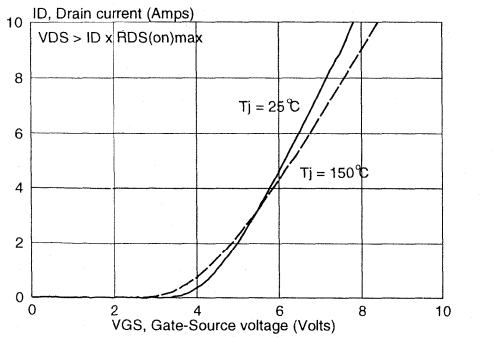


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

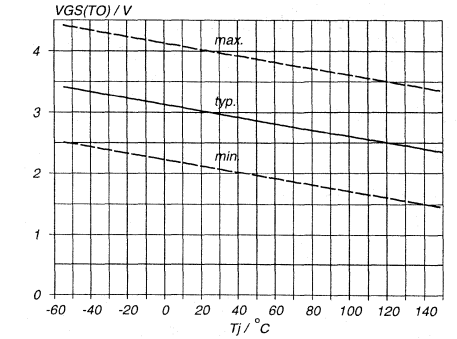


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

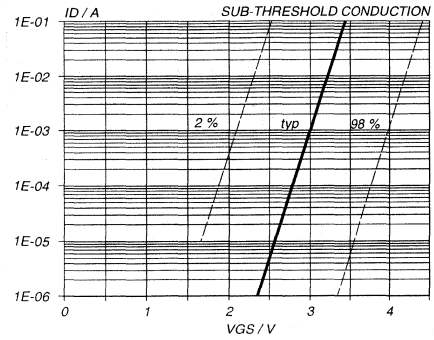


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

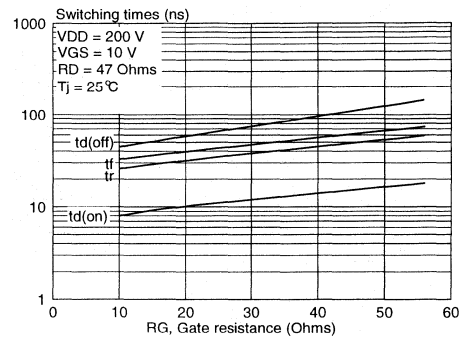


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

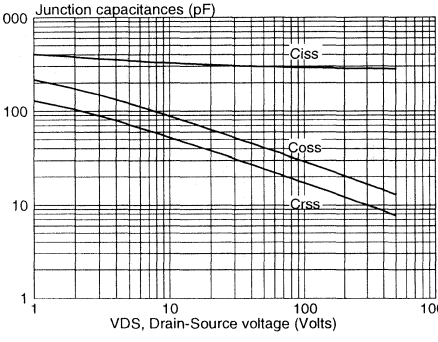


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

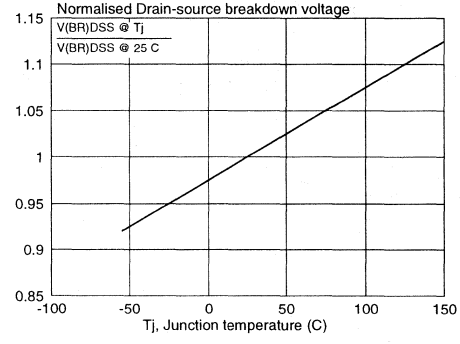


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

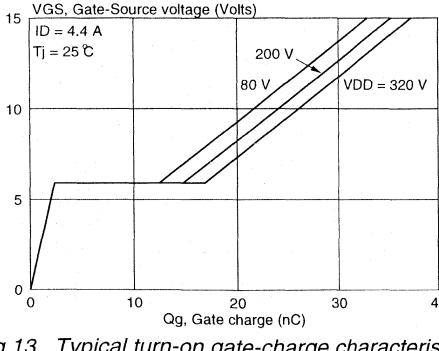


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

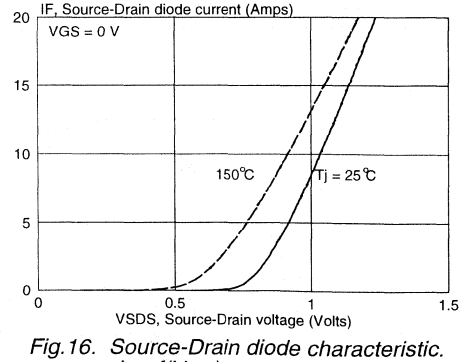


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

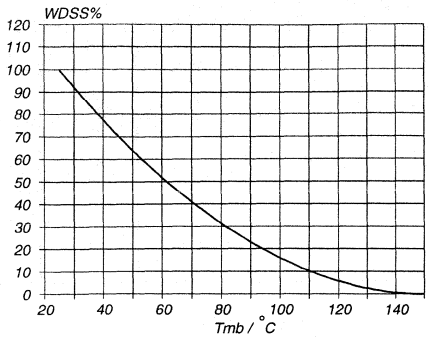


Fig.17. Normalised non-repetitive avalanche energy rating.
$E_{AS}\% = f(T_{mb})$

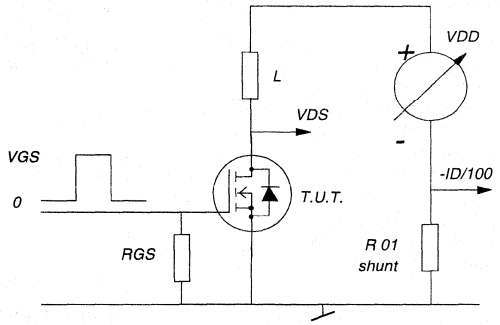


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot \frac{V_{(BR)DSS}}{(V_{(BR)DSS} - V_{DD})}$$

PowerMOS transistor — PHP5N20E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

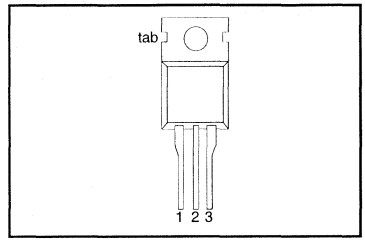
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (DC)	5.0	A
P_{tot}	Total power dissipation	60	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.9	Ω

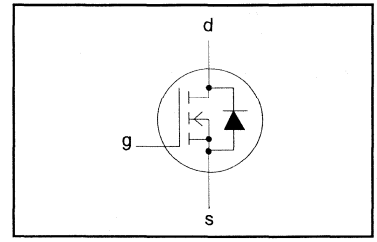
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	5	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	3.5	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	20	A
P_D	Total dissipation	T_{mb} = 25 °C	-	60	W
$\Delta P_D/\Delta T_{mb}$	Linear derating factor	T_{mb} > 25 °C	-	0.4	W/K
V_{GS}	Gate-source voltage		-	± 30	V
E_{AS}	Single pulse avalanche energy	$V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	40	mJ
I_{AS}	Peak avalanche current	$V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	5	A
T_j, T_{stg}	Operating junction and storage temperature range		- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.25	-	V/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 2.5 A	-	0.68	0.9	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 50 V; I_D = 2.5 A	1.5	3.5	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 200 V; V_{GS} = 0 V	-	0.1	25	µA
		V_{DS} = 160 V; V_{GS} = 0 V; T_j = 150 °C	-	1	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$Q_{g(tot)}$	Total gate charge	I_D = 4.8 A; V_{DD} = 160 V; V_{GS} = 10 V	-	11	15	nC
Q_{gs}	Gate-source charge		-	2	3	nC
Q_{gd}	Gate-drain (Miller) charge		-	5.3	7	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 100 V; I_D = 4.8 A;	-	7	-	ns
t_r	Turn-on rise time	R_G = 18 Ω; R_D = 20 Ω	-	29	-	ns
$t_{d(off)}$	Turn-off delay time		-	27	-	ns
t_f	Turn-off fall time		-	22	-	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	300	-	pF
C_{oss}	Output capacitance		-	60	-	pF
C_{rss}	Feedback capacitance		-	20	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	5	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	20	A
V_{SD}	Diode forward voltage	I_S = 5.2 A; V_{GS} = 0 V	-	-	1.5	V
t_{rr}	Reverse recovery time	I_S = 4.8 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	114	-	ns
Q_{rr}	Reverse recovery charge		-	0.8	-	µC

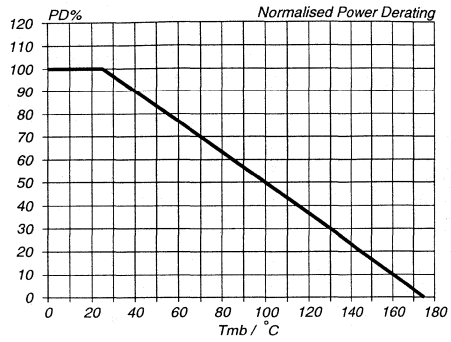


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

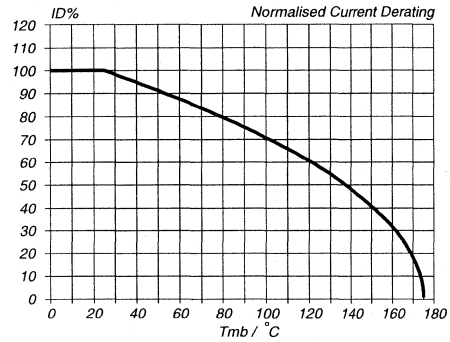


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq 10$ V

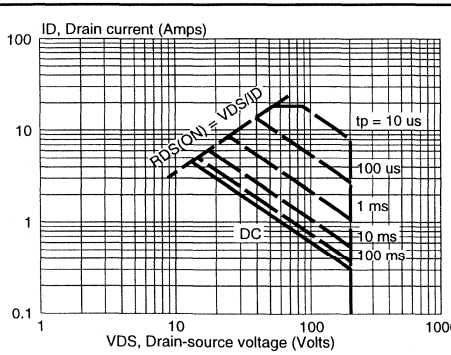


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

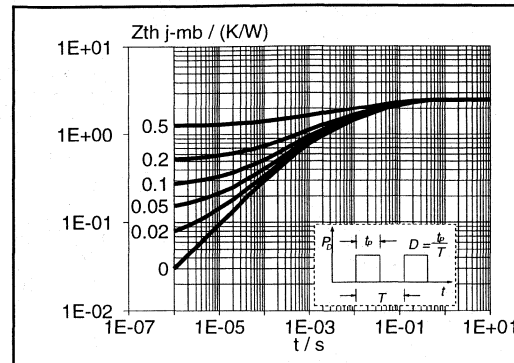


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

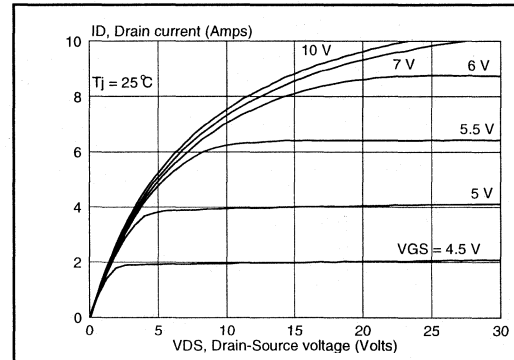


Fig.5. Typical output characteristics.
I_D = f(V_{DS}); parameter V_{GS}

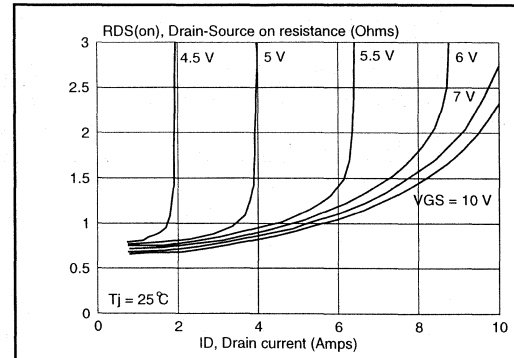


Fig.6. Typical on-state resistance.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

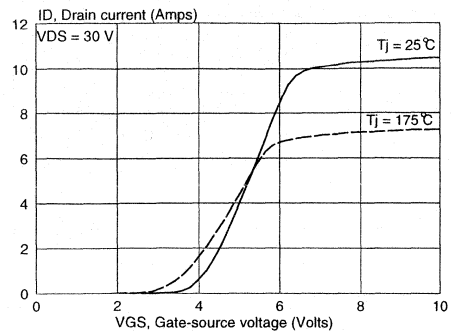


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; parameter T_j

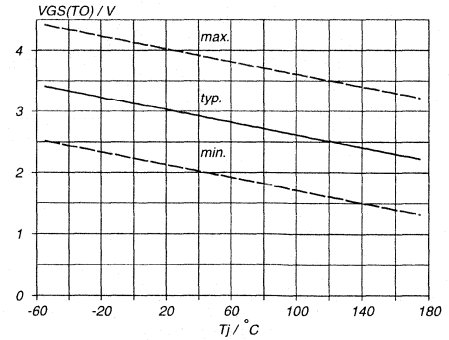


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: $I_D = 0.25$ mA; $V_{DS} = V_{GS}$

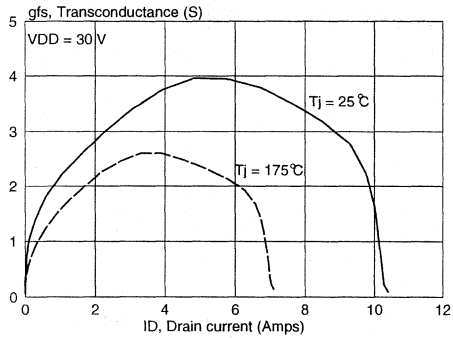


Fig.8. Typical transconductance. $g_{fs} = f(I_D)$; parameter T_j

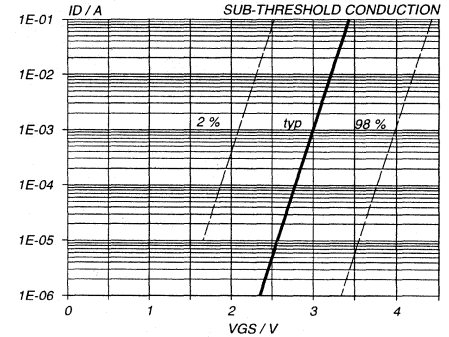


Fig.11. Sub-threshold drain current. $I_D = f(V_{GS})$; conditions: $T_j = 25$ ˚C; $V_{DS} = V_{GS}$

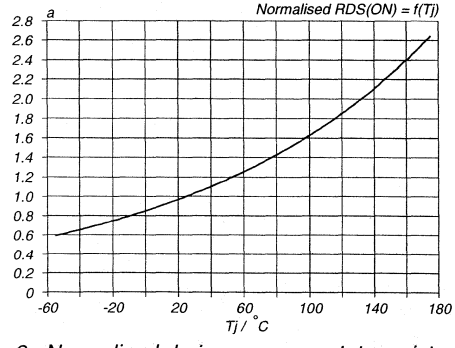


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\ ^\circ C} = f(T_j)$; $I_D = 2.5$ A; $V_{GS} = 10$ V

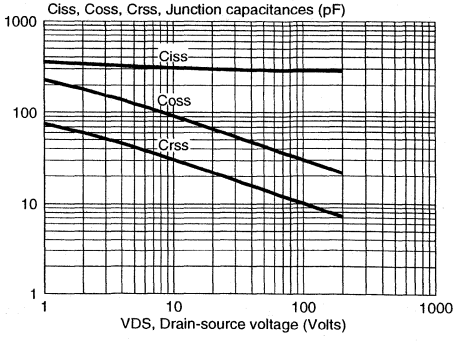


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

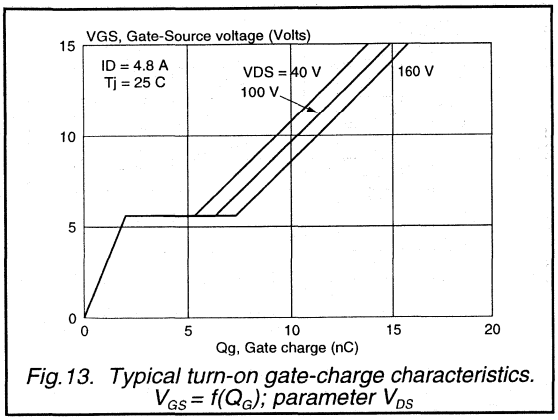


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; *parameter* V_{DS}

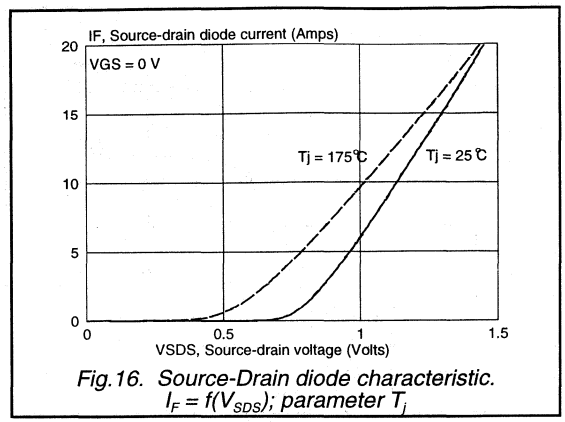


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; *parameter* T_j

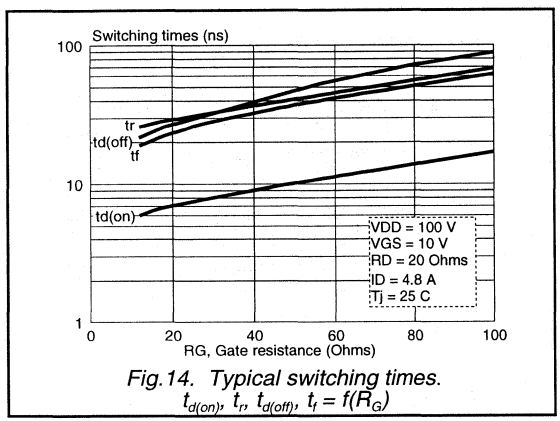


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

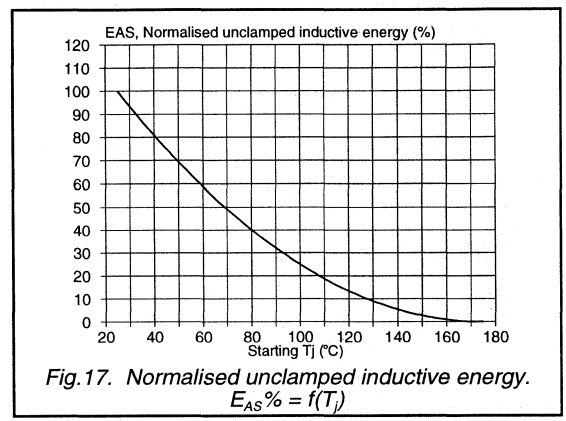


Fig.17. Normalised unclamped inductive energy.
$E_{AS}\% = f(T_j)$

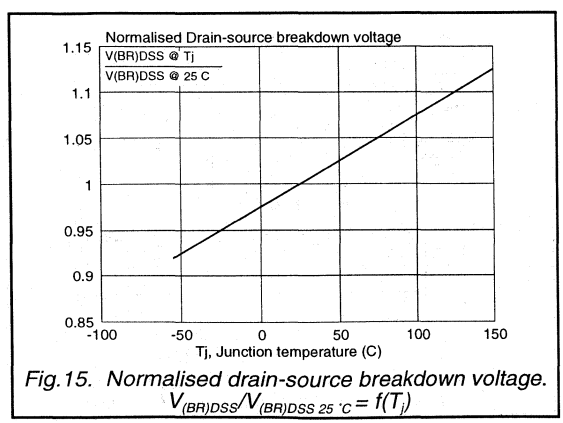


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

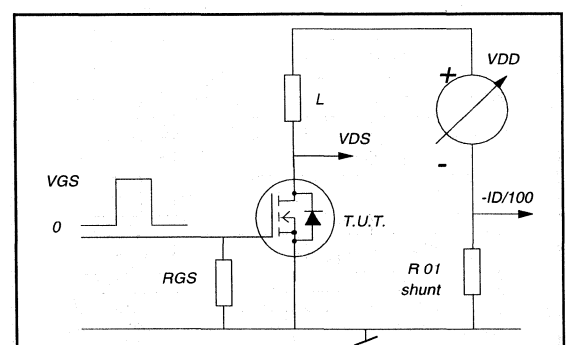


Fig.18. Unclamped inductive test circuit.
$E_{AS} = 0.5 \cdot LI_D^2 \cdot V_{(BR)DSS}/(V_{(BR)DSS} - V_{DD})$

PowerMOS transistor — PHP6N10E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

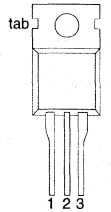
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	6.3	A
P_{tot}	Total power dissipation	50	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.54	Ω

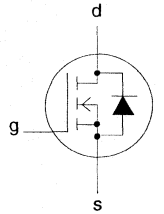
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	6.3	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	4.5	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	25	A
P_D	Total dissipation	T_{mb} = 25 °C	-	50	W
$\Delta P_D/\Delta T_{mb}$	Linear derating factor	T_{mb} > 25 °C	-	0.33	W/K
V_{GS}	Gate-source voltage		-	± 30	V
E_{AS}	Single pulse avalanche energy	$V_{DD} \leq 50$ V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	30	mJ
I_{AS}	Peak avalanche current	$V_{DD} \leq 50$ V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	6.3	A
T_j, T_{stg}	Operating junction and storage temperature range		- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	3	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.15	-	V/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 3.4 A	-	0.25	0.54	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 50 V; I_D = 3.4 A	1.3	3.0	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 100 V; V_{GS} = 0 V	-	0.1	25	µA
		V_{DS} = 80 V; V_{GS} = 0 V; T_j = 150 °C	-	1	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$Q_{g(tot)}$	Total gate charge	I_D = 5.6 A; V_{DD} = 80 V; V_{GS} = 10 V	-	9.2	12	nC
Q_{gs}	Gate-source charge		-	1.7	3	nC
Q_{gd}	Gate-drain (Miller) charge		-	4.7	6	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 50 V; I_D = 5.6 A;	-	7	-	ns
t_r	Turn-on rise time	R_G = 24 Ω; R_D = 8.4 Ω	-	40	-	ns
$t_{d(off)}$	Turn-off delay time		-	22	-	ns
t_f	Turn-off fall time		-	18	-	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	222	-	pF
C_{oss}	Output capacitance		-	74	-	pF
C_{rss}	Feedback capacitance		-	30	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	6.3	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	25	A
V_{SD}	Diode forward voltage	I_S = 5.6 A; V_{GS} = 0 V	-	-	1.5	V
t_{rr}	Reverse recovery time	I_S = 5.6 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	70	-	ns
Q_{rr}	Reverse recovery charge		-	0.4	-	µC

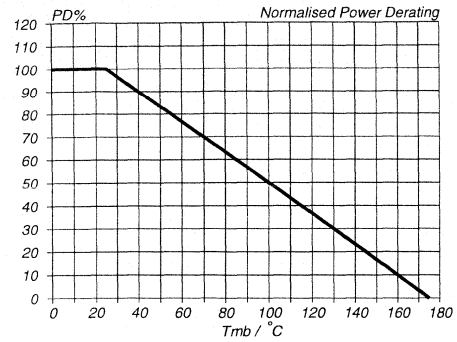


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

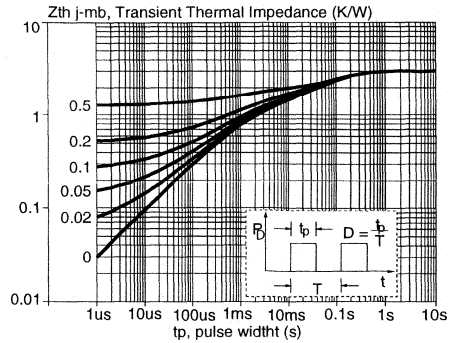


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

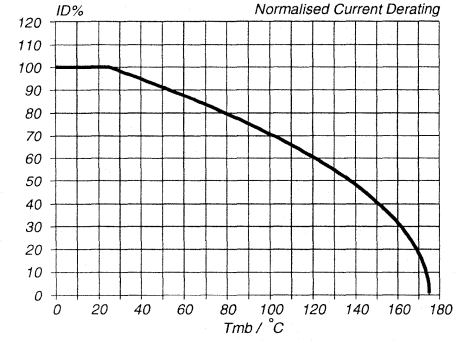


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 5 V

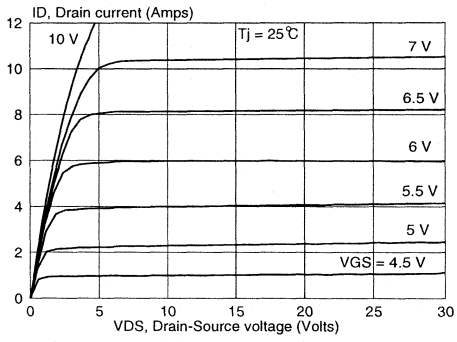


Fig.5. Typical output characteristics.
I_D = f(V_{DS}); parameter V_{GS}

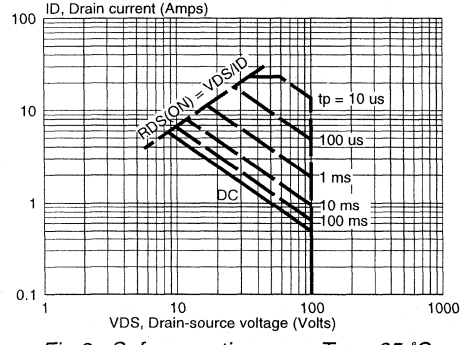


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

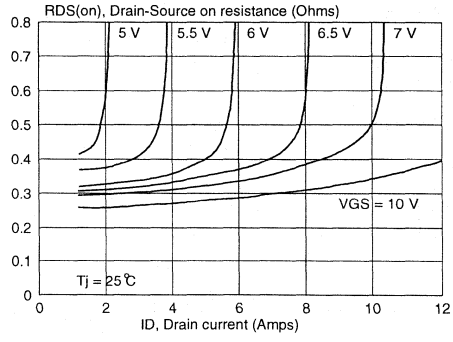


Fig.6. Typical on-state resistance.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

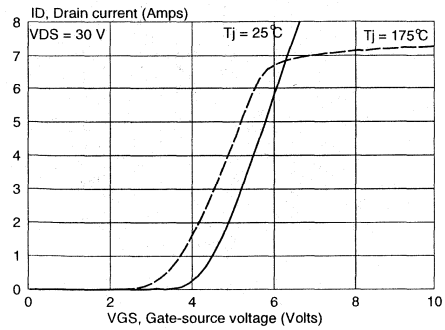


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; parameter T_j

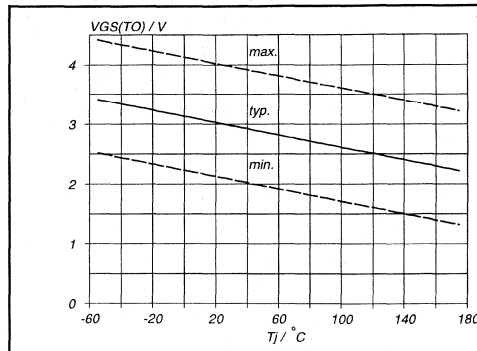


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: $I_D = 0.25$ mA; $V_{DS} = V_{GS}$

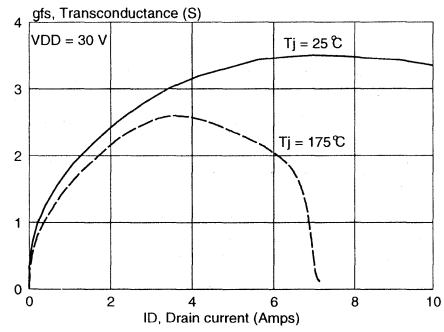


Fig.8. Typical transconductance. $g_{fs} = f(I_D)$; parameter T_j

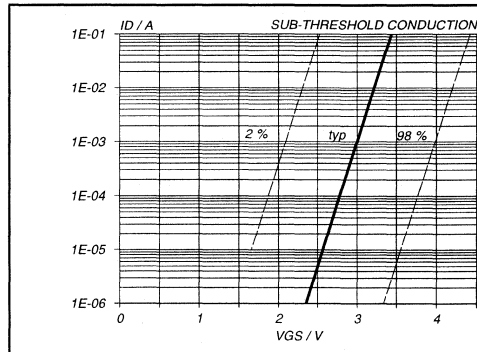


Fig.11. Sub-threshold drain current. $I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

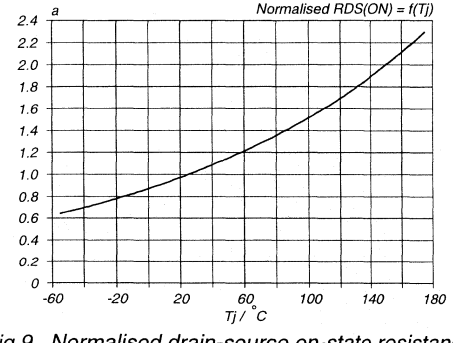


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 5.6$ A; $V_{GS} = 5$ V

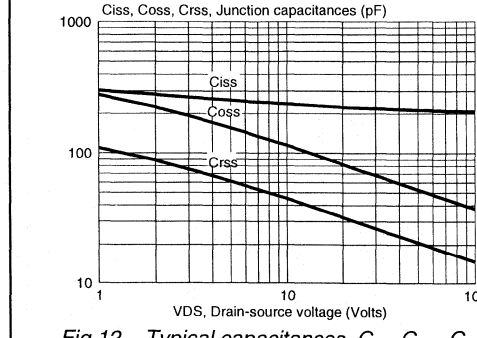


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

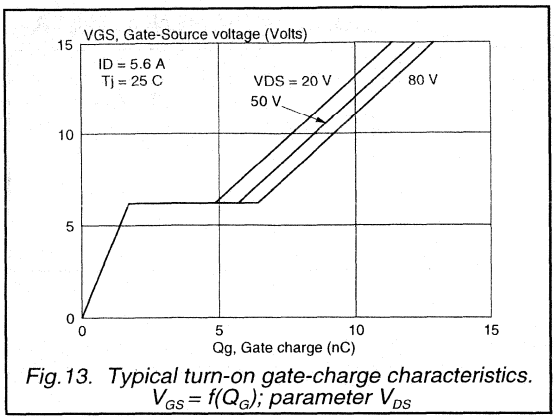


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; *parameter* V_{DS}

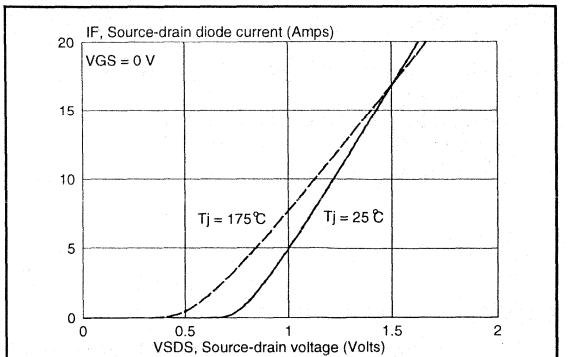


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; *parameter* T_j

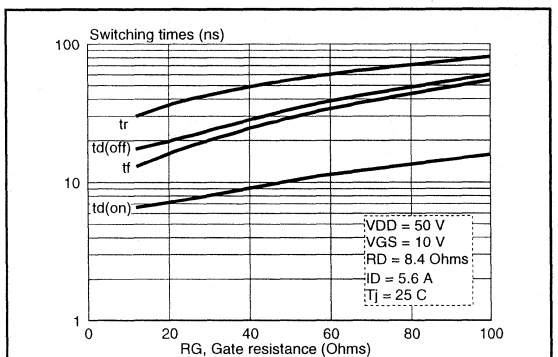


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

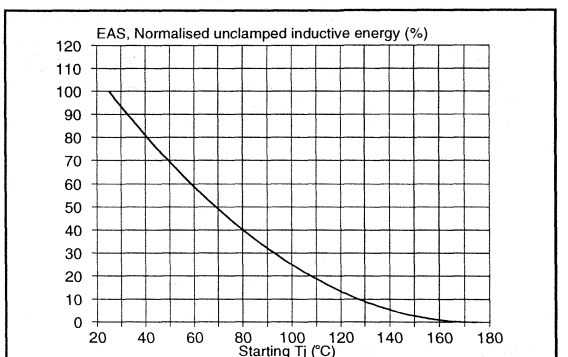


Fig.17. Normalised unclamped inductive energy.
$E_{AS}\% = f(T_j)$

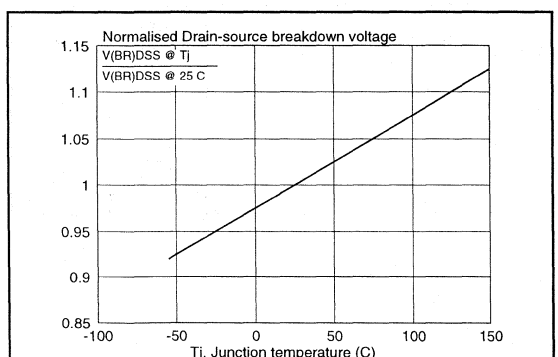


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

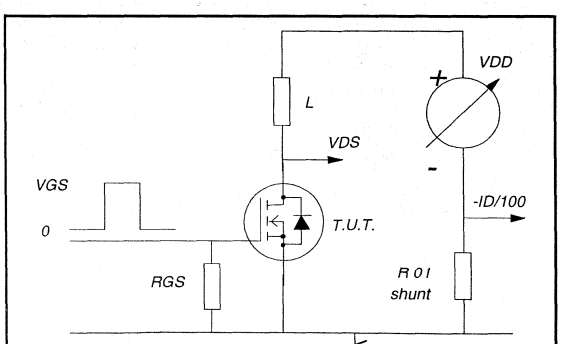


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot V_{(BR)DSS}/(V_{(BR)DSS} - V_{DD})$$

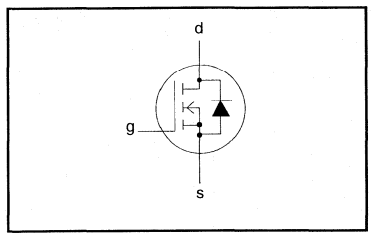
PowerMOS transistors Avalanche energy rated

PHP6N50E, PHB6N50E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 500 V

I_D = 5.9 A

$R_{DS(ON)} \leq 1.5\ \Omega$

GENERAL DESCRIPTION

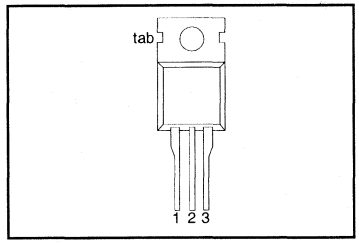
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHP6N50E is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHB6N50E is supplied in the SOT404 surface mounting package.

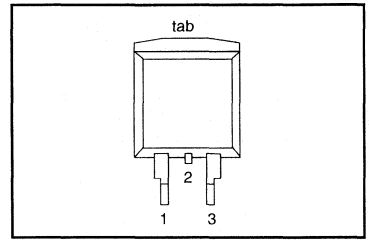
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

SOT78 (TO220AB)



SOT404



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	500	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	500	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	5.9	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	3.7	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	24	A
P_D	Total dissipation	T_{mb} = 25 °C	-	125	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

1 It is not possible to make connection to pin 2 of the SOT404 package.

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 4.5 A; $V_{DD} \leq 50$ V; starting T_j = 25˚C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	280	mJ
E_{AR}	Repetitive avalanche energy[2]		-	7.4	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	4.5	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1	K/W
$R_{th\ j\text{-}a$	Thermal resistance junction to ambient	SOT78 package, in free air	-	60	-	K/W
		SOT404 package, pcb mounted, minimum footprint	-	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	500	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 3 A	-	1.2	1.5	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 3 A	2	3.6	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 500 V; V_{GS} = 0 V	-	1	25	µA
		V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 ˚C	-	30	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 6 A; V_{DD} = 400 V; V_{GS} = 10 V	-	53	64	nC
Q_{gs}	Gate-source charge		-	4	6	nC
Q_{gd}	Gate-drain (Miller) charge		-	28	34	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 250 V; R_D = 39 Ω;	-	10	-	ns
t_r	Turn-on rise time	R_G = 12 Ω	-	33	-	ns
$t_{d(off)}$	Turn-off delay time		-	92	-	ns
t_f	Turn-off fall time		-	40	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	610	-	pF
C_{oss}	Output capacitance		-	96	-	pF
C_{rss}	Feedback capacitance		-	54	-	pF

2 pulse width and repetition rate limited by T_j max.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	5.9	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	24	A
V_{SD}	Diode forward voltage	I_S = 6 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 6 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	390	-	ns
Q_{rr}	Reverse recovery charge		-	4	-	µC

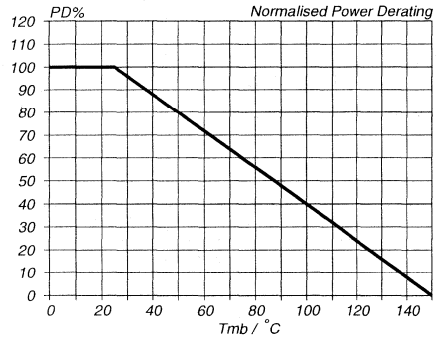


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

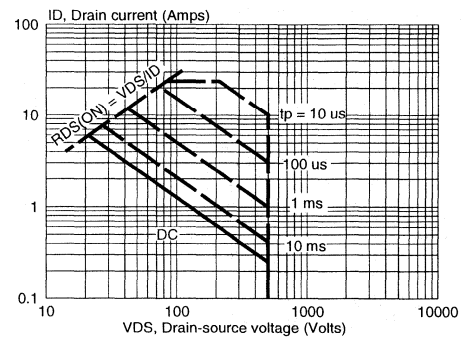


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

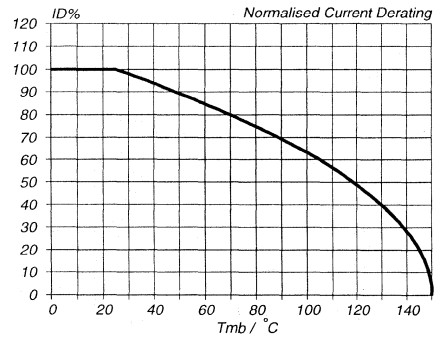


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

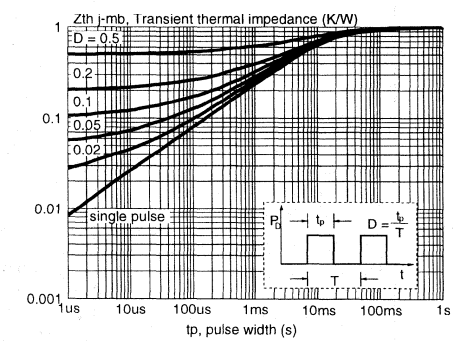


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

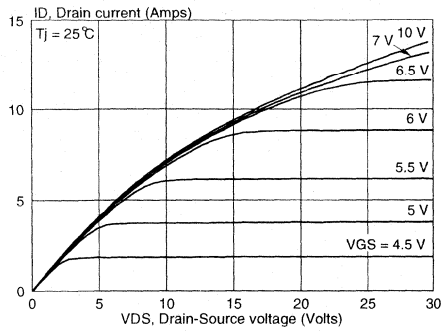


Fig.5. Typical output characteristics. $I_D = f(V_{DS})$; parameter V_{GS}

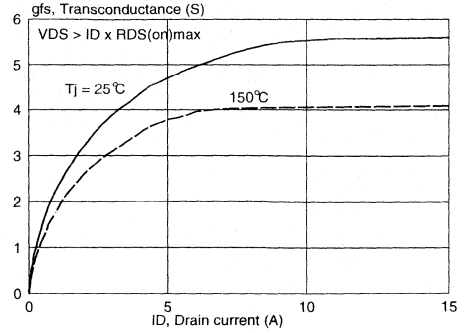


Fig.8. Typical transconductance. $g_{fs} = f(I_D)$; parameter T_j

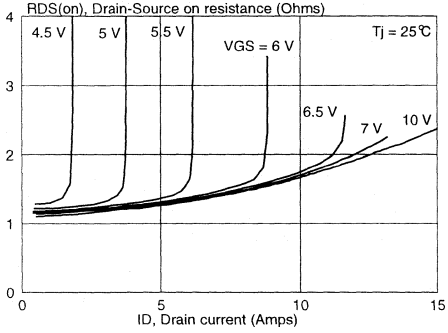


Fig.6. Typical on-state resistance. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

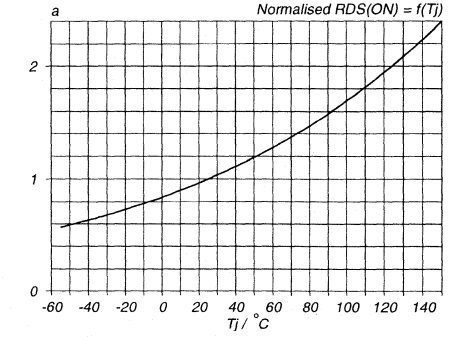


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 3 A; V_{GS} = 10 V

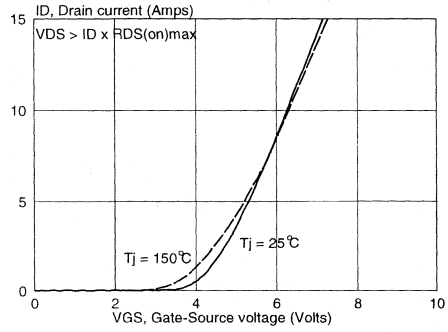


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; parameter T_j

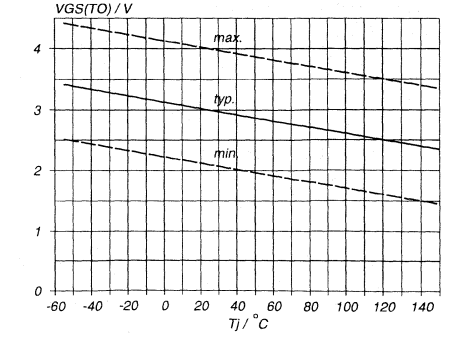


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

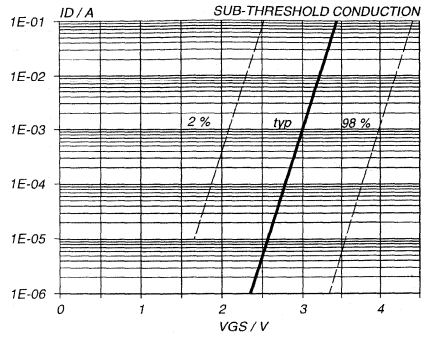


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

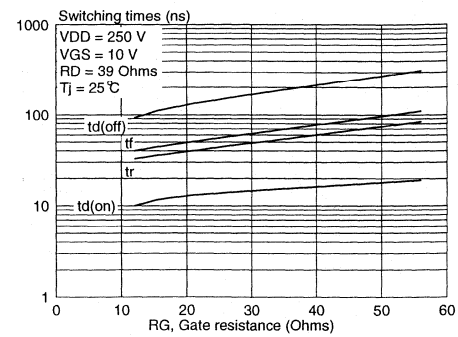


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

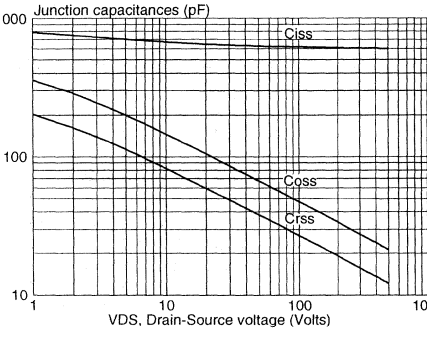


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

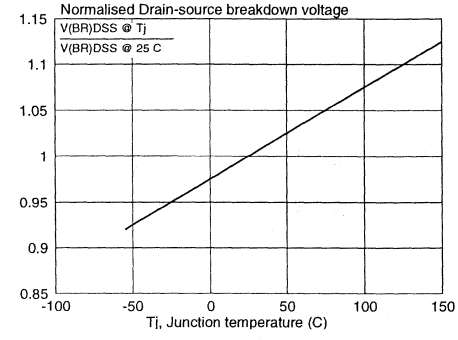


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

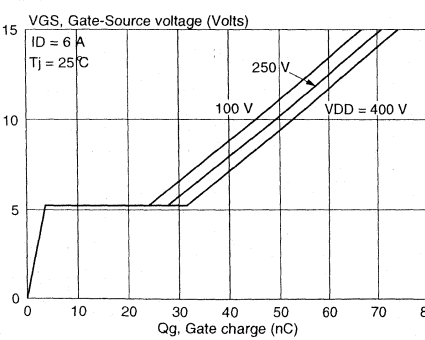


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

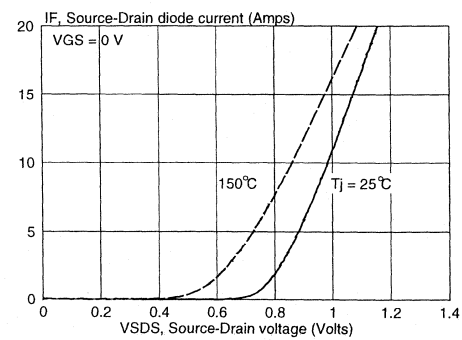


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

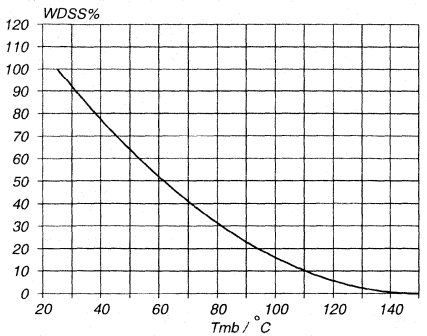


Fig.17. Normalised non-repetitive avalanche energy rating.
$E_{AS}\% = f(T_{mb})$

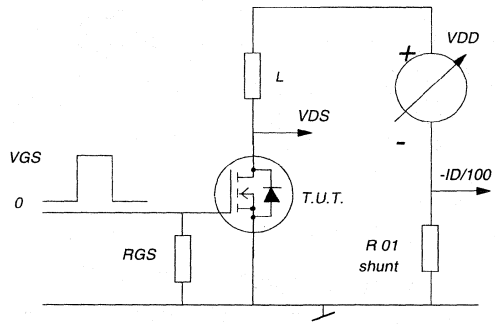


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot \frac{V_{(BR)DSS}}{(V_{(BR)DSS} - V_{DD})}$$

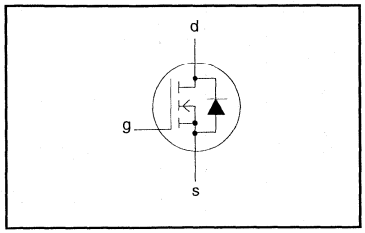
PowerMOS transistors FREDFET, Avalanche energy rated

PHP6ND50E, PHB6ND50E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance
- Fast reverse recovery diode

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 500 V

I_D = 5.9 A

$R_{DS(ON)} \leq 1.5\ \Omega$

t_{rr} = 180 ns

GENERAL DESCRIPTION

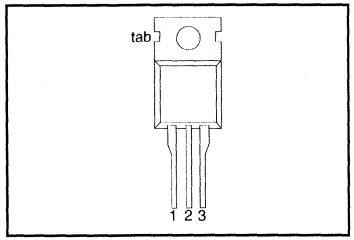
N-channel, enhancement mode field-effect power transistor, incorporating a **F**ast **R**ecovery **E**pitaxial **D**iode (FRED). This gives improved switching performance in half bridge and full bridge converters making this device particularly suitable for inverters, lighting ballasts and motor control circuits.

The PHP6ND50E is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHB6ND50E is supplied in the SOT404 surface mounting package.

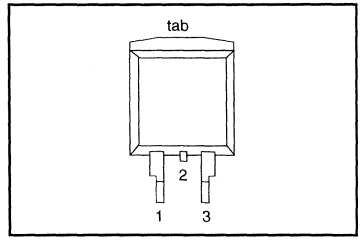
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

SOT78 (TO220AB)



SOT404



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	500	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	500	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	5.9	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	3.7	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	24	A
P_D	Total dissipation	T_{mb} = 25 °C	-	125	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

1 It is not possible to make connection to pin 2 of the SOT404 package.

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 4.5 A; $V_{DD} \leq 50$ V; starting T_j = 25˚C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	280	mJ
E_{AR}	Repetitive avalanche energy[2]		-	7.4	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	4.5	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1	K/W
$R_{th\ j\text{-}a$	Thermal resistance junction to ambient	SOT78 package, in free air	-	60	-	K/W
		SOT404 package, pcb mounted, minimum footprint	-	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	500	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 3 A	-	1.2	1.5	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 3 A	2	3.6	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 500 V; V_{GS} = 0 V	-	1	25	µA
		V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 ˚C	-	30	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 6 A; V_{DD} = 400 V; V_{GS} = 10 V	-	53	64	nC
Q_{gs}	Gate-source charge		-	4	6	nC
Q_{gd}	Gate-drain (Miller) charge		-	28	34	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 250 V; R_D = 39 Ω;	-	10	-	ns
t_r	Turn-on rise time	R_G = 12 Ω	-	33	-	ns
$t_{d(off)}$	Turn-off delay time		-	92	-	ns
t_f	Turn-off fall time		-	40	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	610	-	pF
C_{oss}	Output capacitance		-	96	-	pF
C_{rss}	Feedback capacitance		-	54	-	pF

[2] pulse width and repetition rate limited by T_j max.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	5.9	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	24	A
V_{SD}	Diode forward voltage	I_S = 6 A; V_{GS} = 0 V	-	-	1.5	V
t_{rr}	Reverse recovery time	I_S = 6 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	180	-	ns
		I_S = 6 A; V_{GS} = 0 V; dI/dt = 100 A/µs; 125°C	-	220	-	ns
Q_{rr}	Reverse recovery charge	I_S = 6 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	0.65	-	µC
		I_S = 6 A; V_{GS} = 0 V; dI/dt = 100 A/µs; 125°C	-	2.6	-	µC
I_{rrm}	Peak reverse recovery current	I_S = 6 A; V_{GS} = 0 V; dI/dt = 100 A/µs; 125°C	-	15	-	A

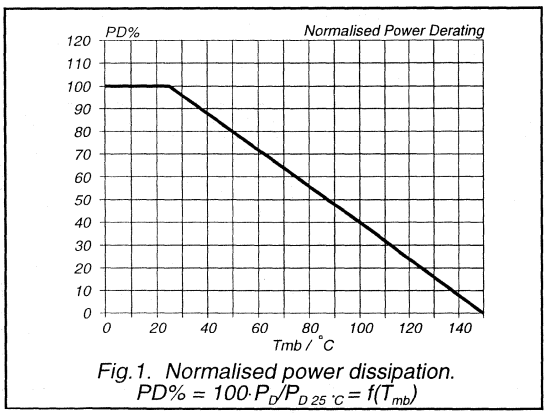


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

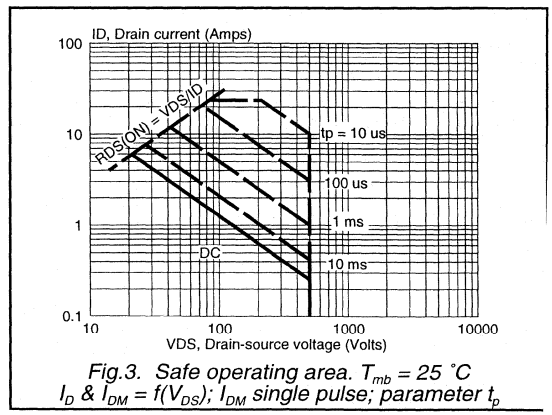


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

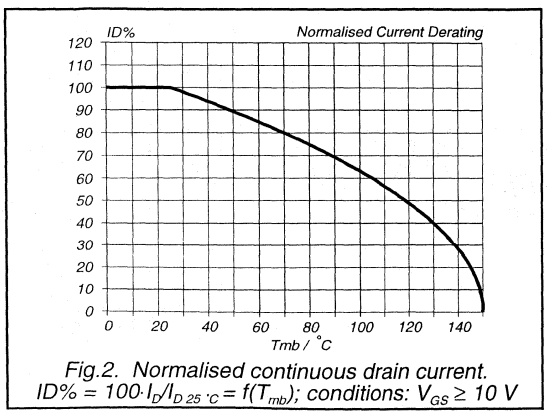


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

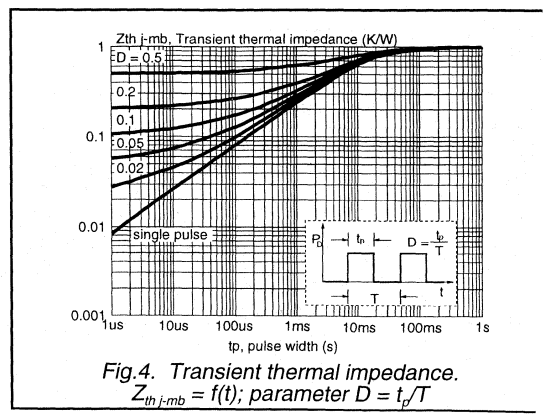


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

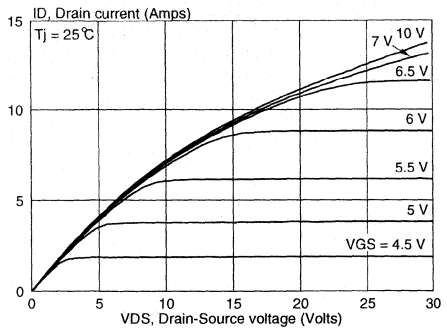


Fig.5. Typical output characteristics.
$I_D = f(V_{DS})$; parameter V_{GS}

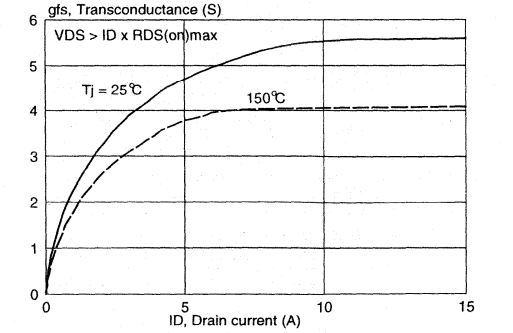


Fig.8. Typical transconductance.
$g_{fs} = f(I_D)$; parameter T_j

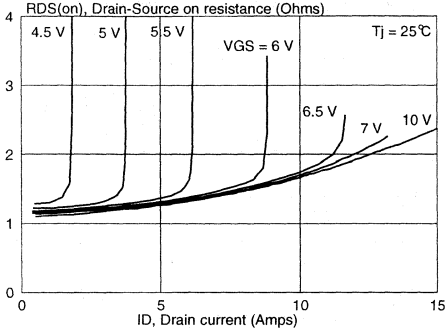


Fig.6. Typical on-state resistance.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

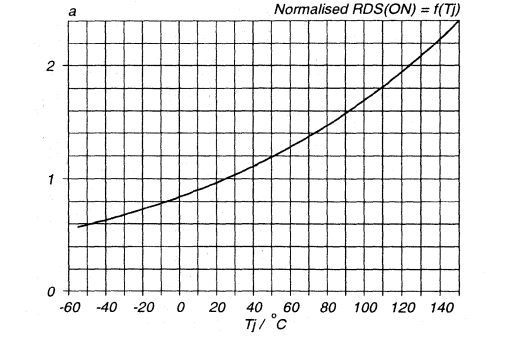


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 3 A; V_{GS} = 10 V

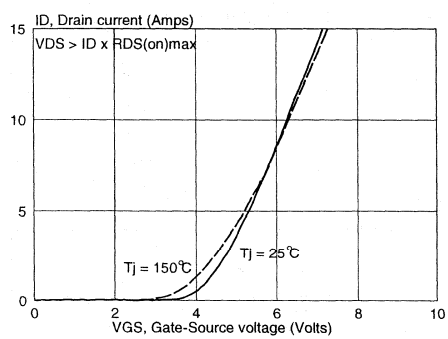


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

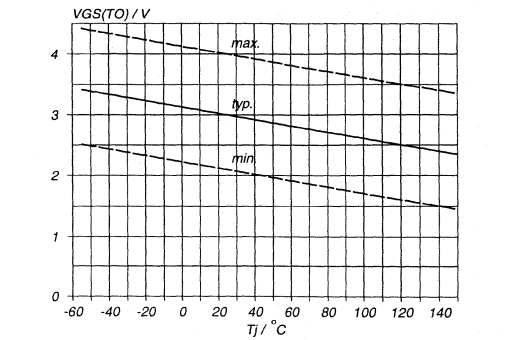


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

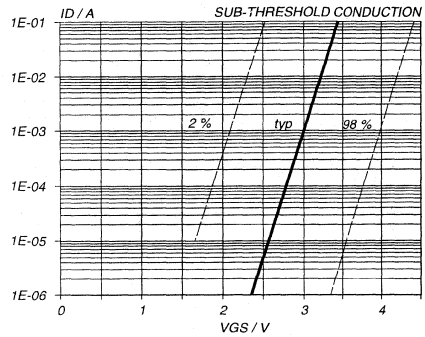


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

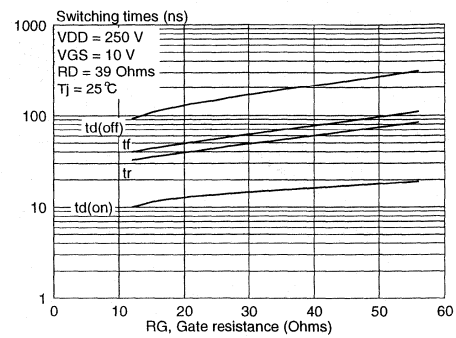


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

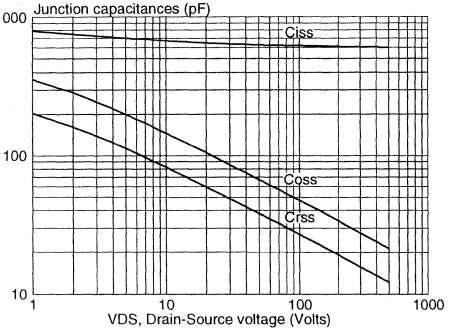


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

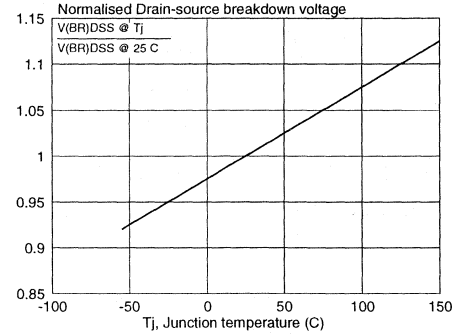


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

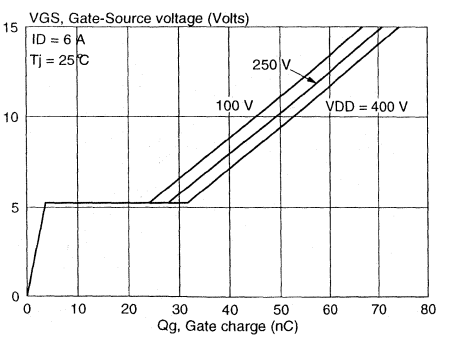


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

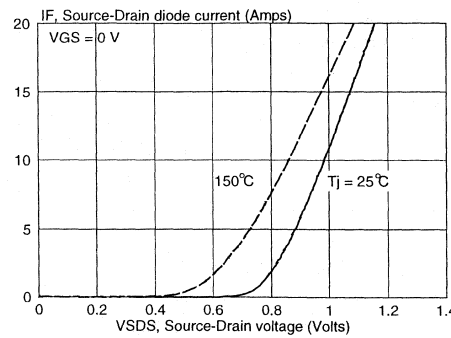


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

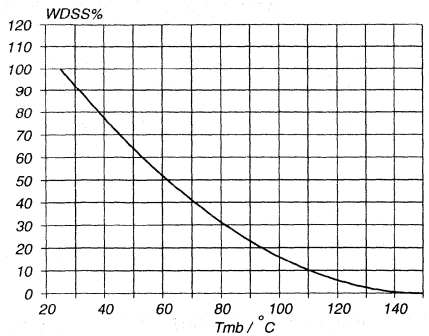


Fig.17. Normalised non-repetitive avalanche energy rating.
$E_{AS}\% = f(T_{mb})$

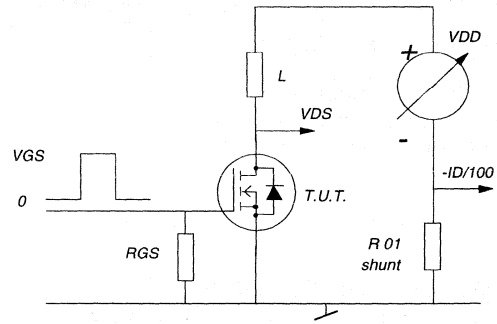


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot \frac{V_{(BR)DSS}}{(V_{(BR)DSS} - V_{DD})}$$

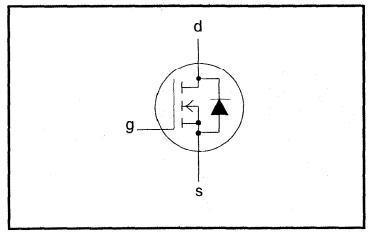
PowerMOS transistors
Avalanche energy rated

PHP6N60E, PHB6N60E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 600 V

I_D = 5.4 A

$R_{DS(ON)} \leq 1.8\ \Omega$

GENERAL DESCRIPTION

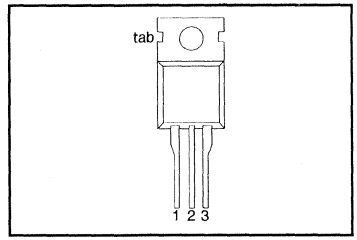
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHP6N60E is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHB6N60E is supplied in the SOT404 surface mounting package.

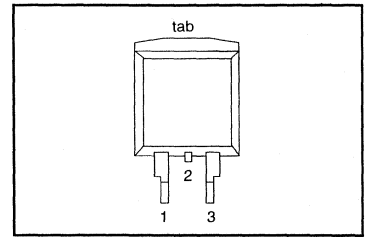
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

SOT78 (TO220AB)



SOT404



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	600	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	600	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	5.4	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	3.4	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	21	A
P_D	Total dissipation	T_{mb} = 25 °C	-	125	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

1 It is not possible to make connection to pin 2 of the SOT404 package.

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 5.4 A; $V_{DD} \leq 50$ V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	420	mJ
E_{AR}	Repetitive avalanche energy[2]		-	10	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	5.4	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	SOT78 package, in free air	-	60	-	K/W
		SOT404 package, pcb mounted, minimum footprint	-	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	600	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 2.7 A	-	1.5	1.8	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 2.7 A	2	3.4	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 600 V; V_{GS} = 0 V	-	2	100	µA
		V_{DS} = 480 V; V_{GS} = 0 V; T_j = 125 °C	-	50	500	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 5.4 A; V_{DD} = 480 V; V_{GS} = 10 V	-	50	65	nC
Q_{gs}	Gate-source charge		-	5	8	nC
Q_{gd}	Gate-drain (Miller) charge		-	26	35	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V; R_D = 56 Ω;	-	15	-	ns
t_r	Turn-on rise time	R_G = 12 Ω	-	35	-	ns
$t_{d(off)}$	Turn-off delay time		-	90	-	ns
t_f	Turn-off fall time		-	40	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	650	-	pF
C_{oss}	Output capacitance		-	85	-	pF
C_{rss}	Feedback capacitance		-	50	-	pF

? pulse width and repetition rate limited by T_j max.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	5.4	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	21	A
V_{SD}	Diode forward voltage	I_S = 5.4 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 5.4 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	480	-	ns
Q_{rr}	Reverse recovery charge		-	4	-	µC

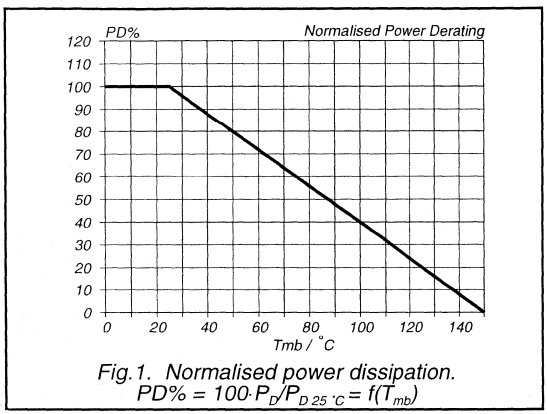


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

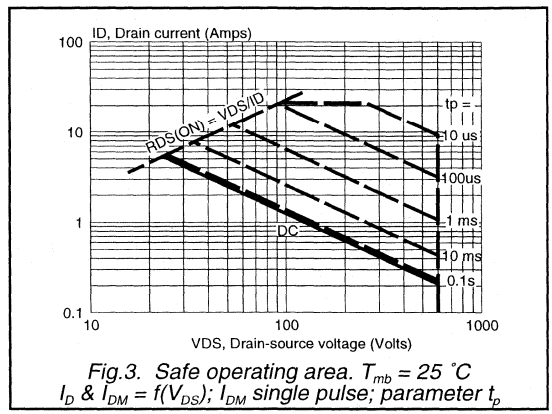


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

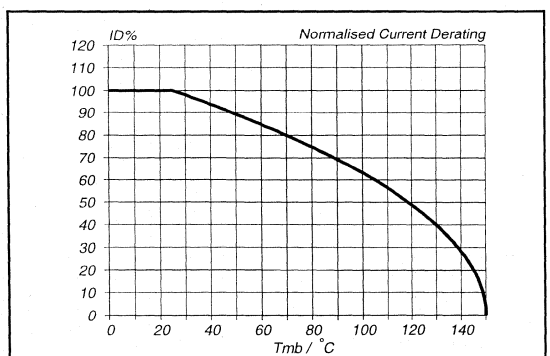


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 10 V

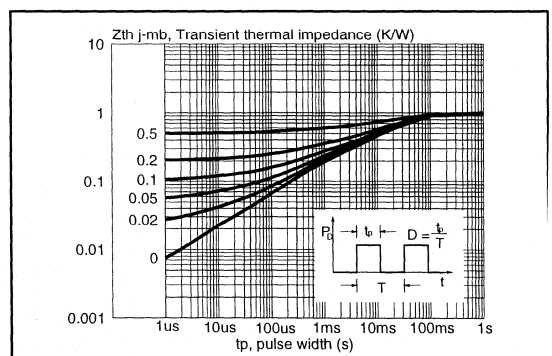


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

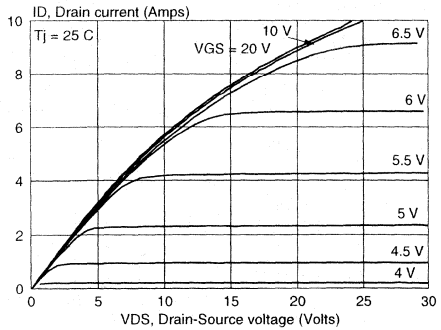


Fig.5. Typical output characteristics. $I_D = f(V_{DS})$; parameter V_{GS}

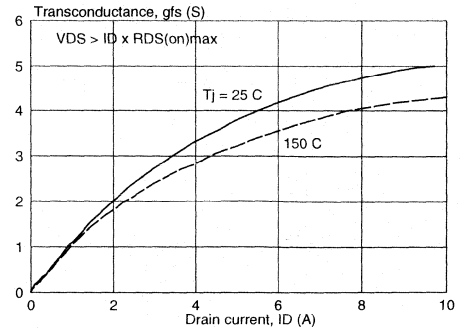


Fig.8. Typical transconductance. $g_{fs} = f(I_D)$; parameter T_j

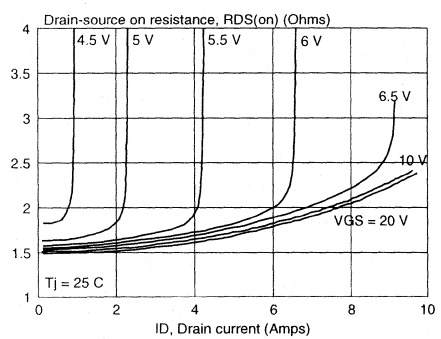


Fig.6. Typical on-state resistance. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

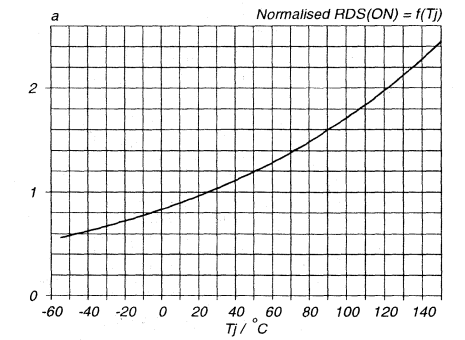


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 2.7$ A; $V_{GS} = 10$ V

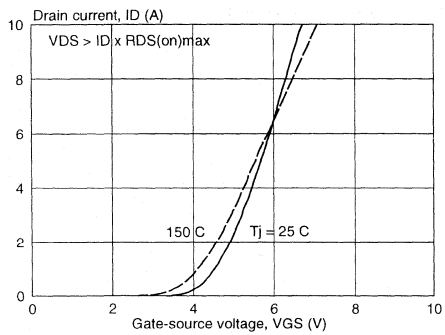


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; parameter T_j

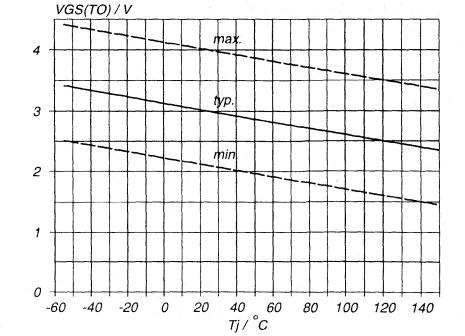


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: $I_D = 0.25$ mA; $V_{DS} = V_{GS}$

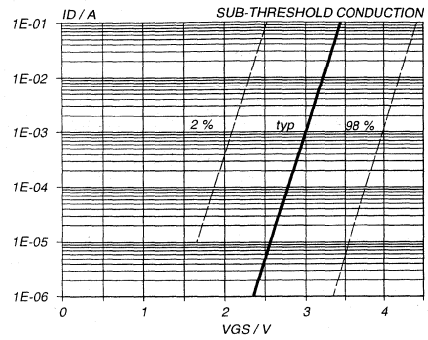


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

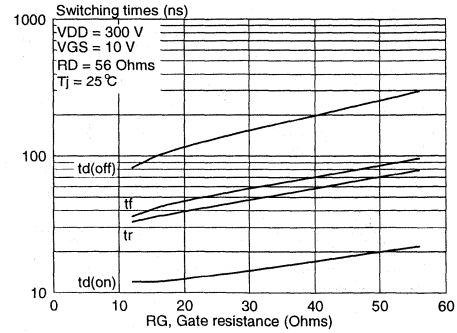


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

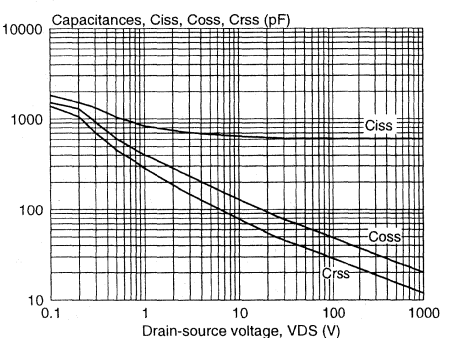


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

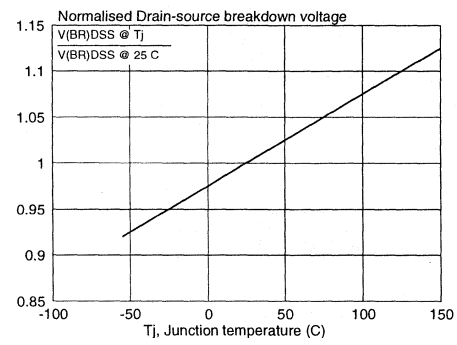


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

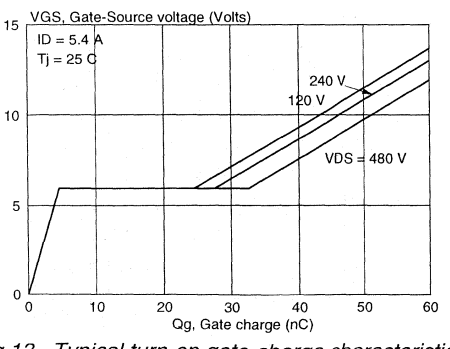


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

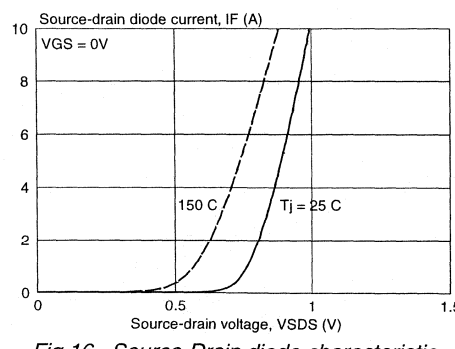


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

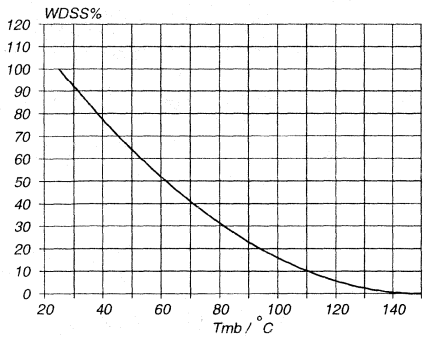


Fig.17. Normalised non-repetitive avalanche energy rating.
$E_{AS}\% = f(T_{mb})$

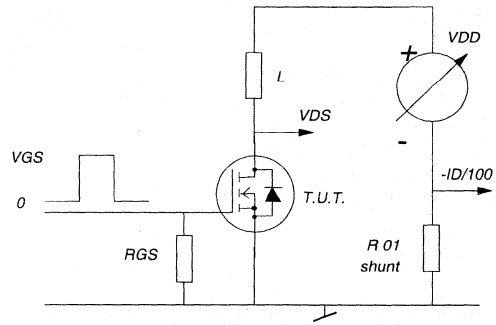


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot \frac{V_{(BR)DSS}}{(V_{(BR)DSS} - V_{DD})}$$

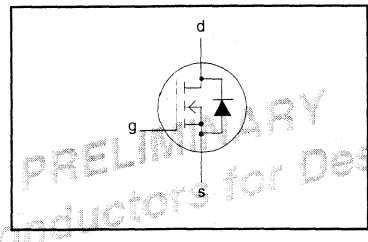
PowerMOS transistors
Low capacitance
Avalanche energy rated

PHP6NA60E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Low feedback capacitance
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 600 V

I_D = 6.5 A

$R_{DS(ON)} \leq 1.2\ \Omega$

PRELIMINARY
Philips Semiconductors for Design-in Information

GENERAL DESCRIPTION

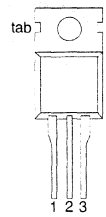
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHP6NA60E is supplied in the SOT78 (TO220AB) conventional leaded package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

SOT78 (TO220AB)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	600	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	600	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	6.5	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	4.3	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	26	A
P_D	Total dissipation	T_{mb} = 25 °C	-	125	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 6.5 A; $V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	570	mJ
E_{AR}	Repetitive avalanche energy[1]		-	9.5	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	6.5	A

1 pulse width and repetition rate limited by T_j max.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	600	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 3.25 A	-	-	1.2	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 3.25 A	3	4.5	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 600 V; V_{GS} = 0 V	-	2	100	μA
		V_{DS} = 480 V; V_{GS} = 0 V; T_j = 125 °C	-	50	500	μA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 3 A; V_{DD} = 480 V; V_{GS} = 10 V	-	-	75	nC
Q_{gs}	Gate-source charge		-	7	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	30	-	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V; R_D = 47 Ω;	-	-	50	ns
t_r	Turn-on rise time	R_G = 9.1 Ω	-	-	125	ns
$t_{d(off)}$	Turn-off delay time		-	-	110	ns
t_f	Turn-off fall time		-	-	30	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	-	1550	pF
C_{oss}	Output capacitance		-	140	-	pF
C_{rss}	Feedback capacitance		-	42	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	6.5	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	26	A
V_{SD}	Diode forward voltage	I_S = 6.5 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 6.5 A; V_{GS} = 0 V; dI/dt = 100 A/μs	-	530	-	ns
Q_{rr}	Reverse recovery charge		-	6.7	-	μC

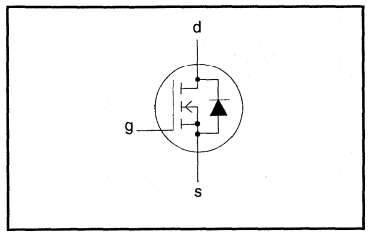
PowerMOS transistors Avalanche energy rated

PHP7N40E, PHB7N40E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 400 V

I_D = 7.2 A

$R_{DS(ON)} \leq 1\ \Omega$

GENERAL DESCRIPTION

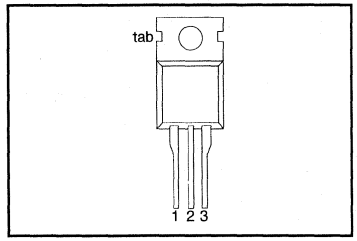
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHP7N40E is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHB7N40E is supplied in the SOT404 surface mounting package.

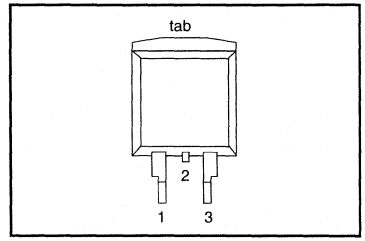
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

SOT78 (TO220AB)



SOT404



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	400	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	400	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	7.2	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	4.6	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	29	A
P_D	Total dissipation	T_{mb} = 25 °C	-	125	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

1 It is not possible to make connection to pin 2 of the SOT404 package.

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 5.5 A; $V_{DD} \leq 50$ V; starting T_j = 25˚C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	290	mJ
E_{AR}	Repetitive avalanche energy[2]		-	7.4	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	5.5	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	SOT78 package, in free air	-	60	-	K/W
		SOT404 package, pcb mounted, minimum footprint	-	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	400	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 3.6 A	-	0.7	1	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 3.6 A	2	4	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 400 V; V_{GS} = 0 V	-	1	25	µA
		V_{DS} = 320 V; V_{GS} = 0 V; T_j = 125 °C	-	30	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 7.2 A; V_{DD} = 320 V; V_{GS} = 10 V	-	52	62	nC
Q_{gs}	Gate-source charge		-	3	5	nC
Q_{gd}	Gate-drain (Miller) charge		-	26	30	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 200 V; R_D = 27 Ω;	-	12	-	ns
t_r	Turn-on rise time	R_G = 12 Ω	-	33	-	ns
$t_{d(off)}$	Turn-off delay time		-	93	-	ns
t_f	Turn-off fall time		-	42	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	620	-	pF
C_{oss}	Output capacitance		-	108	-	pF
C_{rss}	Feedback capacitance		-	63	-	pF

! pulse width and repetition rate limited by T_j max.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	7.2	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	29	A
V_{SD}	Diode forward voltage	I_S = 7.2 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 7.2 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	270	-	ns
Q_{rr}	Reverse recovery charge		-	3.3	-	µC

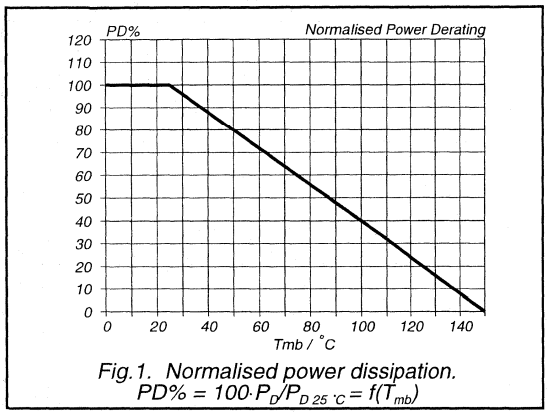


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

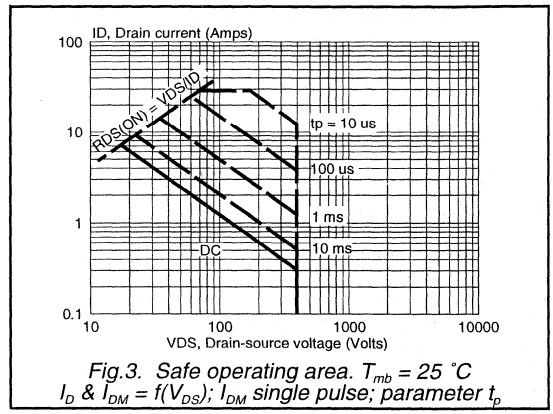


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

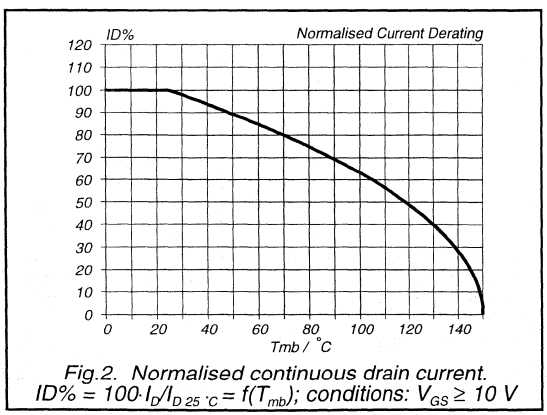


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

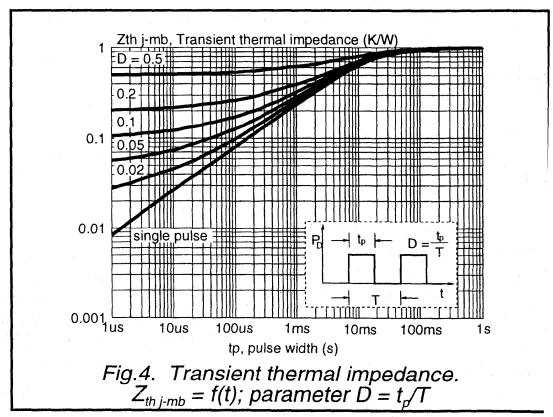


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

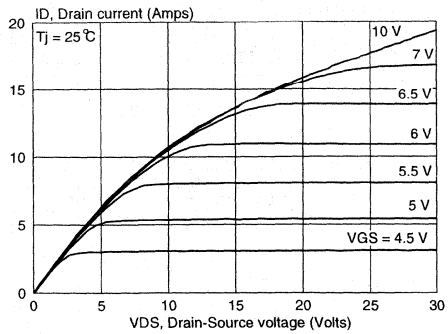


Fig.5. Typical output characteristics.
$I_D = f(V_{DS})$; parameter V_{GS}

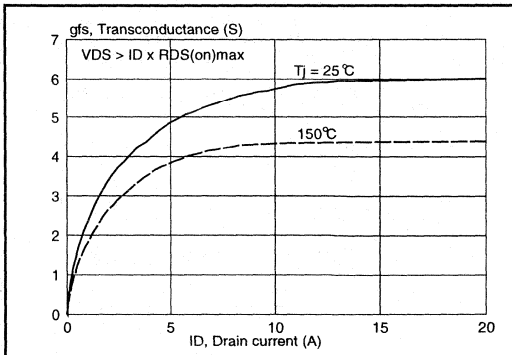


Fig.8. Typical transconductance.
$g_{fs} = f(I_D)$; parameter T_j

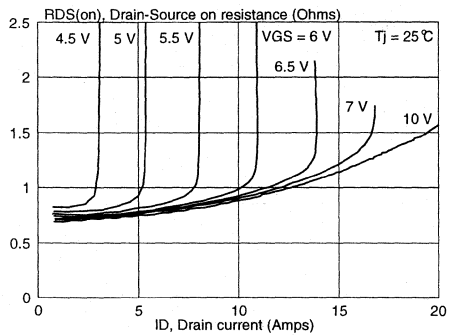


Fig.6. Typical on-state resistance.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

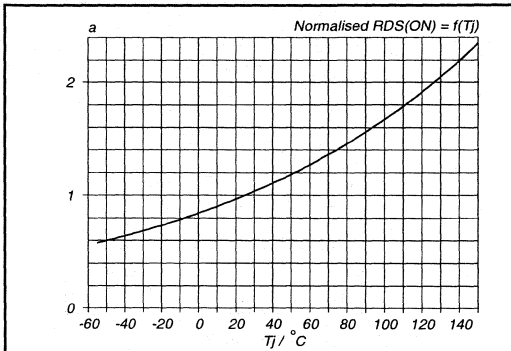


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 3.6 A; V_{GS} = 10 V

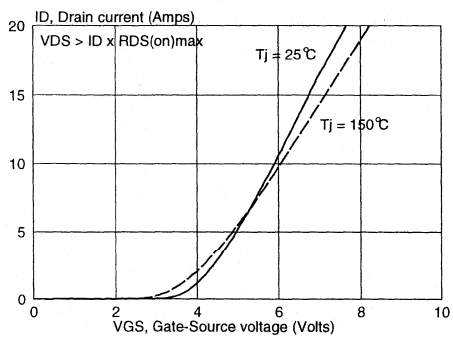


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

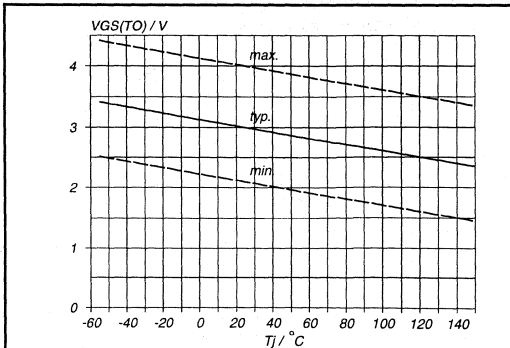


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

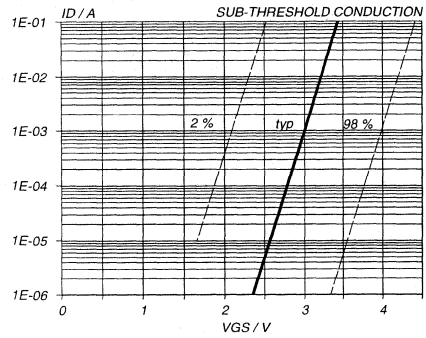


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

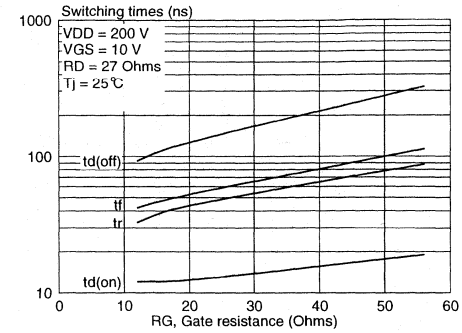


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

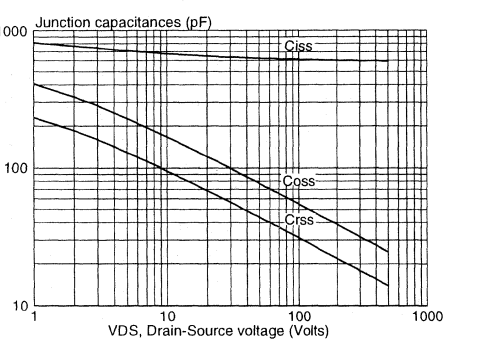


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

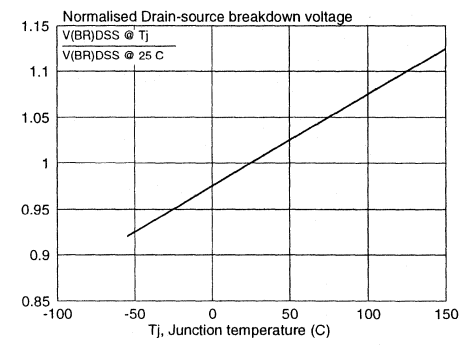


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

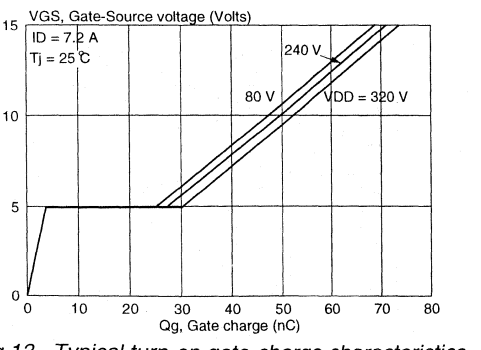


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

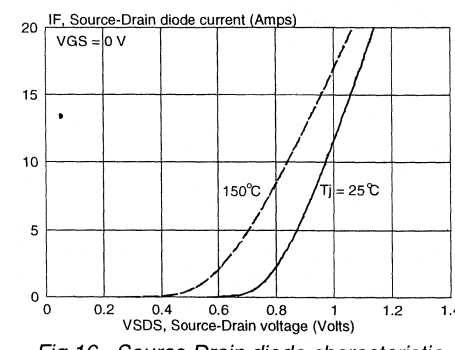


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

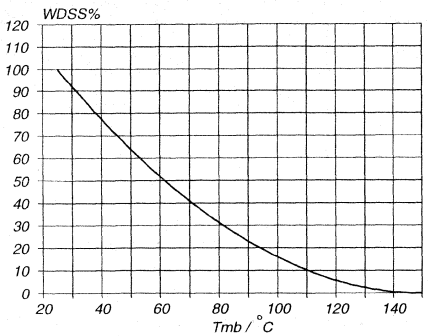


Fig.17. Normalised non-repetitive avalanche energy rating.
$E_{AS}\% = f(T_{mb})$

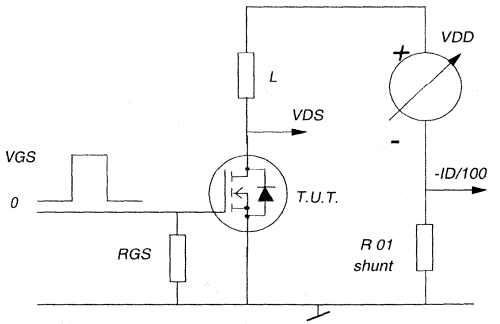


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot \frac{V_{(BR)DSS}}{(V_{(BR)DSS} - V_{DD})}$$

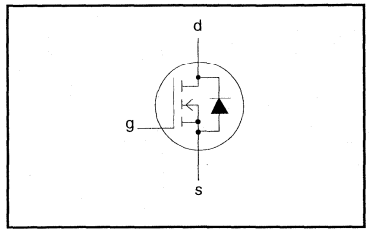
PowerMOS transistors Avalanche energy rated

PHP7N60E, PHB7N60E, PHW7N60E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 600 V

I_D = 7 A

$R_{DS(ON)} \leq 1.2\ \Omega$

GENERAL DESCRIPTION

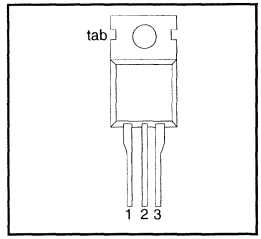
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHP7N60E is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHW7N60E is supplied in the SOT429 (TO247) conventional leaded package.
The PHB7N60E is supplied in the SOT404 surface mounting package.

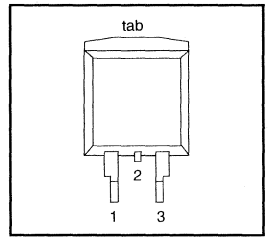
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

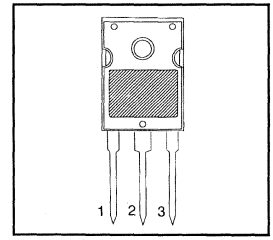
SOT78 (TO220AB)



SOT404



SOT429 (TO247)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	600	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	600	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	7	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	4.5	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	28	A
P_D	Total dissipation	T_{mb} = 25 °C	-	147	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

1 It is not possible to make connection to pin 2 of the SOT404 package.

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 6.2 A; $V_{DD} \leq 50$ V; starting $T_j = 25^{\circ}C$; $R_{GS} = 50\ \Omega$; $V_{GS} = 10$ V	-	570	mJ
E_{AR}	Repetitive avalanche energy[2]		-	13	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	6.2	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	0.85	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	SOT78 package, in free air	-	60	-	K/W
		SOT429 package, in free air	-	45	-	K/W
		SOT404 package, pcb mounted, minimum footprint	-	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	600	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	$V_{DS} = V_{GS}$; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 3.5 A	-	0.9	1.2	Ω
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 3.5 A	3	4.5	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 600 V; V_{GS} = 0 V	-	2	100	µA
		V_{DS} = 480 V; V_{GS} = 0 V; T_j = 125 °C	-	50	500	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 7 A; V_{DD} = 480 V; V_{GS} = 10 V	-	90	110	nC
Q_{gs}	Gate-source charge		-	6	7	nC
Q_{gd}	Gate-drain (Miller) charge		-	44	60	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V; $R_D = 39\ \Omega$;	-	17	-	ns
t_r	Turn-on rise time	$R_G = 9.1\ \Omega$	-	43	-	ns
$t_{d(off)}$	Turn-off delay time		-	118	-	ns
t_f	Turn-off fall time		-	50	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 and SOT429 packages only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1100	-	pF
C_{oss}	Output capacitance		-	140	-	pF
C_{rss}	Feedback capacitance		-	80	-	pF

[2] pulse width and repetition rate limited by T_j max.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	7	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	28	A
V_{SD}	Diode forward voltage	I_S = 7 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 7 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	530	-	ns
Q_{rr}	Reverse recovery charge		-	6.7	-	µC

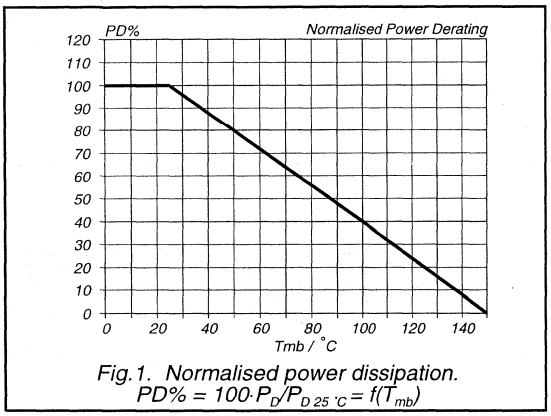


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

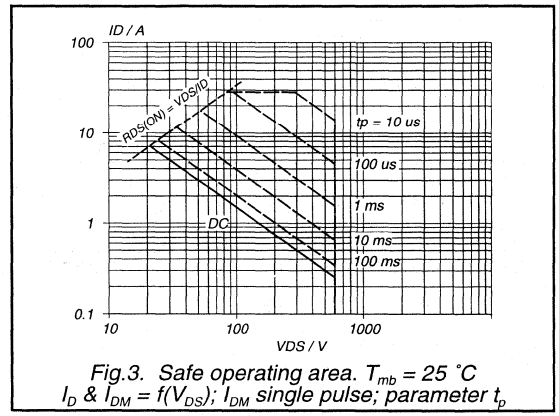


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

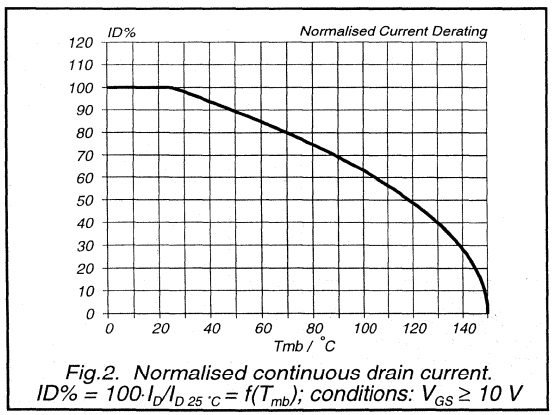


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

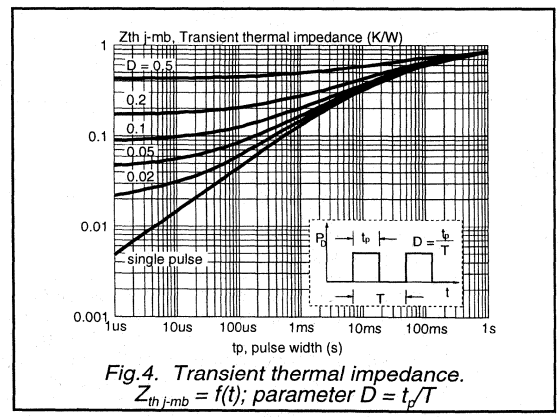


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

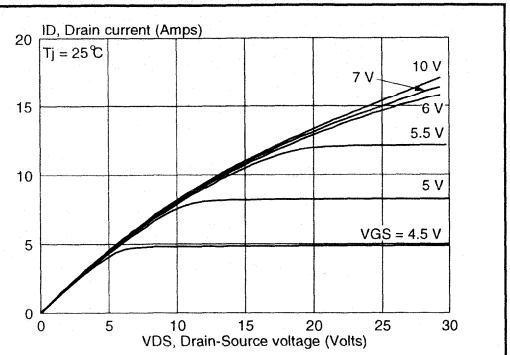


Fig.5. Typical output characteristics. $I_D = f(V_{DS})$; parameter V_{GS}

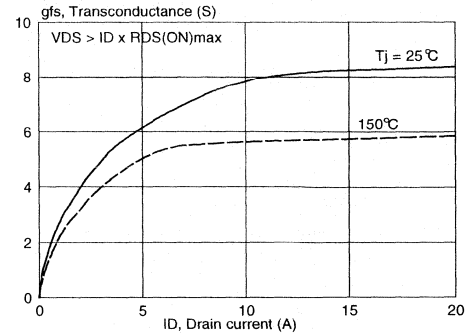


Fig.8. Typical transconductance. $g_{fs} = f(I_D)$; parameter T_j

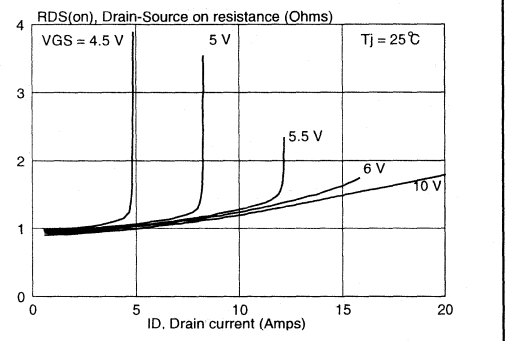


Fig.6. Typical on-state resistance. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

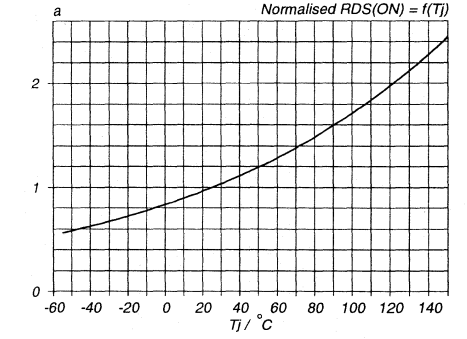


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 3.5$ A; $V_{GS} = 10$ V

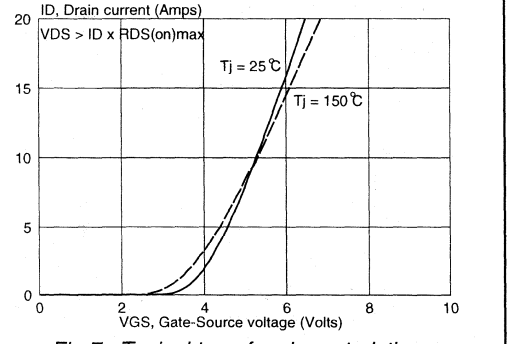


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; parameter T_j

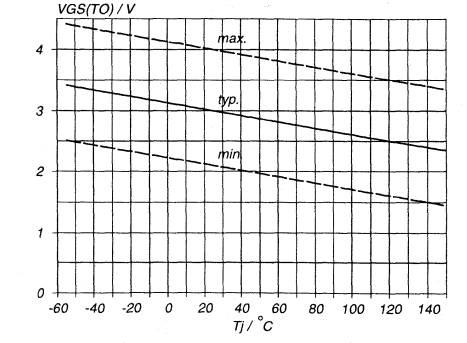


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: $I_D = 0.25$ mA; $V_{DS} = V_{GS}$

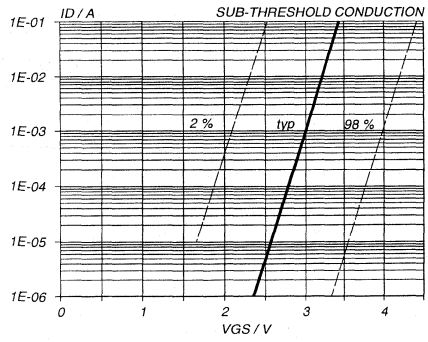


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

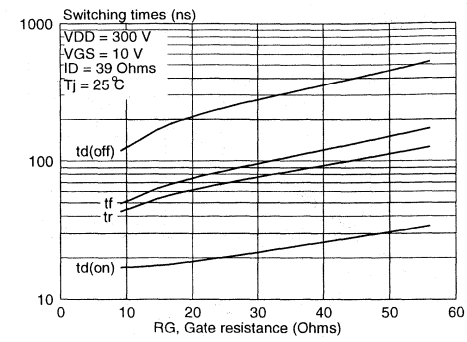


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

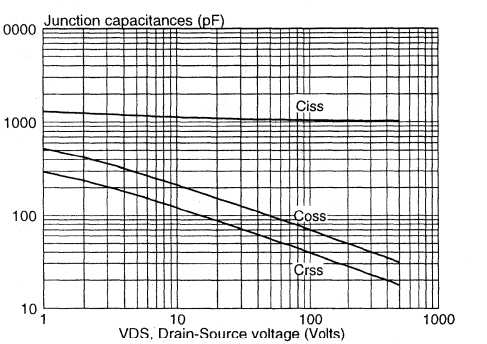


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

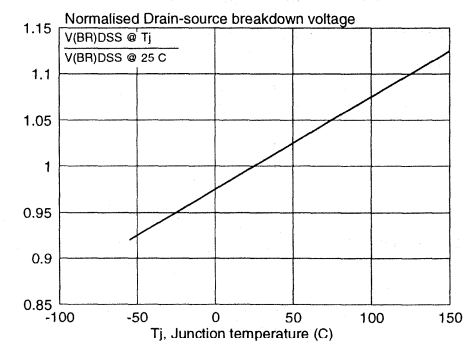


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

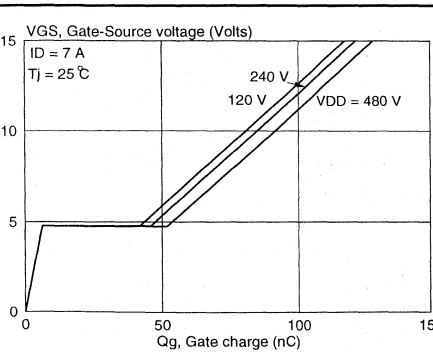


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

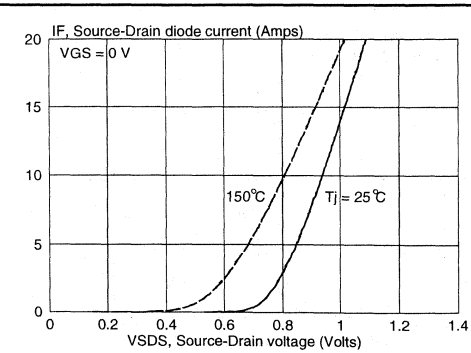


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

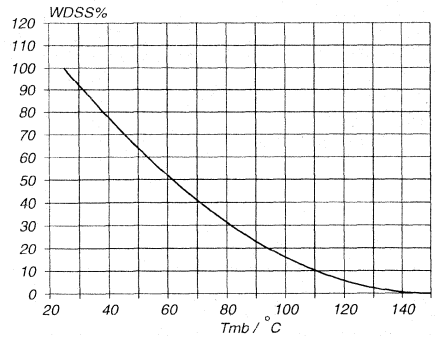


Fig.17. Normalised non-repetitive avalanche energy rating.
$E_{AS}\% = f(T_{mb})$

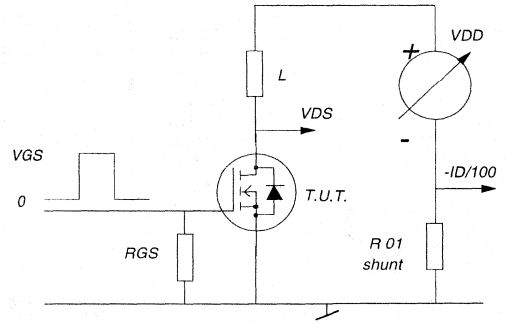


Fig.18. Unclamped inductive load test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot \frac{V_{(BR)DSS}}{(V_{(BR)DSS} - V_{DD})}$$

PowerMOS transistor PHP8N20E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

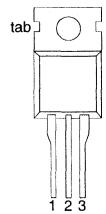
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (DC)	9.2	A
P_{tot}	Total power dissipation	90	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.4	Ω

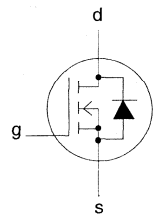
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	9.2	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	6.5	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	37	A
P_D	Total dissipation	T_{mb} = 25 °C	-	90	W
$\Delta P_D/\Delta T_{mb}$	Linear derating factor	T_{mb} > 25 °C	-	0.6	W/K
V_{GS}	Gate-source voltage		-	± 30	V
E_{AS}	Single pulse avalanche energy	$V_{DD} \leq 50$ V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	250	mJ
I_{AS}	Peak avalanche current	$V_{DD} \leq 50$ V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	9.2	A
T_j, T_{stg}	Operating junction and storage temperature range		- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.67	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.25	-	V/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 6.4 A	-	0.35	0.4	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 50 V; I_D = 5.4 A	3.8	4.7	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 200 V; V_{GS} = 0 V	-	1	25	µA
		V_{DS} = 160 V; V_{GS} = 0 V; T_j = 125 °C	-	30	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$Q_{g(tot)}$	Total gate charge	I_D = 5.9 A; V_{DD} = 160 V; V_{GS} = 10 V	-	30	40	nC
Q_{gs}	Gate-source charge		-	4.5	6	nC
Q_{gd}	Gate-drain (Miller) charge		-	15	20	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 100 V; I_D = 5.9 A;	-	12	-	ns
t_r	Turn-on rise time	R_G = 12 Ω; R_D = 16 Ω	-	45	-	ns
$t_{d(off)}$	Turn-off delay time		-	80	-	ns
t_f	Turn-off fall time		-	40	-	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	700	-	pF
C_{oss}	Output capacitance		-	100	-	pF
C_{rss}	Feedback capacitance		-	50	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	9.2	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	37	A
V_{SD}	Diode forward voltage	I_S = 9 A; V_{GS} = 0 V	-	-	1.5	V
t_{rr}	Reverse recovery time	I_S = 5.9 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	180	-	ns
Q_{rr}	Reverse recovery charge		-	1.2	-	µC

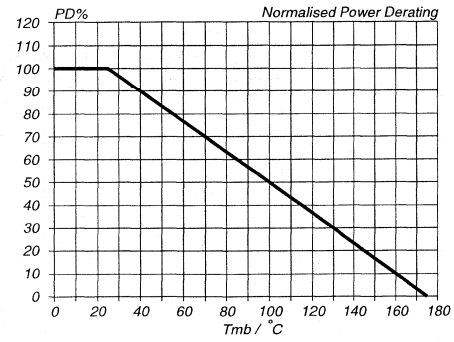


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

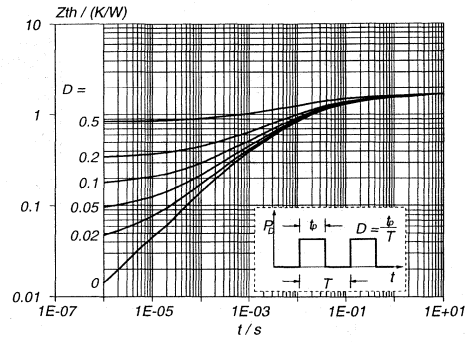


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

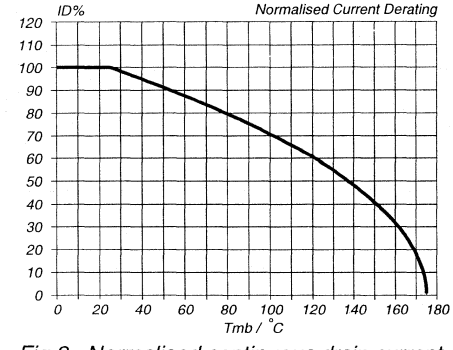


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

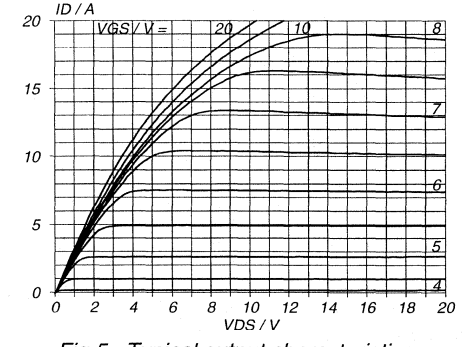


Fig.5. Typical output characteristics.
I_D = f(V_{DS}); parameter V_{GS}

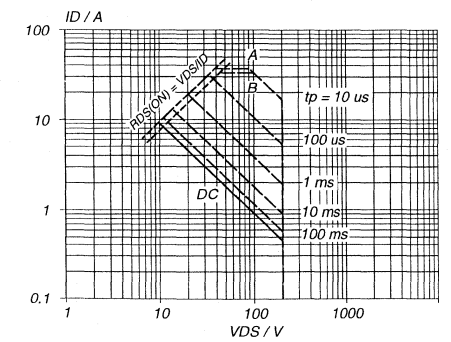


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

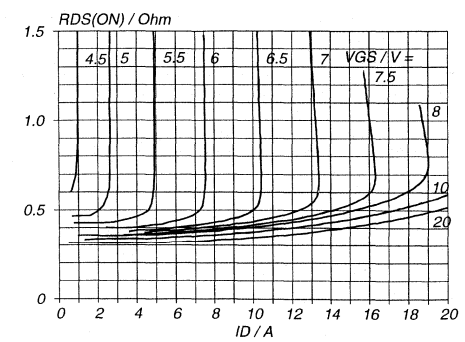


Fig.6. Typical on-state resistance.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

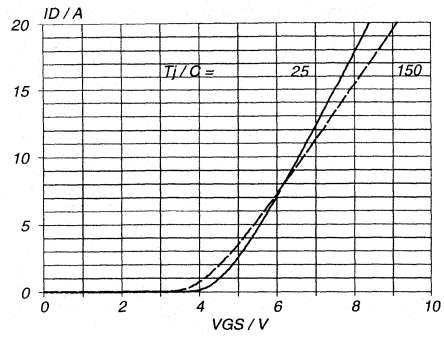


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

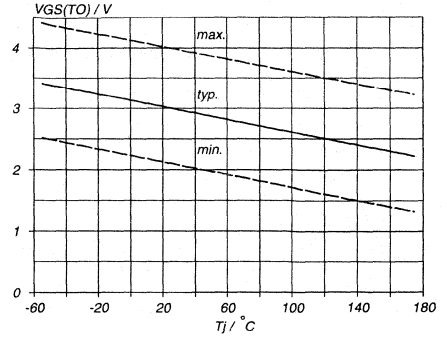


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 0.25$ mA; $V_{DS} = V_{GS}$

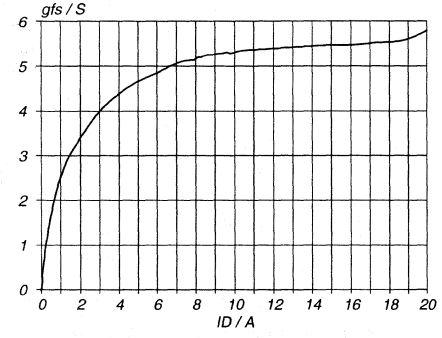


Fig.8. Typical transconductance.
$g_{fs} = f(I_D)$; parameter T_j

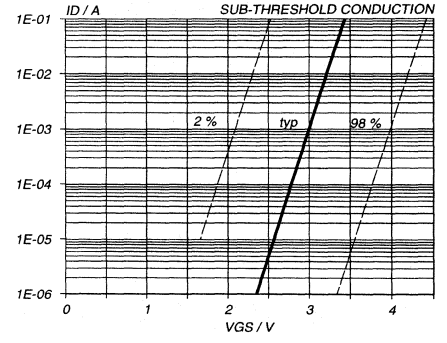


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

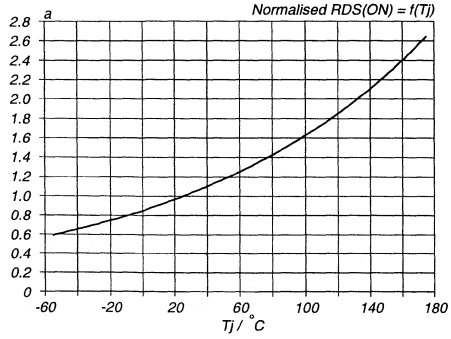


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 5.9$ A; $V_{GS} = 10$ V

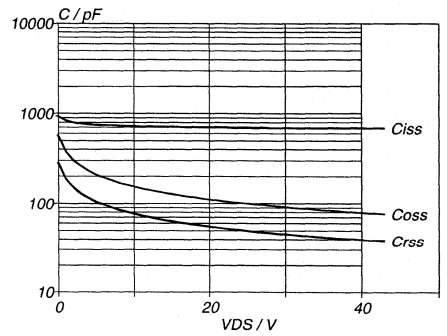


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

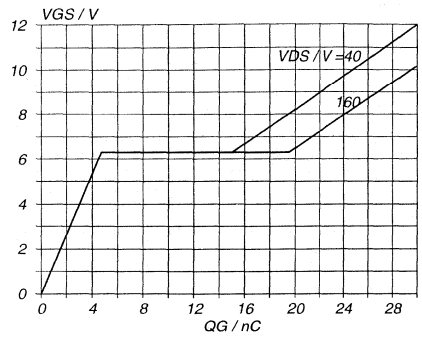


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; parameter V_{DS}

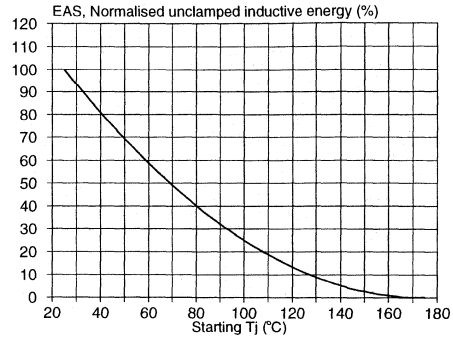


Fig.16. Normalised unclamped inductive energy. $E_{AS}\% = f(T_j)$

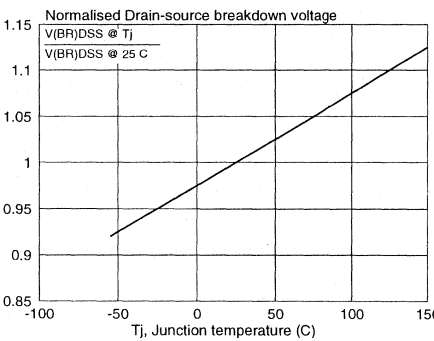


Fig.14. Normalised drain-source breakdown voltage. $V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

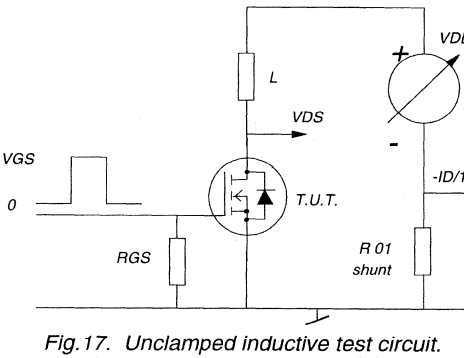


Fig.17. Unclamped inductive test circuit. $E_{AS} = 0.5 \cdot LI_D^2 \cdot V_{(BR)DSS}/(V_{(BR)DSS} - V_{DD})$

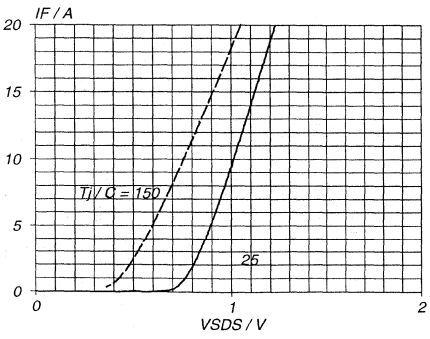


Fig.15. Source-Drain diode characteristic. $I_F = f(V_{SDS})$; parameter T_j

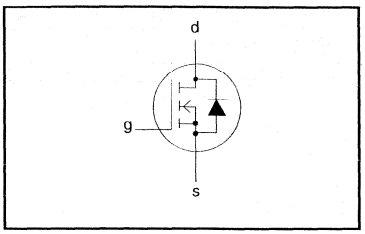
PowerMOS transistors Avalanche energy rated

PHP8N50E, PHB8N50E, PHW8N50E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 500 V

I_D = 8.5 A

$R_{DS(ON)} \leq 0.85\ \Omega$

GENERAL DESCRIPTION

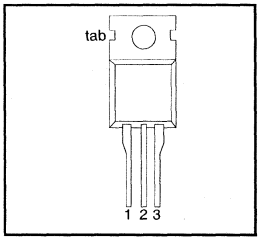
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHP8N50E is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHW8N50E is supplied in the SOT429 (TO247) conventional leaded package.
The PHB8N50E is supplied in the SOT404 surface mounting package.

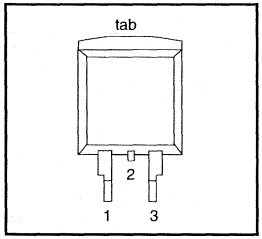
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

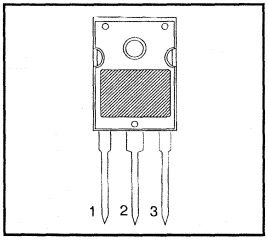
SOT78 (TO220AB)



SOT404



SOT429 (TO247)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	500	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	500	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	8.5	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	5.4	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	34	A
P_D	Total dissipation	T_{mb} = 25 °C	-	147	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

1 It is not possible to make connection to pin 2 of the SOT404 package.

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 8 A; $V_{DD} \leq 50$ V; starting T_j = 25˚C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	510	mJ
E_{AR}	Repetitive avalanche energy[2]		-	13	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	8	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	0.85	K/W
$R_{th\ j\text{-}a$	Thermal resistance junction to ambient	SOT78 package, in free air	-	60	-	K/W
		SOT429 package, in free air	-	45	-	K/W
		SOT404 package, pcb mounted, minimum footprint	-	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	500	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 4.8 A	-	0.7	0.85	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 4.8 A	3.5	6	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 500 V; V_{GS} = 0 V	-	1	25	µA
		V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 ˚C	-	40	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 8.5 A; V_{DD} = 400 V; V_{GS} = 10 V	-	88	110	nC
Q_{gs}	Gate-source charge		-	6	7	nC
Q_{gd}	Gate-drain (Miller) charge		-	47	60	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 250 V; R_D = 30 Ω;	-	18	-	ns
t_r	Turn-on rise time	R_G = 9.1 Ω	-	50	-	ns
$t_{d(off)}$	Turn-off delay time		-	104	-	ns
t_f	Turn-off fall time		-	60	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 and SOT429 packages only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1060	-	pF
C_{oss}	Output capacitance		-	160	-	pF
C_{rss}	Feedback capacitance		-	90	-	pF

2 pulse width and repetition rate limited by T_j max.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	8.5	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	34	A
V_{SD}	Diode forward voltage	I_S = 8.5 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 8.5 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	440	-	ns
Q_{rr}	Reverse recovery charge		-	6.4	-	µC

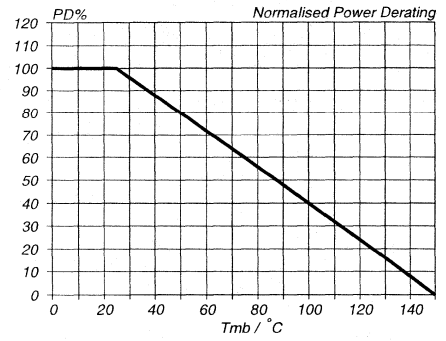


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

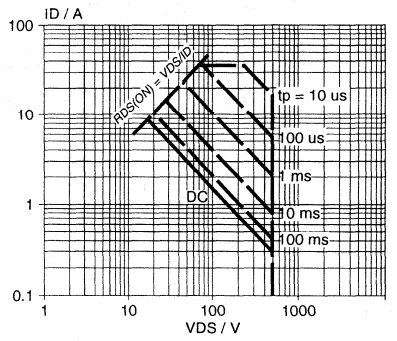


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

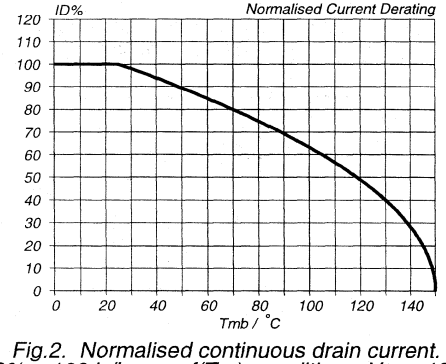


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

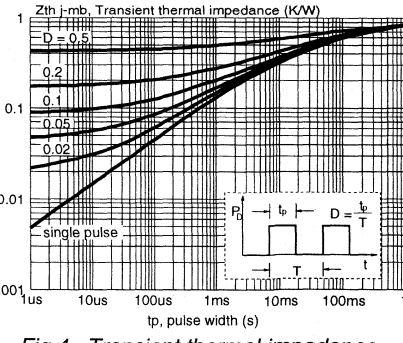


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

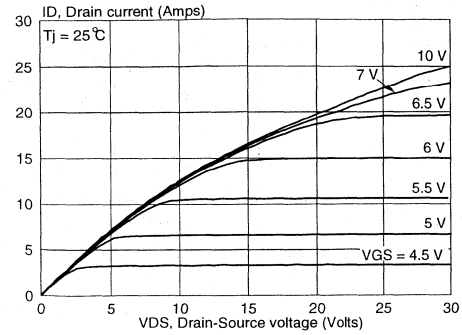


Fig.5. Typical output characteristics.
$I_D = f(V_{DS})$; parameter V_{GS}

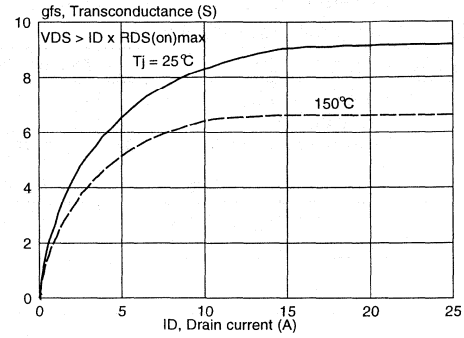


Fig.8. Typical transconductance.
$g_{fs} = f(I_D)$; parameter T_j

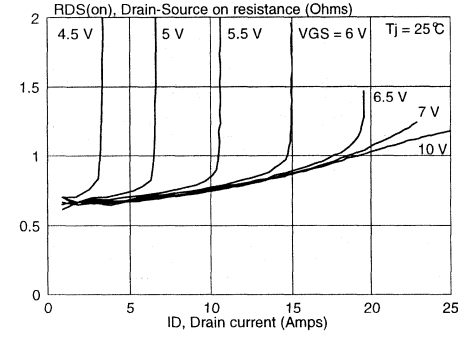


Fig.6. Typical on-state resistance.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

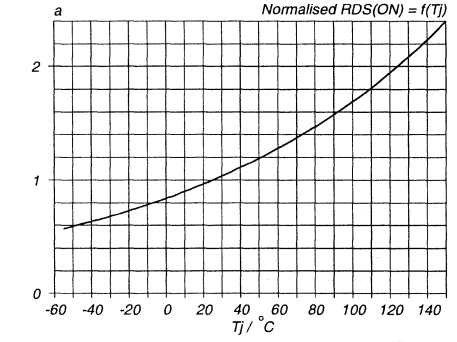


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 4.25$ A; $V_{GS} = 10$ V

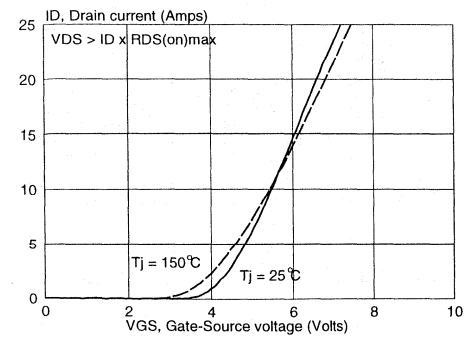


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

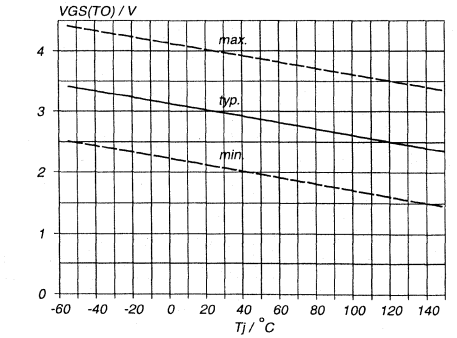


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 0.25$ mA; $V_{DS} = V_{GS}$

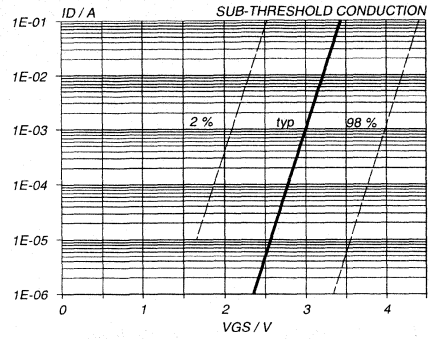


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

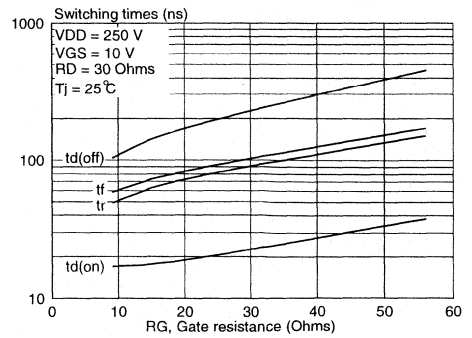


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

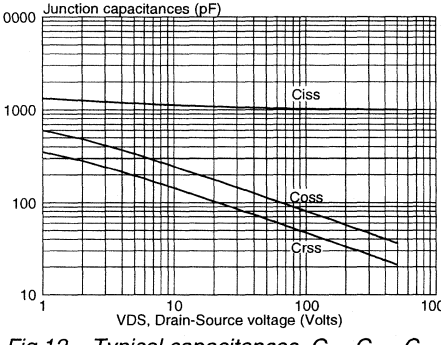


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

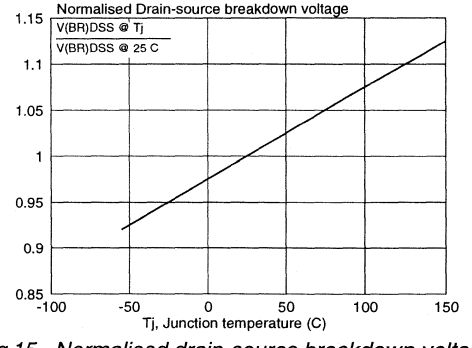


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

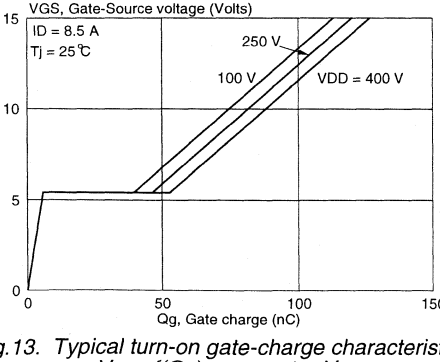


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

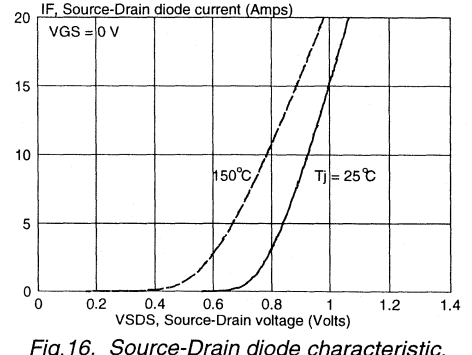


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

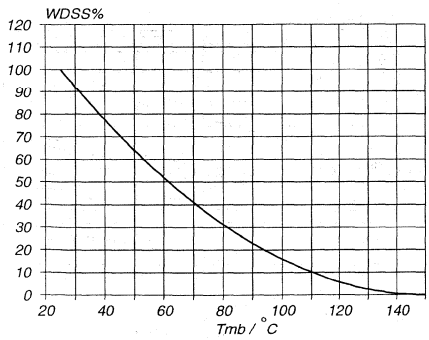


Fig.17. Normalised non-repetitive avalanche energy rating.
$E_{AS}\% = f(T_{mb})$

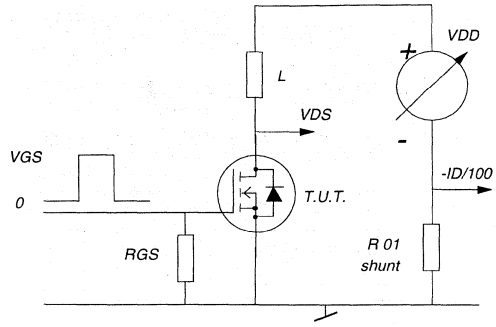


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot \frac{V_{(BR)DSS}}{(V_{(BR)DSS} - V_{DD})}$$

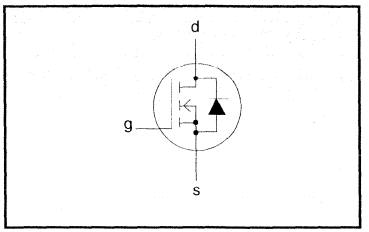
PowerMOS transistors FREDFET, Avalanche energy rated

PHP8ND50E, PHB8ND50E, PHW8ND50E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance
- Fast reverse recovery diode

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 500 V

I_D = 8.5 A

$R_{DS(ON)} \leq 0.85\ \Omega$

t_{rr} = 180 ns

GENERAL DESCRIPTION

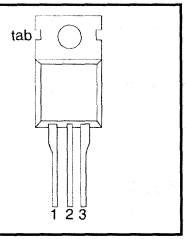
N-channel, enhancement mode field-effect power transistor, incorporating a **F**ast **R**ecovery **E**pitaxial **D**iode (FRED). This gives improved switching performance in half bridge and full bridge converters making this device particularly suitable for inverters, lighting ballasts and motor control circuits.

The PHP8ND50E is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHW8ND50E is supplied in the SOT429 (TO247) conventional leaded package.
The PHB8ND50E is supplied in the SOT404 surface mounting package.

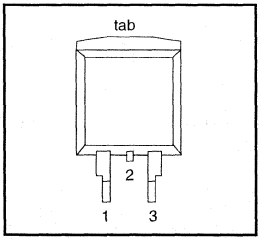
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

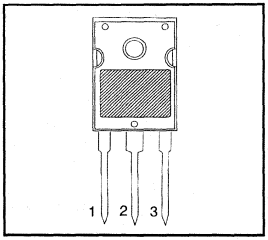
SOT78 (TO220AB)



SOT404



SOT429 (TO247)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	500	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	500	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	8.5	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	5.4	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	34	A
P_D	Total dissipation	T_{mb} = 25 °C	-	147	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

[1] It is not possible to make connection to pin 2 of the SOT404 package.

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 8 A; $V_{DD} \leq 50$ V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	510	mJ
E_{AR}	Repetitive avalanche energy[2]		-	13	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	8	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	0.85	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	SOT78 package, in free air	-	60	-	K/W
		SOT429 package, in free air	-	45	-	K/W
		SOT404 package, pcb mounted, minimum footprint	-	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	500	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 4.8 A	-	0.7	0.85	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 4.8 A	3.5	6	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 500 V; V_{GS} = 0 V	-	1	25	µA
		V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 °C	-	40	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 8.5 A; V_{DD} = 400 V; V_{GS} = 10 V	-	88	110	nC
Q_{gs}	Gate-source charge		-	6	7	nC
Q_{gd}	Gate-drain (Miller) charge		-	47	60	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 250 V; R_D = 30 Ω;	-	18	-	ns
t_r	Turn-on rise time	R_G = 9.1 Ω	-	50	-	ns
$t_{d(off)}$	Turn-off delay time		-	104	-	ns
t_f	Turn-off fall time		-	60	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 and SOT429 packages only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1060	-	pF
C_{oss}	Output capacitance		-	160	-	pF
C_{rss}	Feedback capacitance		-	90	-	pF

2 pulse width and repetition rate limited by T_j max.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	8.5	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	34	A
V_{SD}	Diode forward voltage	I_S = 8.5 A; V_{GS} = 0 V	-	-	1.5	V
t_{rr}	Reverse recovery time	I_S = 8.5 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	180	-	ns
		I_S = 8.5 A; V_{GS} = 0 V; dI/dt = 100 A/µs; 125°C	-	220	-	ns
Q_{rr}	Reverse recovery charge	I_S = 8.5 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	0.65	-	µC
		I_S = 8.5 A; V_{GS} = 0 V; dI/dt = 100 A/µs; 125°C	-	2.6	-	µC
I_{rrm}	Peak reverse recovery current	I_S = 8.5 A; V_{GS} = 0 V; dI/dt = 100 A/µs; 125°C	-	15	-	A

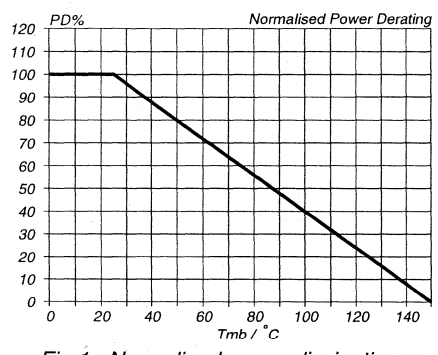


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

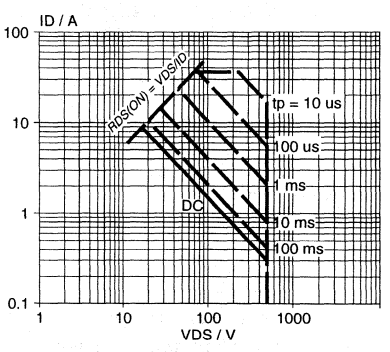


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

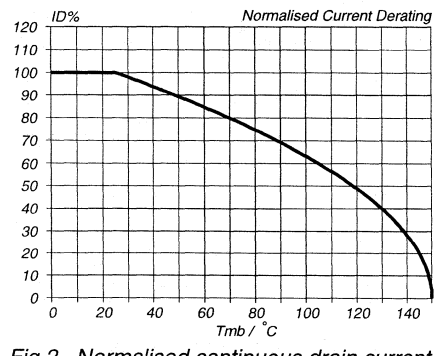


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

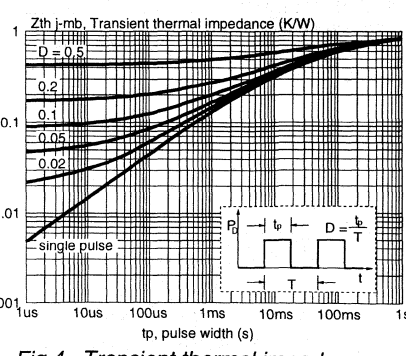


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

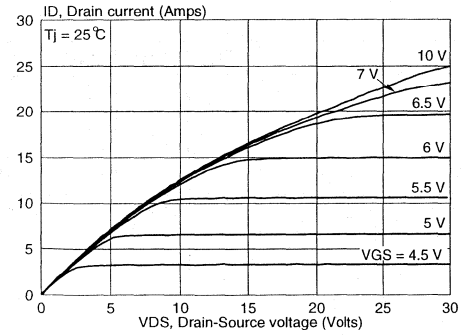


Fig.5. Typical output characteristics.
$I_D = f(V_{DS})$; parameter V_{GS}

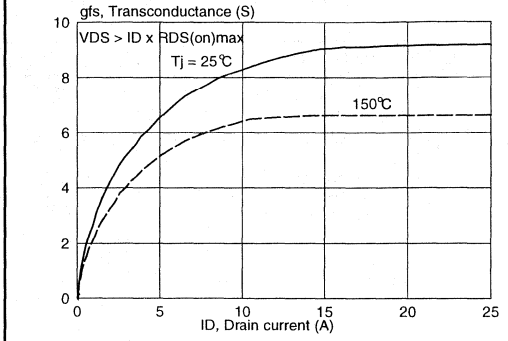


Fig.8. Typical transconductance.
$g_{fs} = f(I_D)$; parameter T_j

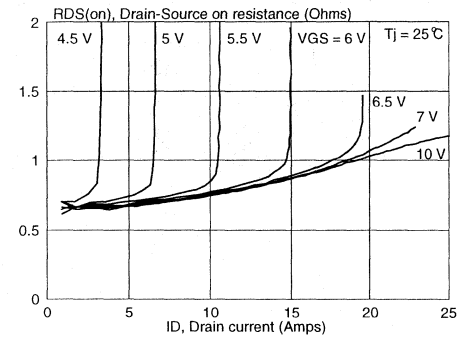


Fig.6. Typical on-state resistance.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

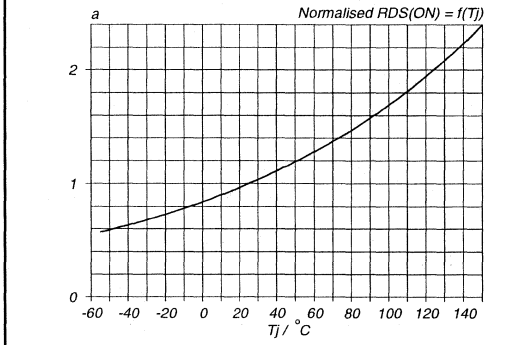


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 4.25 A; V_{GS} = 10 V

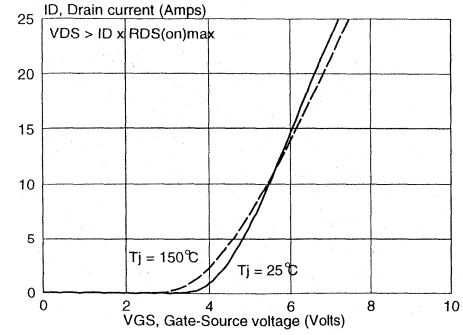


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

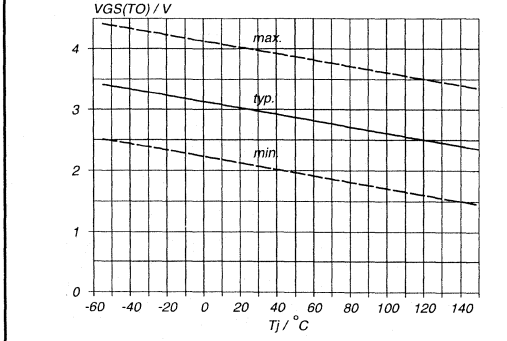


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

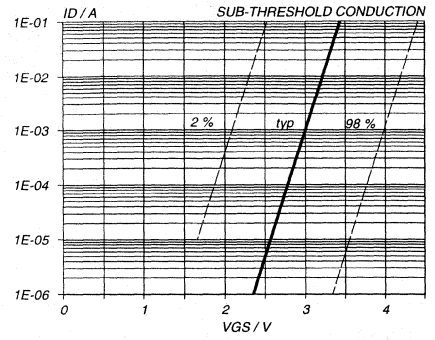


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

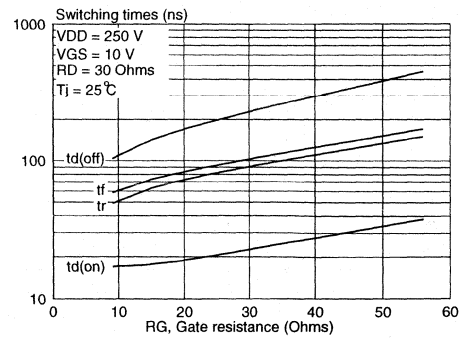


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

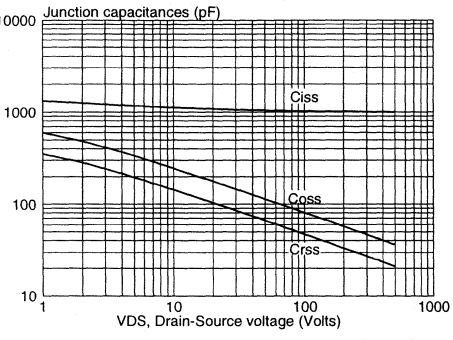


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

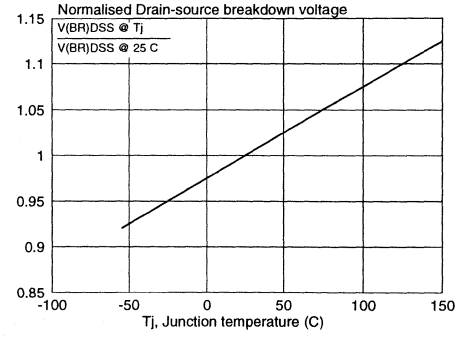


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

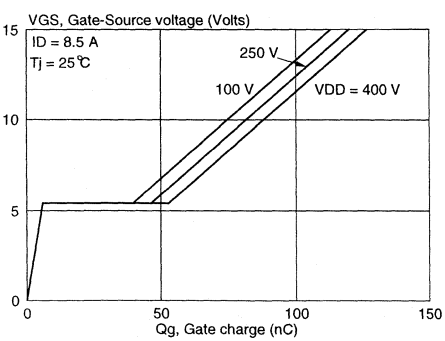


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

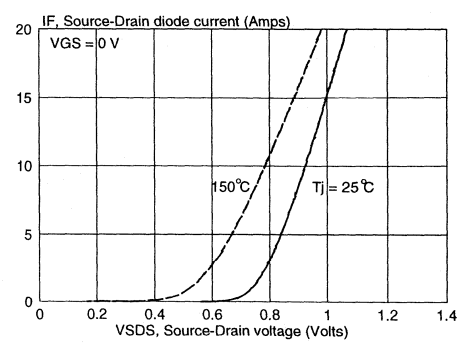


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

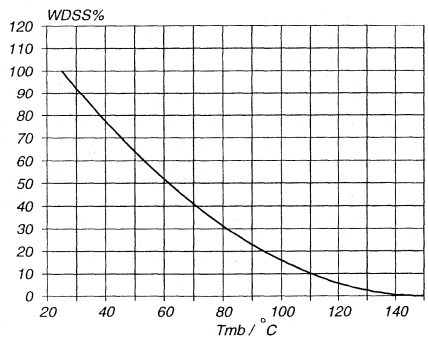


Fig.17. Normalised non-repetitive avalanche energy rating.
$E_{AS}\% = f(T_{mb})$

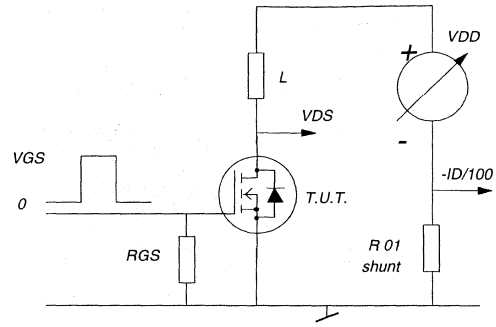


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot \frac{V_{(BR)DSS}}{(V_{(BR)DSS} - V_{DD})}$$

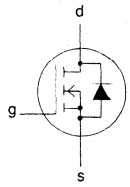
PowerMOS transistors Avalanche energy rated

PHB9N60E, PHW9N60E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 600 V

I_D = 8.7 A

$R_{DS(ON)} \leq 0.85\ \Omega$

GENERAL DESCRIPTION

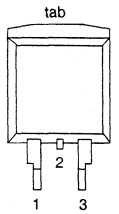
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHW9N60E is supplied in the SOT429 (TO247) conventional leaded package.
The PHB9N60E is supplied in the SOT404 surface mounting package.

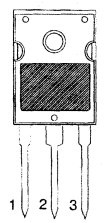
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

SOT404



SOT429 (TO247)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	600	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	600	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	8.7	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	5.5	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	35	A
P_D	Total dissipation	T_{mb} = 25 °C	-	156	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

PRELIMINARY
Philips Semiconductors for Design-in information

1 It is not possible to make connection to pin 2 of the SOT404 package.

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_{AS} = 8.7 A; t_p = 0.2 ms; T_j prior to avalanche = 25˚C; $V_{DD} \leq$ 50 V; R_{GS} = 50 Ω; V_{GS} = 10 V	-	813	mJ
E_{AR}	Repetitive avalanche energy[2]	I_{AR} = 8.7 A; t_p = 1 µs; T_j prior to avalanche = 25˚C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	28	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	8.7	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	0.8	K/W
$R_{th\ j\text{-}a$	Thermal resistance junction to ambient	SOT429 package, in free air	-	45	-	K/W
		SOT404 package, pcb mounted, minimum footprint	-	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	600	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 4.4 A	-	0.7	0.85	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 4.4 A	4	5.5	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 600 V; V_{GS} = 0 V	-	2	100	µA
		V_{DS} = 480 V; V_{GS} = 0 V; T_j = 125 ˚C	-	80	1000	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 8.7 A; V_{DD} = 480 V; V_{GS} = 10 V	-	130	150	nC
Q_{gs}	Gate-source charge		-	8	10	nC
Q_{gd}	Gate-drain (Miller) charge		-	60	85	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V; R_D = 33 Ω;	-	20	-	ns
t_r	Turn-on rise time	R_G = 5.6 Ω	-	55	-	ns
$t_{d(off)}$	Turn-off delay time		-	160	-	ns
t_f	Turn-off fall time		-	70	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT429 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1500	-	pF
C_{oss}	Output capacitance		-	200	-	pF
C_{rss}	Feedback capacitance		-	112	-	pF

2 pulse width and repetition rate limited by T_j max.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	8.7	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	35	A
V_{SD}	Diode forward voltage	I_S = 8.7 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 8.7 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	740	-	ns
Q_{rr}	Reverse recovery charge		-	9	-	µC

MECHANICAL DATA

Dimensions in mm

Net Mass: 1.4 g

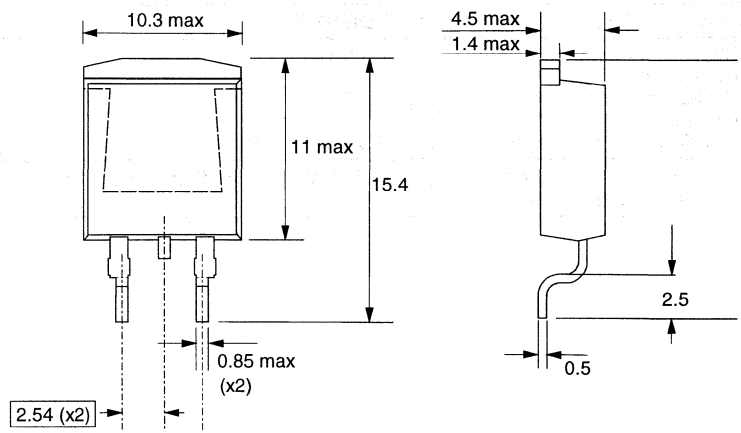


Fig.1. SOT404 : centre pin connected to mounting base.

MOUNTING INSTRUCTIONS

Dimensions in mm

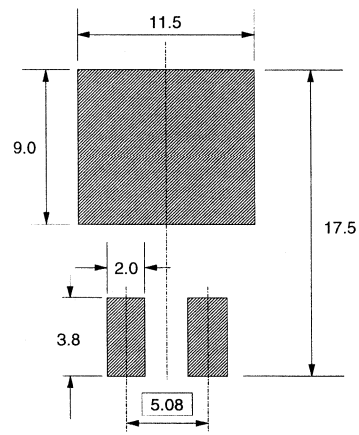


Fig.2. SOT404 : soldering pattern for surface mounting.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Epoxy meets UL94 V0 at 1/8".

PowerMOS transistor — PHP10N10E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

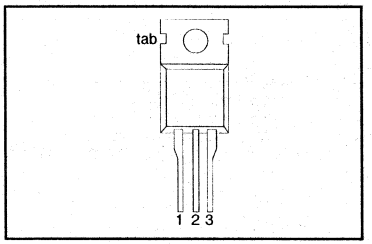
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	11	A
P_{tot}	Total power dissipation	60	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.25	Ω

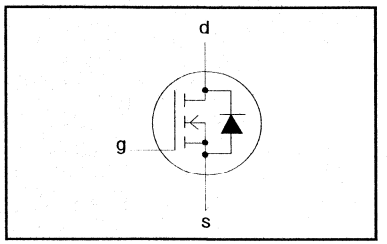
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	11	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	7.7	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	44	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	60	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction Temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 5.5 A	-	0.22	0.25	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5.5 A	3	4.2	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	400	500	pF
C_{oss}	Output capacitance		-	90	120	pF
C_{rss}	Feedback capacitance		-	35	50	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	9	14	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	30	45	ns
t_f	Turn-off fall time		-	20	40	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	11	A
I_{DRM}	Pulsed reverse drain current	-	-	-	44	A
V_{SD}	Diode forward voltage	I_F = 11 A ; V_{GS} = 0 V	-	1.2	1.5	V
t_{rr}	Reverse recovery time	I_F = 11 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.35	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 11 A ; V_{DD} ≤ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	35	mJ

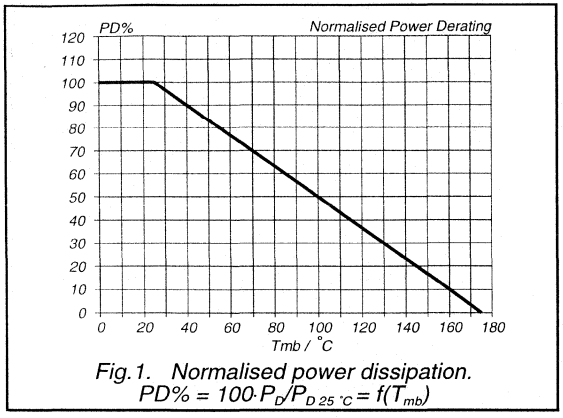


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

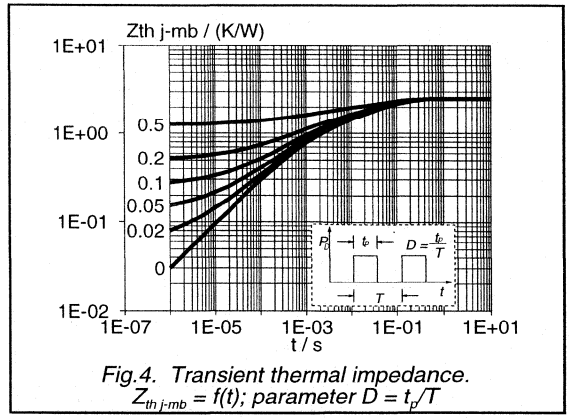


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

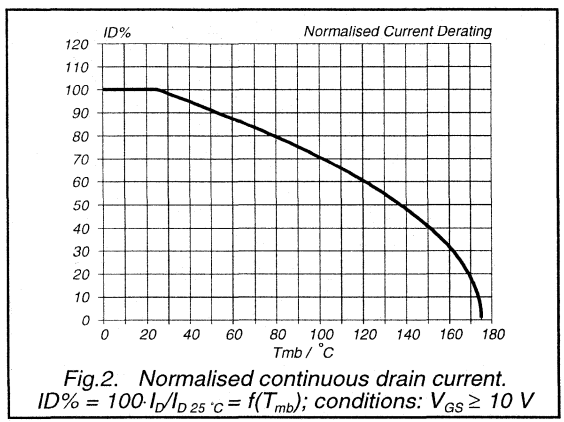


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

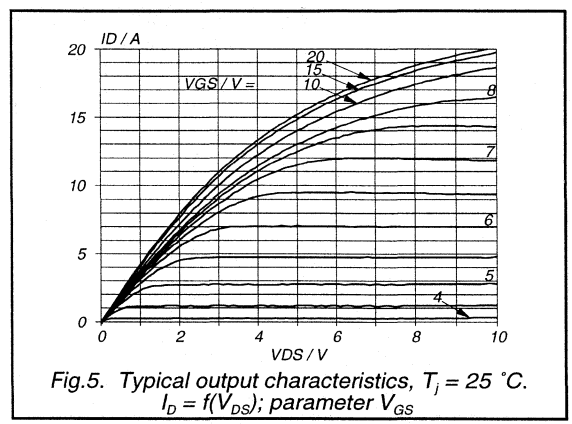


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

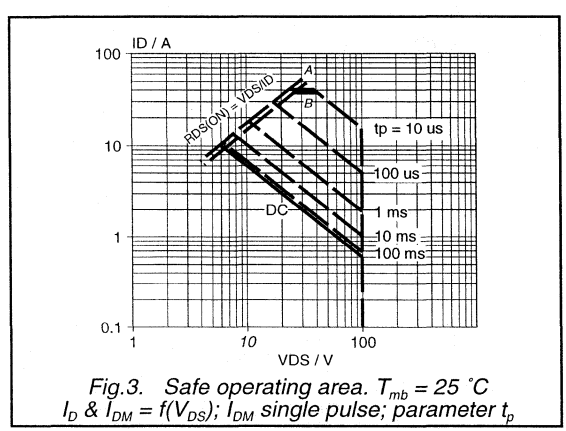


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

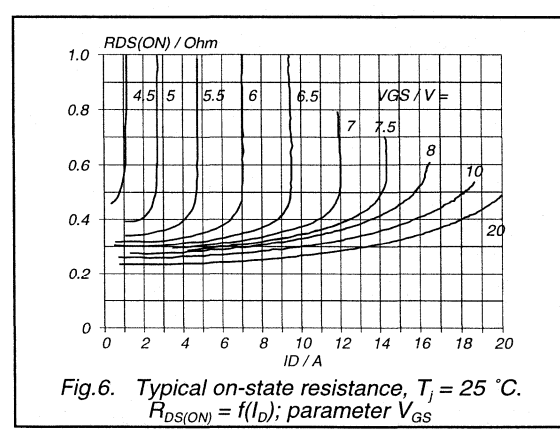


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

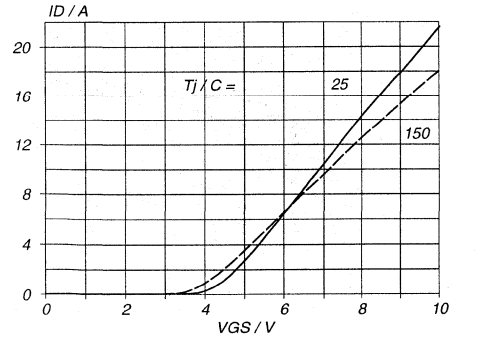


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

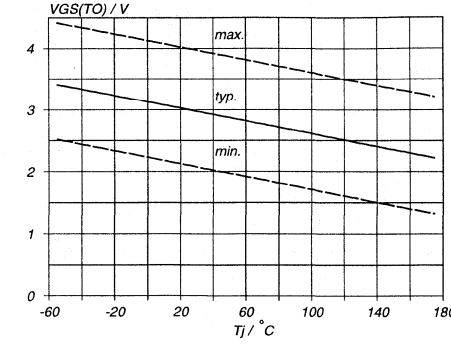


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

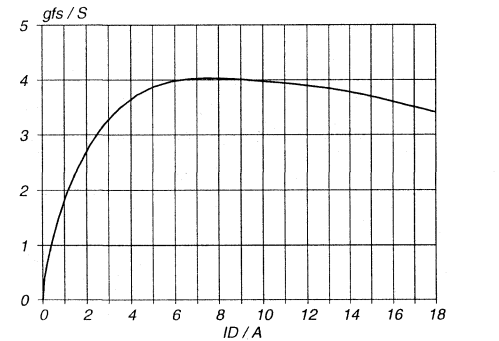


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

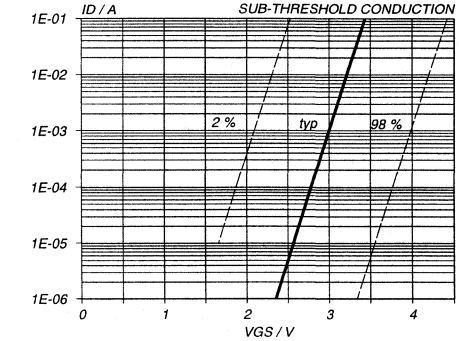


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

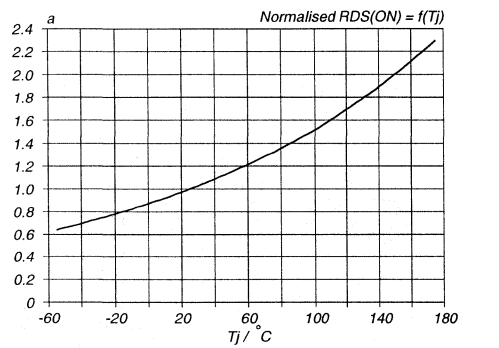


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 5.5 A; V_{GS} = 10 V

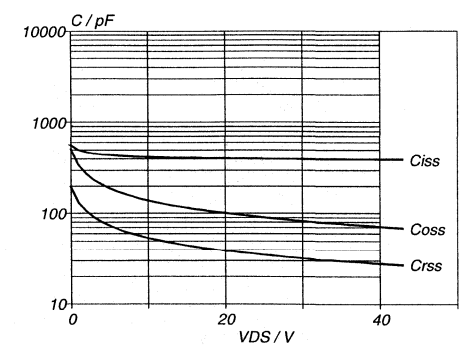


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

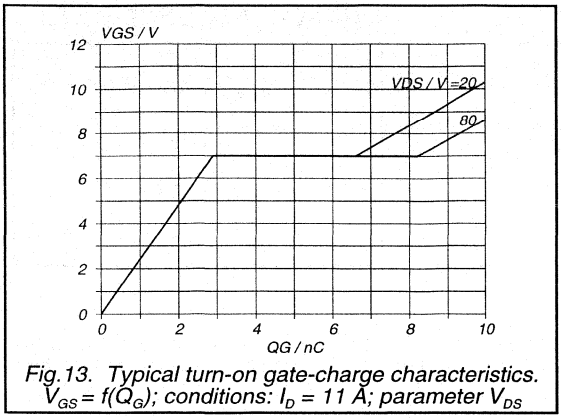


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: I_D = 11 A; parameter V_{DS}

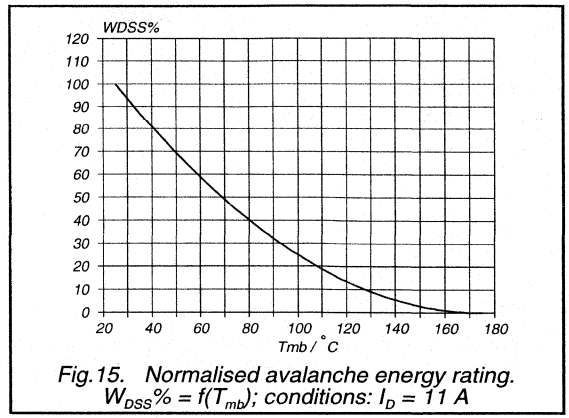


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: I_D = 11 A

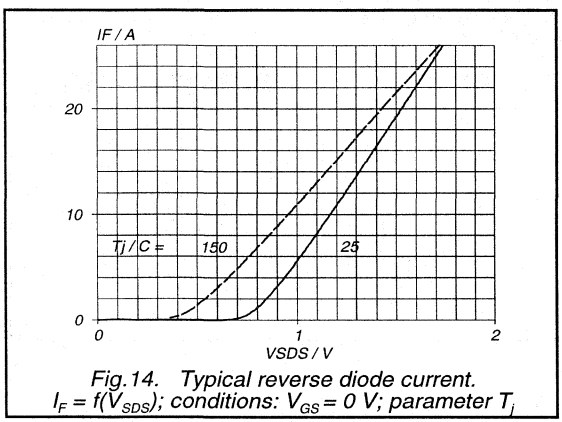


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

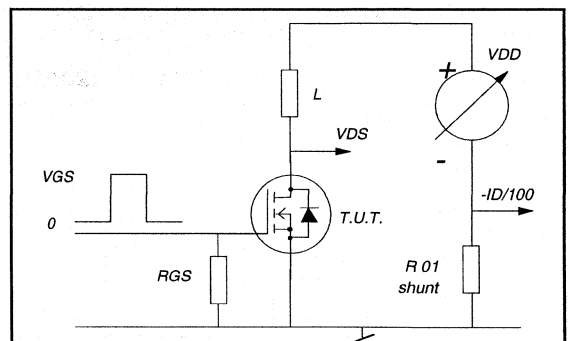


Fig.16. Avalanche energy test circuit.
$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

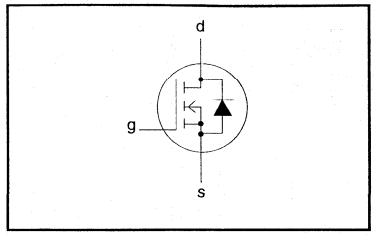
PowerMOS transistors Avalanche energy rated

PHP10N40E, PHB10N40E, PHW10N40E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 400 V

I_D = 10.6 A

$R_{DS(ON)} \leq 0.55\ \Omega$

GENERAL DESCRIPTION

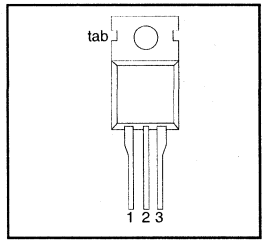
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHP10N40E is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHW10N40E is supplied in the SOT429 (TO247) conventional leaded package.
The PHB10N40E is supplied in the SOT404 surface mounting package.

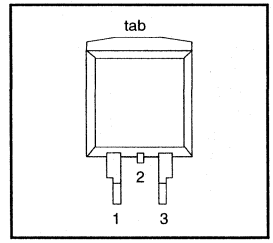
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

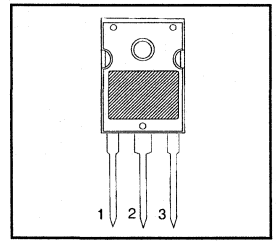
SOT78 (TO220AB)



SOT404



SOT429 (TO247)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	400	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	400	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	10.6	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	6.7	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	42	A
P_D	Total dissipation	T_{mb} = 25 °C	-	147	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

1 It is not possible to make connection to pin 2 of the SOT404 package.

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 10 A; $V_{DD} \leq 50$ V; starting $T_j = 25$˚C; $R_{GS} = 50\ \Omega$; $V_{GS} = 10$ V	-	520	mJ
E_{AR}	Repetitive avalanche energy[2]		-	13	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	10	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	0.85	K/W
$R_{th\ j\text{-}a$	Thermal resistance junction to ambient	SOT78 package, in free air	-	60	-	K/W
		SOT429 package, in free air	-	45	-	K/W
		SOT404 package, pcb mounted, minimum footprint	-	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	400	-	-	V
$\Delta V_{(BR)DSS} / \Delta T_j$	Drain-source breakdown voltage temperature coefficient	$V_{DS} = V_{GS}$; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 5.3 A	-	0.42	0.55	Ω
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 5.3 A	3.5	6	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 400 V; V_{GS} = 0 V	-	1	25	µA
		V_{DS} = 320 V; V_{GS} = 0 V; T_j = 125 ˚C	-	30	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 10.6 A; V_{DD} = 320 V; V_{GS} = 10 V	-	90	110	nC
Q_{gs}	Gate-source charge		-	7	9	nC
Q_{gd}	Gate-drain (Miller) charge		-	49	60	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 200 V; $R_D = 18\ \Omega$;	-	13	-	ns
t_r	Turn-on rise time	$R_G = 9.1\ \Omega$	-	65	-	ns
$t_{d(off)}$	Turn-off delay time		-	108	-	ns
t_f	Turn-off fall time		-	70	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1080	-	pF
C_{oss}	Output capacitance		-	190	-	pF
C_{rss}	Feedback capacitance		-	110	-	pF

2 pulse width and repetition rate limited by T_j max.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	10.6	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	42	A
V_{SD}	Diode forward voltage	I_S = 10.6 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 10.6 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	330	-	ns
Q_{rr}	Reverse recovery charge		-	4.8	-	µC

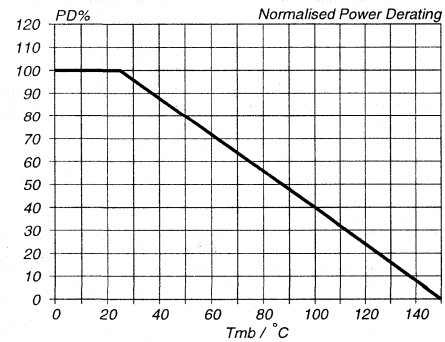


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

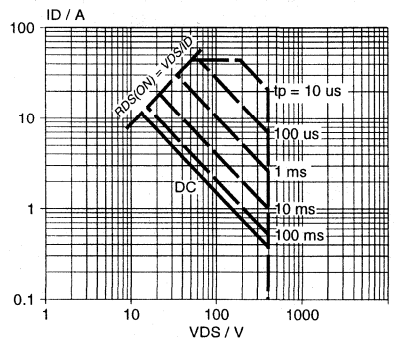


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

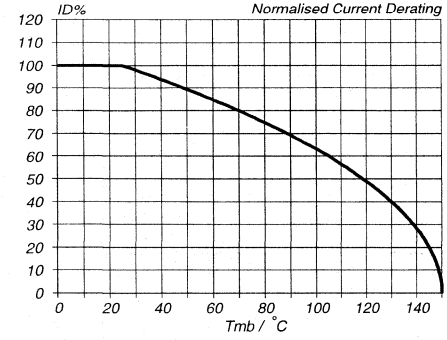


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

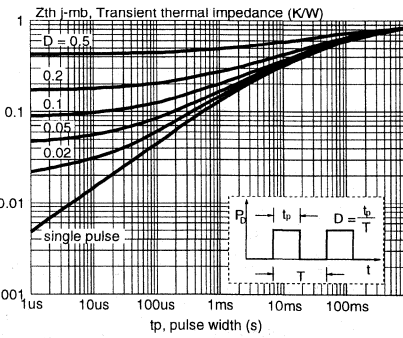


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

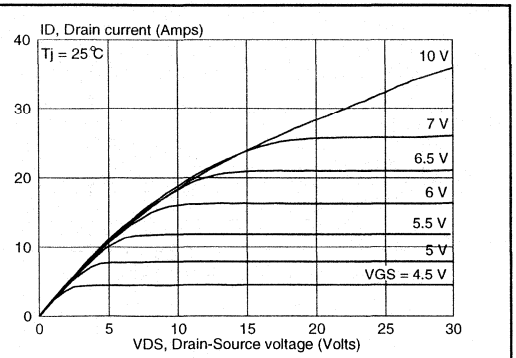


Fig.5. Typical output characteristics.
$I_D = f(V_{DS})$; parameter V_{GS}

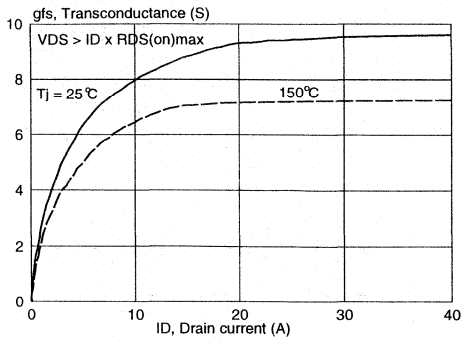


Fig.8. Typical transconductance.
$g_{fs} = f(I_D)$; parameter T_j

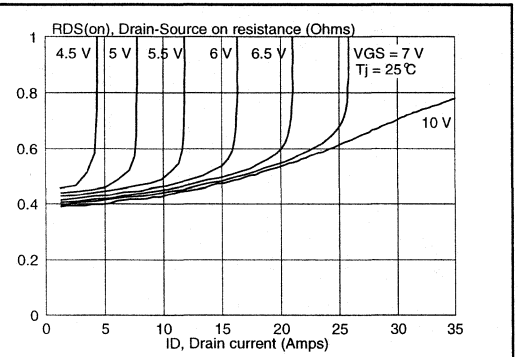


Fig.6. Typical on-state resistance.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

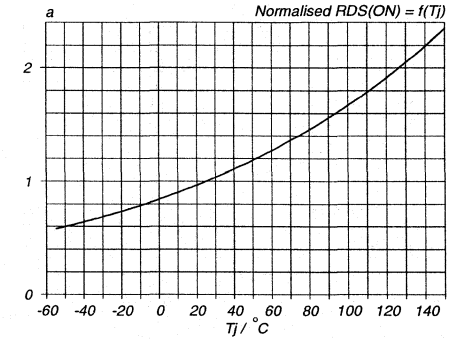


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 5.3 A; V_{GS} = 10 V

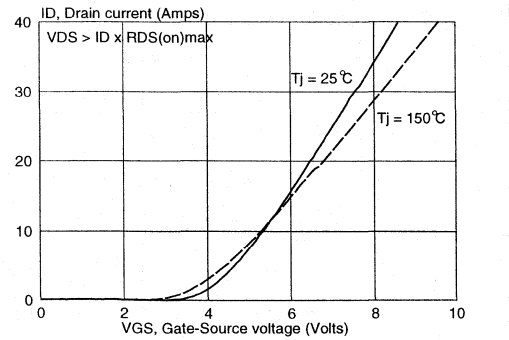


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

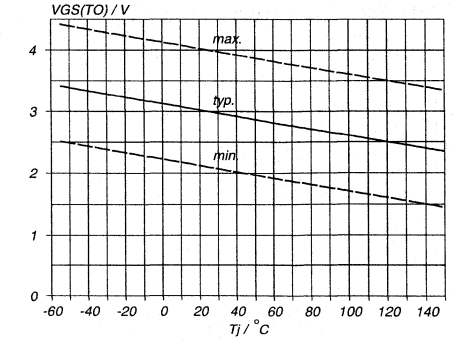


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

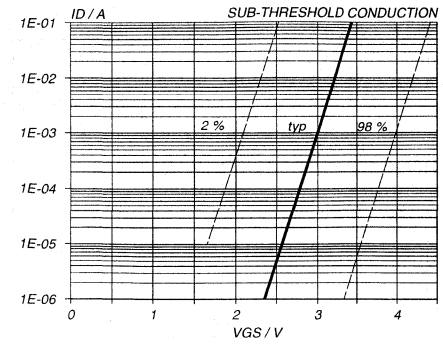


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

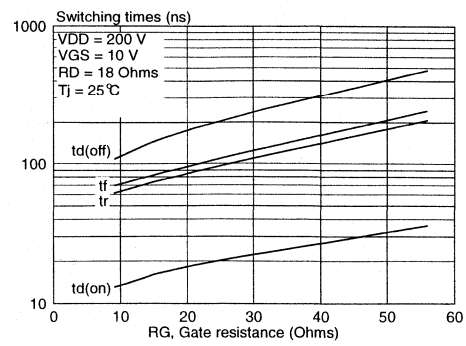


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

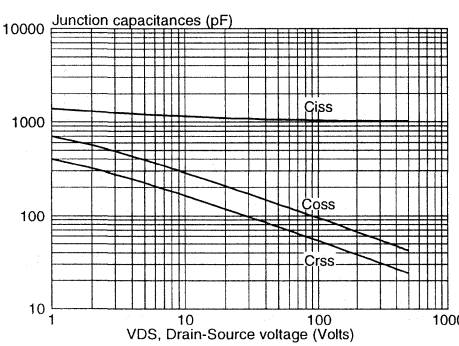


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

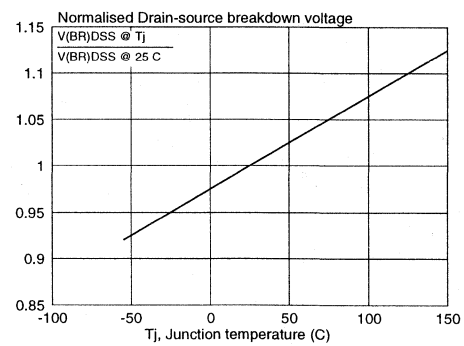


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

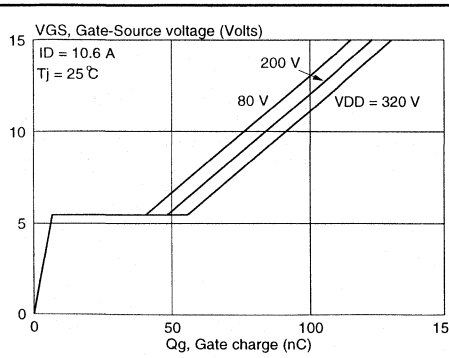


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

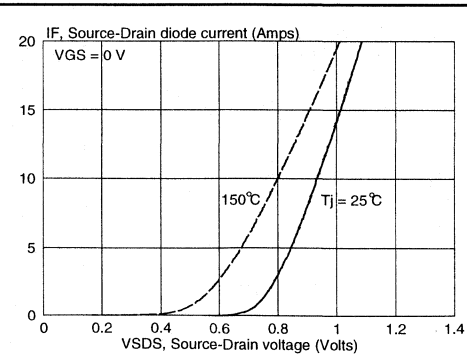


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

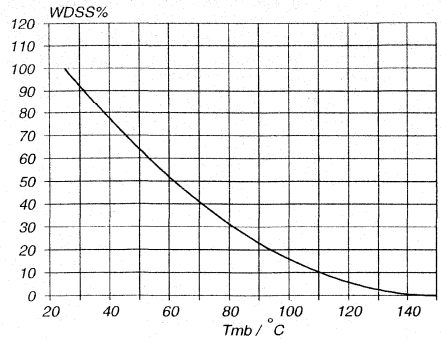


Fig.17. Normalised non-repetitive avalanche energy rating.
$E_{AS}\% = f(T_{mb})$

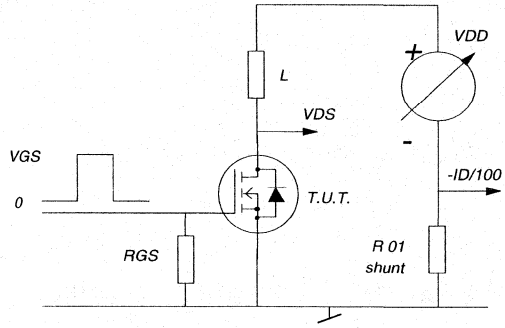


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot \frac{V_{(BR)DSS}}{(V_{(BR)DSS} - V_{DD})}$$

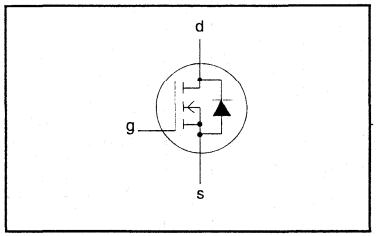
PowerMOS transistors Avalanche energy rated

PHP10N60E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 600 V

I_D = 9.6 A

$R_{DS(ON)} \leq 0.75\ \Omega$

GENERAL DESCRIPTION

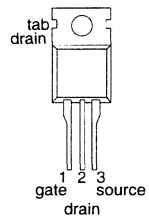
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHP10N60E is supplied in the SOT78 (TO220AB) conventional leaded package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	drain

SOT78 (TO220AB)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	600	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	600	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	9.6	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	6.1	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	38	A
P_D	Total dissipation	T_{mb} = 25 °C	-	167	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_{AS} = 9.6 A; t_p = 0.2 ms; T_j prior to avalanche = 25°C; $V_{DD} \leq 50$ V; R_{GS} = 50 Ω; V_{GS} = 10 V	-	813	mJ
E_{AR}	Repetitive avalanche energy[1]	I_{AR} = 9.6 A; t_p = 1 µs; T_j prior to avalanche = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	28	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	9.6	A

Preliminary design-in information
See Philips Semiconductors for

1 pulse width and repetition rate limited by T_j max.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	0.75	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	600	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 4.4 A	-	0.7	0.75	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 4.4 A	4	5.5	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 600 V; V_{GS} = 0 V	-	2	100	µA
		V_{DS} = 480 V; V_{GS} = 0 V; T_j = 125 °C	-	80	1000	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 8.7 A; V_{DD} = 480 V; V_{GS} = 10 V	-	130	150	nC
Q_{gs}	Gate-source charge		-	8	10	nC
Q_{gd}	Gate-drain (Miller) charge		-	60	85	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V; R_D = 33 Ω;	-	20	-	ns
t_r	Turn-on rise time	R_G = 5.6 Ω	-	55	-	ns
$t_{d(off)}$	Turn-off delay time		-	160	-	ns
t_f	Turn-off fall time		-	70	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1500	-	pF
C_{oss}	Output capacitance		-	200	-	pF
C_{rss}	Feedback capacitance		-	112	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	9.6	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	38	A
V_{SD}	Diode forward voltage	I_S = 9.6 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 9.6 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	740	-	ns
Q_{rr}	Reverse recovery charge		-	9	-	µC

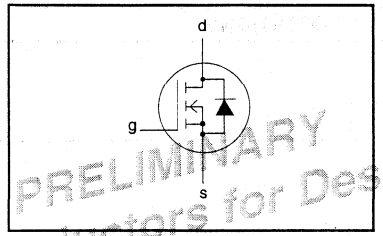
PowerMOS transistors Avalanche energy rated

PHP11N50E, PHB11N50E, PHW11N50E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 500 V

I_D = 10.4 A

$R_{DS(ON)} \leq 0.6\ \Omega$

PRELIMINARY
Philips Semiconductors for Design-in information

GENERAL DESCRIPTION

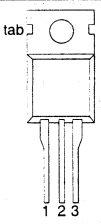
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHP11N50E is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHW11N50E is supplied in the SOT429 (TO247) conventional leaded package.
The PHB11N50E is supplied in the SOT404 surface mounting package.

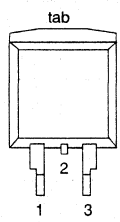
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

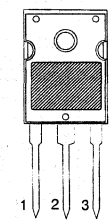
SOT78 (TO220AB)



SOT404



SOT429 (TO247)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	500	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	500	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	10.4	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	6.6	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	42	A
P_D	Total dissipation	T_{mb} = 25 °C	-	156	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

1 It is not possible to make connection to pin 2 of the SOT404 package.

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 10.4 A; $V_{DD} \leq 50$ V; starting T_j = 25˚C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	676	mJ
E_{AR}	Repetitive avalanche energy[2]		-	16.9	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	10.4	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	0.8	K/W
$R_{th\ j\text{-}a$	Thermal resistance junction to ambient	SOT78 package, in free air	-	60	-	K/W
		SOT429 package, in free air	-	45	-	K/W
		SOT404 package, pcb mounted, minimum footprint	-	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	500	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 5.2 A	-	0.5	0.6	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 5.2 A	4	7	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 500 V; V_{GS} = 0 V	-	1	25	µA
		V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 ˚C	-	60	500	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 10.4 A; V_{DD} = 400 V; V_{GS} = 10 V	-	120	150	nC
Q_{gs}	Gate-source charge		-	8	10	nC
Q_{gd}	Gate-drain (Miller) charge		-	65	85	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 250 V; R_D = 22 Ω;	-	22	-	ns
t_r	Turn-on rise time	R_G = 5.6 Ω	-	70	-	ns
$t_{d(off)}$	Turn-off delay time		-	145	-	ns
t_f	Turn-off fall time		-	84	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 and SOT429 packages only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1400	-	pF
C_{oss}	Output capacitance		-	220	-	pF
C_{rss}	Feedback capacitance		-	125	-	pF

2 pulse width and repetition rate limited by T_j max.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	10.4	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	42	A
V_{SD}	Diode forward voltage	I_S = 10.4 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 10.4 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	600	-	ns
Q_{rr}	Reverse recovery charge		-	9	-	µC

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

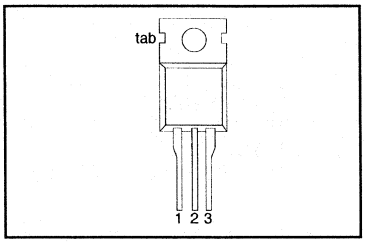
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	14	A
P_{tot}	Total power dissipation	75	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.16	Ω

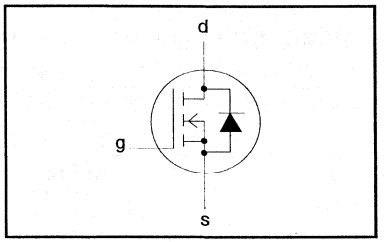
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	14	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	10	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	56	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	75	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction Temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A	-	0.15	0.16	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5 A	4.0	5.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	660	825	pF
C_{oss}	Output capacitance		-	140	200	pF
C_{rss}	Feedback capacitance		-	60	100	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	10	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	60	90	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	14	A
I_{DRM}	Pulsed reverse drain current	-	-	-	56	A
V_{SD}	Diode forward voltage	I_F = 14 A ; V_{GS} = 0 V	-	1.2	1.5	V
t_{rr}	Reverse recovery time	I_F = 14 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.6	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 14 A ; $V_{DD} \leq$ 50 V; V_{GS} = 10 V ; R_{GS} = 50Ω	-	-	70	mJ

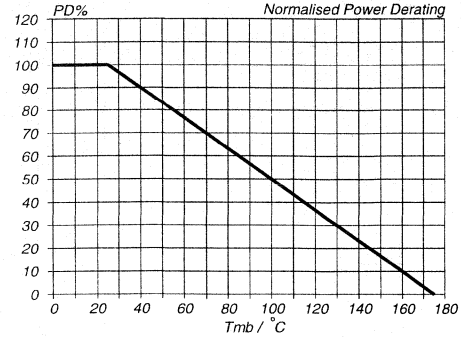


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

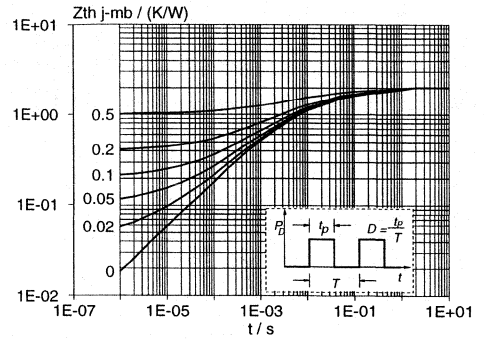


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

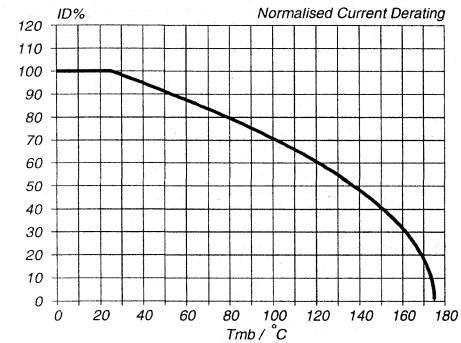


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

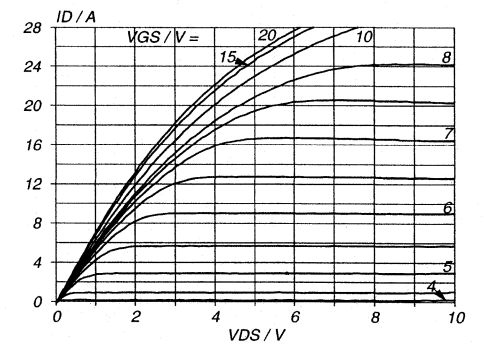


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

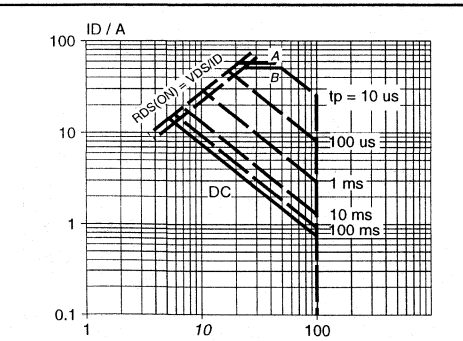


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

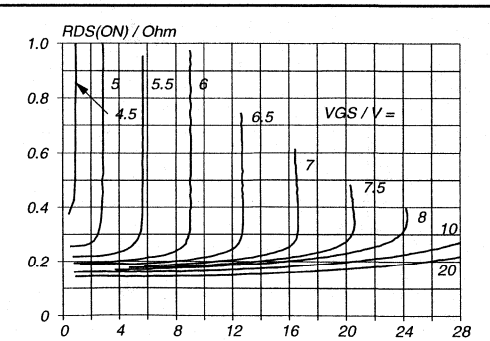


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

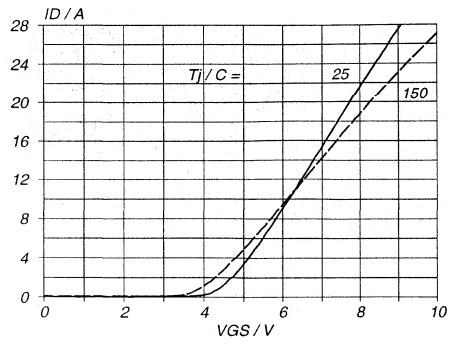


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

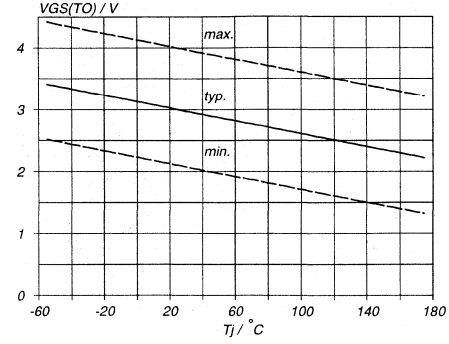


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

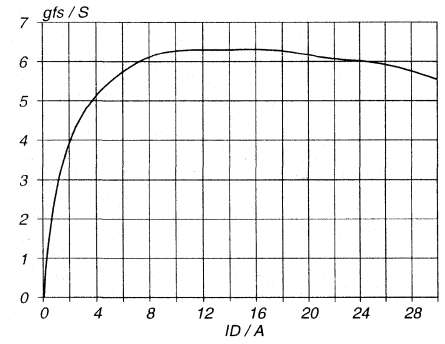


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

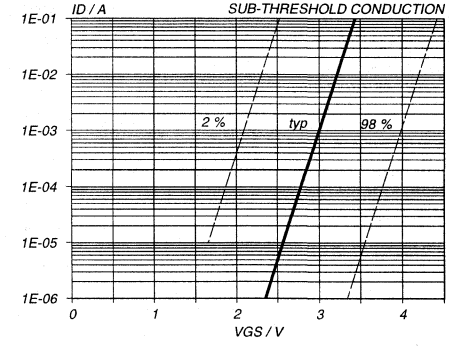


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

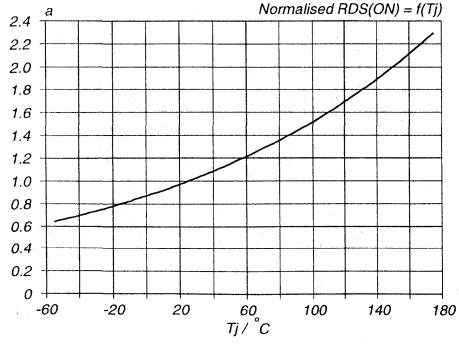


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 5 A; V_{GS} = 10 V

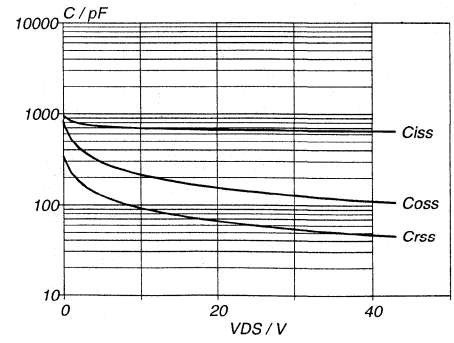


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

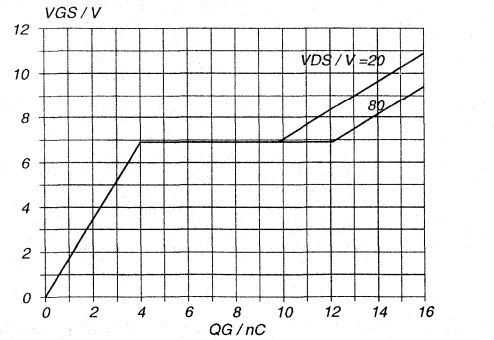


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: I_D = 14 A; parameter V_{DS}

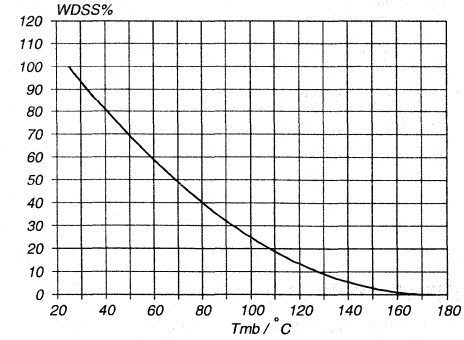


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: I_D = 14 A

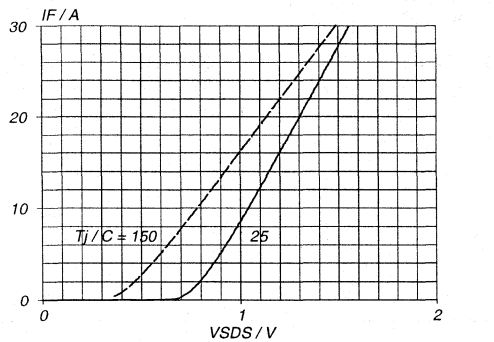


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

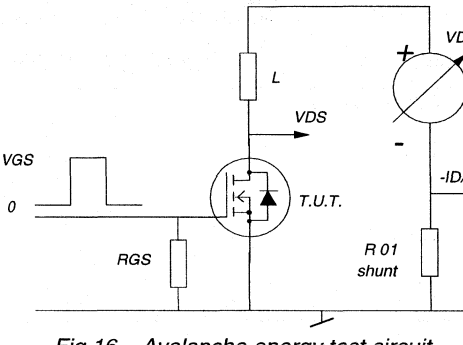


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

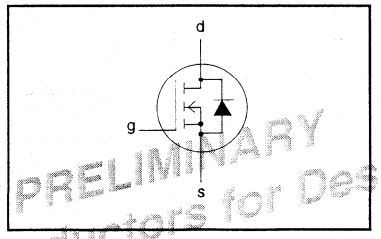
PowerMOS transistors Avalanche energy rated

PHP13N40E, PHB13N40E, PHW13N40E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 400 V

I_D = 12.8 A

$R_{DS(ON)} \leq 0.4\ \Omega$

PRELIMINARY
Philips Semiconductors for Design-in information
Philips Semiconductors

GENERAL DESCRIPTION

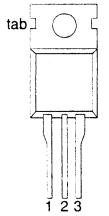
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHP13N40E is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHW13N40E is supplied in the SOT429 (TO247) conventional leaded package.
The PHB13N40E is supplied in the SOT404 surface mounting package.

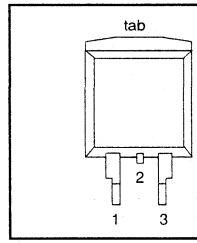
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

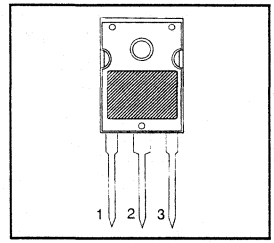
SOT78 (TO220AB)



SOT404



SOT429 (TO247)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	400	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	400	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	12.8	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	8.1	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	51	A
P_D	Total dissipation	T_{mb} = 25 °C	-	156	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

1 It is not possible to make connection to pin 2 of the SOT404 package.

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 12.8 A; $V_{DD} \leq 50$ V; starting $T_j = 25^{\circ}C$; $R_{GS} = 50\ \Omega$; $V_{GS} = 10$ V	-	666	mJ
E_{AR}	Repetitive avalanche energy[2]		-	16.6	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	12.8	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	0.8	K/W
$R_{th\ j\text{-}a$	Thermal resistance junction to ambient	SOT78 package, in free air	-	60	-	K/W
		SOT429 package, in free air	-	45	-	K/W
		SOT404 package, pcb mounted, minimum footprint	-	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	400	-	-	V
$\Delta V_{(BR)DSS} / \Delta T_j$	Drain-source breakdown voltage temperature coefficient	$V_{DS} = V_{GS}$; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 6.4 A	-	0.35	0.4	Ω
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 6.4 A	4	8	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 400 V; V_{GS} = 0 V	-	1	25	µA
		V_{DS} = 320 V; V_{GS} = 0 V; T_j = 125 °C	-	50	500	µA
I_{GSS}	Gate-source leakage current	$V_{GS} = \pm 30$ V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 12.8 A; V_{DD} = 320 V; V_{GS} = 10 V	-	125	150	nC
Q_{gs}	Gate-source charge		-	10	13	nC
Q_{gd}	Gate-drain (Miller) charge		-	68	85	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 200 V; $R_D = 15\ \Omega$;	-	18	-	ns
t_r	Turn-on rise time	$R_G = 5.6\ \Omega$	-	90	-	ns
$t_{d(off)}$	Turn-off delay time		-	150	-	ns
t_f	Turn-off fall time		-	100	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1400	-	pF
C_{oss}	Output capacitance		-	260	-	pF
C_{rss}	Feedback capacitance		-	150	-	pF

2 pulse width and repetition rate limited by T_j max.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	12.8	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	51	A
V_{SD}	Diode forward voltage	I_S = 12.8 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 12.8 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	460	-	ns
Q_{rr}	Reverse recovery charge		-	6.7	-	µC

PowerMOS transistor — PHP18N20E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

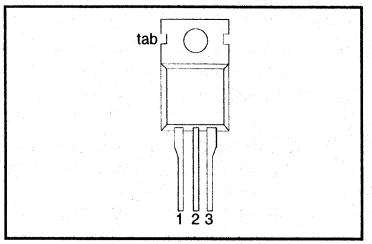
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (DC)	18	A
P_{tot}	Total power dissipation	150	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.18	Ω

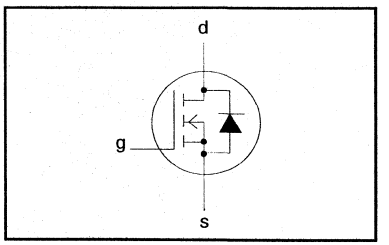
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	18	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	12.5	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	72	A
P_D	Total dissipation	T_{mb} = 25 °C	-	150	W
$\Delta P_D/\Delta T_{mb}$	Linear derating factor	T_{mb} > 25 °C	-	1.0	W/K
V_{GS}	Gate-source voltage		-	± 30	V
E_{AS}	Single pulse avalanche energy	$V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	150	mJ
I_{AS}	Peak avalanche current	$V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	18	A
T_j, T_{stg}	Operating junction and storage temperature range		- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$\Delta V_{(BR)DSS} / \Delta T_j$	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.25	-	V/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 11 A	-	0.13	0.18	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 50 V; I_D = 11 A	6.7	13	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 200 V; V_{GS} = 0 V	-	1	25	µA
		V_{DS} = 160 V; V_{GS} = 0 V; T_j = 150 °C	-	4	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$Q_{g(tot)}$	Total gate charge	I_D = 18 A; V_{DD} = 160 V; V_{GS} = 10 V	-	53	60	nC
Q_{gs}	Gate-source charge		-	8	10	nC
Q_{gd}	Gate-drain (Miller) charge		-	25	30	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 100 V; I_D = 18 A;	-	15	-	ns
t_r	Turn-on rise time	R_G = 9.1 Ω; R_D = 5.4 Ω	-	63	-	ns
$t_{d(off)}$	Turn-off delay time		-	66	-	ns
t_f	Turn-off fall time		-	50	-	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1370	-	pF
C_{oss}	Output capacitance		-	240	-	pF
C_{rss}	Feedback capacitance		-	70	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	18	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	72	A
V_{SD}	Diode forward voltage	I_S = 18 A; V_{GS} = 0 V	-	-	1.5	V
t_{rr}	Reverse recovery time	I_S = 18 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	200	-	ns
Q_{rr}	Reverse recovery charge		-	1.5	-	µC

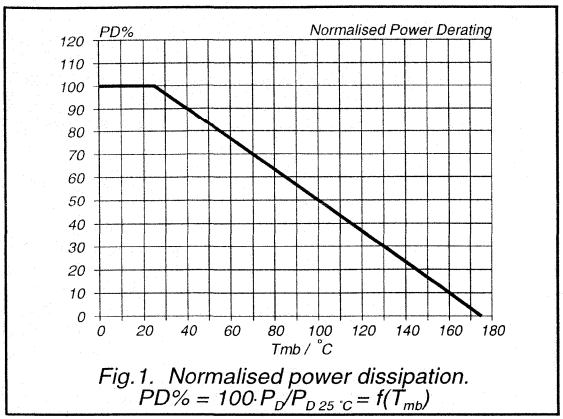


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

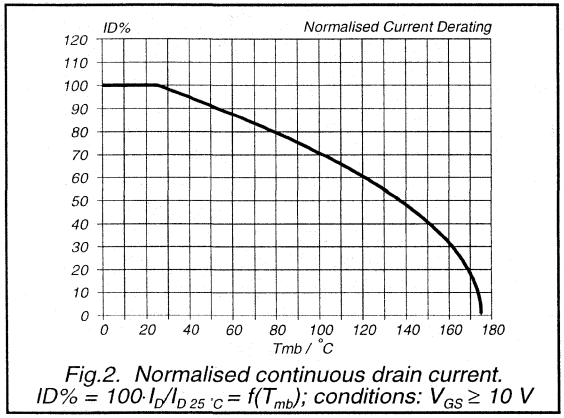


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 10 V

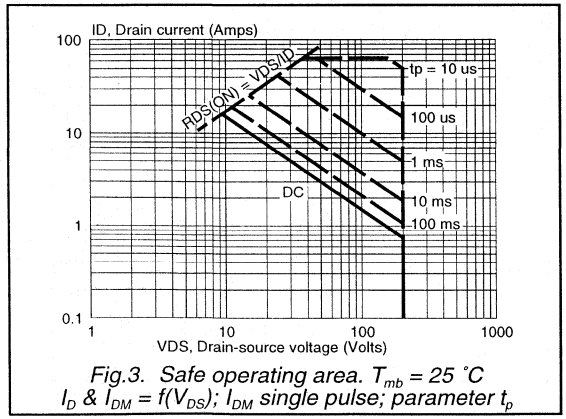


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

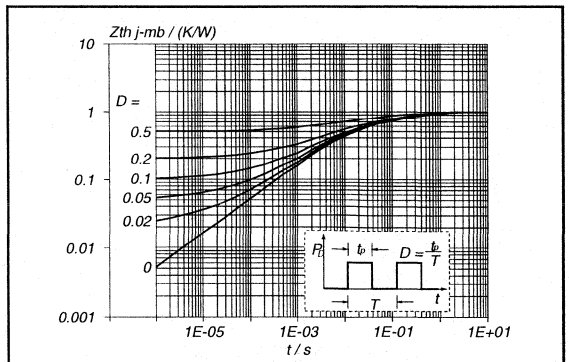


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

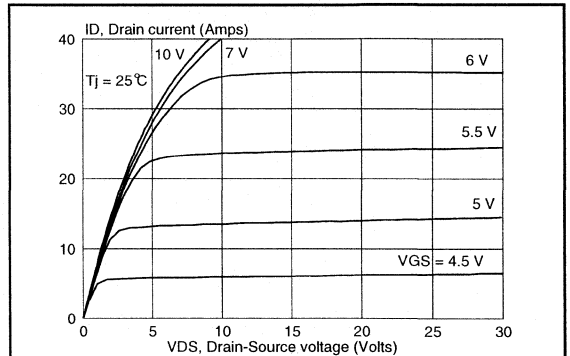


Fig.5. Typical output characteristics.
I_D = f(V_{DS}); parameter V_{GS}

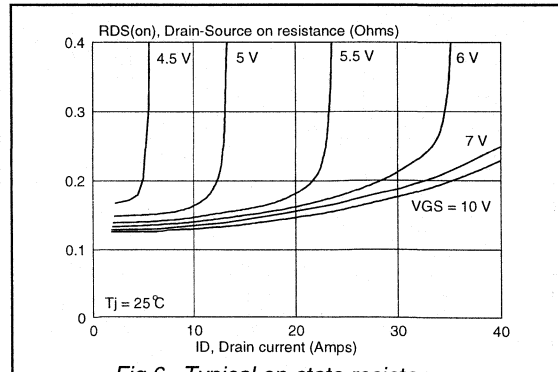


Fig.6. Typical on-state resistance.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

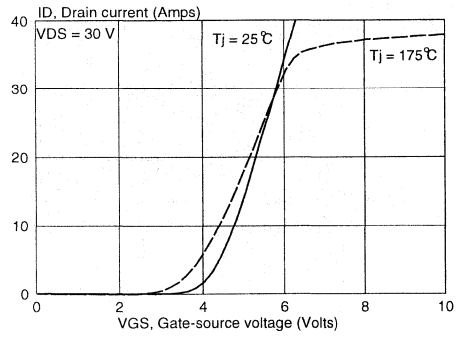


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; parameter T_j

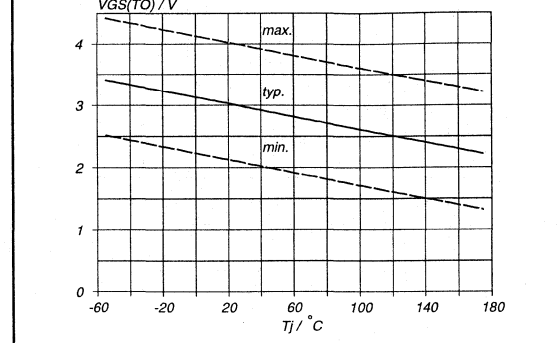


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

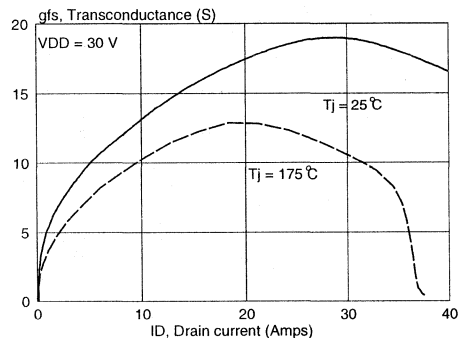


Fig.8. Typical transconductance. $g_{fs} = f(I_D)$; parameter T_j

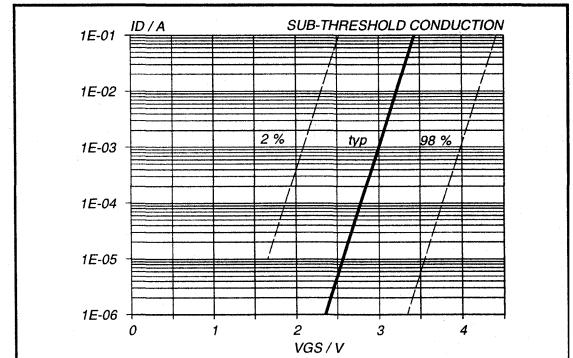


Fig.11. Sub-threshold drain current. $I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

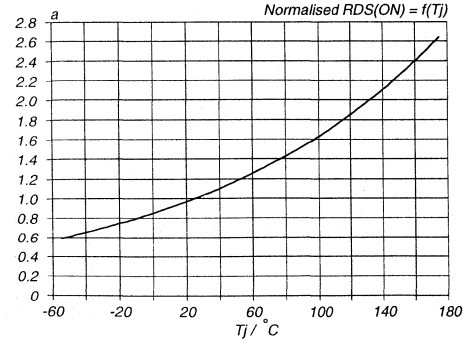


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,^{\circ}C} = f(T_j)$; I_D = 18 A; V_{GS} = 10 V

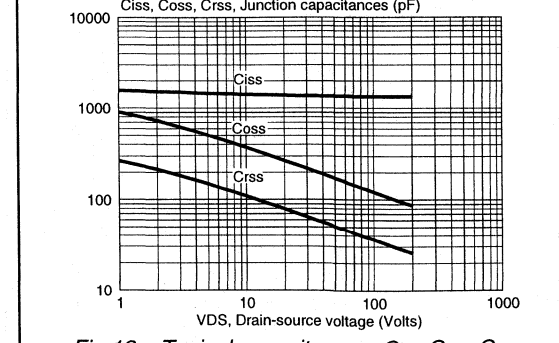


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

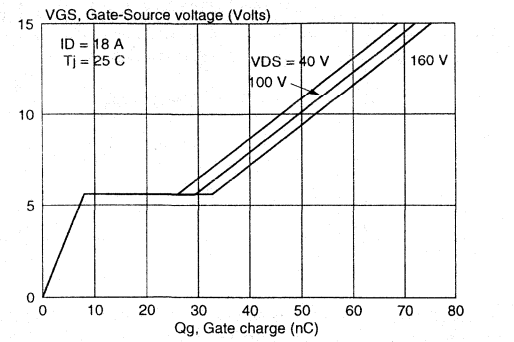


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; *parameter* V_{DS}

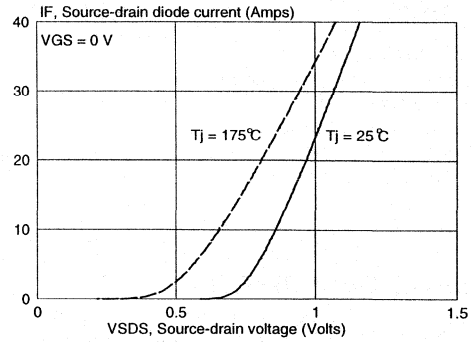


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; *parameter* T_j

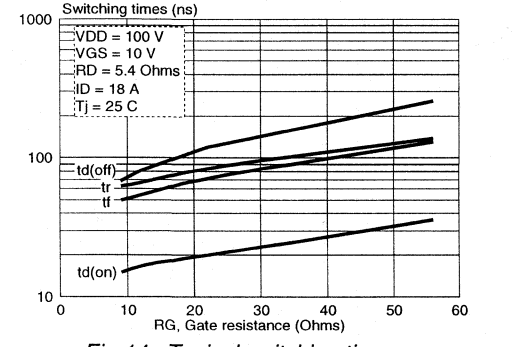


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

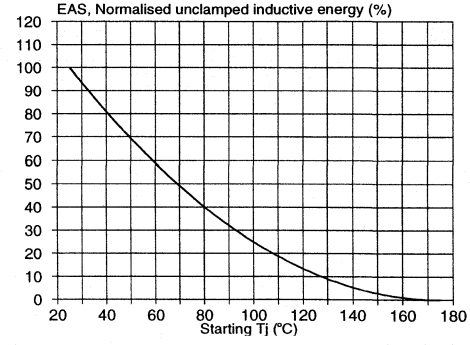


Fig.17. Normalised unclamped inductive energy.
$E_{AS}\% = f(T_j)$

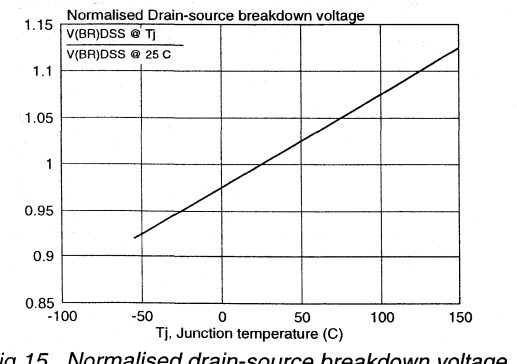


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ ^\circ C} = f(T_j)$

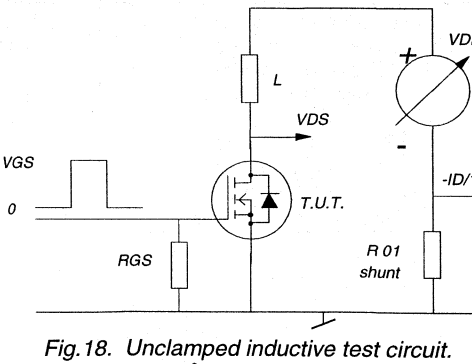


Fig.18. Unclamped inductive test circuit.
$E_{AS} = 0.5 \cdot LI_D^2 \cdot V_{(BR)DSS}/(V_{(BR)DSS} - V_{DD})$

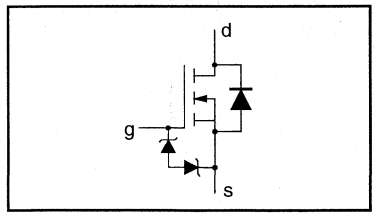
TrenchMOS™ transistor Logic level FET

PHP21N06LT, PHB21N06LT

FEATURES

- **'Trench'** technology
- Very low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 55 V

I_D = 21 A

$R_{DS(ON)} \leq 75\ m\Omega$ (V_{GS} = 5 V)

$R_{DS(ON)} \leq 70\ m\Omega$ (V_{GS} = 10 V)

GENERAL DESCRIPTION

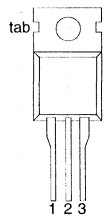
N-channel enhancement mode, logic level, field-effect power transistor in a plastic envelope using **'trench'** technology. The device has very low on-state resistance. It is intended for use in dc to dc converters and general purpose switching applications.

The PHP21N06LT is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHB21N06LT is supplied in the SOT404 surface mounting package.

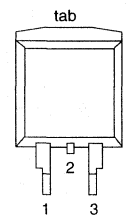
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

SOT78 (TO220AB)



SOT404



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 175°C	-	55	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 175°C; R_{GS} = 20 kΩ	-	55	V
V_{GS}	Gate-source voltage		-	± 13	V
I_D	Continuous drain current	T_{mb} = 25 °C	-	21	A
		T_{mb} = 100 °C	-	14.7	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	84	A
P_D	Total power dissipation	T_{mb} = 25 °C	-	69	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	175	°C

1 It is not possible to make connection to pin 2 of the SOT404 package.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	2.18	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	SOT78 package, in free air	60	-	K/W
		SOT404 package, pcb mounted, minimum footprint	50	-	K/W

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

ELECTRICAL CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 10 A	-	60	75	mΩ
		V_{GS} = 10 V; I_D = 10 A	-	55	70	mΩ
		T_j = 175˚C	-	-	157	mΩ
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 10 A	5	20	-	S
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	20	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
$Q_{g(tot)}$	Total gate charge	I_D = 20 A; V_{DD} = 44 V; V_{GS} = 5 V	-	10.5	-	nC
Q_{gs}	Gate-source charge		-	3	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	5	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	10	15	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω	-	47	70	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	28	40	ns
t_f	Turn-off fall time		-	33	45	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	500	650	pF
C_{oss}	Output capacitance		-	110	135	pF
C_{rss}	Feedback capacitance		-	60	85	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)		-	-	21	A
I_{SM}	Pulsed source current (body diode)		-	-	84	A
V_{SD}	Diode forward voltage	I_F = 19.7 A; V_{GS} = 0 V	-	0.95	1.2	V
t_{rr}	Reverse recovery time	I_F = 19.7 A; -dI_F/dt = 100 A/µs;	-	32	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.12	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 10 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 ˚C	-	30	mJ

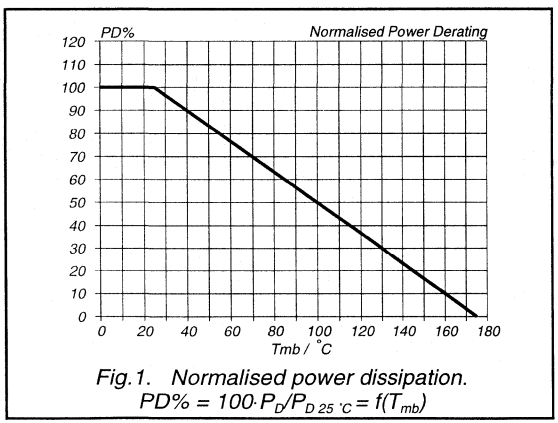


Fig.1. Normalised power dissipation.
PD% = 100·$P_D/P_{D\ 25\ ^\circ C}$ = f(T_{mb})

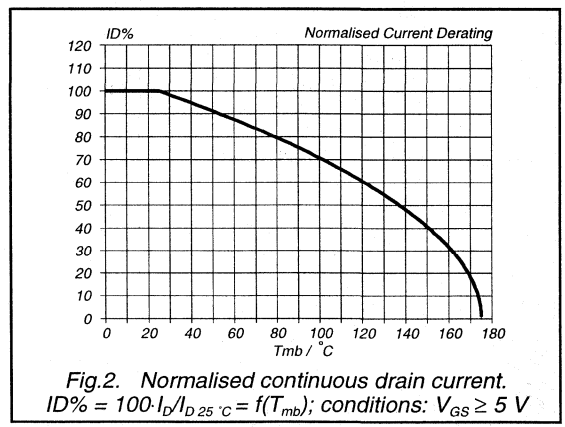


Fig.2. Normalised continuous drain current.
ID% = 100·$I_D/I_{D\ 25\ ^\circ C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

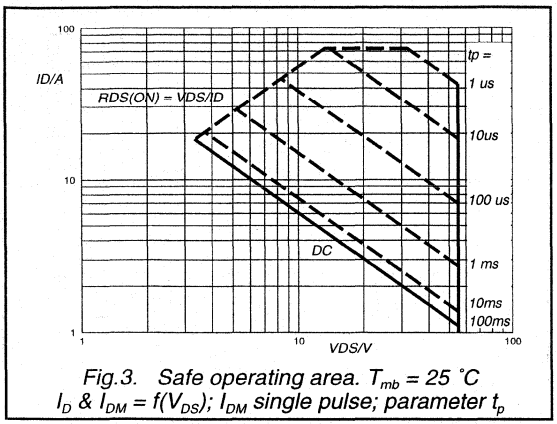


Fig.3. Safe operating area. T_{mb} = 25 ˚C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

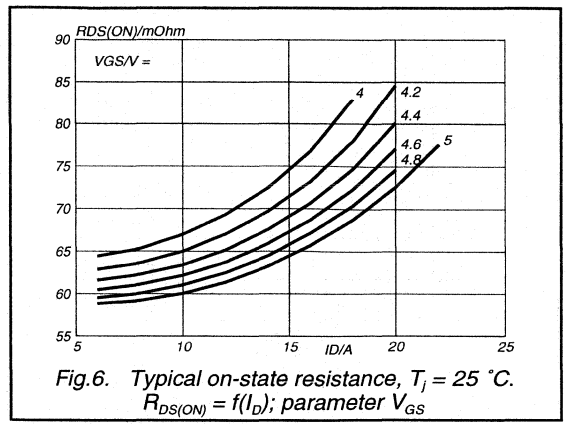


Fig.6. Typical on-state resistance, T_j = 25 ˚C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

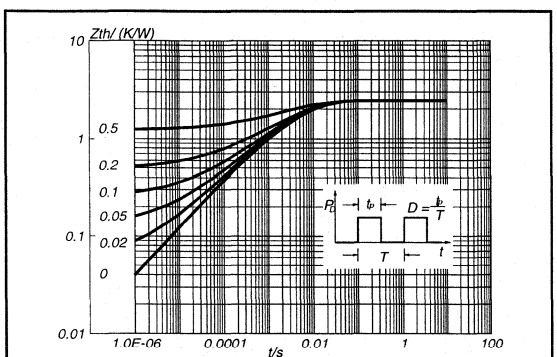


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

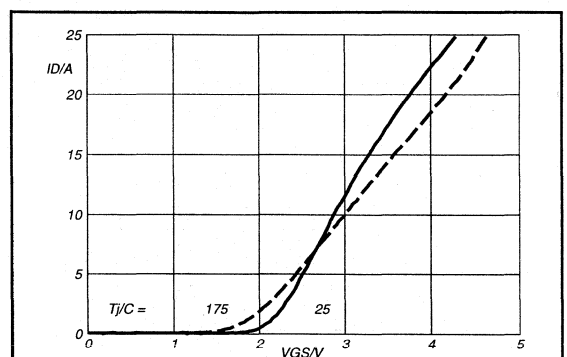


Fig.7. Typical transfer characteristics.
I_D = f(V_{GS}) ; conditions: V_{DS} = 25 V; parameter T_j

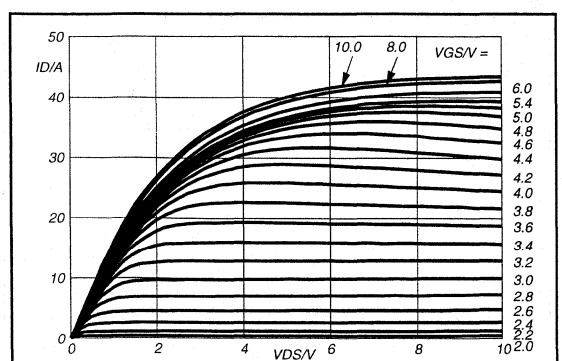


Fig.5. Typical output characteristics, T_j = 25 ˚C.
I_D = f(V_{DS}); parameter V_{GS}

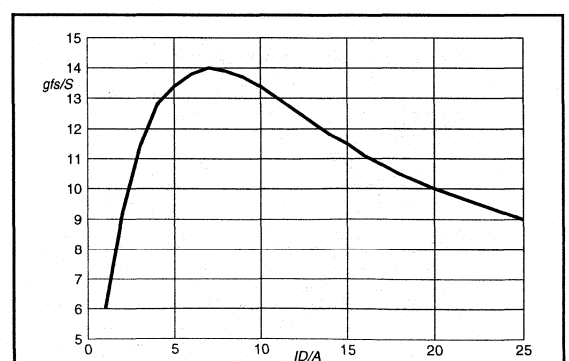


Fig.8. Typical transconductance, T_j = 25 ˚C.
g_{fs} = f(I_D); conditions: V_{DS} = 25 V

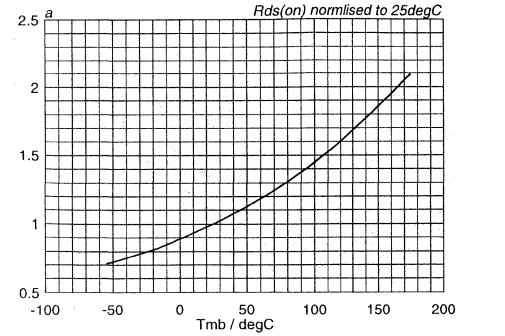


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 10 A; V_{GS} = 5 V

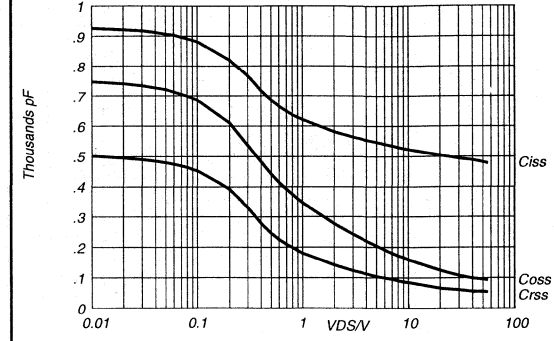


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

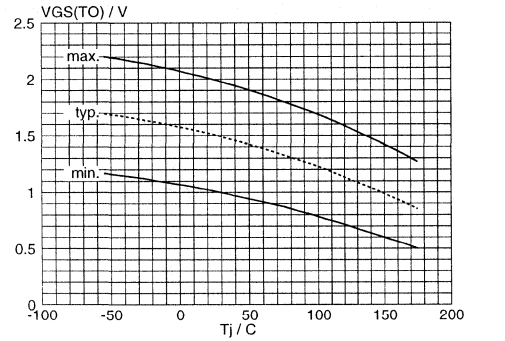


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

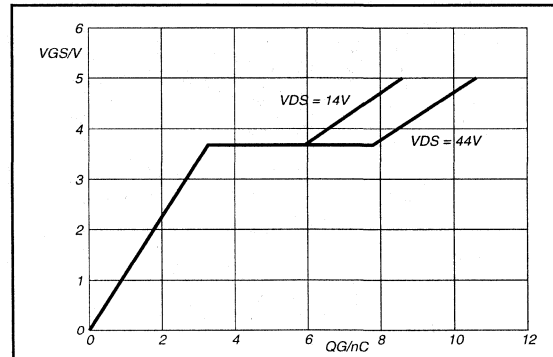


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 20 A; parameter V_{DS}

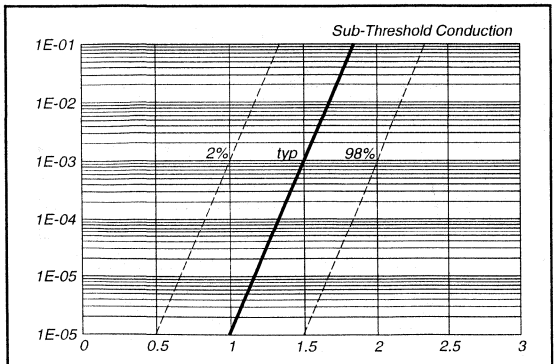


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

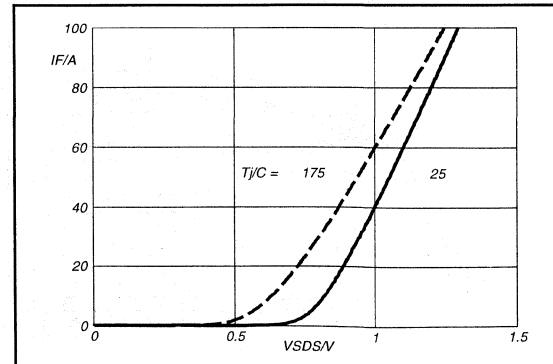


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

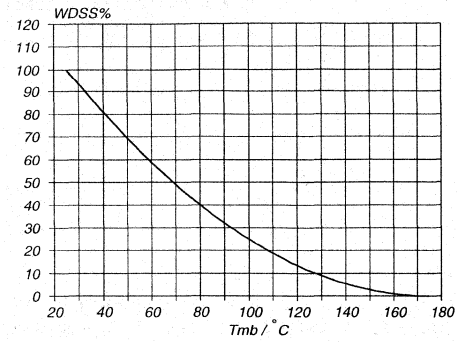


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; *conditions:* I_D = 10 A

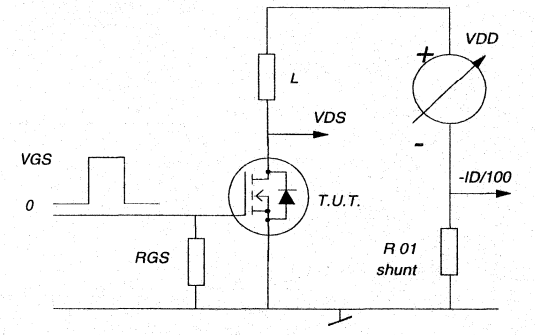


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

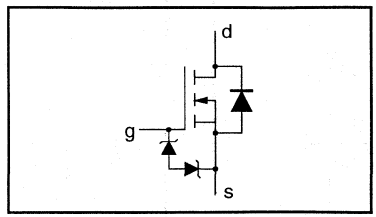
TrenchMOS™ transistor Logic level FET

PHP24N03LT, PHB24N03LT

FEATURES

- **'Trench'** technology
- Very low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 30 V

I_D = 24 A

$R_{DS(ON)} \leq 56\ m\Omega$ (V_{GS} = 5 V)

$R_{DS(ON)} \leq 50\ m\Omega$ (V_{GS} = 10 V)

GENERAL DESCRIPTION

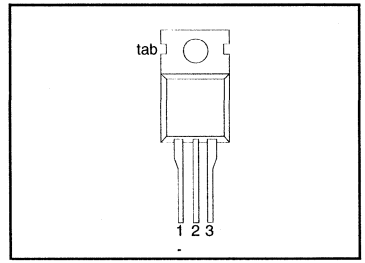
N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using **'trench'** technology. The device has very low on-state resistance. It is intended for use in dc to dc converters and general purpose switching applications.

The PHP24N03LT is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHB24N03LT is supplied in the SOT404 surface mounting package.

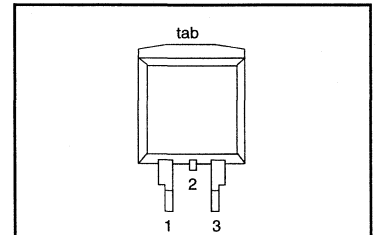
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

SOT78 (TO220AB)



SOT404



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 175°C	-	30	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 175°C; R_{GS} = 20 kΩ	-	30	V
V_{GS}	Gate-source voltage		-	± 13	V
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 5 V	-	24	A
		T_{mb} = 100 °C; V_{GS} = 5 V	-	20	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	96	A
P_D	Total power dissipation	T_{mb} = 25 °C	-	60	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	175	°C

1 It is not possible to make connection to pin 2 of the SOT404 package.

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	SOT78 package, in free air	-	60	-	K/W
		SOT404 package, pcb mounted, minimum footprint	-	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	30	-	-	V
		T_j = -55˚C	27	-	-	V
$V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = 1 mA	10	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	1.5	2	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	50	56	mΩ
		V_{GS} = 10 V; I_D = 25 A	-	45	50	mΩ
		V_{GS} = 5 V; I_D = 12 A; T_j = 175˚C	-	-	104	mΩ
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 12 A	3	5	-	S
I_{GSS}	Gate-source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V;	-	0.02	1	µA
		T_j = 175˚C	-	-	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 30 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
$Q_{g(tot)}$	Total gate charge	I_D = 10 A; V_{DD} = 30 V; V_{GS} = 5 V	-	9	-	nC
Q_{gs}	Gate-source charge		-	2.3	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	5.4	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	12	-	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω	-	50	-	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	30	-	ns
t_f	Turn-off fall time		-	36	-	ns
L_d	Internal drain inductance	Measured tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	460	-	pF
C_{oss}	Output capacitance		-	144	-	pF
C_{rss}	Feedback capacitance		-	78	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)		-	-	24	A
I_{SM}	Pulsed source current (body diode)		-	-	96	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	1.05	1.5	V
t_{rr}	Reverse recovery time	I_F = 12 A; -dI_F/dt = 100 A/µs;	-	50	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 25 V	-	0.1	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 12 A; $V_{DD} \leq$ 15 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 ˚C	-	15	mJ

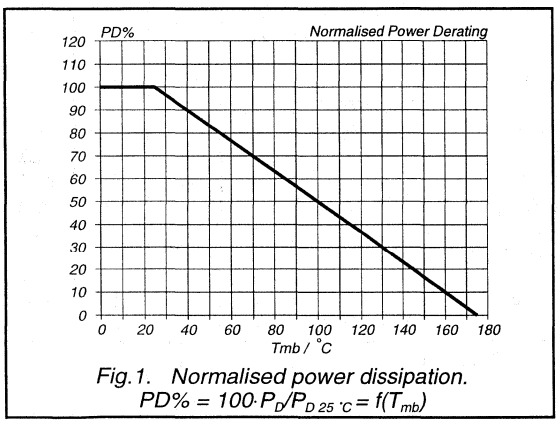


Fig.1. Normalised power dissipation.
PD% = 100·$P_D/P_{D\ 25\ ˚C}$ = f(T_{mb})

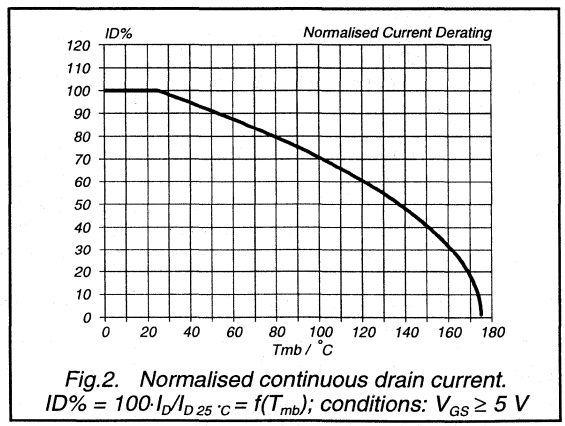


Fig.2. Normalised continuous drain current.
ID% = 100·$I_D/I_{D\ 25\ ˚C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

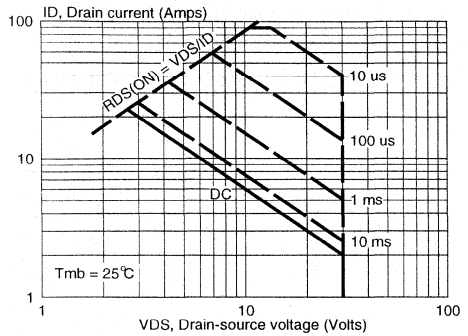


Fig.3. Safe operating area. T_{mb} = 25 ˚C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

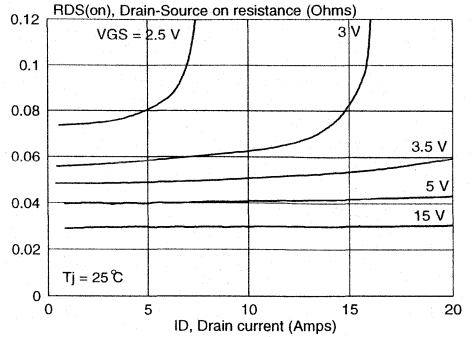


Fig.6. Typical on-state resistance, T_j = 25 ˚C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

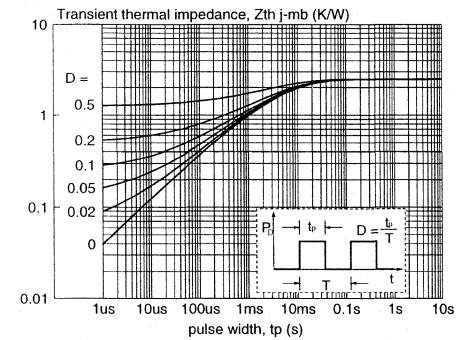


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

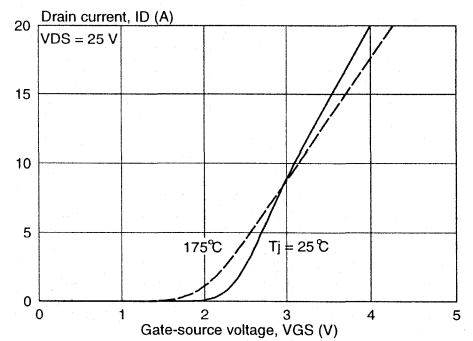


Fig.7. Typical transfer characteristics.
I_D = f(V_{GS}); parameter T_j

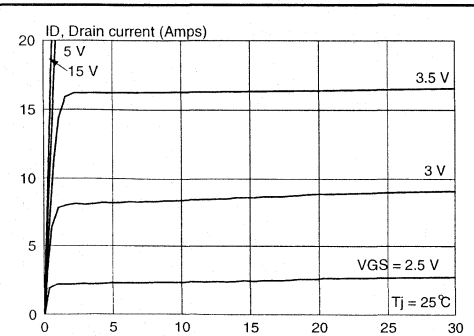


Fig.5. Typical output characteristics, T_j = 25 ˚C.
I_D = f(V_{DS}); parameter V_{GS}

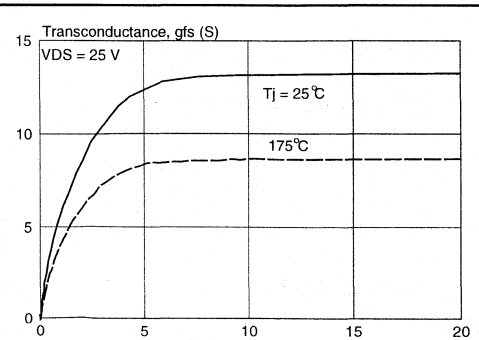


Fig.8. Typical transconductance, T_j = 25 ˚C.
g_{fs} = f(I_D)

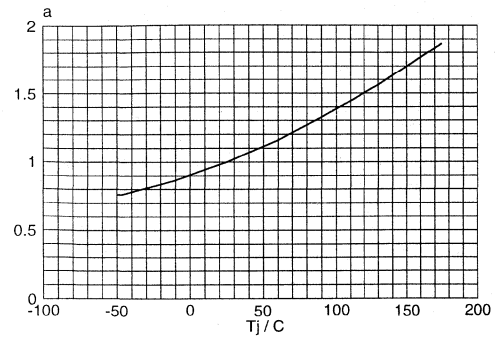


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 12 A; V_{GS} = 5 V

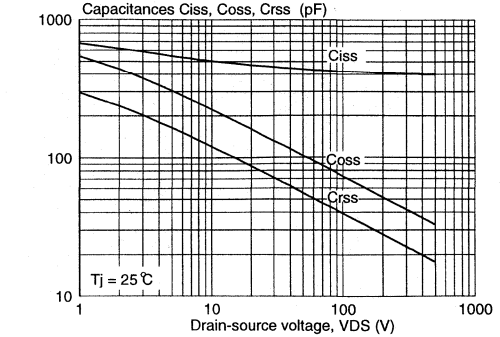


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

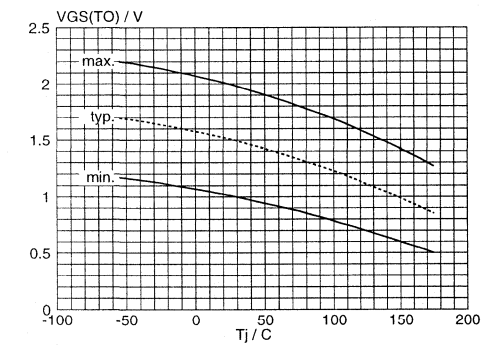


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

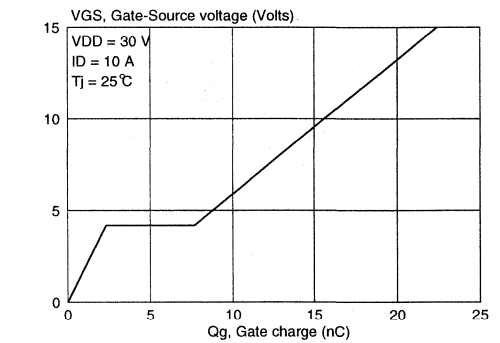


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

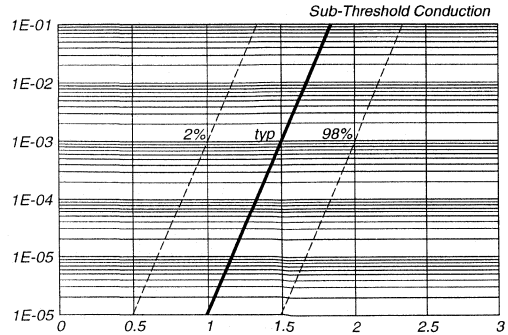


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

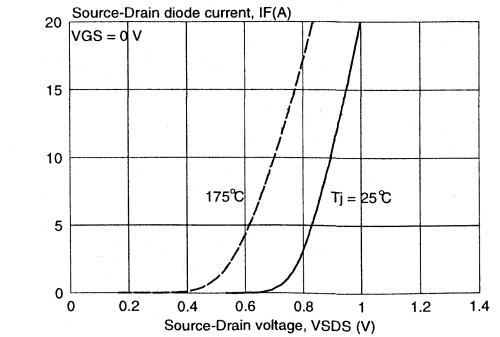


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; parameter T_j

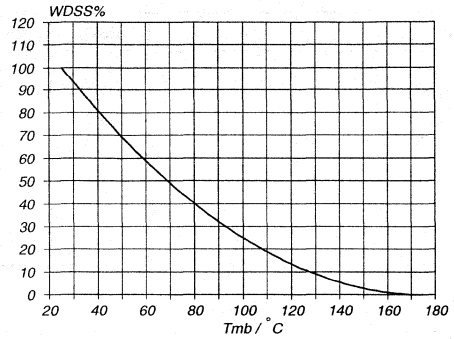


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$

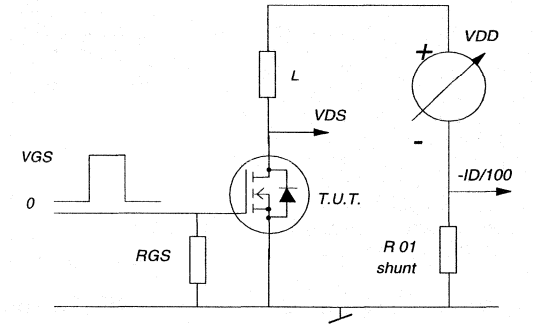


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor — PHP26N10E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

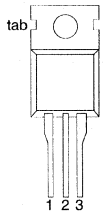
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	26	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.08	Ω

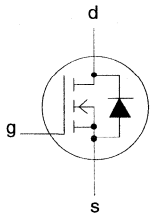
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	26	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	18	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	104	A
P_D	Total dissipation	T_{mb} = 25 °C	-	125	W
$\Delta P_D/\Delta T_{mb}$	Linear derating factor	T_{mb} > 25 °C	-	0.833	W/K
V_{GS}	Gate-source voltage		-	± 30	V
E_{AS}	Single pulse avalanche energy	$V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	230	mJ
I_{AS}	Peak avalanche current	$V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	26	A
T_j, T_{stg}	Operating junction and storage temperature range		- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$\Delta V_{(BR)DSS} / \Delta T_j$	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.15	-	V/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 17 A	-	0.07	0.08	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 50 V; I_D = 17 A	8.7	16	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 100 V; V_{GS} = 0 V	-	1	25	µA
		V_{DS} = 80 V; V_{GS} = 0 V; T_j = 150 °C	-	100	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$Q_{g(tot)}$	Total gate charge	I_D = 17 A; V_{DD} = 80 V; V_{GS} = 10 V	-	35	45	nC
Q_{gs}	Gate-source charge		-	7	9	nC
Q_{gd}	Gate-drain (Miller) charge		-	17	25	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 50 V; I_D = 17 A;	-	18	-	ns
t_r	Turn-on rise time	R_G = 9.1 Ω; R_D = 2.9 Ω	-	40	-	ns
$t_{d(off)}$	Turn-off delay time		-	125	-	ns
t_f	Turn-off fall time		-	50	-	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1650	-	pF
C_{oss}	Output capacitance		-	350	-	pF
C_{rss}	Feedback capacitance		-	100	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	26	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	104	A
V_{SD}	Diode forward voltage	I_S = 28 A; V_{GS} = 0 V	-	-	1.7	V
t_{rr}	Reverse recovery time	I_S = 17 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	90	-	ns
Q_{rr}	Reverse recovery charge		-	0.8	-	µC

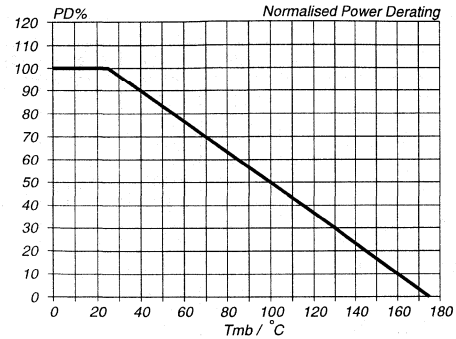


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

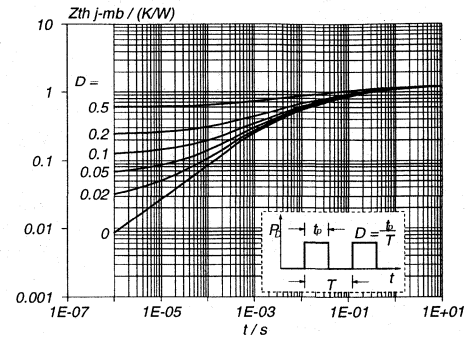


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

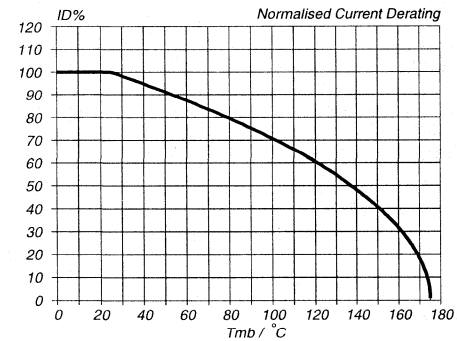


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

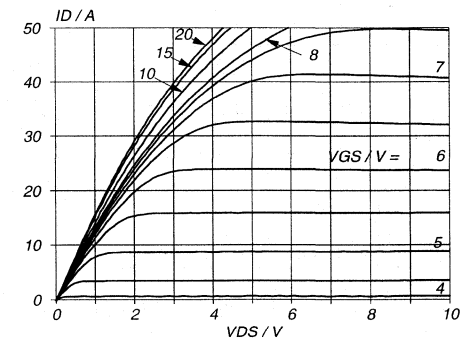


Fig.5. Typical output characteristics.
I_D = f(V_{DS}); parameter V_{GS}

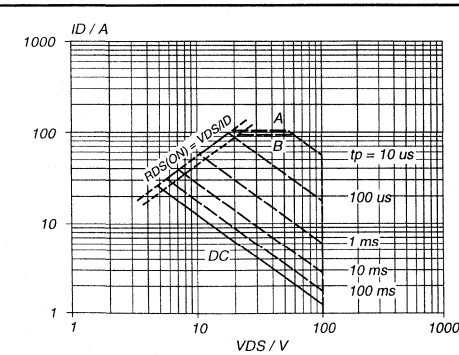


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

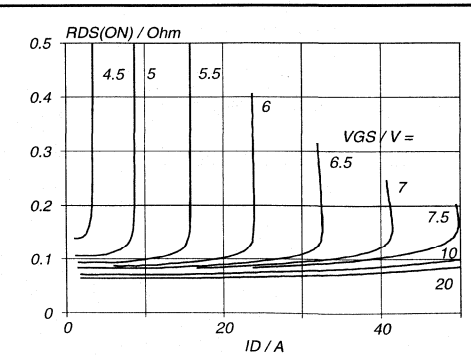


Fig.6. Typical on-state resistance.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

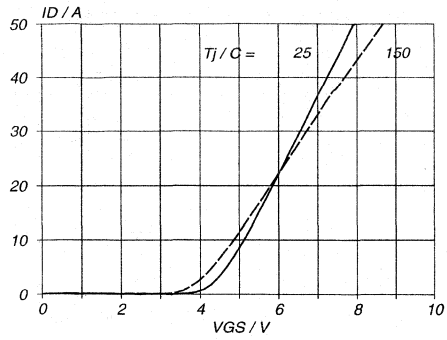


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

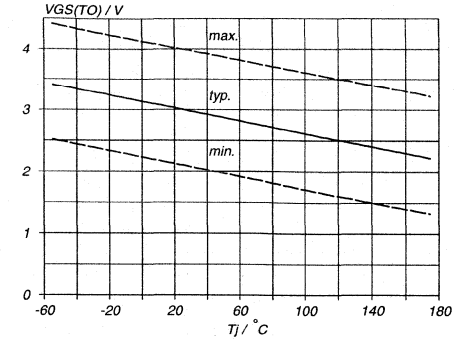


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

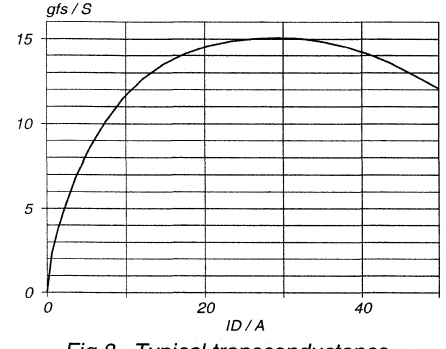


Fig.8. Typical transconductance.
$g_{fs} = f(I_D)$; parameter T_j

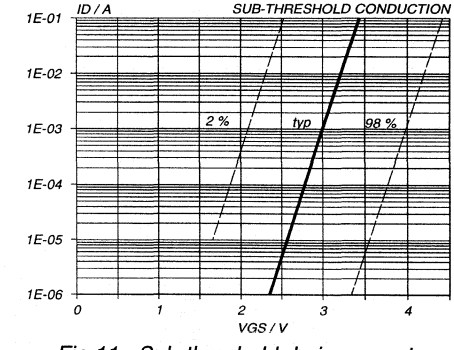


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

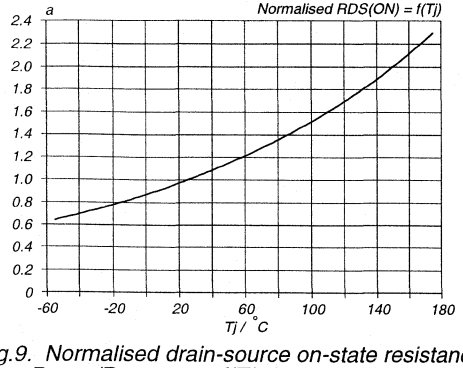


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ °C} = f(T_j)$; I_D = 17 A; V_{GS} = 10 V

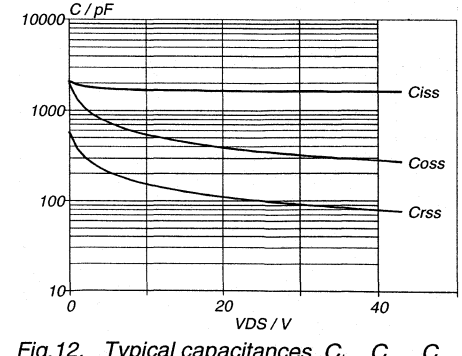


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

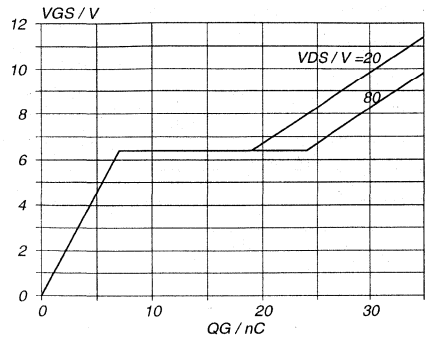


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

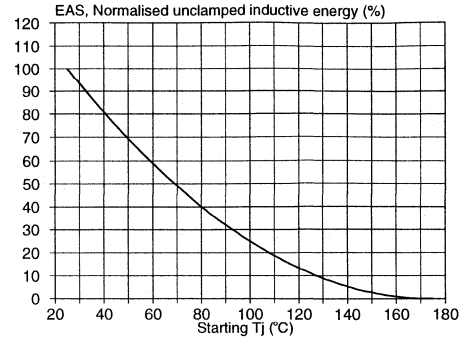


Fig.16. Normalised unclamped inductive energy.
$E_{AS}\% = f(T_j)$

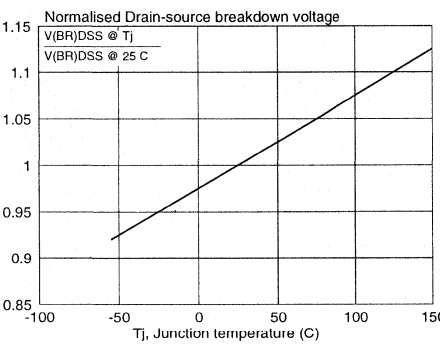


Fig.14. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

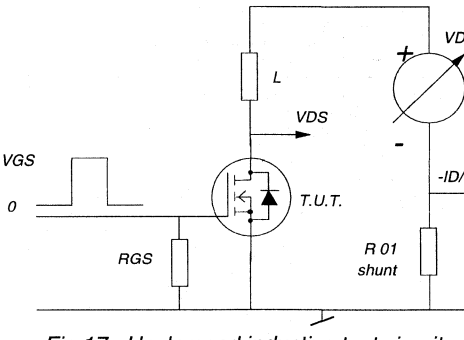


Fig.17. Unclamped inductive test circuit.
$E_{AS} = 0.5 \cdot LI_D^2 \cdot V_{(BR)DSS}/(V_{(BR)DSS} - V_{DD})$

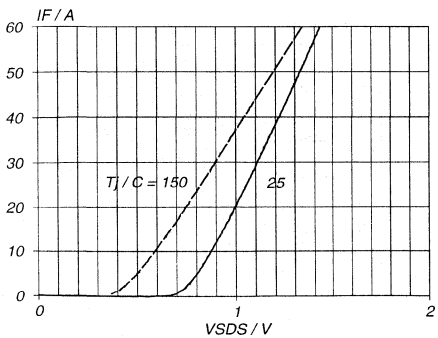


Fig.15. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

PowerMOS transistor | PHP33N10

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope featuring stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

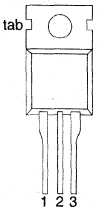
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	34	A
P_{tot}	Total power dissipation	175	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.057	Ω

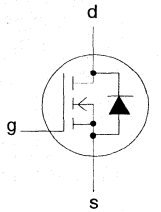
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	34	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	24	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	136	A
P_D	Total dissipation	T_{mb} = 25 °C	-	150	W
$\Delta P_D/\Delta T_{mb}$	Linear derating factor	T_{mb} > 25 °C	-	1.167	W/K
V_{GS}	Gate-source voltage		-	± 30	V
T_j, T_{stg}	Operating junction and storage temperature range		- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.15	-	V/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 17 A	-	0.052	0.057	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 50 V; I_D = 17 A	12	16	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 100 V; V_{GS} = 0 V	-	1	25	µA
		V_{DS} = 80 V; V_{GS} = 0 V; T_j = 150 °C	-	100	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$Q_{g(tot)}$	Total gate charge	I_D = 17 A; V_{DD} = 80 V; V_{GS} = 10 V	-	42	50	nC
Q_{gs}	Gate-source charge		-	8	11	nC
Q_{gd}	Gate-drain (Miller) charge		-	20	30	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 50 V; I_D = 17 A;	-	18	-	ns
t_r	Turn-on rise time	R_G = 9.1 Ω; R_D = 2.9 Ω	-	40	-	ns
$t_{d(off)}$	Turn-off delay time		-	125	-	ns
t_f	Turn-off fall time		-	50	-	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1500	-	pF
C_{oss}	Output capacitance		-	450	-	pF
C_{rss}	Feedback capacitance		-	130	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	34	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	136	A
V_{SD}	Diode forward voltage	I_S = 34 A; V_{GS} = 0 V	-	-	1.5	V
t_{rr}	Reverse recovery time	I_S = 17 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	200	-	ns
Q_{rr}	Reverse recovery charge		-	1.0	-	µC

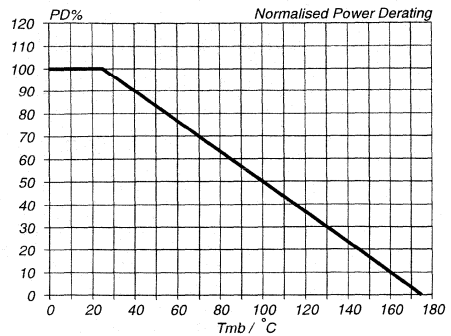


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

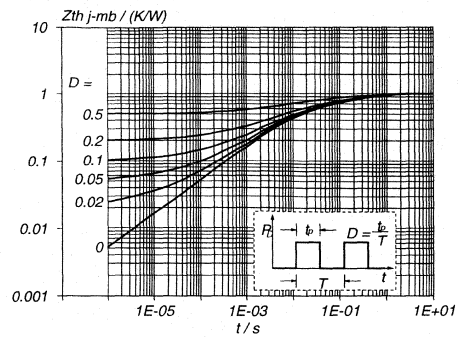


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

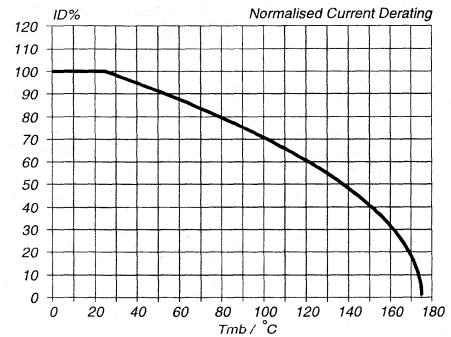


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

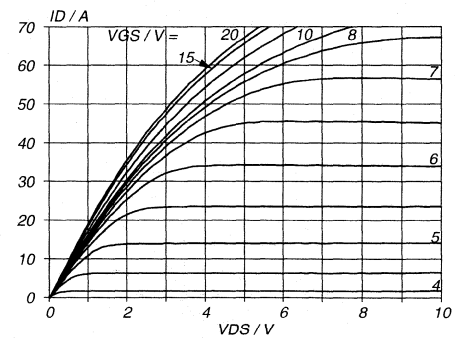


Fig.5. Typical output characteristics.
I_D = f(V_{DS}); parameter V_{GS}

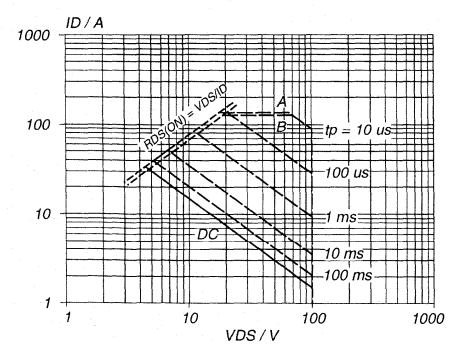


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

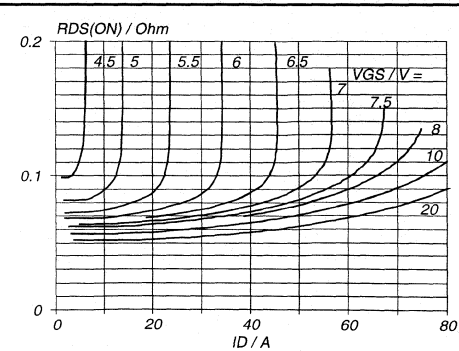


Fig.6. Typical on-state resistance.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

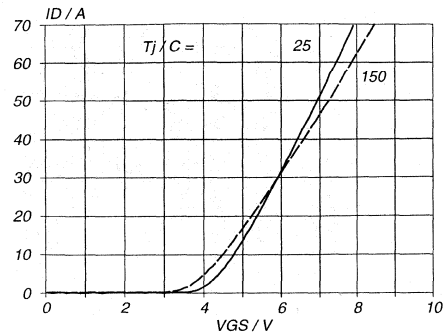


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

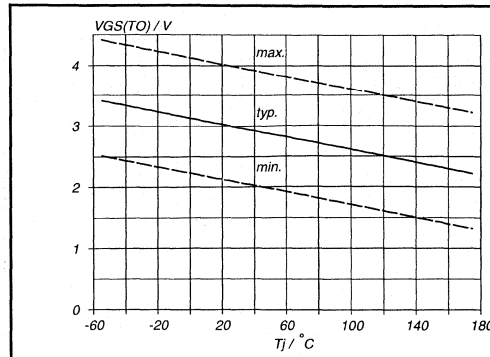


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 0.25$ mA; $V_{DS} = V_{GS}$

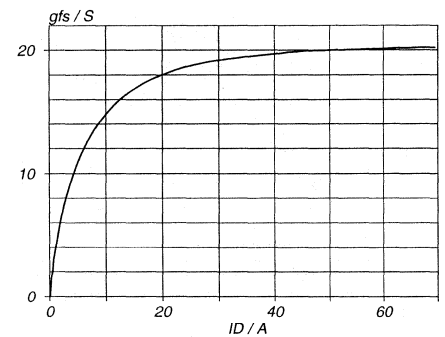


Fig.8. Typical transconductance.
$g_{fs} = f(I_D)$; parameter T_j

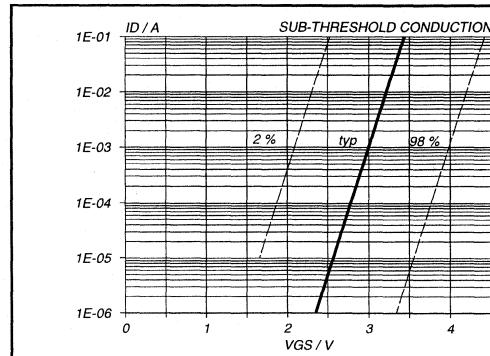


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

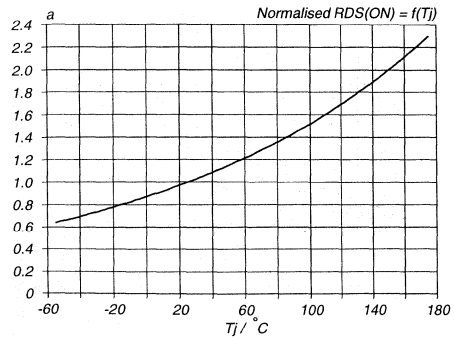


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 17$ A; $V_{GS} = 10$ V

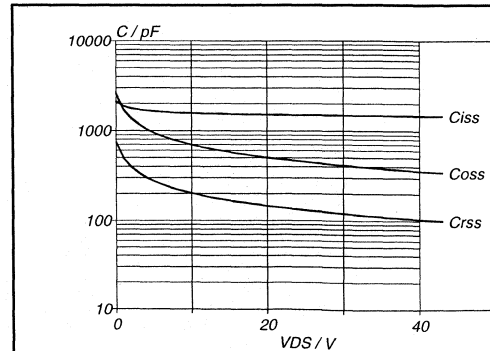


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

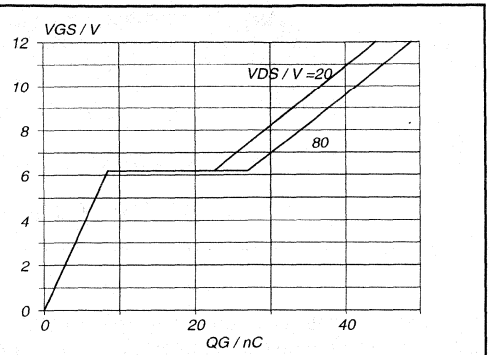


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; parameter V_{DS}

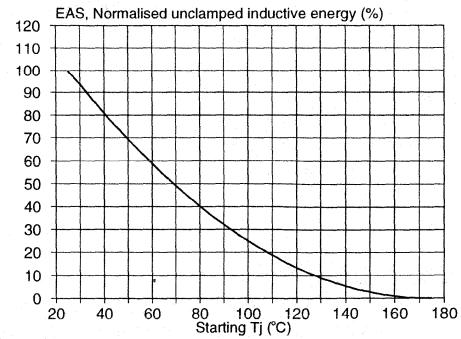


Fig.16. Normalised unclamped inductive energy. $E_{AS}\% = f(T_j)$

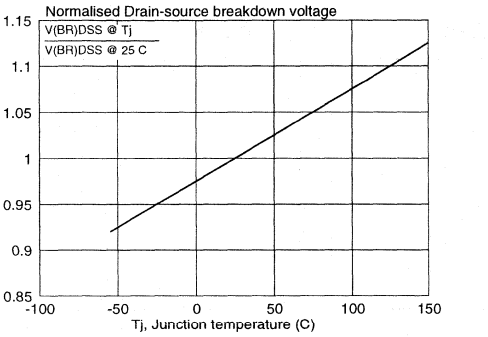


Fig.14. Normalised drain-source breakdown voltage. $V_{(BR)DSS}/V_{(BR)DSS\ 25\ ^\circ C} = f(T_j)$

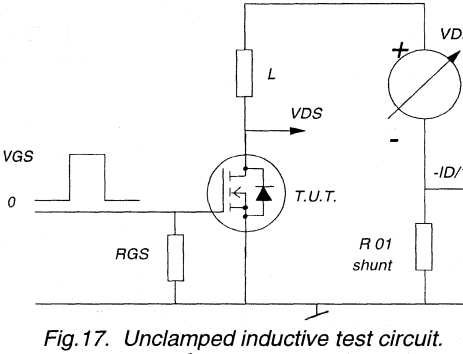


Fig.17. Unclamped inductive test circuit. $E_{AS} = 0.5 \cdot LI_D^2 \cdot V_{(BR)DSS}/(V_{(BR)DSS} - V_{DD})$

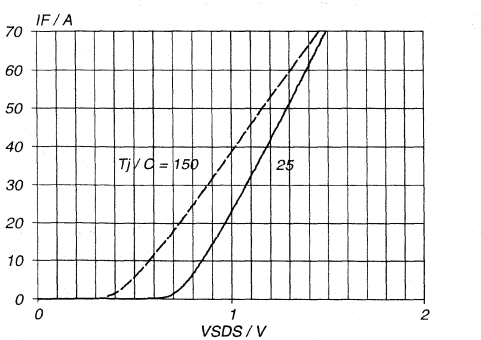


Fig.15. Source-Drain diode characteristic. $I_F = f(V_{SDS})$; parameter T_j

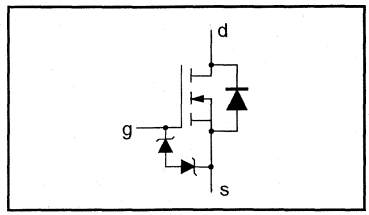
TrenchMOS™ transistor Logic level FET

PHP37N06LT, PHB37N06LT

FEATURES

- **'Trench'** technology
- Very low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 55 V

I_D = 37 A

$R_{DS(ON)} \leq 35\ m\Omega$ (V_{GS} = 5 V)

$R_{DS(ON)} \leq 32\ m\Omega$ (V_{GS} = 10 V)

GENERAL DESCRIPTION

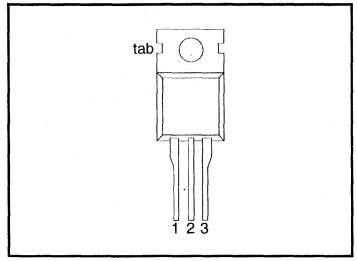
N-channel enhancement mode, logic level, field-effect power transistor in a plastic envelope using **'trench'** technology. The device has very low on-state resistance. It is intended for use in dc to dc converters and general purpose switching applications.

The PHP37N06LT is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHB37N06LT is supplied in the SOT404 surface mounting package.

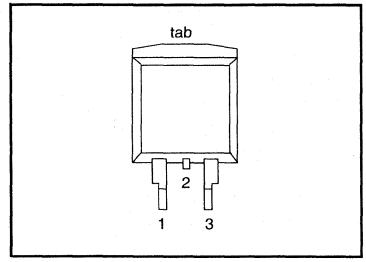
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

SOT78 (TO220AB)



SOT404



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 175°C	-	55	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 175°C; R_{GS} = 20 kΩ	-	55	V
V_{GS}	Gate-source voltage		-	± 13	V
I_D	Continuous drain current	T_{mb} = 25 °C	-	37	A
		T_{mb} = 100 °C	-	26	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	148	A
P_D	Total power dissipation	T_{mb} = 25 °C	-	100	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	175	°C

1 It is not possible to make connection to pin 2 of the SOT404 package.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	1.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	SOT78 package, in free air	60	-	K/W
		SOT404 package, pcb mounted, minimum footprint	50	-	K/W

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

ELECTRICAL CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 17 A	-	28	35	mΩ
		V_{GS} = 10 V; I_D = 17 A	-	26	32	mΩ
		T_j = 175˚C	-	-	74	mΩ
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 15 A	12	40	-	S
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	20	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
$Q_{g(tot)}$	Total gate charge	I_D = 30 A; V_{DD} = 44 V; V_{GS} = 5 V	-	22.5	-	nC
Q_{gs}	Gate-source charge		-	6	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	11	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	14	21	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω	-	77	110	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	55	80	ns
t_f	Turn-off fall time		-	48	65	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1050	1400	pF
C_{oss}	Output capacitance		-	205	245	pF
C_{rss}	Feedback capacitance		-	113	150	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)		-	-	37	A
I_{SM}	Pulsed source current (body diode)		-	-	148	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 34 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 34 A; -dI_F/dt = 100 A/µs;	-	40	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.16	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 20 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 ˚C	-	45	mJ

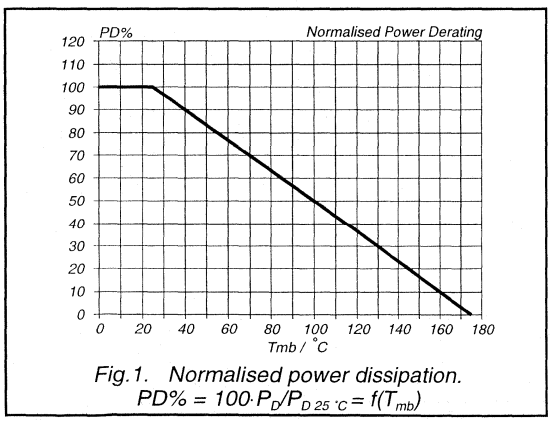


Fig.1. Normalised power dissipation.
PD% = 100·$P_D/P_{D\,25\,°C}$ = f(T_{mb})

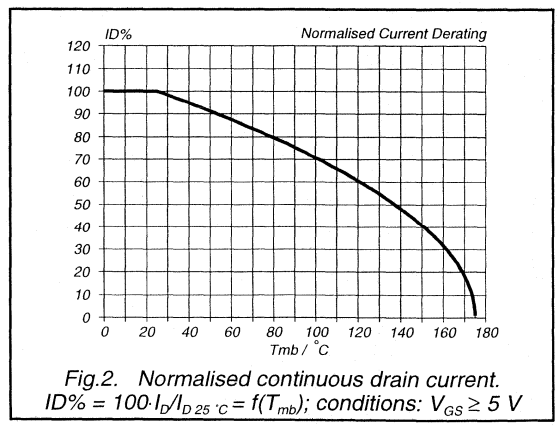


Fig.2. Normalised continuous drain current.
ID% = 100·$I_D/I_{D\,25\,°C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

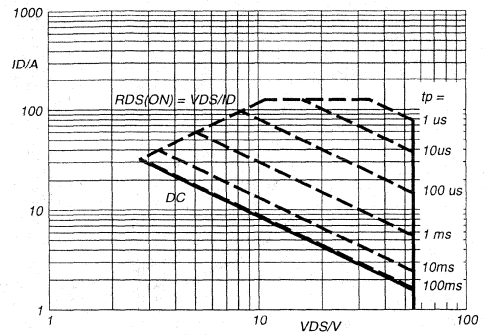


Fig.3. Safe operating area. T_{mb} = 25 ˚C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

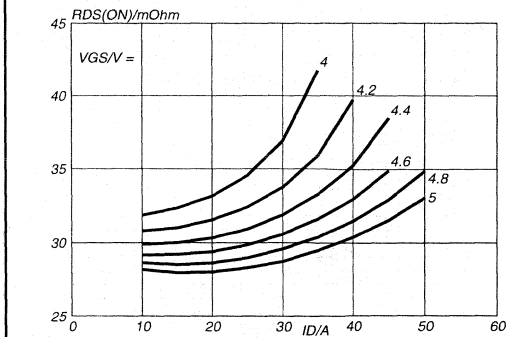


Fig.6. Typical on-state resistance, T_j = 25 ˚C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

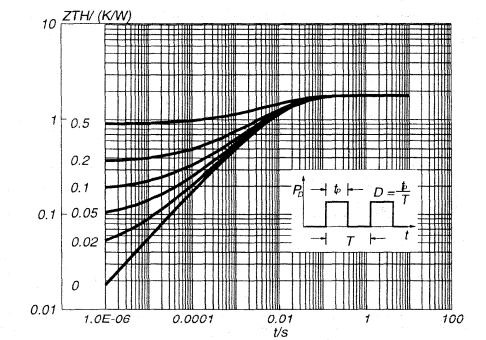


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

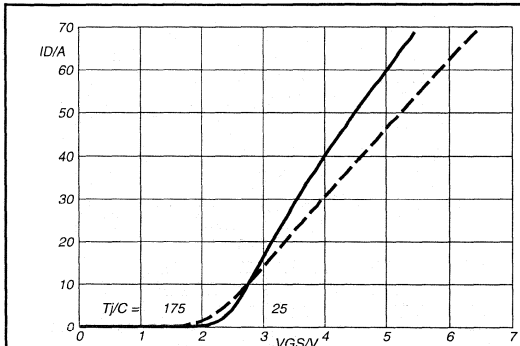


Fig.7. Typical transfer characteristics.
I_D = f(V_{GS}) ; conditions: V_{DS} = 25 V; parameter T_j

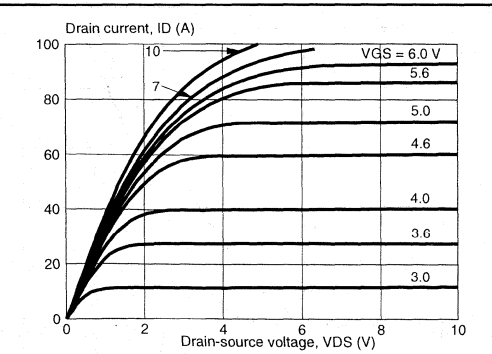


Fig.5. Typical output characteristics, T_j = 25 ˚C.
I_D = f(V_{DS}); parameter V_{GS}

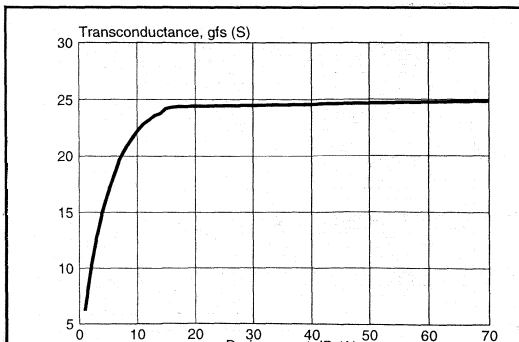


Fig.8. Typical transconductance, T_j = 25 ˚C.
g_{fs} = f(I_D); conditions: V_{DS} = 25 V

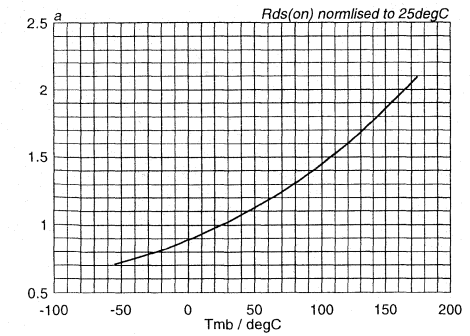


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 17 A; V_{GS} = 5 V

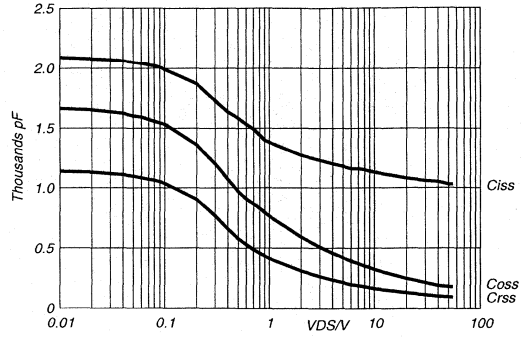


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

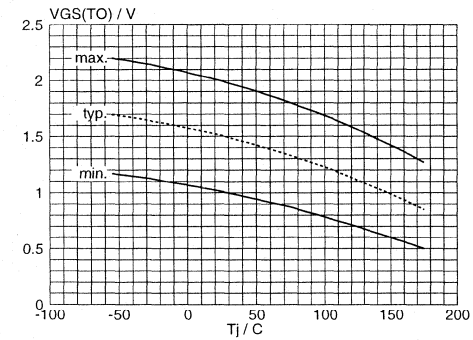


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

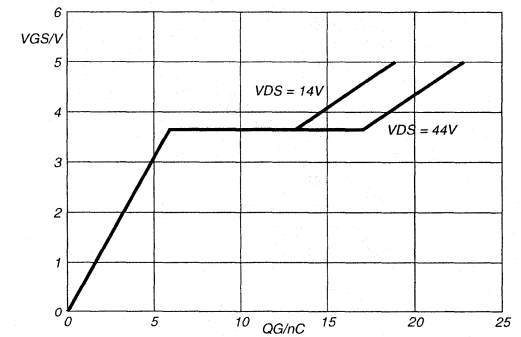


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 30 A; parameter V_{DS}

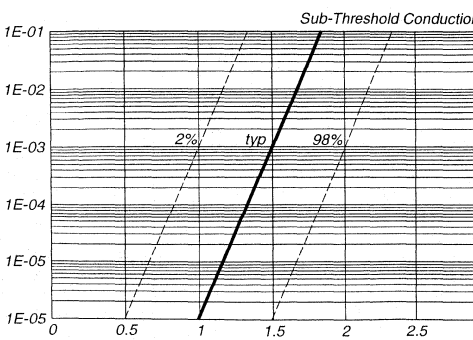


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

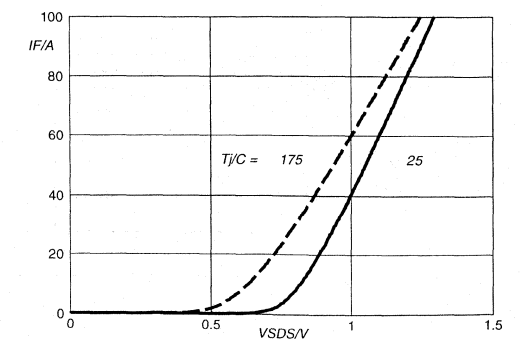


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

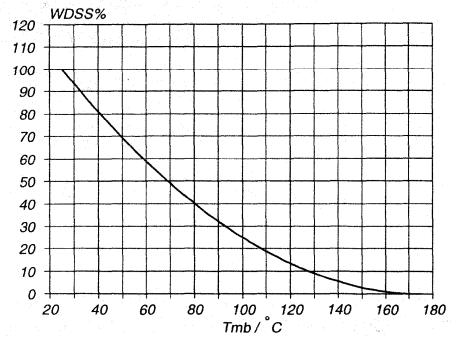


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: I_D = 20 A

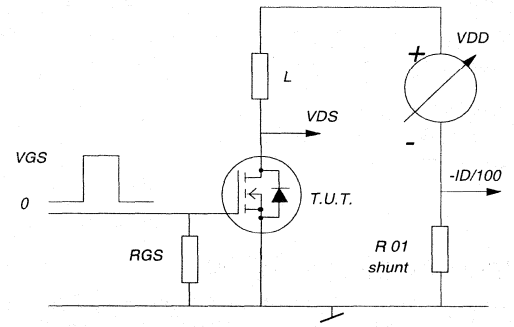


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

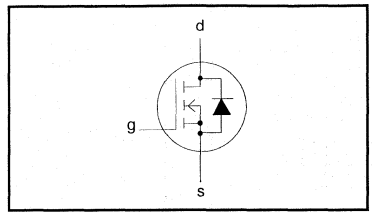
TrenchMOS™ transistor Logic level FET

PHP42N03LT, PHB42N03LT, PHD42N03LT

FEATURES

- **'Trench'** technology
- Very low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 30 V

I_D = 42 A

$R_{DS(ON)} \leq 26\ m\Omega$ (V_{GS} = 5 V)

$R_{DS(ON)} \leq 23\ m\Omega$ (V_{GS} = 10 V)

GENERAL DESCRIPTION

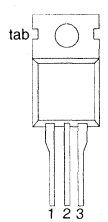
N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using **'trench'** technology. The device has very low on-state resistance. It is intended for use in dc to dc converters and general purpose switching applications.

The PHP42N03LT is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHB42N03LT is supplied in the SOT404 surface mounting package.
The PHD42N03LT is supplied in the SOT428 surface mounting package.

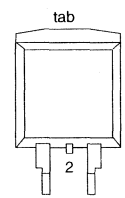
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

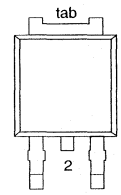
SOT78 (TO220AB)



SOT404



SOT428



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 175°C	-	30	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 175°C; R_{GS} = 20 kΩ	-	30	V
V_{GS}	Gate-source voltage		-	± 15	V
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 5 V	-	42	A
		T_{mb} = 100 °C; V_{GS} = 5 V	-	30	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	168	A
P_D	Total power dissipation	T_{mb} = 25 °C	-	86	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	175	°C

1 It is not possible to make connection to pin 2 of the SOT428 or SOT404 packages.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.75	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	SOT78 package, in free air	-	60	-	K/W
		SOT404 and SOT428 packages, pcb mounted, minimum footprint	-	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	30	-	-	V
		T_j = -55˚C	27	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	1.5	2	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	20	26	mΩ
		V_{GS} = 10 V; I_D = 25 A	-	16	23	mΩ
		V_{GS} = 5 V; I_D = 25 A; T_j = 175˚C	-	-	48	mΩ
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	8	27	-	S
I_{DSS}	Zero gate voltage drain current	V_{DS} = 30 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	10	100	nA
$Q_{g(tot)}$	Total gate charge	I_D = 40 A; V_{DD} = 24 V; V_{GS} = 5 V	-	23	-	nC
Q_{gs}	Gate-source charge		-	7	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	10	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 15 V; I_D = 25 A;	-	12	20	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 5 Ω	-	80	130	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	35	60	ns
t_f	Turn-off fall time		-	31	45	ns
L_d	Internal drain inductance	Measured tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1050	-	pF
C_{oss}	Output capacitance		-	270	-	pF
C_{rss}	Feedback capacitance		-	140	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)		-	-	45	A
I_{SM}	Pulsed source current (body diode)		-	-	180	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V I_F = 40 A; V_{GS} = 0 V	- -	0.95 1.0	1.2 -	V
t_{rr} Q_{rr}	Reverse recovery time Reverse recovery charge	I_F = 40 A; -dI_F/dt = 100 A/µs; V_{GS} = -10 V; V_R = 25 V	- -	52 0.08	- -	ns µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 25 A; $V_{DD} \leq$ 15 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 ˚C	-	60	mJ

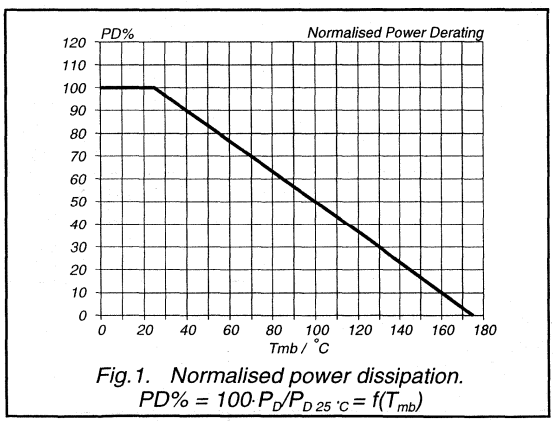


Fig.1. Normalised power dissipation.
PD% = 100·$P_D/P_{D\ 25\ ˚C}$ = f(T_{mb})

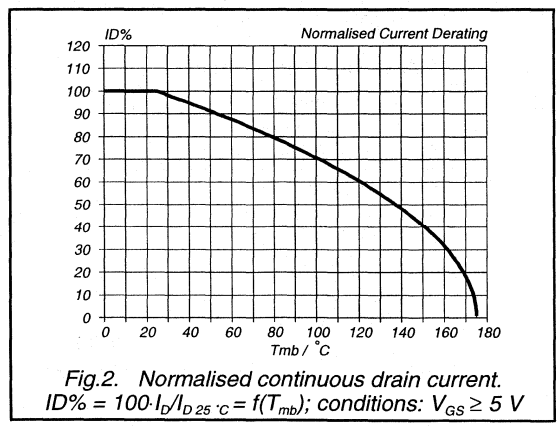


Fig.2. Normalised continuous drain current.
ID% = 100·$I_D/I_{D\ 25\ ˚C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

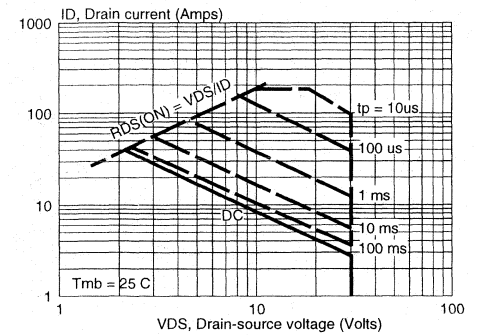


Fig.3. Safe operating area
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

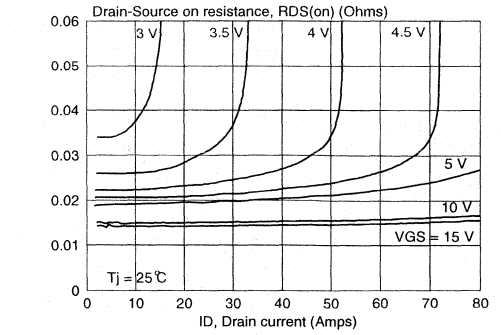


Fig.6. Typical on-state resistance
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

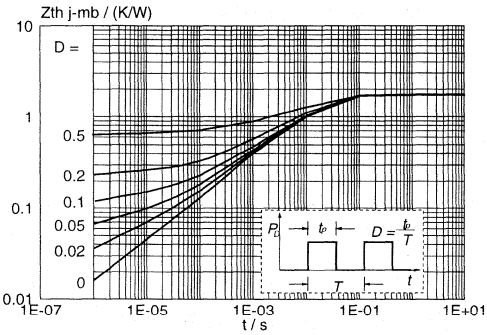


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

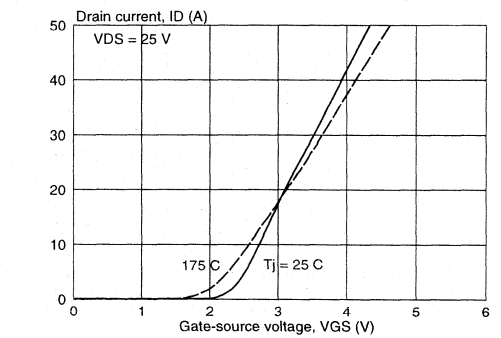


Fig.7. Typical transfer characteristics.
I_D = f(V_{GS})

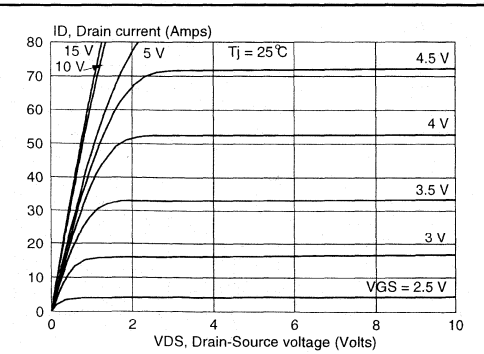


Fig.5. Typical output characteristics
I_D = f(V_{DS}); parameter V_{GS}

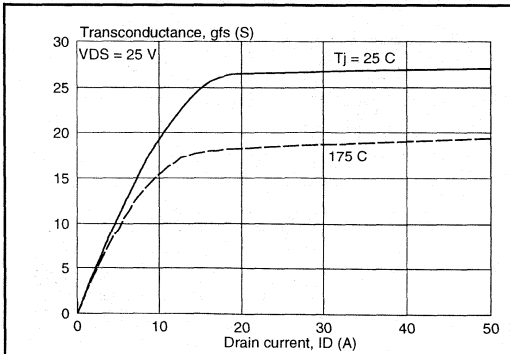


Fig.8. Typical transconductance
g_{fs} = f(I_D)

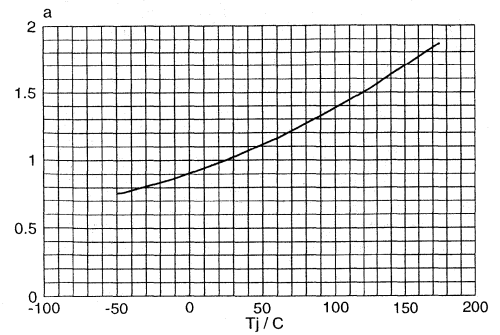


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

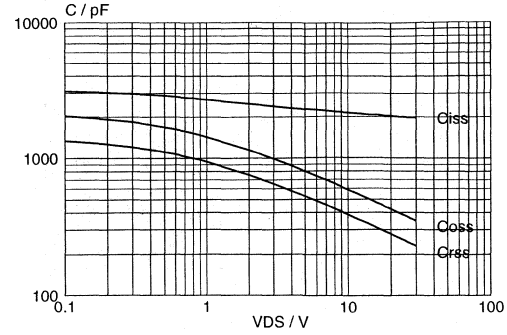


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; V_{GS} = 0 V; f = 1 MHz

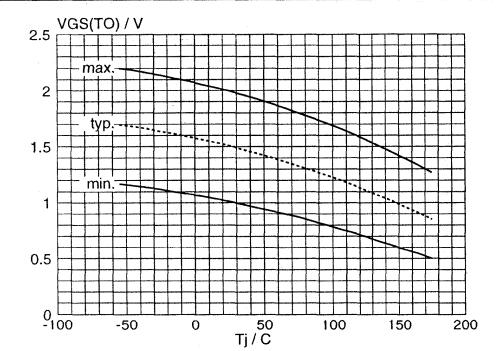


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

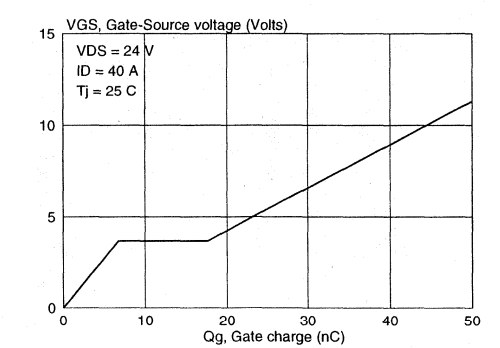


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$

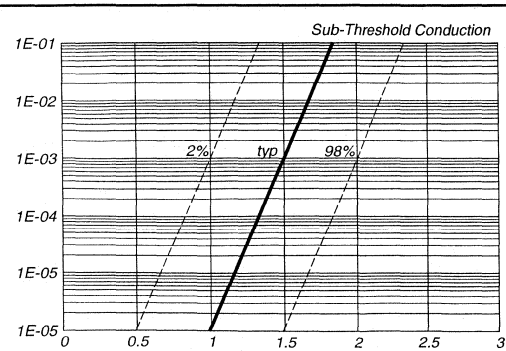


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; $V_{DS} = V_{GS}$

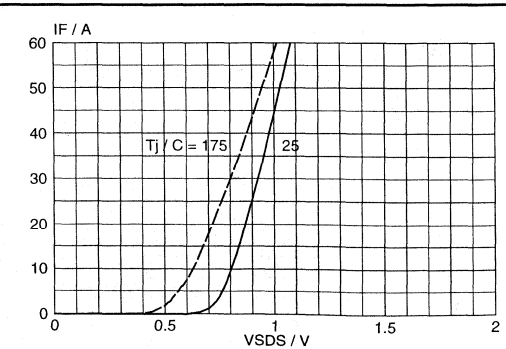


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$

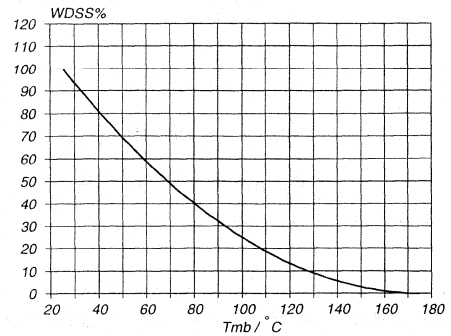


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; I_D = 25 A

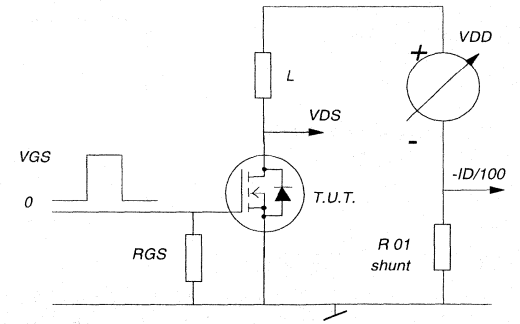


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

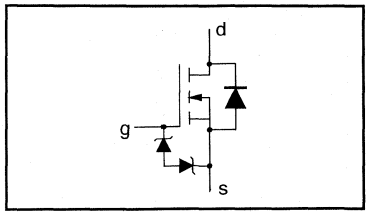
TrenchMOS™ transistor Logic level FET

PHP44N06LT, PHB44N06LT

FEATURES

- **'Trench'** technology
- Very low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 55 V

I_D = 44 A

$R_{DS(ON)} \leq 28\ m\Omega$ (V_{GS} = 5 V)

$R_{DS(ON)} \leq 26\ m\Omega$ (V_{GS} = 10 V)

GENERAL DESCRIPTION

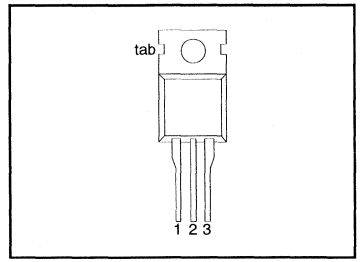
N-channel enhancement mode, logic level, field-effect power transistor in a plastic envelope using **'trench'** technology. The device has very low on-state resistance. It is intended for use in dc to dc converters and general purpose switching applications.

The PHP44N06LT is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHB44N06LT is supplied in the SOT404 surface mounting package.

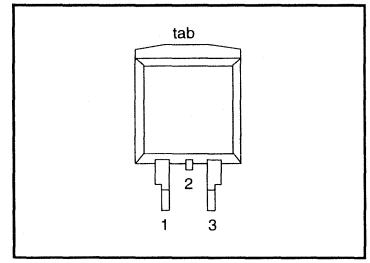
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

SOT78 (TO220AB)



SOT404



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 175°C	-	55	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 175°C; R_{GS} = 20 kΩ	-	55	V
V_{GS}	Gate-source voltage		-	± 13	V
I_D	Continuous drain current	T_{mb} = 25 °C	-	44	A
		T_{mb} = 100 °C	-	31	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	176	A
P_D	Total power dissipation	T_{mb} = 25 °C	-	114	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	175	°C

1 It is not possible to make connection to pin 2 of the SOT404 package.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	1.31	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	SOT78 package, in free air	60	-	K/W
		SOT404 package, pcb mounted, minimum footprint	50	-	K/W

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

ELECTRICAL CHARACTERISTICS

T_j= 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55°C	50	-	-	V
$V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
		T_j = 175°C	0.5	-	-	V
		T_j = -55°C	-	-	2.3	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 20 A	-	22	28	mΩ
		V_{GS} = 10 V; I_D = 20 A	-	20	26	mΩ
		T_j = 175°C	-	-	59	mΩ
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	13	40	-	S
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175°C	-	-	20	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175°C	-	-	500	µA
$Q_{g(tot)}$	Total gate charge	I_D = 40 A; V_{DD} = 44 V; V_{GS} = 5 V	-	27.5	-	nC
Q_{gs}	Gate-source charge		-	7	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	13	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	22	32	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω	-	85	125	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	70	95	ns
t_f	Turn-off fall time		-	64	85	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1300	1700	pF
C_{oss}	Output capacitance		-	250	300	pF
C_{rss}	Feedback capacitance		-	130	180	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)		-	-	44	A
I_{SM}	Pulsed source current (body diode)		-	-	176	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 40 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 40 A; -dI_F/dt = 100 A/µs;	-	41	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.16	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 35 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	70	mJ

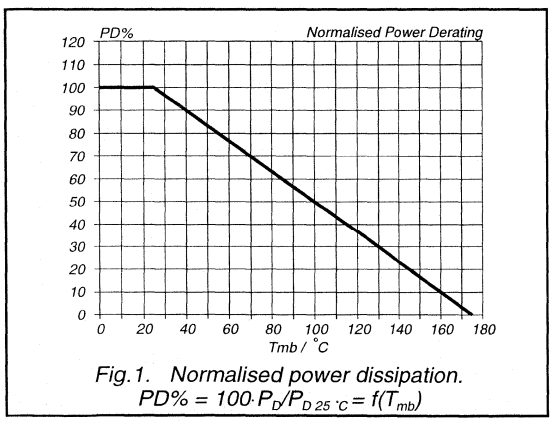


Fig.1. Normalised power dissipation.
PD% = 100·$P_D/P_{D\ 25\ °C}$ = f(T_{mb})

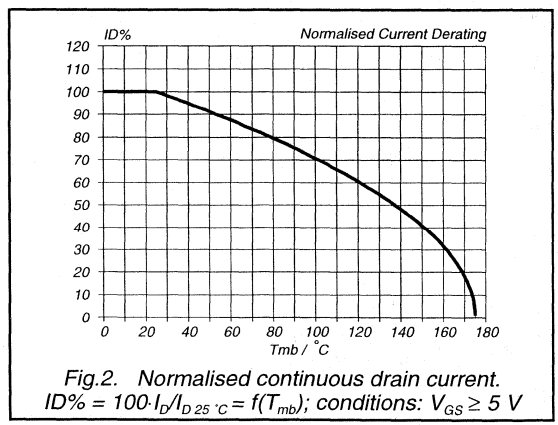


Fig.2. Normalised continuous drain current.
ID% = 100·$I_D/I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

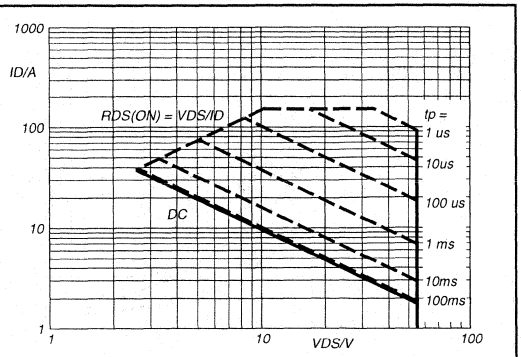


Fig.3. Safe operating area. T_{mb} = 25 ˚C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

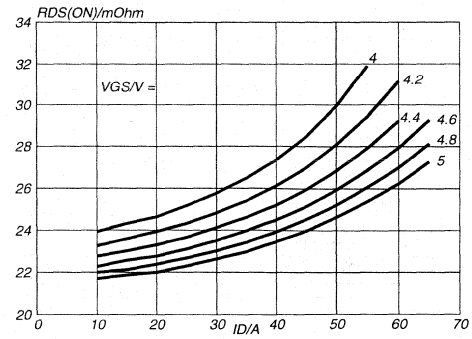


Fig.6. Typical on-state resistance, T_j = 25 ˚C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

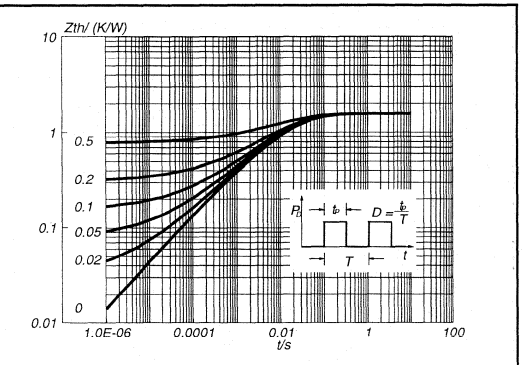


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

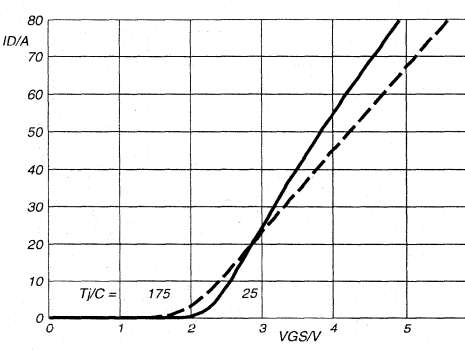


Fig.7. Typical transfer characteristics.
I_D = f(V_{GS}) ; conditions: V_{DS} = 25 V; parameter T_j

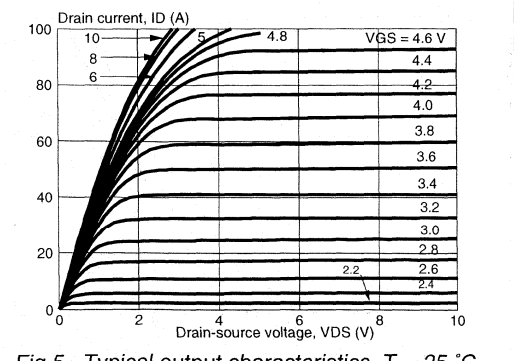


Fig.5. Typical output characteristics, T_j = 25 ˚C.
I_D = f(V_{DS}); parameter V_{GS}

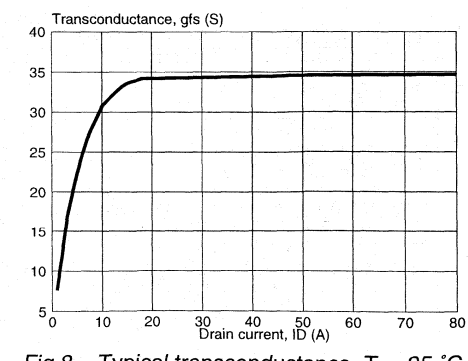


Fig.8. Typical transconductance, T_j = 25 ˚C.
g_{fs} = f(I_D); conditions: V_{DS} = 25 V

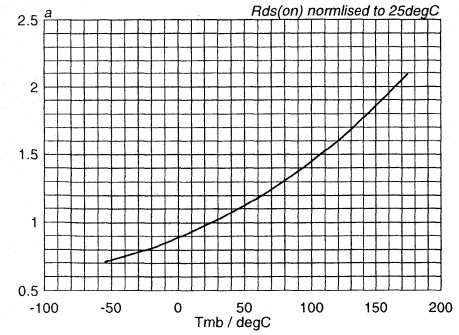


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 20 A; V_{GS} = 5 V

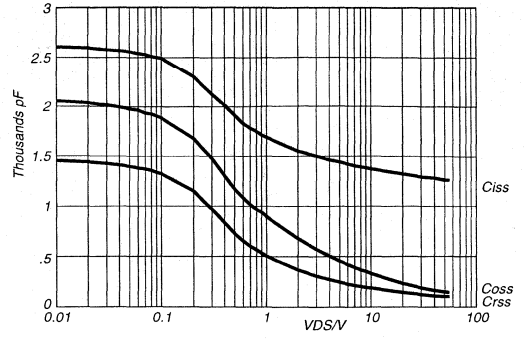


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

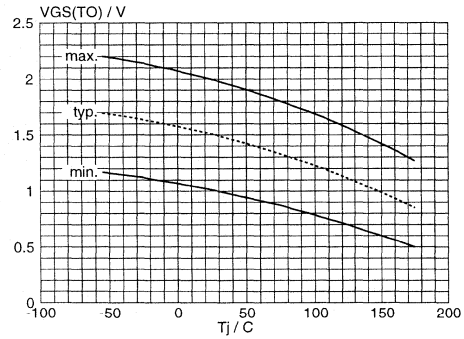


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

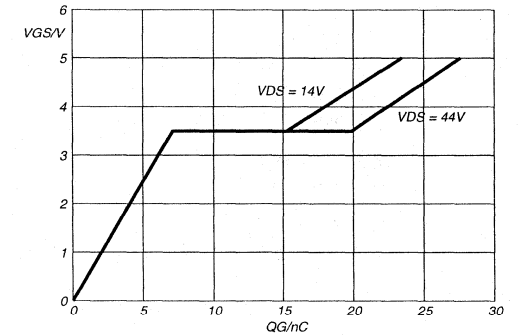


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 40 A; parameter V_{DS}

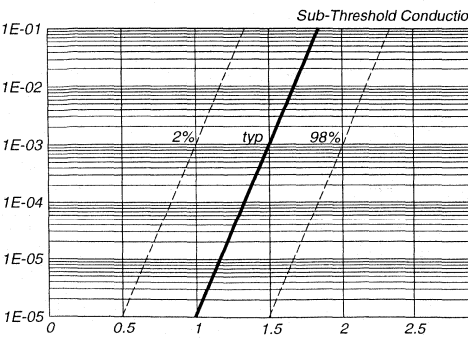


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

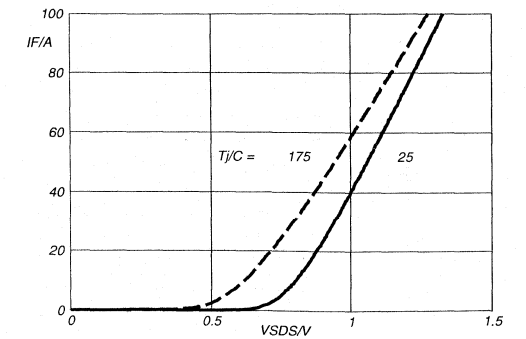


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

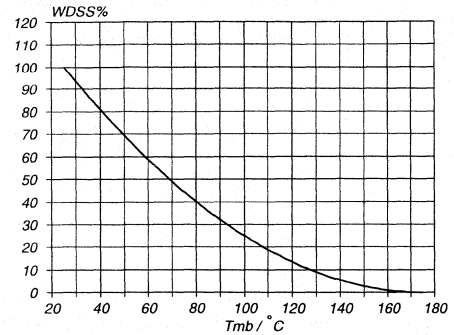


Fig.15. Normalised avalanche energy rating.
W_{DSS}% = f(T_{mb}); conditions: I_D = 35 A

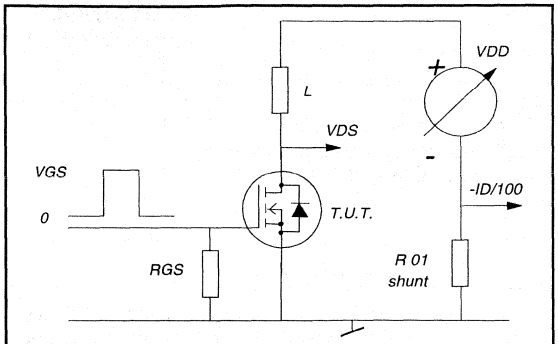


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

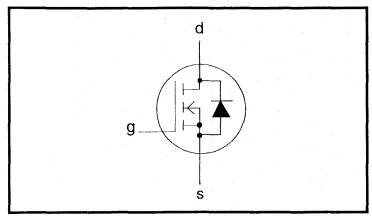
TrenchMOS™ transistor Logic level FET

PHP45N03LT, PHB45N03LT, PHD45N03LT

FEATURES

- **'Trench'** technology
- Very low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 30 V

I_D = 45 A

$R_{DS(ON)} \leq 24\ m\Omega$ (V_{GS} = 5 V)

$R_{DS(ON)} \leq 21\ m\Omega$ (V_{GS} = 10 V)

GENERAL DESCRIPTION

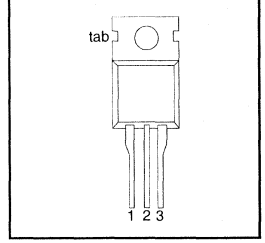
N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using **'trench'** technology. The device has very low on-state resistance. It is intended for use in dc to dc converters and general purpose switching applications.

The PHP45N03LT is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHB45N03LT is supplied in the SOT404 surface mounting package.
The PHD45N03LT is supplied in the SOT428 surface mounting package.

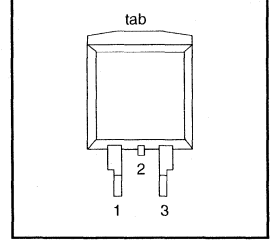
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

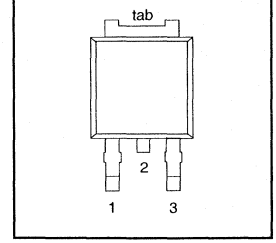
SOT78 (TO220AB)



SOT404



SOT428



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 175°C	-	30	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 175°C; R_{GS} = 20 kΩ	-	30	V
V_{GS}	Gate-source voltage		-	± 15	V
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	45	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	33	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	180	A
P_D	Total power dissipation	T_{mb} = 25 °C	-	86	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	175	°C

1 It is not possible to make connection to pin 2 of the SOT428 or SOT404 packages.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.75	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	SOT78 package, in free air	-	60	-	K/W
		SOT404 and SOT428 packages, pcb mounted, minimum footprint	-	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	30	-	-	V
		T_j = -55˚C	27	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	1.5	2	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	20	24	mΩ
		V_{GS} = 10 V; I_D = 25 A	-	16	21	mΩ
		V_{GS} = 5 V; I_D = 25 A; T_j = 175˚C	-	-	45	mΩ
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	8	27	-	S
I_{DSS}	Zero gate voltage drain current	V_{DS} = 30 V; V_{GS} = 0 V;	-	0.05	10	μA
		T_j = 175˚C	-	-	500	μA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	10	100	nA
$Q_{g(tot)}$	Total gate charge	I_D = 40 A; V_{DD} = 24 V; V_{GS} = 5 V	-	23	-	nC
Q_{gs}	Gate-source charge		-	7	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	10	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 15 V; I_D = 25 A;	-	12	20	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 5 Ω	-	80	130	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	35	60	ns
t_f	Turn-off fall time		-	31	45	ns
L_d	Internal drain inductance	Measured tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1050	-	pF
C_{oss}	Output capacitance		-	270	-	pF
C_{rss}	Feedback capacitance		-	140	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)		-	-	45	A
I_{SM}	Pulsed source current (body diode)		-	-	180	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 40 A; V_{GS} = 0 V	-	1.0	-	
t_{rr}	Reverse recovery time	I_F = 40 A; -dI_F/dt = 100 A/µs;	-	52	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 25 V	-	0.08	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 25 A; $V_{DD} \leq$ 15 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 ˚C	-	60	mJ

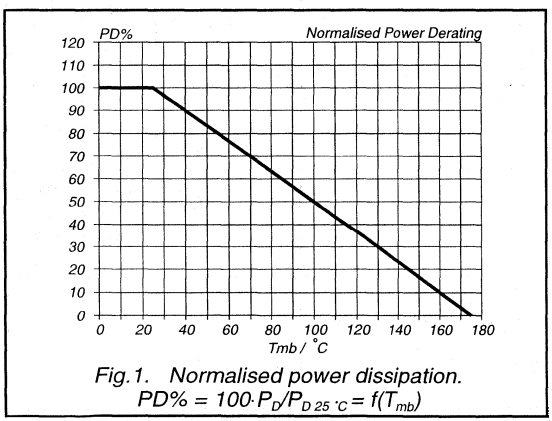


Fig.1. Normalised power dissipation.
PD% = 100·$P_D/P_{D\ 25\ ˚C}$ = f(T_{mb})

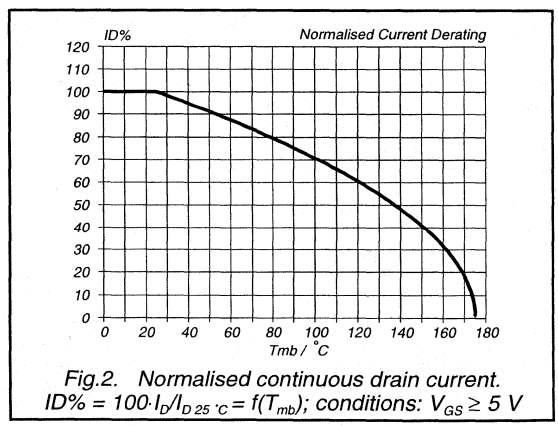


Fig.2. Normalised continuous drain current.
ID% = 100·$I_D/I_{D\ 25\ ˚C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

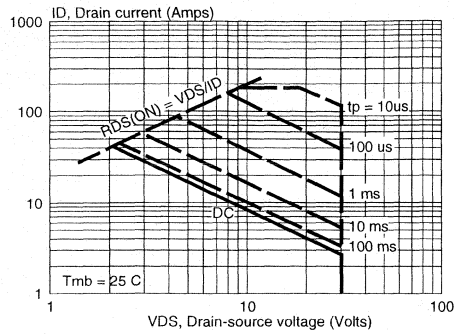


Fig.3. Safe operating area
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

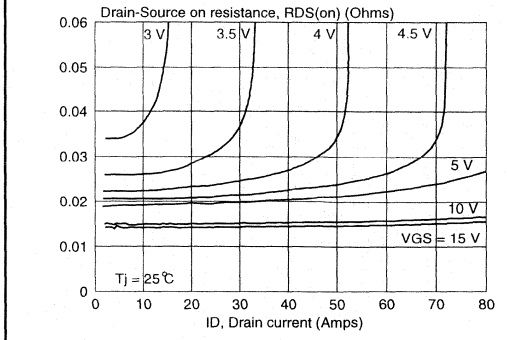


Fig.6. Typical on-state resistance
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

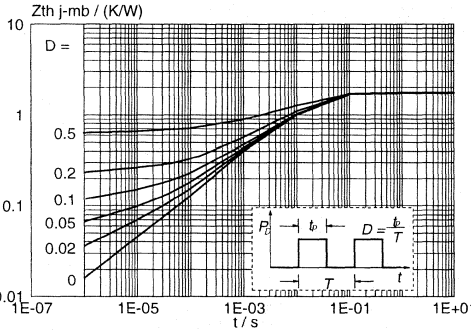


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

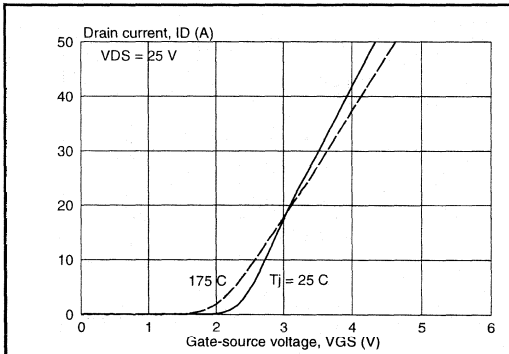


Fig.7. Typical transfer characteristics.
I_D = f(V_{GS})

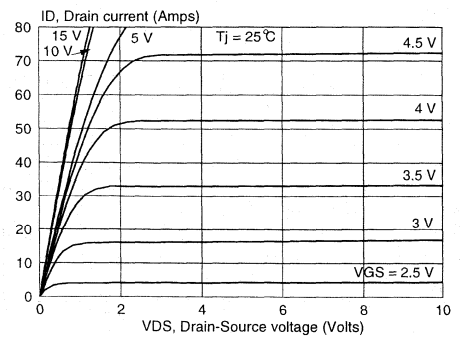


Fig.5. Typical output characteristics
I_D = f(V_{DS}); parameter V_{GS}

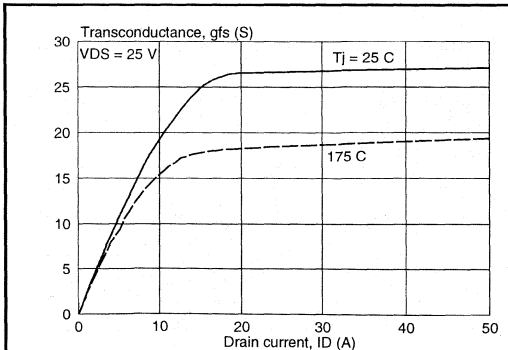


Fig.8. Typical transconductance
g_{fs} = f(I_D)

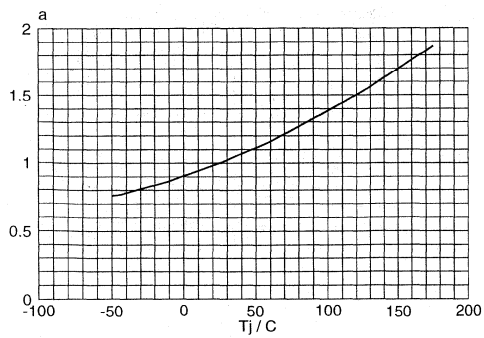


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

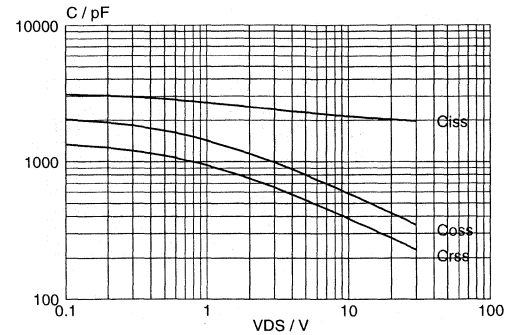


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; V_{GS} = 0 V; f = 1 MHz

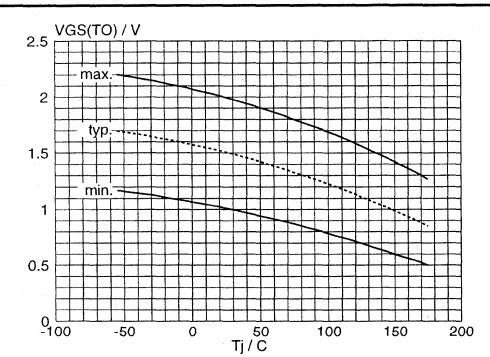


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

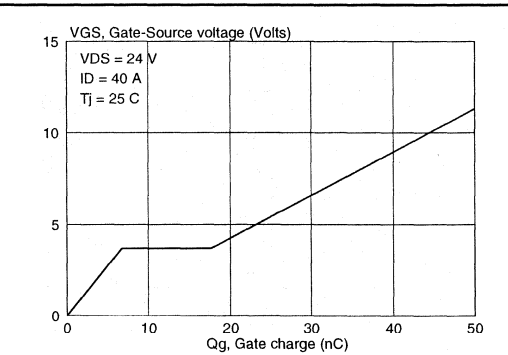


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$

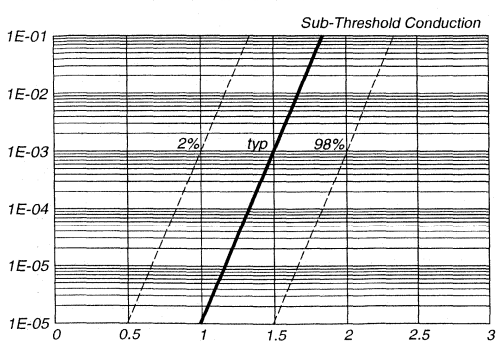


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; $V_{DS} = V_{GS}$

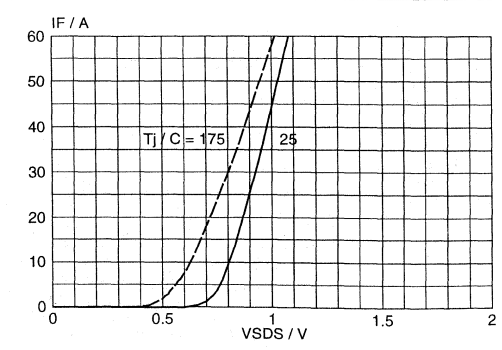


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$

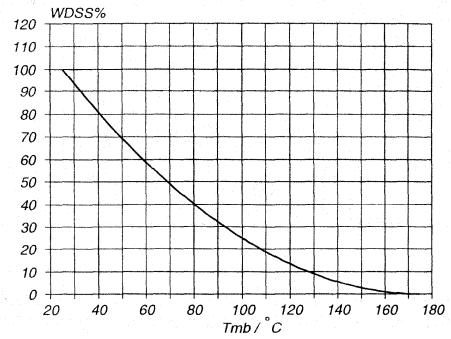


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; I_D = 25 A

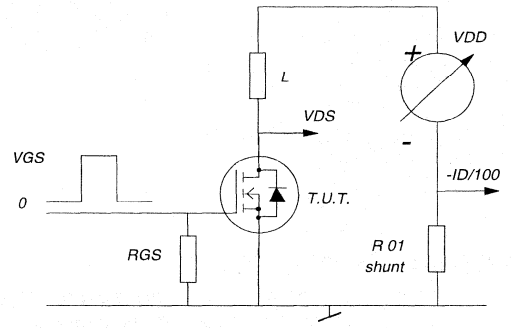


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

TrenchMOS™ transistor Logic level FET

PHP50N03LT, PHB50N03LT, PHD50N03LT

FEATURES

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- Very low on-state resistance
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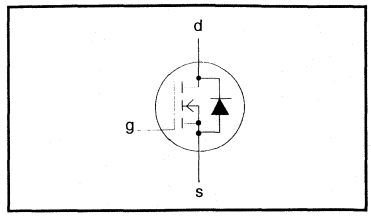
SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 25 V

I_D = 48 A

$R_{DS(ON)} \leq 21\ m\Omega$ (V_{GS} = 5 V)

$R_{DS(ON)} \leq 16\ m\Omega$ (V_{GS} = 10 V)

GENERAL DESCRIPTION

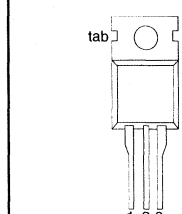
N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using **'trench'** technology. The combination of very low on-state resistance and low switching losses make this device the optimum choice in high speed computer motherboard d.c. to d.c. converters.

The PHP50N03LT is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHB505N03LT is supplied in the SOT404 surface mounting package.
The PHD50N03LT is supplied in the SOT428 surface mounting package.

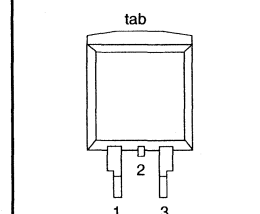
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

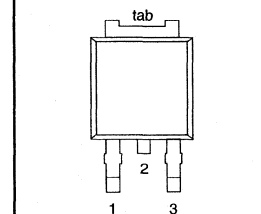
SOT78 (TO220AB)



SOT404



SOT428



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 175°C	-	25	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 175°C; R_{GS} = 20 kΩ	-	25	V
V_{GS}	Gate-source voltage		-	± 15	V
V_{GSM}	Pulsed gate-source voltage	$T_j \leq$ 150°C	-	± 20	V
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	48	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	34	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	180	A
P_D	Total power dissipation	T_{mb} = 25 °C	-	86	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	175	°C

1 It is not possible to make connection to pin 2 of the SOT428 or SOT404 packages.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.75	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	SOT78 package, in free air	-	60	-	K/W
		SOT404 and SOT428 packages, pcb mounted, minimum footprint	-	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	25	-	-	V
		T_j = -55˚C	22	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	1.5	2	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A	-	13	16	mΩ
		V_{GS} = 10 V; I_D = 25 A (SOT428 package)	-	15	18	mΩ
		V_{GS} = 5 V; I_D = 25 A	-	18	21	mΩ
		V_{GS} = 5 V; I_D = 25 A; T_j = 175˚C	-	-	39	mΩ
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	8	27	-	S
I_{DSS}	Zero gate voltage drain current	V_{DS} = 25 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	10	100	nA
$Q_{g(tot)}$	Total gate charge	I_D = 20 A; V_{DD} = 24 V; V_{GS} = 10 V	-	40	-	nC
Q_{gs}	Gate-source charge		-	7	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	10	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 15 V; I_D = 25 A;	-	10	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 5 Ω	-	50	75	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	50	75	ns
t_f	Turn-off fall time		-	30	45	ns
L_d	Internal drain inductance	Measured tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1050	-	pF
C_{oss}	Output capacitance		-	270	-	pF
C_{rss}	Feedback capacitance		-	140	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)		-	-	48	A
I_{SM}	Pulsed source current (body diode)		-	-	180	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 40 A; V_{GS} = 0 V	-	1.0	-	
t_{rr}	Reverse recovery time	I_F = 40 A; -dI_F/dt = 100 A/µs;	-	52	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 25 V	-	0.08	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 25 A; $V_{DD} \leq$ 15 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 ˚C	-	60	mJ

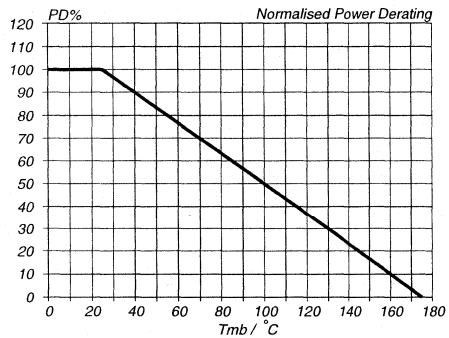


Fig.1. Normalised power dissipation.
PD% = 100·$P_D/P_{D\ 25\ ^\circ C}$ = f(T_{mb})

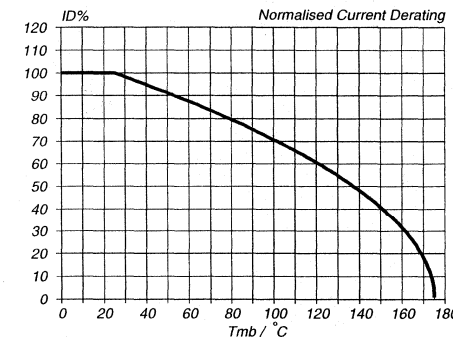


Fig.2. Normalised continuous drain current.
ID% = 100·$I_D/I_{D\ 25\ ^\circ C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

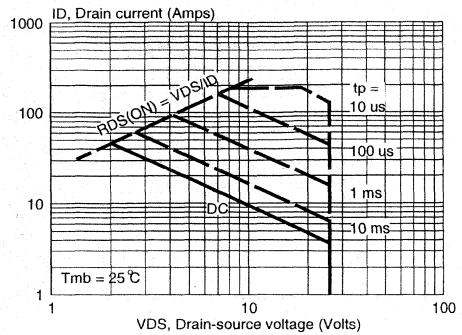


Fig.3. Safe operating area
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

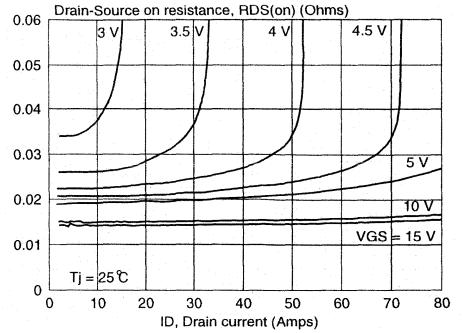


Fig.6. Typical on-state resistance
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

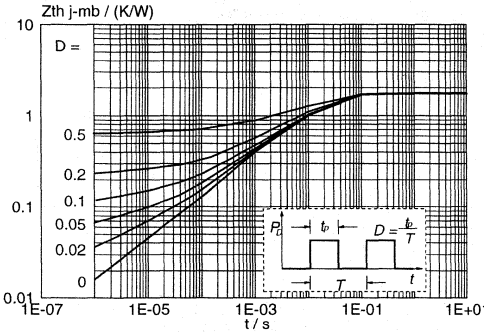


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

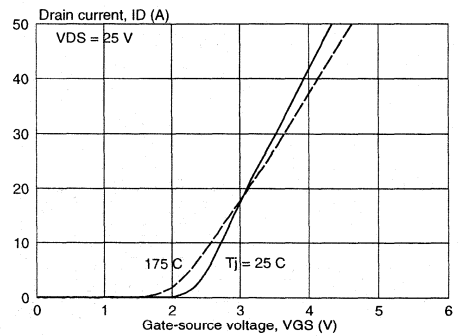


Fig.7. Typical transfer characteristics.
I_D = f(V_{GS})

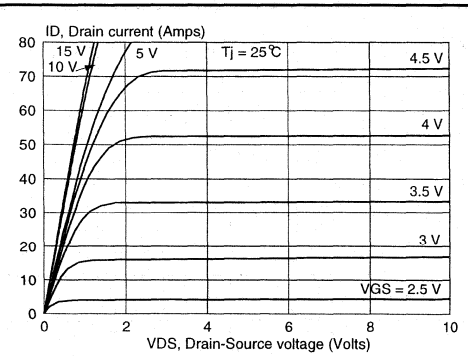


Fig.5. Typical output characteristics
I_D = f(V_{DS}); parameter V_{GS}

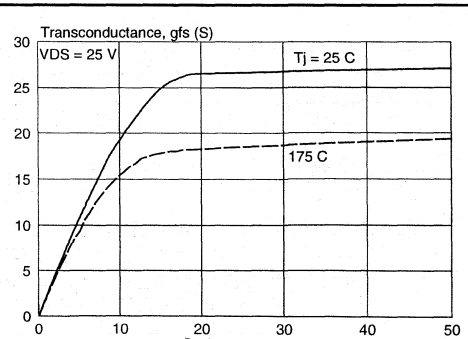


Fig.8. Typical transconductance
g_{fs} = f(I_D)

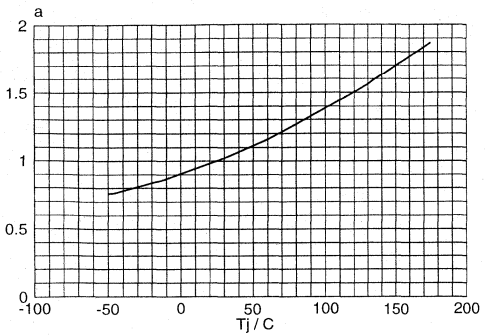


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$

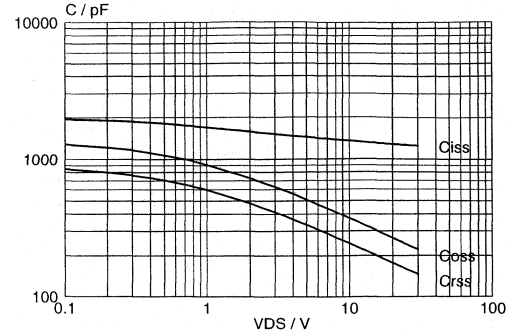


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz

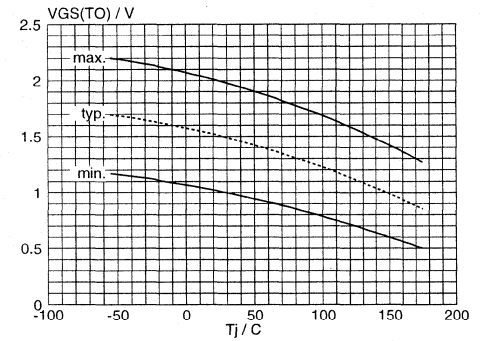


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

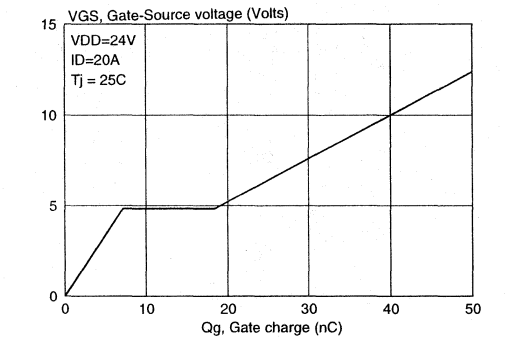


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$

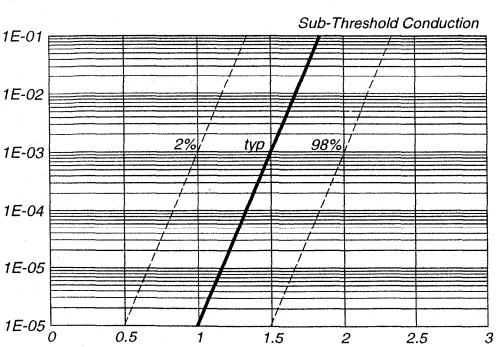


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; $V_{DS} = V_{GS}$

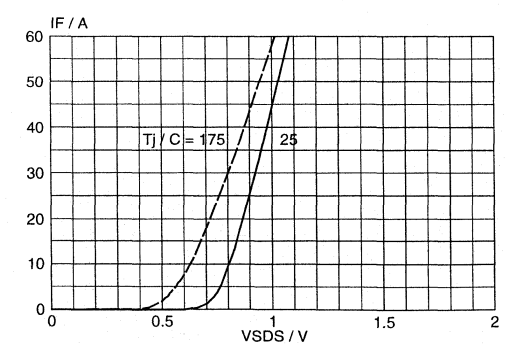


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$

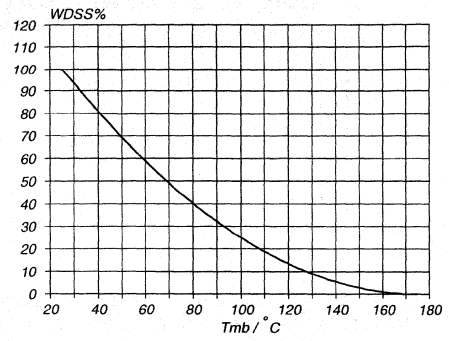


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$

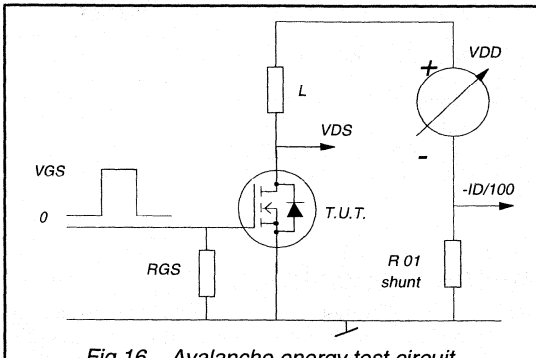


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

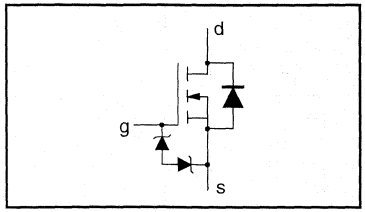
TrenchMOS™ transistor Logic level FET

PHP50N06LT, PHB50N06LT

FEATURES

- **'Trench'** technology
- Very low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 55 V

I_D = 50 A

$R_{DS(ON)} \leq 24\ m\Omega$ (V_{GS} = 5 V)

$R_{DS(ON)} \leq 22\ m\Omega$ (V_{GS} = 10 V)

GENERAL DESCRIPTION

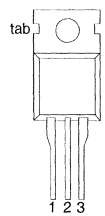
N-channel enhancement mode, logic level, field-effect power transistor in a plastic envelope using **'trench'** technology. The device has very low on-state resistance. It is intended for use in dc to dc converters and general purpose switching applications.

The PHP50N06LT is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHB50N06LT is supplied in the SOT404 surface mounting package.

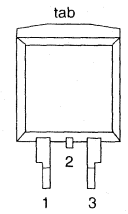
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

SOT78 (TO220AB)



SOT404



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 175°C	-	55	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 175°C; R_{GS} = 20 kΩ	-	55	V
V_{GS}	Gate-source voltage		-	± 13	V
I_D	Continuous drain current	T_{mb} = 25 °C	-	50	A
		T_{mb} = 100 °C	-	35	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	200	A
P_D	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	175	°C

1 It is not possible to make connection to pin 2 of the SOT404 package.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	SOT78 package, in free air	60	-	K/W
		SOT404 package, pcb mounted, minimum footprint	50	-	K/W

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

ELECTRICAL CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	19	24	mΩ
		V_{GS} = 10 V; I_D = 25 A	-	17	22	mΩ
		T_j = 175˚C	-	-	50	mΩ
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	15	40	-	S
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	20	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
$Q_{g(tot)}$	Total gate charge	I_D = 50 A; V_{DD} = 44 V; V_{GS} = 5 V	-	27	-	nC
Q_{gs}	Gate-source charge		-	4	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	14	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	30	45	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω	-	80	130	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	95	135	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1500	2000	pF
C_{oss}	Output capacitance		-	300	360	pF
C_{rss}	Feedback capacitance		-	150	200	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)		-	-	50	A
I_{SM}	Pulsed source current (body diode)		-	-	200	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 40 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 40 A; -dI_F/dt = 100 A/µs;	-	40	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.07	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 40 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	80	mJ

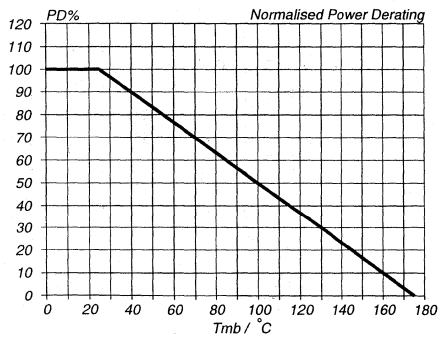


Fig.1. Normalised power dissipation.
PD% = 100·$P_D/P_{D\,25\,°C}$ = f(T_{mb})

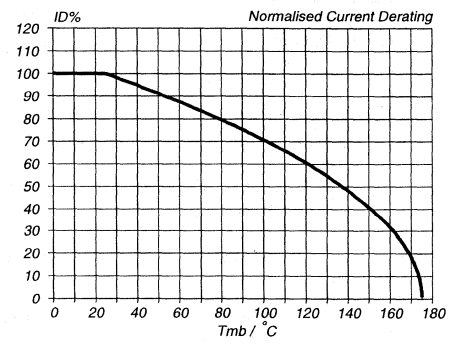


Fig.2. Normalised continuous drain current.
ID% = 100·$I_D/I_{D\,25\,°C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

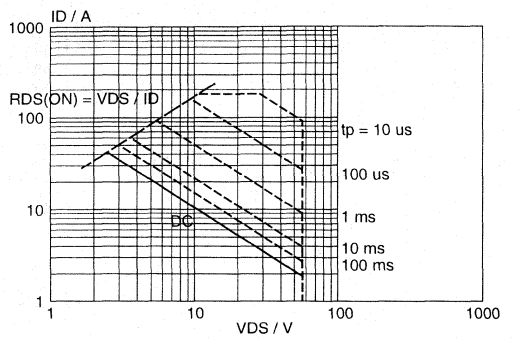


Fig.3. Safe operating area. T_{mb} = 25 ˚C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

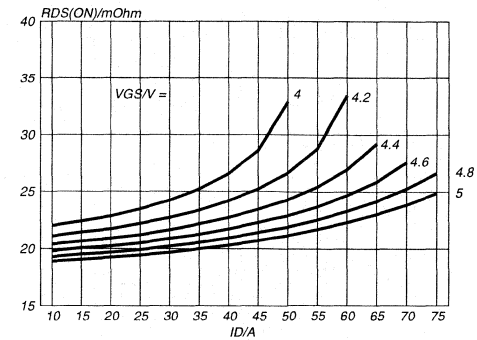


Fig.6. Typical on-state resistance, T_j = 25 ˚C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

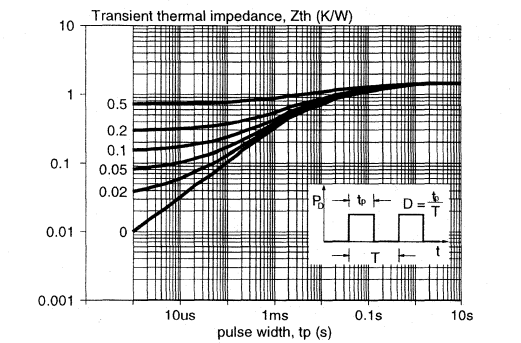


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

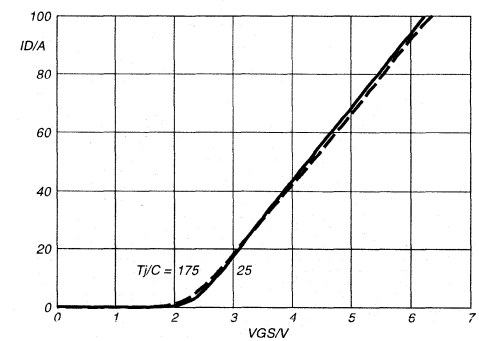


Fig.7. Typical transfer characteristics.
I_D = f(V_{GS}) ; conditions: V_{DS} = 25 V; parameter T_j

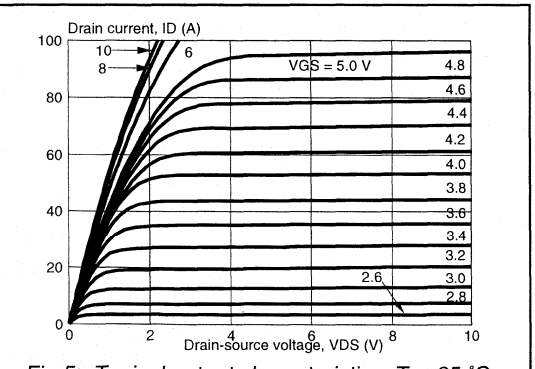


Fig.5. Typical output characteristics, T_j = 25 ˚C.
I_D = f(V_{DS}); parameter V_{GS}

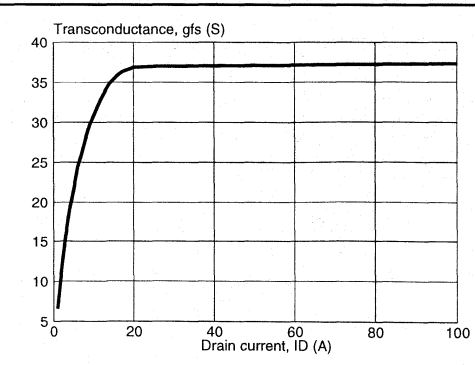


Fig.8. Typical transconductance, T_j = 25 ˚C.
g_{fs} = f(I_D); conditions: V_{DS} = 25 V

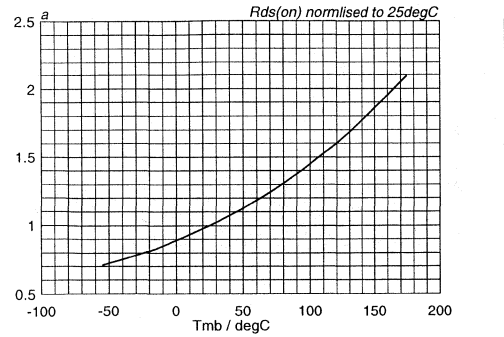


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

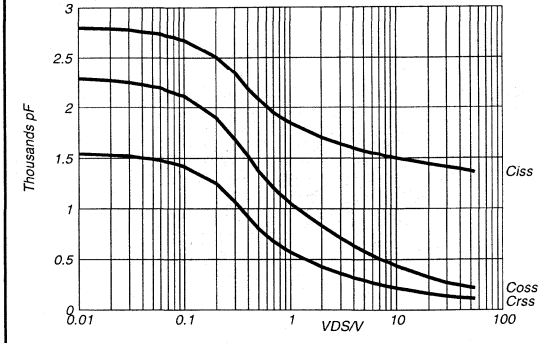


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

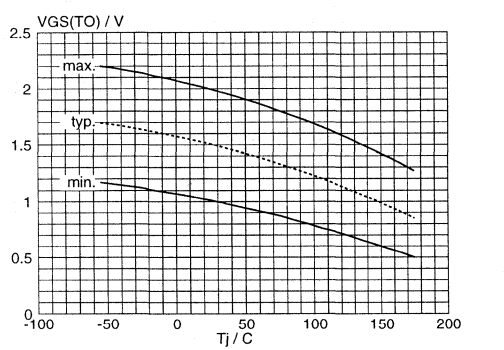


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

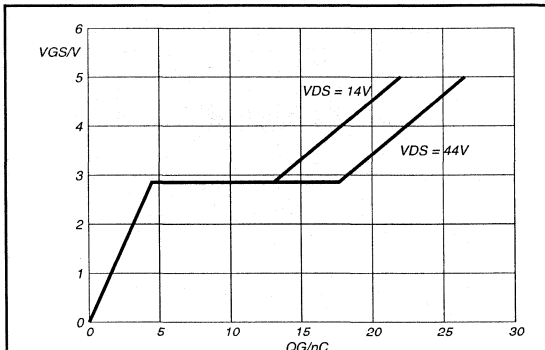


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 50 A; parameter V_{DS}

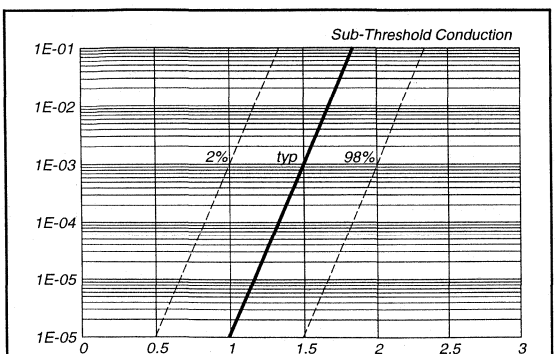


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

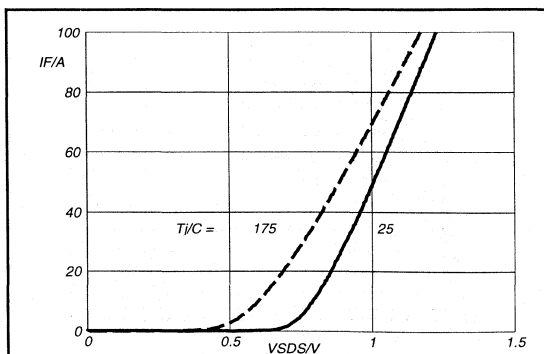


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

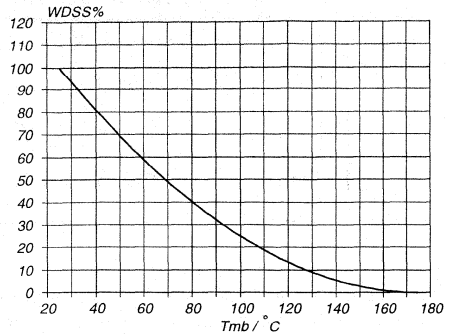


Fig.15. Normalised avalanche energy rating. W_{DSS}% = f(T_{mb}); conditions: I_D = 40 A

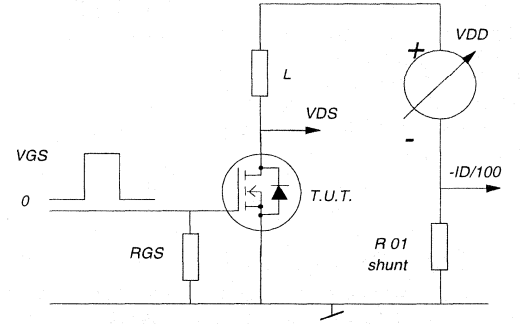


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

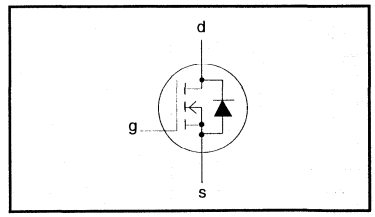
TrenchMOS™ transistor Logic level FET

PHP55N03LT, PHB55N03LT, PHD55N03LT

FEATURES

- **'Trench'** technology
- Very low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 25 V

I_D = 55 A

$R_{DS(ON)} \leq 18\ m\Omega$ (V_{GS} = 5 V)

$R_{DS(ON)} \leq 14\ m\Omega$ (V_{GS} = 10 V)

GENERAL DESCRIPTION

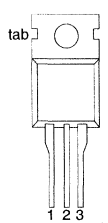
N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using **'trench'** technology. The combination of very low on-state resistance and low switching losses make this device the optimum choice in high speed computer motherboard d.c. to d.c. converters.

The PHP55N03LT is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHB55N03LT is supplied in the SOT404 surface mounting package.
The PHD55N03LT is supplied in the SOT428 surface mounting package.

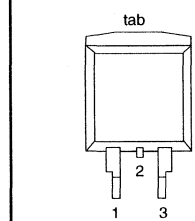
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

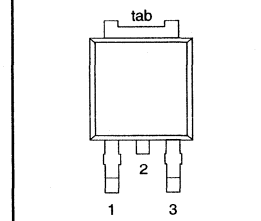
SOT78 (TO220AB)



SOT404



SOT428



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 175°C	-	25	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 175°C; R_{GS} = 20 kΩ	-	25	V
V_{GS}	Gate-source voltage		-	± 15	V
V_{GSM}	Pulsed gate-source voltage	$T_j \leq$ 150°C	-	± 20	V
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 5 V	-	55	A
		T_{mb} = 100 °C; V_{GS} = 5 V	-	38	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	220	A
P_D	Total power dissipation	T_{mb} = 25 °C	-	103	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	175	°C

1 It is not possible to make connection to pin 2 of the SOT428 or SOT404 packages.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.45	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	SOT78 package, in free air	-	60	-	K/W
		SOT404 and SOT428 packages, pcb mounted, minimum footprint	-	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	25	-	-	V
		T_j = -55˚C	22	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	1.5	2	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A	-	9	14	mΩ
		V_{GS} = 5 V; I_D = 25 A	-	13	18	mΩ
		V_{GS} = 5 V; I_D = 25 A; T_j = 175˚C	-	-	34	mΩ
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	10	20	-	S
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	10	100	nA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 25 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
$Q_{g(tot)}$	Total gate charge	I_D = 20 A; V_{DD} = 24 V; V_{GS} = 10 V	-	52	-	nC
Q_{gs}	Gate-source charge		-	5.6	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	14	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 15 V; I_D = 25 A;	-	8.4	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 5 Ω	-	63	100	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	60	100	ns
t_f	Turn-off fall time		-	66	100	ns
L_d	Internal drain inductance	Measured tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1300	-	pF
C_{oss}	Output capacitance		-	430	-	pF
C_{rss}	Feedback capacitance		-	228	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)		-	-	55	A
I_{SM}	Pulsed source current (body diode)		-	-	220	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 55 A; V_{GS} = 0 V	-	1.0	-	
t_{rr}	Reverse recovery time	I_F = 55 A; -dI_F/dt = 100 A/µs;	-	70	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 25 V	-	0.1	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 25 A; $V_{DD} \leq$ 15 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 ˚C	-	60	mJ

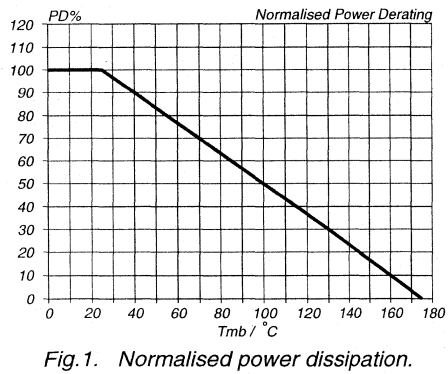


Fig.1. Normalised power dissipation.
PD% = 100·$P_D/P_{D\ 25\ ˚C}$ = f(T_{mb})

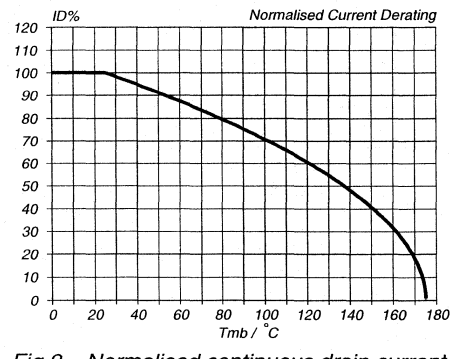


Fig.2. Normalised continuous drain current.
ID% = 100·$I_D/I_{D\ 25\ ˚C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

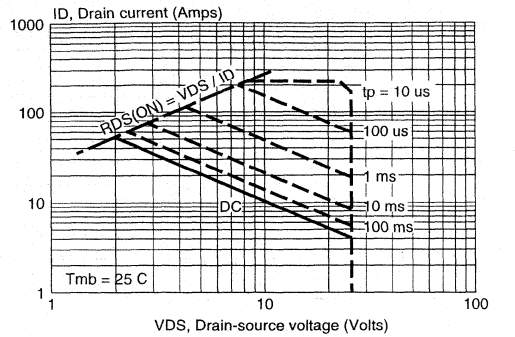


Fig.3. Safe operating area
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

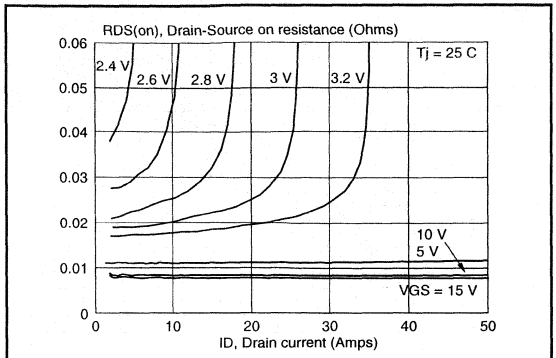


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

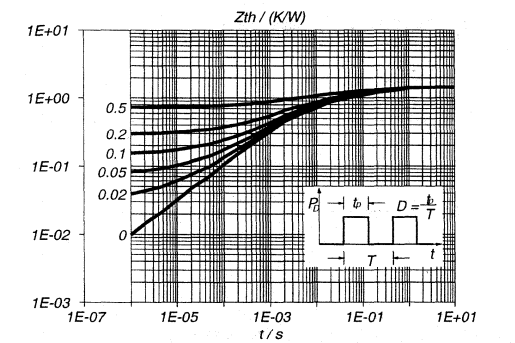


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

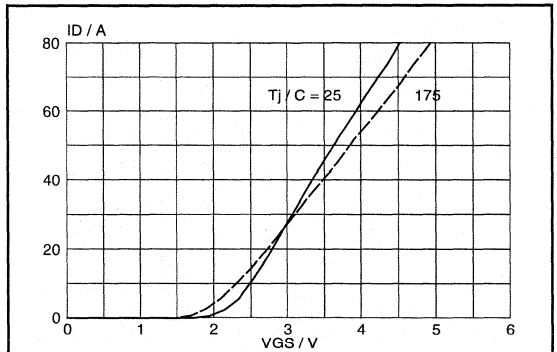


Fig.7. Typical transfer characteristics.
I_D = f(V_{GS}) ; conditions: V_{DS} = 25 V; parameter T_j

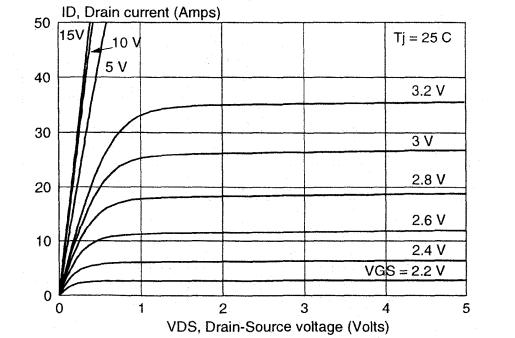


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

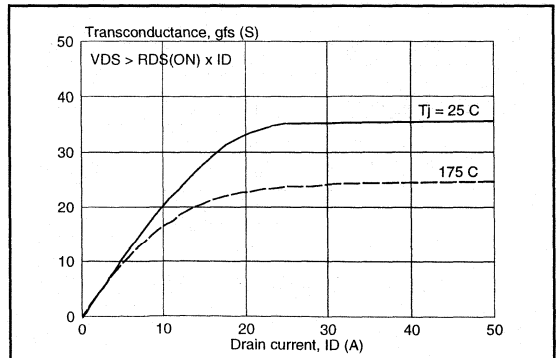


Fig.8. Typical transconductance, T_j = 25 °C.
g_{fs} = f(I_D); conditions: V_{DS} = 25 V

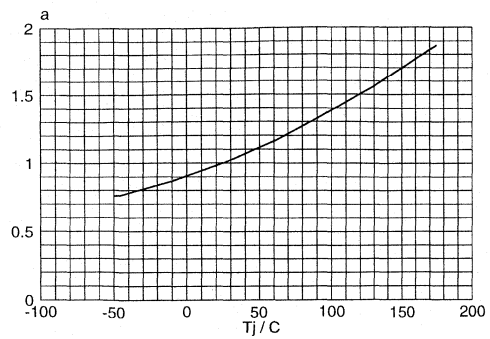


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$

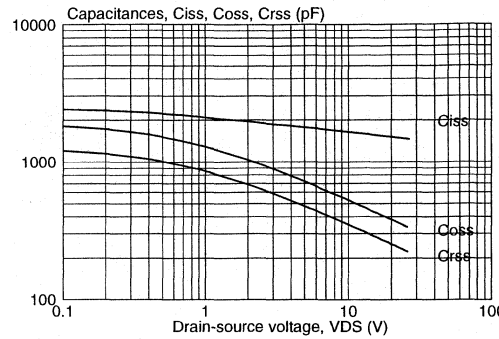


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

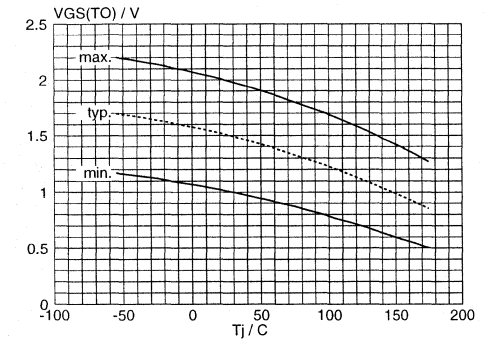


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

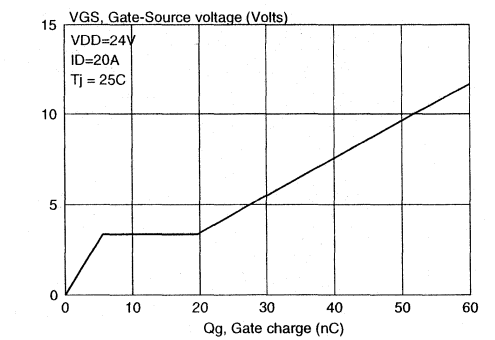


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

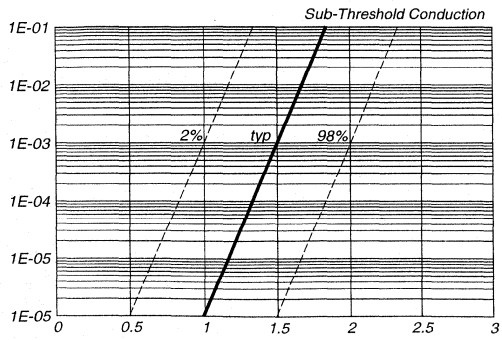


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

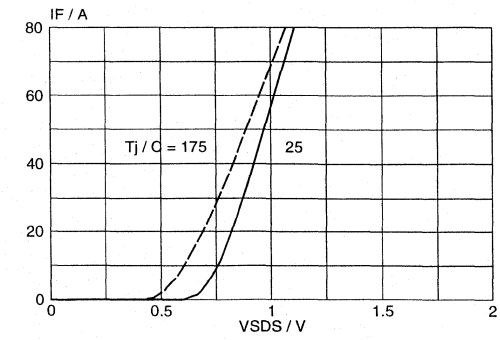


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

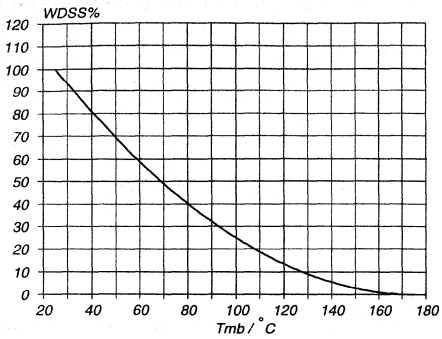


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$

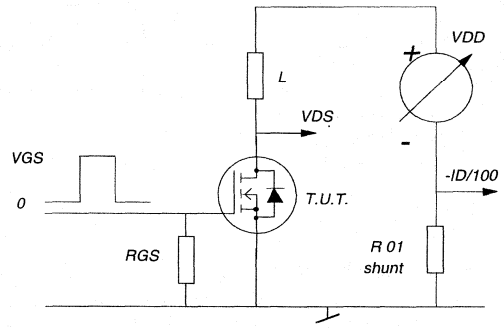


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

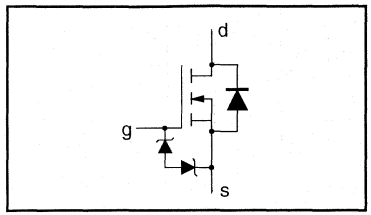
TrenchMOS™ transistor Logic level FET

PHP60N06LT, PHB60N06LT

FEATURES

- **'Trench'** technology
- Very low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 55 V

I_D = 58 A

$R_{DS(ON)} \leq 20\ m\Omega$ (V_{GS} = 5 V)

$R_{DS(ON)} \leq 18\ m\Omega$ (V_{GS} = 10 V)

GENERAL DESCRIPTION

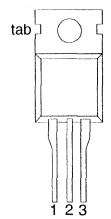
N-channel enhancement mode, logic level, field-effect power transistor in a plastic envelope using **'trench'** technology. The device has very low on-state resistance. It is intended for use in dc to dc converters and general purpose switching applications.

The PHP60N06LT is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHB60N06LT is supplied in the SOT404 surface mounting package.

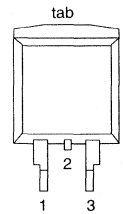
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

SOT78 (TO220AB)



SOT404



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 175°C	-	55	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 175°C; R_{GS} = 20 kΩ	-	55	V
V_{GS}	Gate-source voltage		-	± 13	V
I_D	Continuous drain current	T_{mb} = 25 °C	-	58	A
		T_{mb} = 100 °C	-	40	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	232	A
P_D	Total power dissipation	T_{mb} = 25 °C	-	150	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	175	°C

1 It is not possible to make connection to pin 2 of the SOT404 package.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	1.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	SOT78 package, in free air	60	-	K/W
		SOT404 package, pcb mounted, minimum footprint	50	-	K/W

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

ELECTRICAL CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	15	20	mΩ
		V_{GS} = 10 V; I_D = 25 A	-	16	18	mΩ
		T_j = 175˚C	-	-	42	mΩ
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	20	52	-	S
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	20	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
$Q_{g(tot)}$	Total gate charge	I_D = 50 A; V_{DD} = 44 V; V_{GS} = 5 V	-	37	-	nC
Q_{gs}	Gate-source charge		-	10	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	17	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	28	40	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω	-	110	160	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	95	135	ns
t_f	Turn-off fall time		-	70	90	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1800	2400	pF
C_{oss}	Output capacitance		-	350	420	pF
C_{rss}	Feedback capacitance		-	170	235	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)		-	-	58	A
I_{SM}	Pulsed source current (body diode)		-	-	232	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 40 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 40 A; -dI_F/dt = 100 A/µs;	-	47	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.15	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 45 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	110	mJ

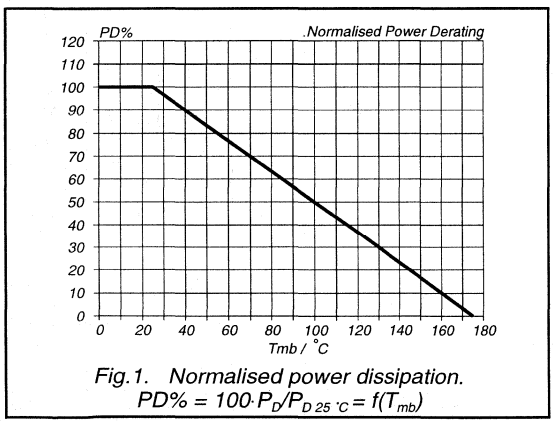


Fig.1. Normalised power dissipation.
PD% = 100·$P_D/P_{D\ 25\ °C}$ = f(T_{mb})

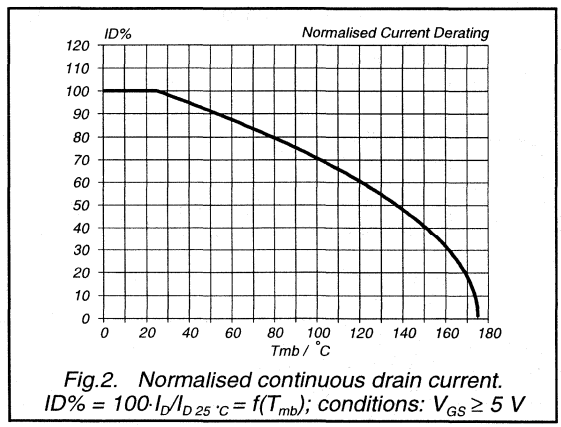


Fig.2. Normalised continuous drain current.
ID% = 100·$I_D/I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

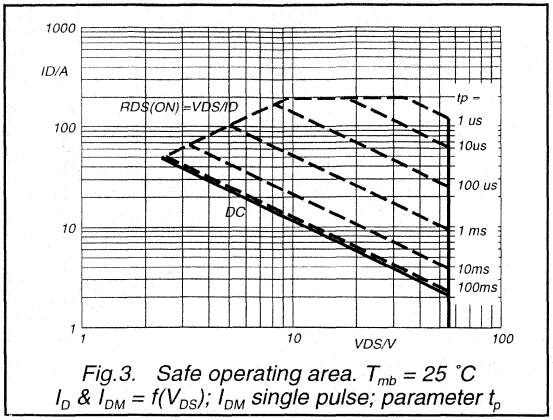


Fig.3. Safe operating area. T_{mb} = 25 ˚C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

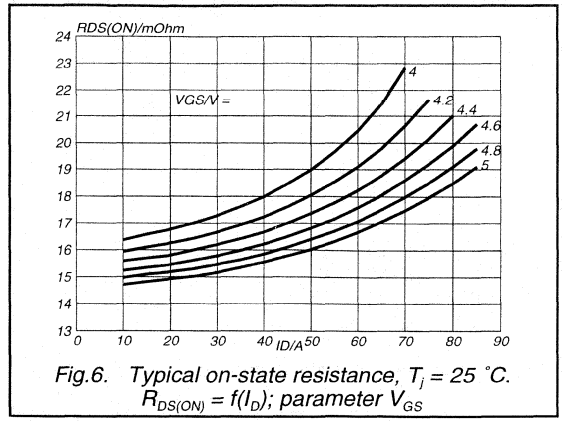


Fig.6. Typical on-state resistance, T_j = 25 ˚C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

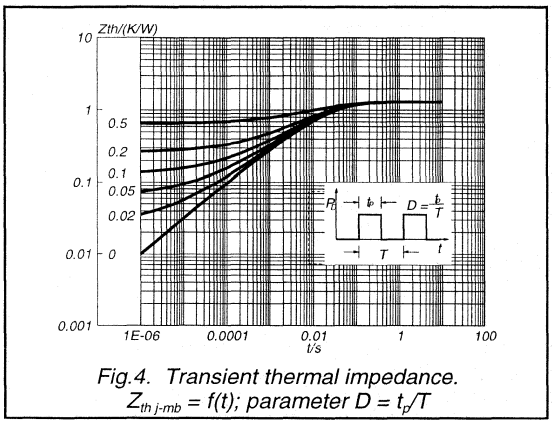


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

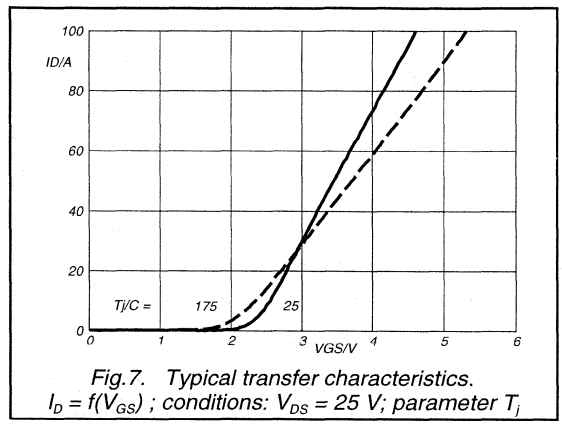


Fig.7. Typical transfer characteristics.
I_D = f(V_{GS}) ; conditions: V_{DS} = 25 V; parameter T_j

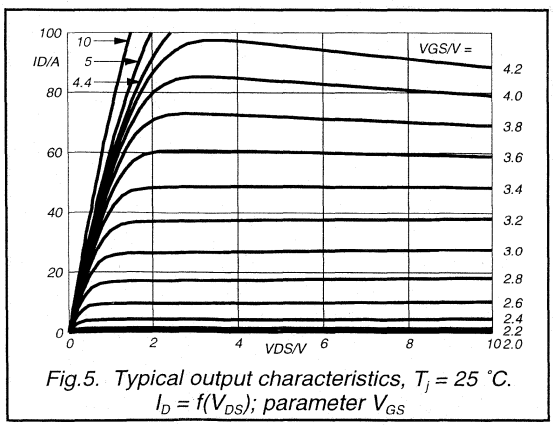


Fig.5. Typical output characteristics, T_j = 25 ˚C.
I_D = f(V_{DS}); parameter V_{GS}

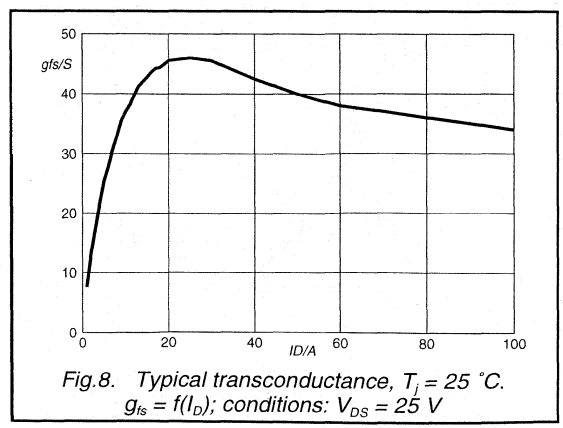


Fig.8. Typical transconductance, T_j = 25 ˚C.
g_{fs} = f(I_D); conditions: V_{DS} = 25 V

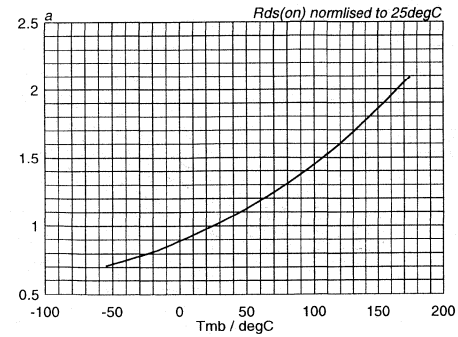


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

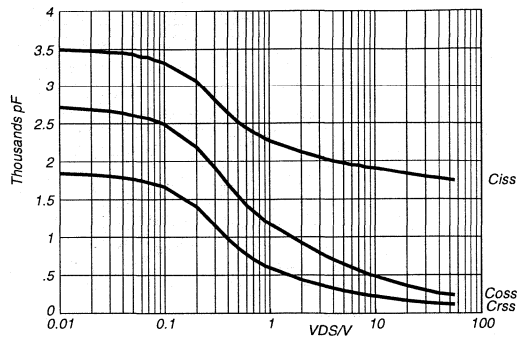


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

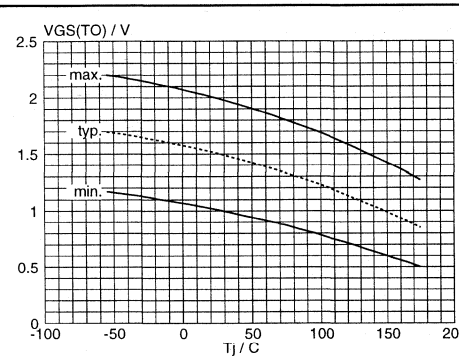


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

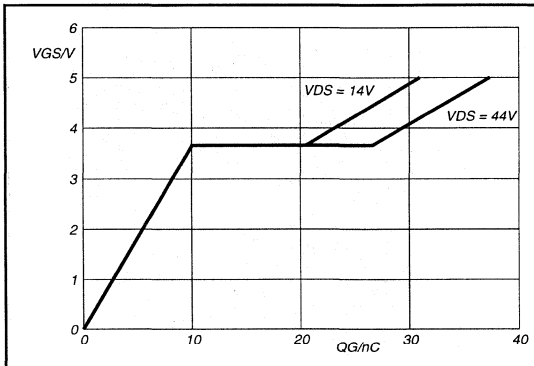


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 50 A; parameter V_{DS}

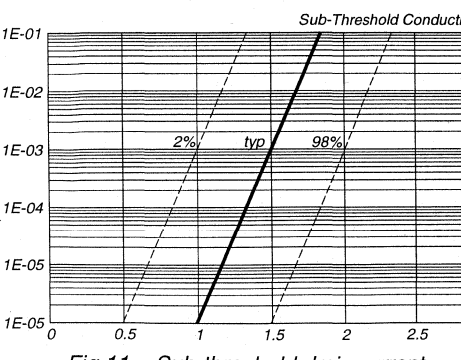


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

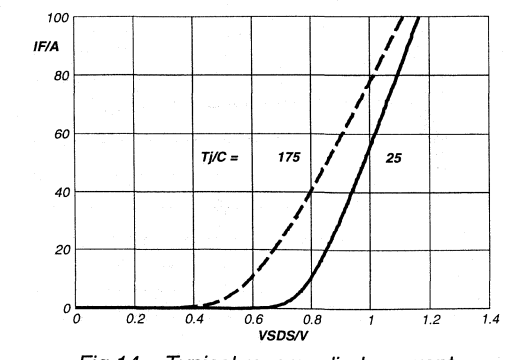


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

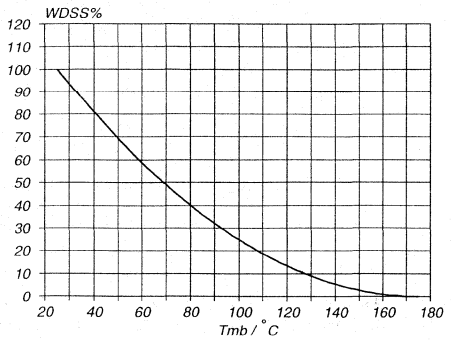


Fig.15. Normalised avalanche energy rating. W_{DSS}% = f(T_{mb}); conditions: I_D = 45 A

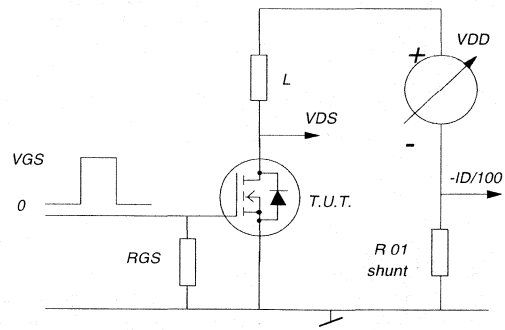


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

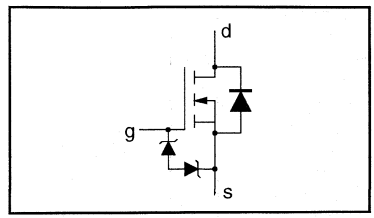
TrenchMOS™ transistor Logic level FET

PHP65N06LT, PHB65N06LT

FEATURES

- **'Trench'** technology
- Very low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 55 V

I_D = 63 A

$R_{DS(ON)} \leq 18\ m\Omega$ (V_{GS} = 5 V)

$R_{DS(ON)} \leq 16\ m\Omega$ (V_{GS} = 10 V)

GENERAL DESCRIPTION

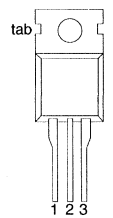
N-channel enhancement mode, logic level, field-effect power transistor in a plastic envelope using **'trench'** technology. The device has very low on-state resistance. It is intended for use in dc to dc converters and general purpose switching applications.

The PHP65N06LT is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHB65N06LT is supplied in the SOT404 surface mounting package.

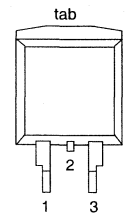
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

SOT78 (TO220AB)



SOT404



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 175°C	-	55	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 175°C; R_{GS} = 20 kΩ	-	55	V
V_{GS}	Gate-source voltage		-	± 13	V
I_D	Continuous drain current	T_{mb} = 25 °C	-	63	A
		T_{mb} = 100 °C	-	44	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	240	A
P_D	Total power dissipation	T_{mb} = 25 °C	-	150	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	175	°C

1 It is not possible to make connection to pin 2 of the SOT404 package.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	1.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	SOT78 package, in free air	60	-	K/W
		SOT404 package, pcb mounted, minimum footprint	50	-	K/W

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

ELECTRICAL CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	15	18	mΩ
		V_{GS} = 10 V; I_D = 25 A	-	13	16	mΩ
		T_j = 175˚C	-	-	38	mΩ
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	25	52	-	S
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	20	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
$Q_{g(tot)}$	Total gate charge	I_D = 50 A; V_{DD} = 44 V; V_{GS} = 5 V	-	34	-	nC
Q_{gs}	Gate-source charge		-	8	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	17	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	30	45	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω	-	80	130	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	100	140	ns
t_f	Turn-off fall time		-	50	75	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	2000	2600	pF
C_{oss}	Output capacitance		-	390	490	pF
C_{rss}	Feedback capacitance		-	200	290	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)		-	-	63	A
I_{SM}	Pulsed source current (body diode)		-	-	240	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 50 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 50 A; -dI_F/dt = 100 A/µs;	-	48	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.1	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 50 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 ˚C	-	125	mJ

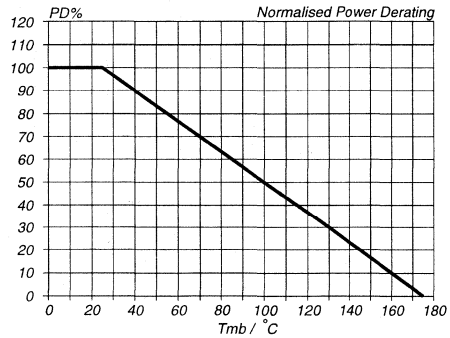


Fig.1. Normalised power dissipation.
PD% = 100·$P_D/P_{D\,25\,°C}$ = f(T_{mb})

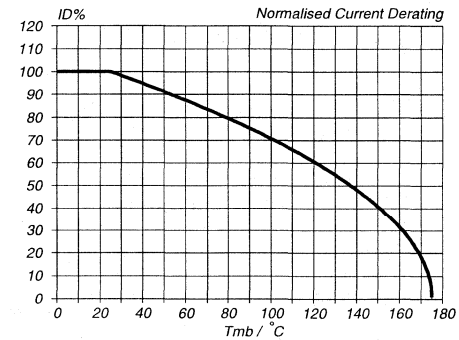


Fig.2. Normalised continuous drain current.
ID% = 100·$I_D/I_{D\,25\,°C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

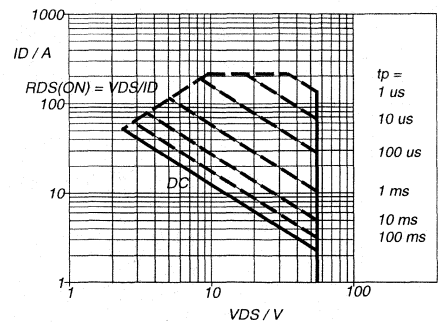


Fig.3. Safe operating area. T_{mb} = 25 ˚C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

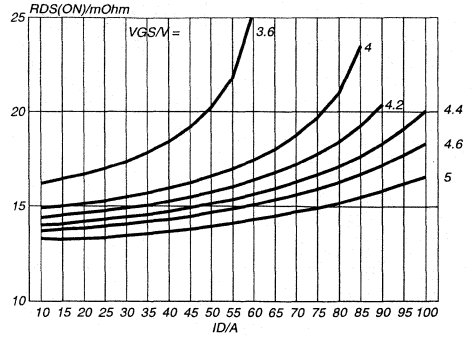


Fig.6. Typical on-state resistance, T_j = 25 ˚C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

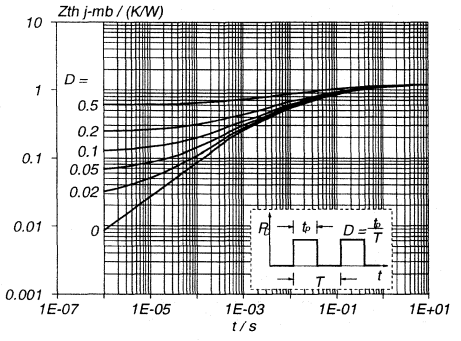


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

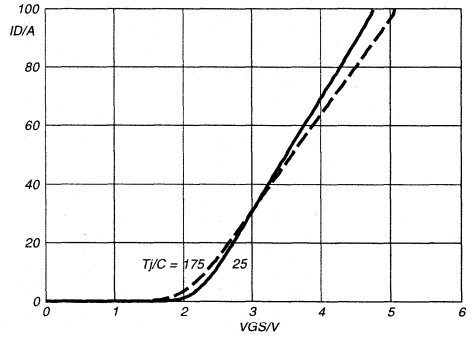


Fig.7. Typical transfer characteristics.
I_D = f(V_{GS}) ; conditions: V_{DS} = 25 V; parameter T_j

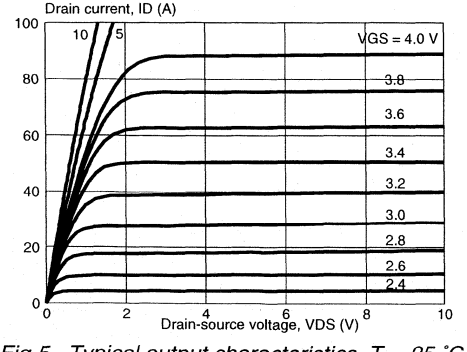


Fig.5. Typical output characteristics, T_j = 25 ˚C.
I_D = f(V_{DS}); parameter V_{GS}

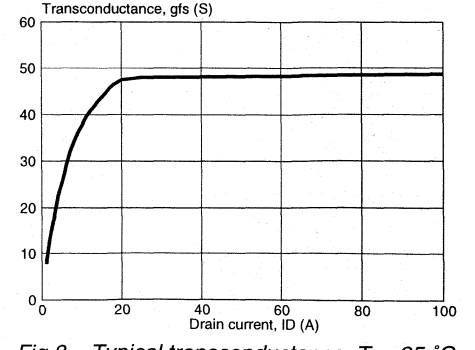


Fig.8. Typical transconductance, T_j = 25 ˚C.
g_{fs} = f(I_D); conditions: V_{DS} = 25 V

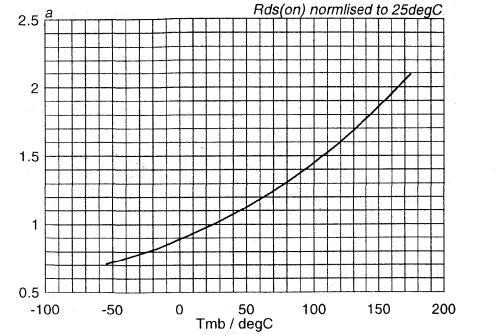


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

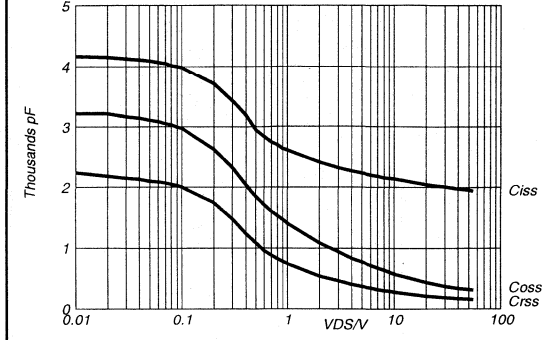


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

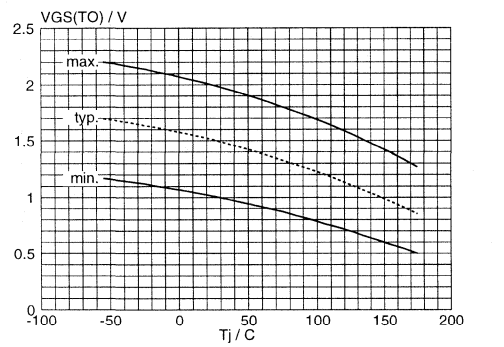


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

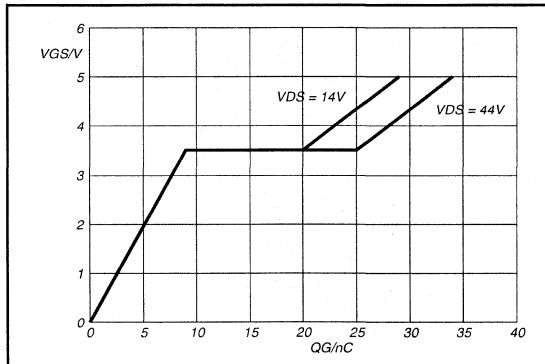


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 50 A; parameter V_{DS}

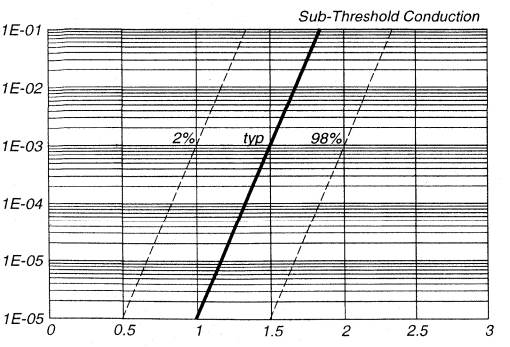


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

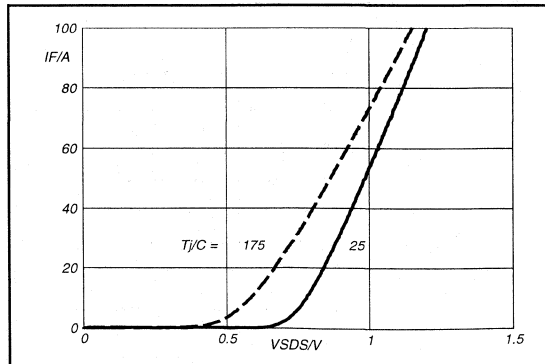


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

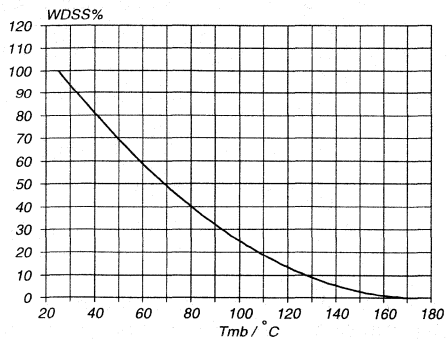


Fig.15. Normalised avalanche energy rating. W_{DSS}% = f(T_{mb}); conditions: I_D = 50 A

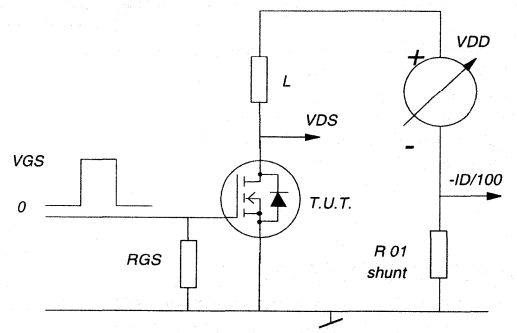


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

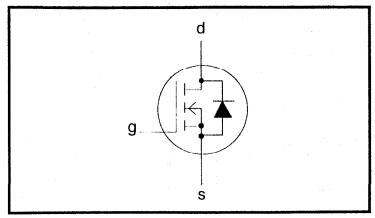
TrenchMOS™ transistor Logic level FET

PHP69N03LT, PHB69N03LT, PHD69N03LT

FEATURES

- **'Trench'** technology
- Very low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 25 V

I_D = 69 A

$R_{DS(ON)} \leq 14\ m\Omega$ (V_{GS} = 5 V)

$R_{DS(ON)} \leq 12\ m\Omega$ (V_{GS} = 10 V)

GENERAL DESCRIPTION

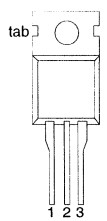
N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using **'trench'** technology. The combination of very low on-state resistance and low switching losses make this device the optimum choice in high speed computer motherboard d.c. to d.c. converters.

The PHP69N03LT is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHB69N03LT is supplied in the SOT404 surface mounting package.
The PHD69N03LT is supplied in the SOT428 surface mounting package.

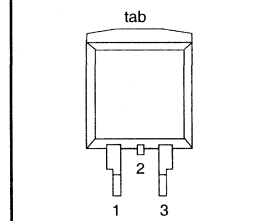
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

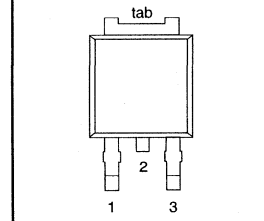
SOT78 (TO220AB)



SOT404



SOT428



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 175°C	-	25	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 175°C; R_{GS} = 20 kΩ	-	25	V
V_{GS}	Gate-source voltage		-	± 15	V
V_{GSM}	Pulsed gate-source voltage	$T_j \leq$ 150°C	-	± 20	V
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 5 V	-	69	A
		T_{mb} = 100 °C; V_{GS} = 5 V	-	48	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	240	A
P_D	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	175	°C

1 It is not possible to make connection to pin 2 of the SOT428 or SOT404 packages.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	SOT78 package, in free air	-	60	-	K/W
		SOT404 and SOT428 packages, pcb mounted, minimum footprint	-	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	25	-	-	V
		T_j = -55˚C	22	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	1.5	2	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A	-	8.5	12	mΩ
		V_{GS} = 5 V; I_D = 25 A	-	11	14	mΩ
		V_{GS} = 5 V; I_D = 25 A; T_j = 175˚C	-	-	26	mΩ
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	12	25	-	S
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	10	100	nA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 25 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
$Q_{g(tot)}$	Total gate charge	I_D = 20 A; V_{DD} = 24 V; V_{GS} = 10 V	-	70	-	nC
Q_{gs}	Gate-source charge		-	9	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	20	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 15 V; I_D = 25 A;	-	10	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 5 Ω	-	50	75	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	80	120	ns
t_f	Turn-off fall time		-	50	75	ns
L_d	Internal drain inductance	Measured tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1700	-	pF
C_{oss}	Output capacitance		-	480	-	pF
C_{rss}	Feedback capacitance		-	250	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)		-	-	69	A
I_{SM}	Pulsed source current (body diode)		-	-	240	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 69 A; V_{GS} = 0 V	-	1.0	-	
t_{rr}	Reverse recovery time	I_F = 69 A; -dI_F/dt = 100 A/µs;	-	65	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 25 V	-	0.1	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 25 A; $V_{DD} \leq$ 15 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 ˚C	-	60	mJ

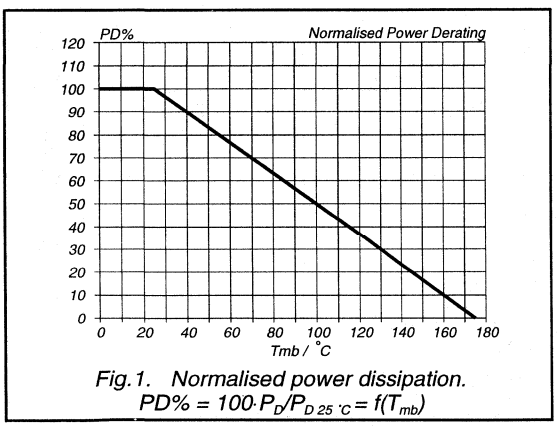


Fig.1. Normalised power dissipation.
PD% = 100·$P_D/P_{D\ 25\ ^\circ C}$ = f(T_{mb})

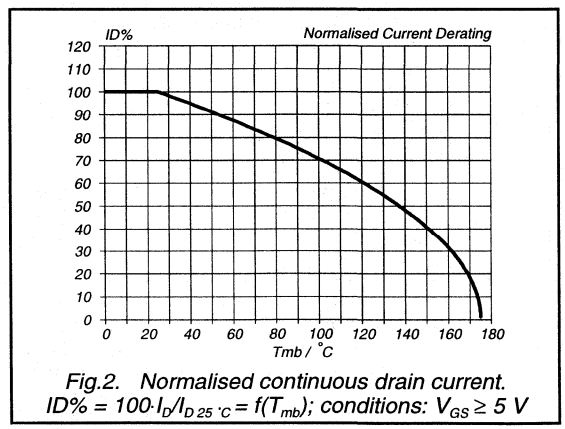


Fig.2. Normalised continuous drain current.
ID% = 100·$I_D/I_{D\ 25\ ^\circ C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

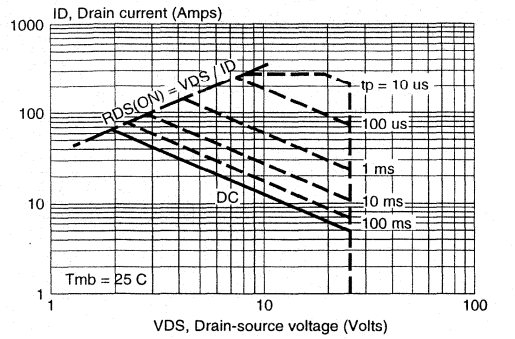


Fig.3. Safe operating area
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

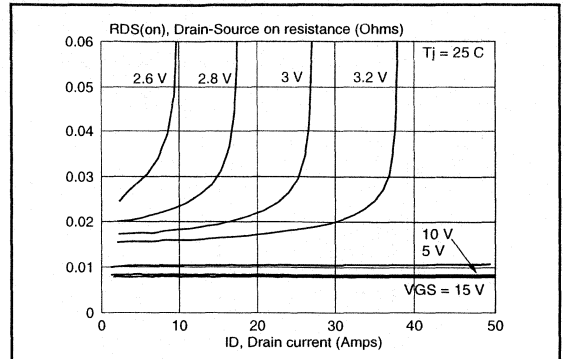


Fig.6. Typical on-state resistance, T_j = 25 ˚C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

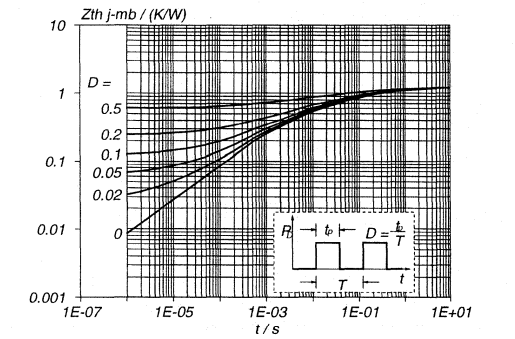


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

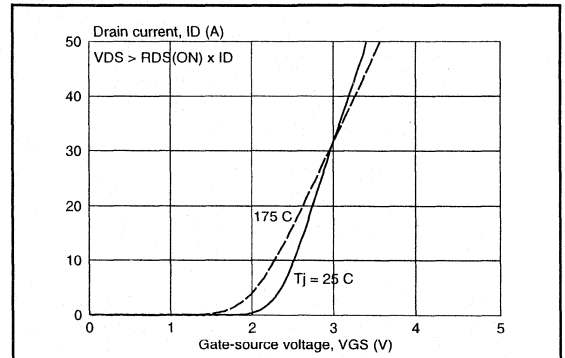


Fig.7. Typical transfer characteristics.
I_D = f(V_{GS}) ; conditions: V_{DS} = 25 V; parameter T_j

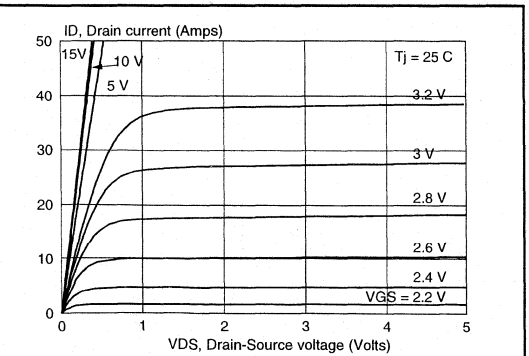


Fig.5. Typical output characteristics, T_j = 25 ˚C.
I_D = f(V_{DS}); parameter V_{GS}

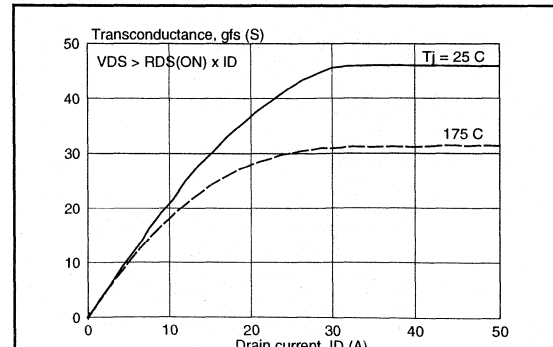


Fig.8. Typical transconductance, T_j = 25 ˚C.
g_{fs} = f(I_D)

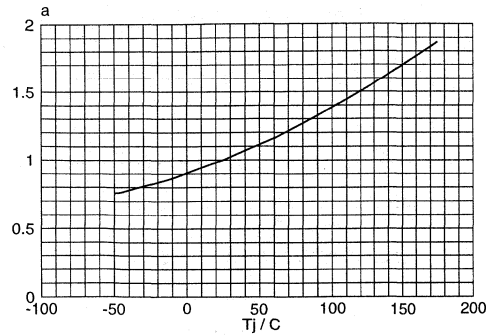


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$

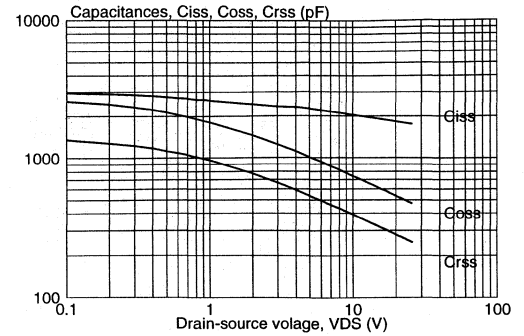


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; f = 1 MHz

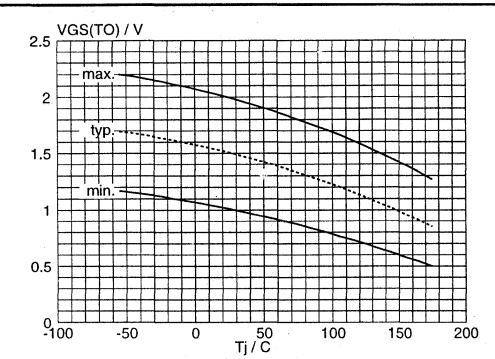


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

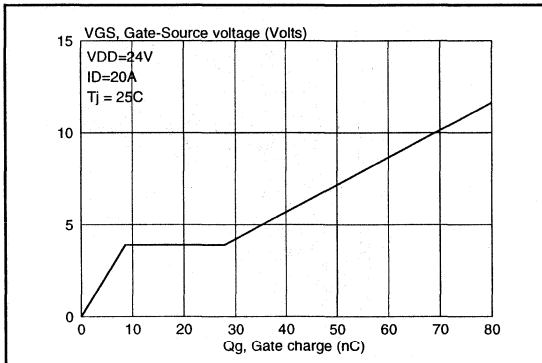


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

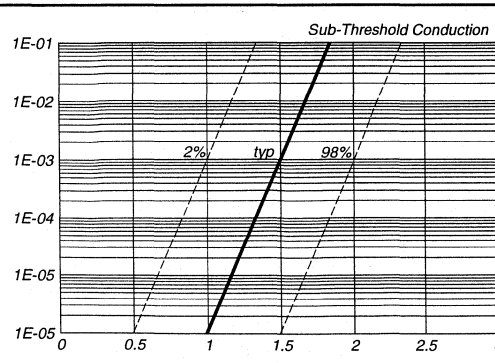


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

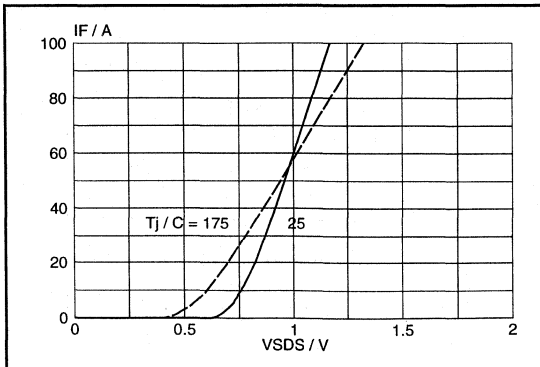


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

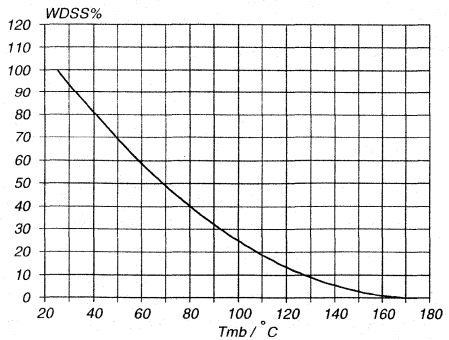


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$

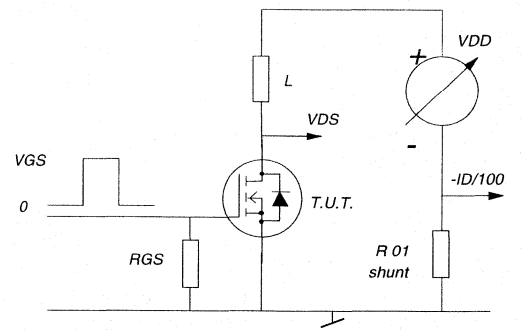


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

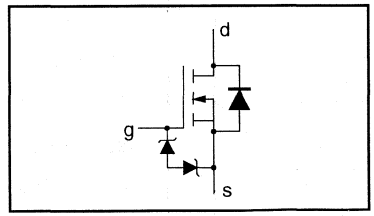
TrenchMOS™ transistor Logic level FET

PHP80N06LT, PHB80N06LT

FEATURES

- **'Trench'** technology
- Very low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 55 V

I_D = 75 A

$R_{DS(ON)} \leq 14\ m\Omega$ (V_{GS} = 5 V)

$R_{DS(ON)} \leq 13\ m\Omega$ (V_{GS} = 10 V)

GENERAL DESCRIPTION

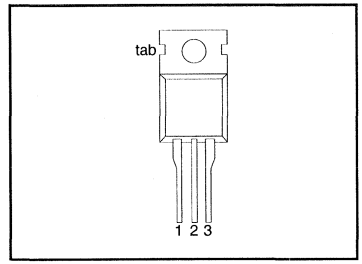
N-channel enhancement mode, logic level, field-effect power transistor in a plastic envelope using **'trench'** technology. The device has very low on-state resistance. It is intended for use in dc to dc converters and general purpose switching applications.

The PHP80N06LT is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHB80N06LT is supplied in the SOT404 surface mounting package.

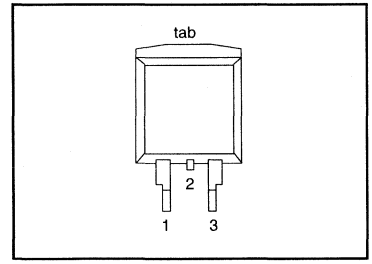
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

SOT78 (TO220AB)



SOT404



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 175°C	-	55	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 175°C; R_{GS} = 20 kΩ	-	55	V
V_{GS}	Gate-source voltage		-	± 13	V
I_D	Continuous drain current	T_{mb} = 25 °C	-	75	A
		T_{mb} = 100 °C	-	56	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	240	A
P_D	Total power dissipation	T_{mb} = 25 °C	-	178	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	175	°C

1 It is not possible to make connection to pin 2 of the SOT404 package.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	0.84	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	SOT78 package, in free air	60	-	K/W
		SOT404 package, pcb mounted, minimum footprint	50	-	K/W

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

ELECTRICAL CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	12	14	mΩ
		V_{GS} = 10 V; I_D = 25 A	-	10	13	mΩ
		T_j = 175˚C	-	-	30	mΩ
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	30	65	-	S
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	20	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
$Q_{g(tot)}$	Total gate charge	I_D = 50 A; V_{DD} = 44 V; V_{GS} = 5 V	-	43	-	nC
Q_{gs}	Gate-source charge		-	13	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	20	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	35	50	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω	-	95	145	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	130	180	ns
t_f	Turn-off fall time		-	60	80	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	2900	3800	pF
C_{oss}	Output capacitance		-	500	600	pF
C_{rss}	Feedback capacitance		-	240	330	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)		-	-	68	A
I_{SM}	Pulsed source current (body diode)		-	-	240	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 65 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 65 A; -dI_F/dt = 100 A/µs;	-	57	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.14	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 65 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 ˚C	-	200	mJ

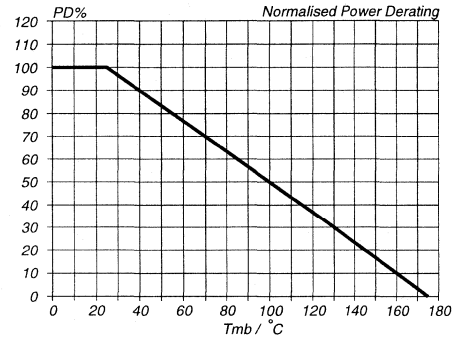


Fig.1. Normalised power dissipation.
PD% = 100·$P_D/P_{D\ 25\ ˚C}$ = f(T_{mb})

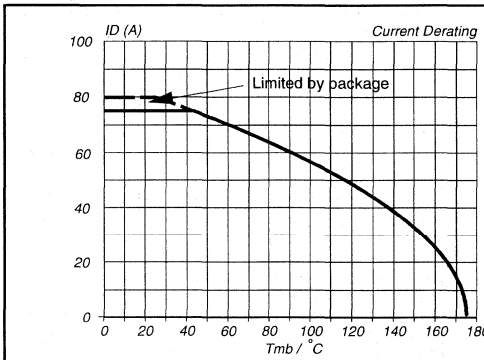


Fig.2. Normalised continuous drain current.
ID% = 100·$I_D/I_{D\ 25\ ˚C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

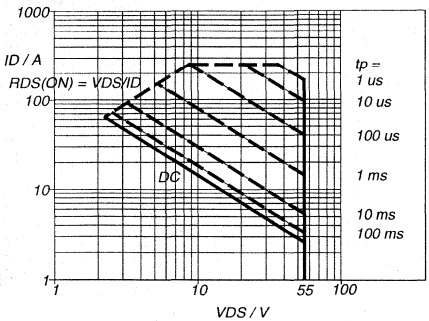


Fig.3. Safe operating area. T_{mb} = 25 ˚C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

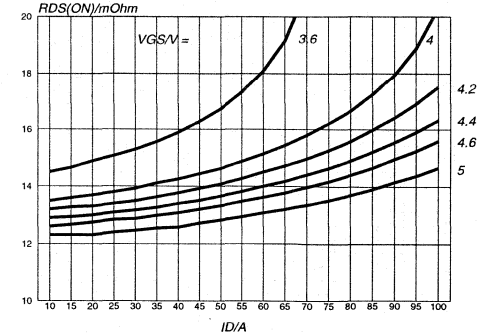


Fig.6. Typical on-state resistance, T_j = 25 ˚C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

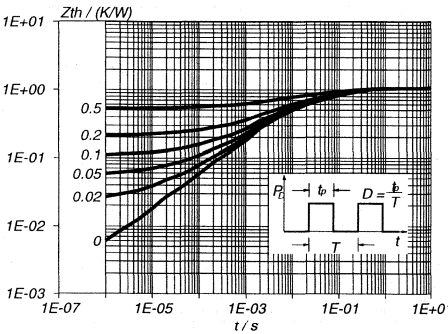


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

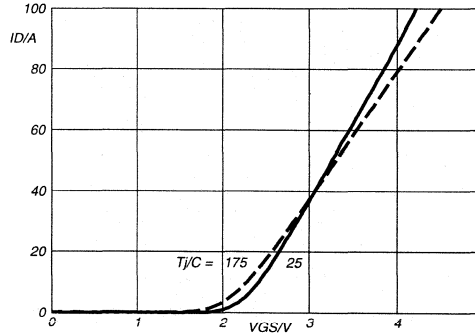


Fig.7. Typical transfer characteristics.
I_D = f(V_{GS}) ; conditions: V_{DS} = 25 V; parameter T_j

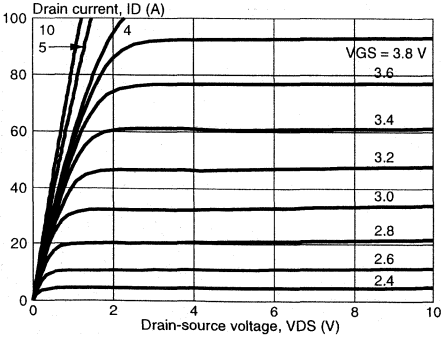


Fig.5. Typical output characteristics, T_j = 25 ˚C.
I_D = f(V_{DS}); parameter V_{GS}

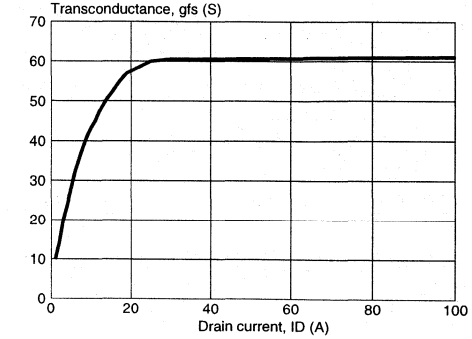


Fig.8. Typical transconductance, T_j = 25 ˚C.
g_{fs} = f(I_D); conditions: V_{DS} = 25 V

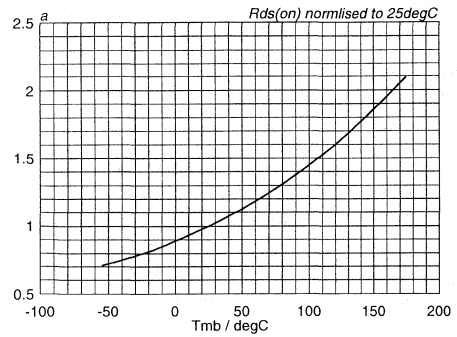


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

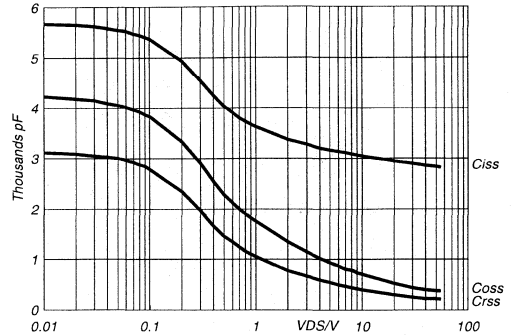


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

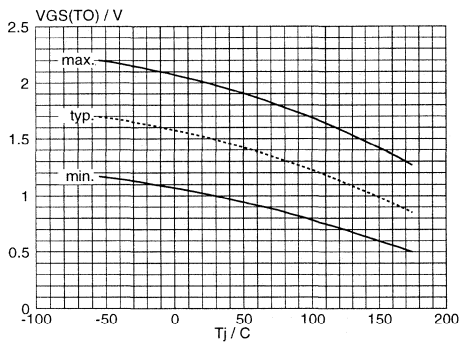


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

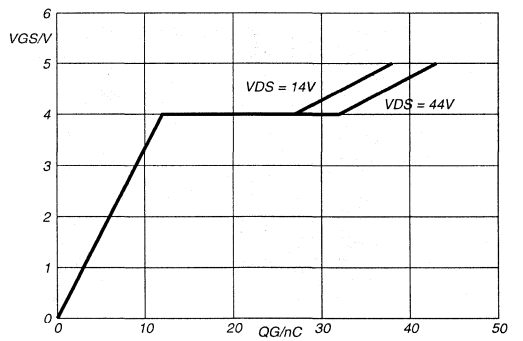


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: I_D = 50 A; parameter V_{DS}

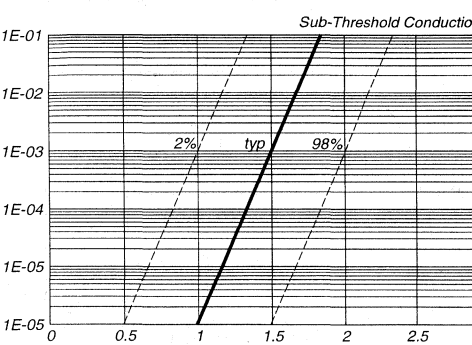


Fig.11. Sub-threshold drain current. $I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

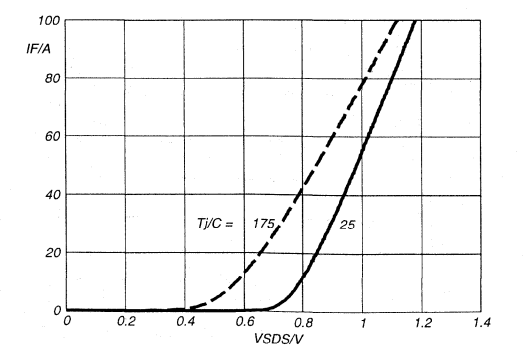


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

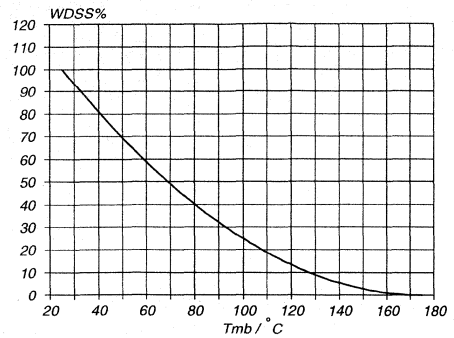


Fig.15. Normalised avalanche energy rating.
W_{DSS}% = f(T_{mb}); conditions: I_D = 75 A

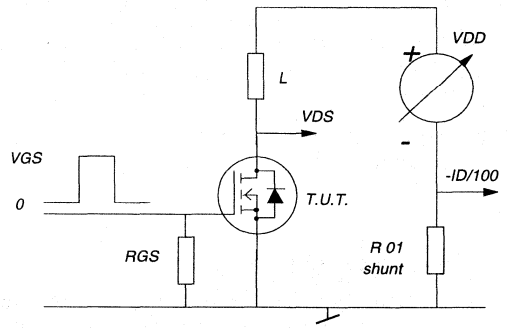


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

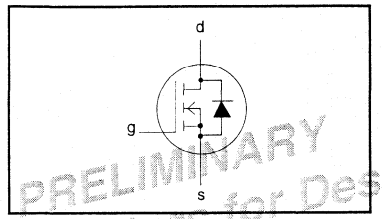
TrenchMOS™ transistor Logic level FET

PHP87N03LT, PHB87N03LT

FEATURES

- **'Trench'** technology
- Very low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 25 V

I_D = 75 A

$R_{DS(ON)} \leq 10.5\ m\Omega$ (V_{GS} = 5 V)

$R_{DS(ON)} \leq 9.5\ m\Omega$ (V_{GS} = 10 V)

PRELIMINARY
See Philips Semiconductors for Design-in information

GENERAL DESCRIPTION

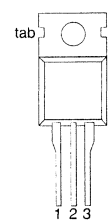
N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using '**trench**' technology. The device has very low on-state resistance. It is intended for use in dc to dc converters and general purpose switching applications.

The PHP87N03LT is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHB87N03LT is supplied in the SOT404 surface mounting package.

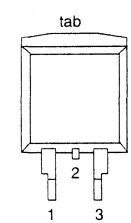
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

SOT78 (TO220AB)



SOT404



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 ˚C to 175˚C	-	25	V
V_{DGR}	Drain-gate voltage	T_j = 25 ˚C to 175˚C; R_{GS} = 20 kΩ	-	25	V
V_{GS}	Gate-source voltage		-	± 15	V
I_D	Continuous drain current	T_{mb} = 25 ˚C; V_{GS} = 5 V	-	75	A
		T_{mb} = 100 ˚C; V_{GS} = 5 V	-	61	A
I_{DM}	Pulsed drain current	T_{mb} = 25 ˚C	-	240	A
P_D	Total power dissipation	T_{mb} = 25 ˚C	-	142	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	175	˚C

1 It is not possible to make connection to pin 2 of the SOT404 package.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.05	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	SOT78 package, in free air	-	60	-	K/W
		SOT404 package, pcb mounted, minimum footprint	-	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	25	-	-	V
		T_j = -55˚C	22	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	1.5	2	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	9	10.5	mΩ
		V_{GS} = 10 V; I_D = 25 A	-	8.5	9.5	mΩ
		V_{GS} = 5 V; I_D = 25 A; T_j = 175˚C	-	-	19.5	mΩ
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	12	25	-	S
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	10	100	nA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 25 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
$Q_{g(tot)}$	Total gate charge	I_D = 75 A; V_{DD} = 24 V; V_{GS} = 5 V	-	58	-	nC
Q_{gs}	Gate-source charge		-	6	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	24	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 15 V; I_D = 25 A;	-	35	50	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 5 Ω	-	95	145	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	130	180	ns
t_f	Turn-off fall time		-	60	80	ns
L_d	Internal drain inductance	Measured tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	2500	-	pF
C_{oss}	Output capacitance		-	640	-	pF
C_{rss}	Feedback capacitance		-	320	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)		-	-	75	A
I_{SM}	Pulsed source current (body diode)		-	-	240	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 40 A; V_{GS} = 0 V	-	1.0	-	
t_{rr}	Reverse recovery time	I_F = 75 A; -dI_F/dt = 100 A/µs;	-	70	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 25 V	-	0.14	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 45 A; $V_{DD} \leq$ 15 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	200	mJ

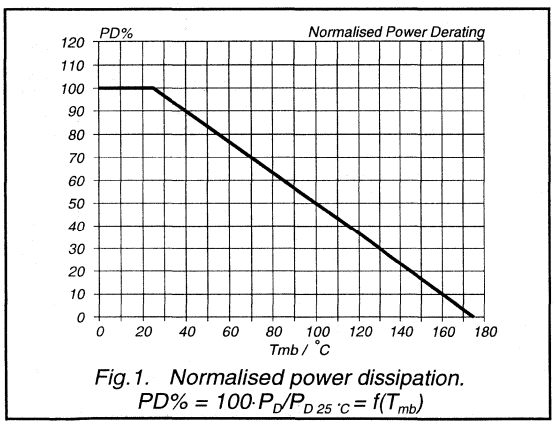


Fig.1. Normalised power dissipation.
PD% = 100·$P_D/P_{D\ 25\ °C}$ = f(T_{mb})

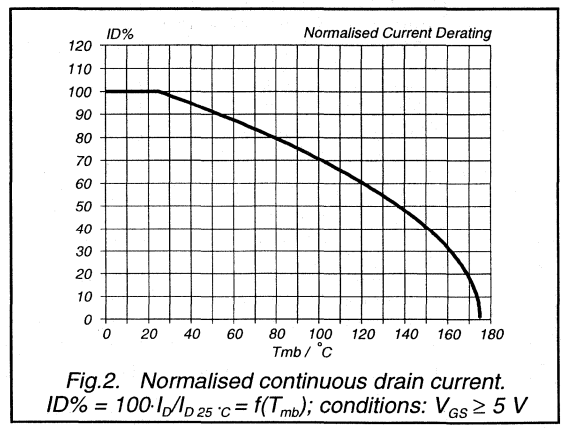


Fig.2. Normalised continuous drain current.
ID% = 100·$I_D/I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

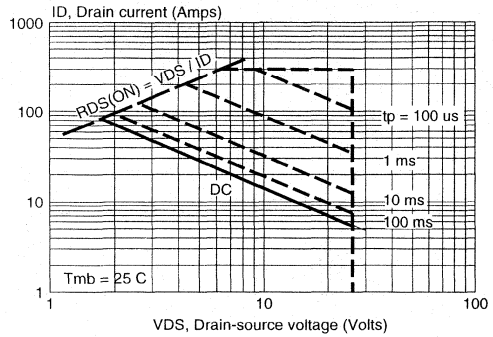


Fig.3. Safe operating area
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

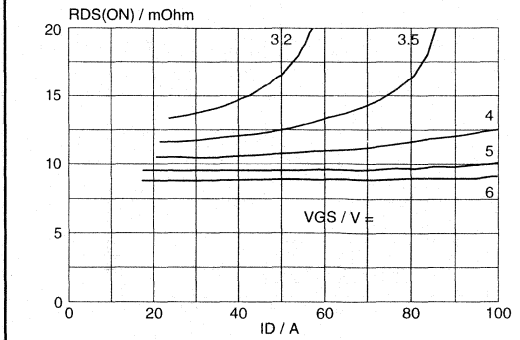


Fig.6. Typical on-state resistance, T_j = 25 ˚C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

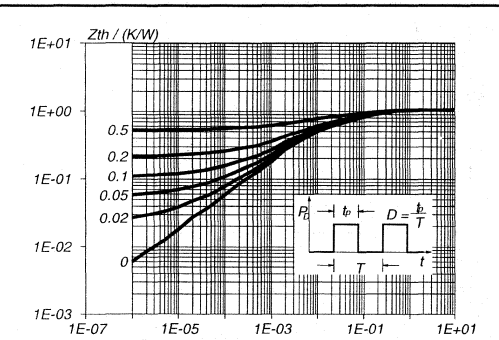


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

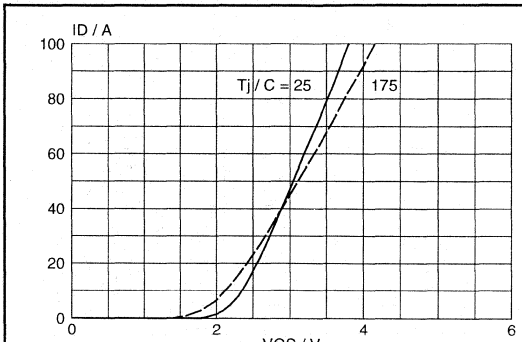


Fig.7. Typical transfer characteristics.
I_D = f(V_{GS}) ; conditions: V_{DS} = 25 V; parameter T_j

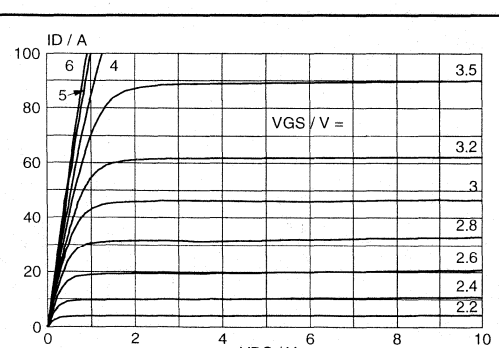


Fig.5. Typical output characteristics, T_j = 25 ˚C.
I_D = f(V_{DS}); parameter V_{GS}

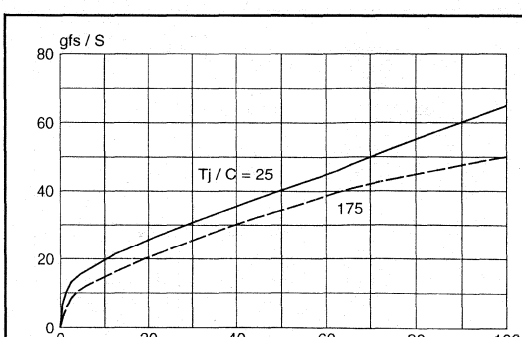


Fig.8. Typical transconductance, T_j = 25 ˚C.
g_{fs} = f(I_D); conditions: V_{DS} = 25 V

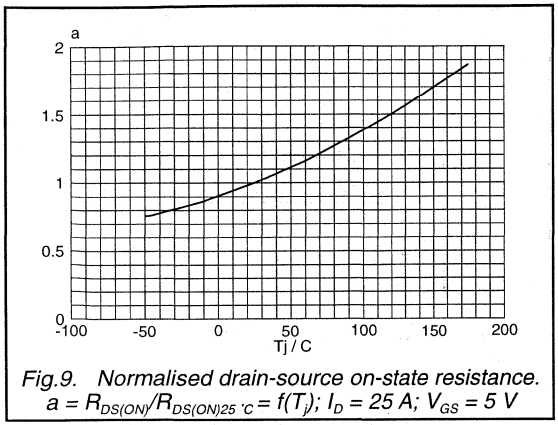


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

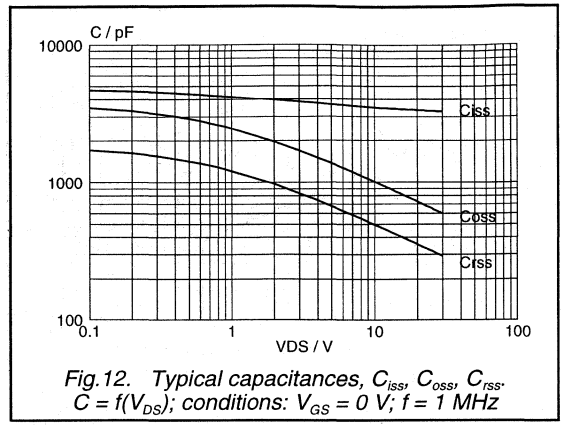


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

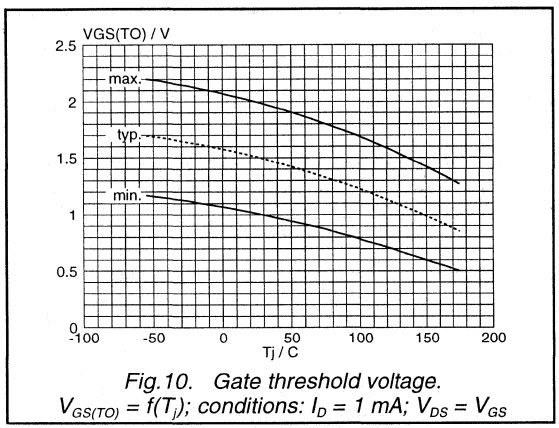


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

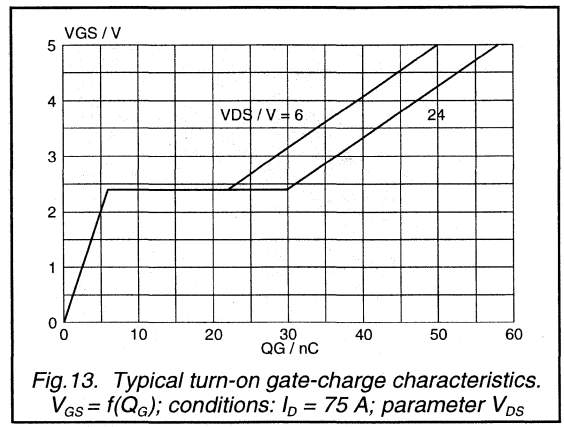


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: I_D = 75 A; parameter V_{DS}

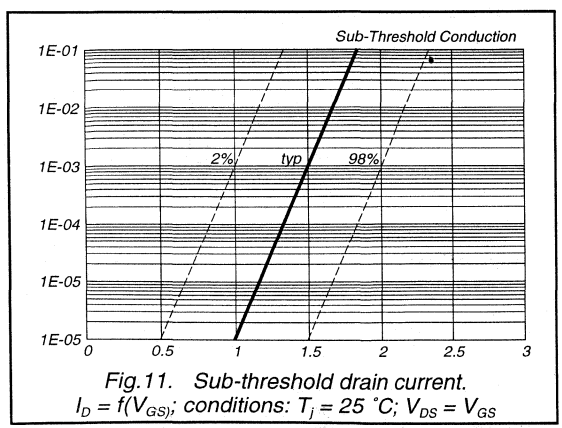


Fig.11. Sub-threshold drain current. $I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

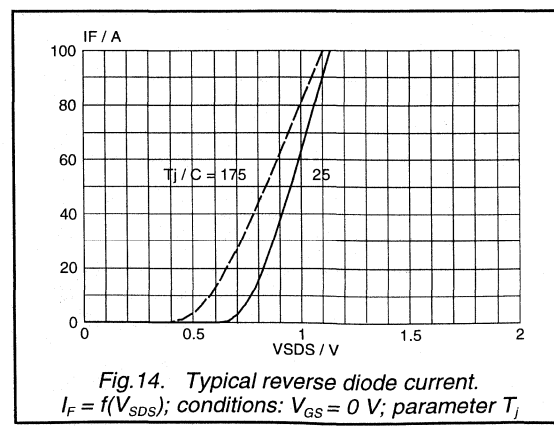


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

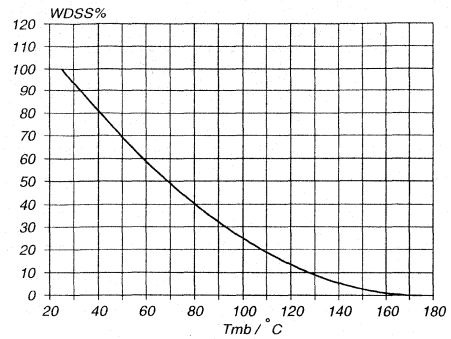


Fig.15. Normalised avalanche energy rating.
W_{DSS}% = f(T_{mb}); conditions: I_D = 45 A

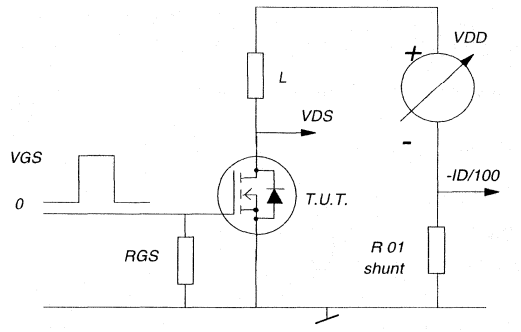


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

P-channel enhancement mode MOS transistor

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FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

DESCRIPTION

P-channel enhancement mode MOS transistor in an 8-pin plastic SO8 (SOT96-1) package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SO8 (SOT96-1)

PIN	SYMBOL	DESCRIPTION
1	n.c.	not connected
2	s	source
3	s	source
4	g	gate
5	d	drain
6	d	drain
7	d	drain
8	d	drain

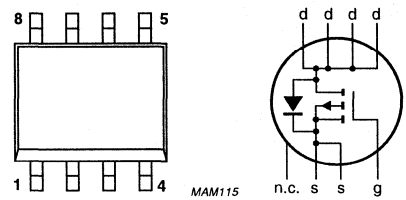

Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{SD}	source-drain diode forward voltage	I_S = –1.25 A	–	–1.3	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = –1 mA; V_{DS} = V_{GS}	–1	–2.8	V
I_D	drain current (DC)	T_s = 80 °C	–	–5	A
R_{DSon}	drain-source on-state resistance	I_D = –2.5 A; V_{GS} = –10 V	–	0.09	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	4	W

P-channel enhancement mode MOS transistor

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	–5	A
I_{DM}	peak drain current	note 2	–	–20	A
P_{tot}	total power dissipation	T_s = 80 °C	–	4	W
		T_{amb} = 25 °C; note 3	–	2.7	W
		T_{amb} = 25 °C; note 4	–	1.15	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–65	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	–3	A
I_{SM}	peak pulsed source current	note 2	–	–12	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Value based on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Value based on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

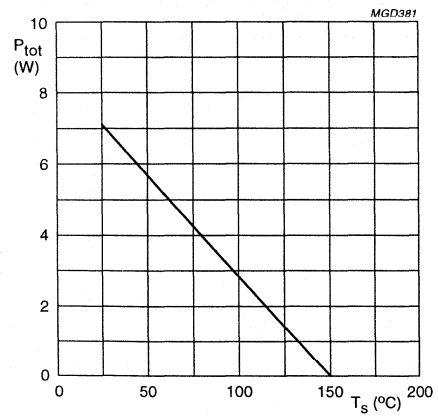
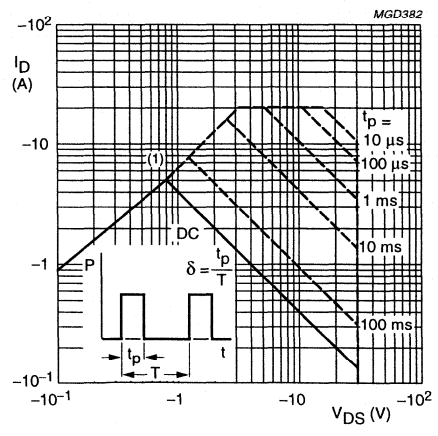


Fig.2 Power derating curve.



δ = 0.01; T_S = 80 °C.
(1) R_{DSon} limitation.

Fig.3 SOAR.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	17.5	K/W

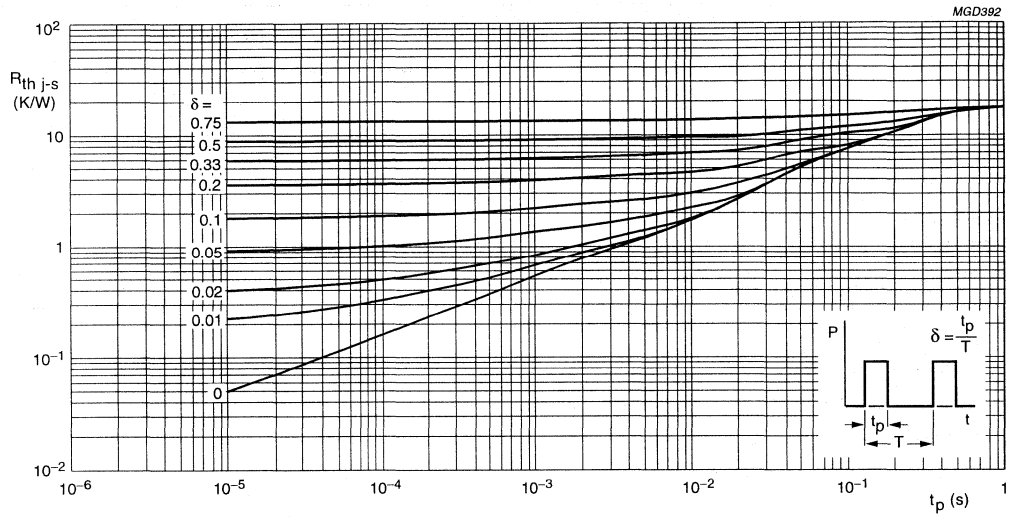


Fig.4 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

P-channel enhancement mode MOS transistor

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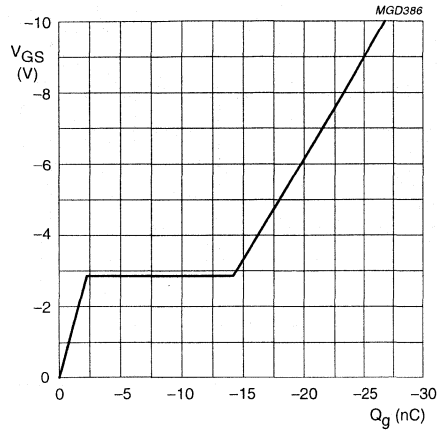
CHARACTERISTICS

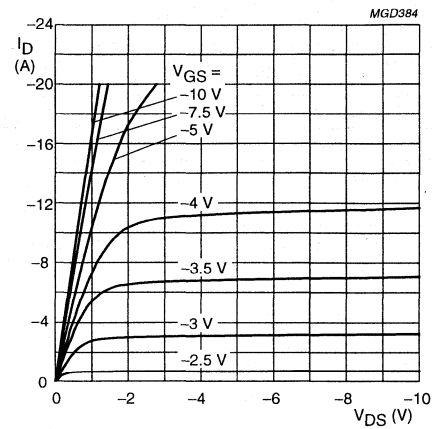
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−1	–	−2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −24 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = −4.5 V; I_D = −1.25 A	–	–	0.15	Ω
		V_{GS} = −10 V; I_D = −2.5 A	–	–	0.09	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	825	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	350	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	150	–	pF
Q_G	total gate charge	V_{GS} = −10 V; V_{DD} = −15 V; I_D = −2.5 A	–	30	40	nC
Q_{GS}	gate-source charge	V_{GS} = −10 V; V_{DD} = −15 V; I_D = −2.5 A	–	3	–	nC
Q_{GD}	gate-drain charge	V_{GS} = −10 V; V_{DD} = −15 V; I_D = −2.5 A	–	12	–	nC
Switching times (see Fig.11)						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to −10 V; V_{DD} = −15 V; I_D = −1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	7	–	ns
t_f	fall time		–	10	–	ns
t_{on}	turn-on switching time		–	17	35	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = −10 to 0 V; V_{DD} = −15 V; I_D = −1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	60	–	ns
t_r	rise time		–	40	–	ns
t_{off}	turn-off switching time		–	100	200	ns
Source-drain diode						
V_{SD}	source-drain forward voltage	V_{GD} = 0; I_S = −1.25 A	–	–	−1.3	V
t_{rr}	reverse recovery time	I_S = −1.25 A; di/dt = 100 A/μs	–	70	–	ns



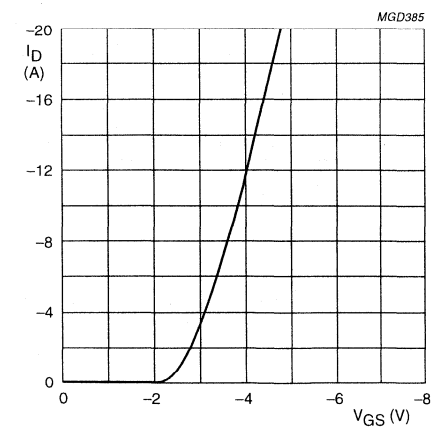
V_{DD} = −15 V; I_D = −2.5 A.

Fig.5 Gate-source voltage as a function of total gate charge; typical values.



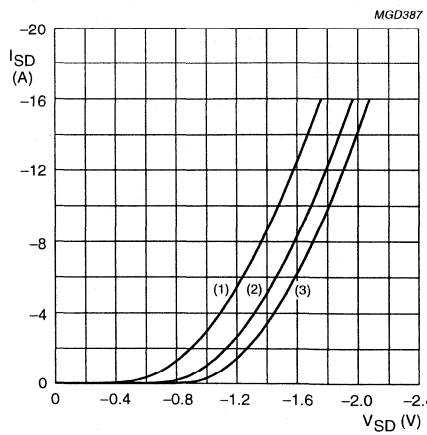
T_j = 25 °C.

Fig.6 Output characteristics; typical values.



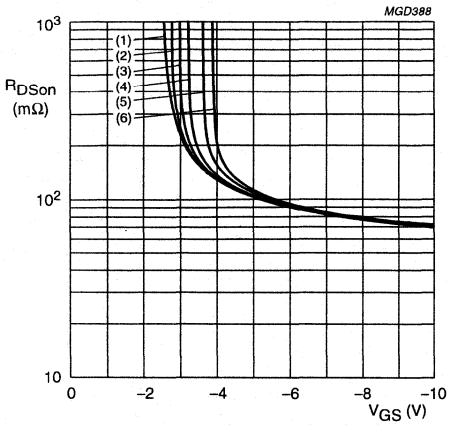
V_{DS} = −10 V; T_j = 25 °C.

Fig.7 Transfer characteristics; typical values.



V_{GD} = 0.
(1) T_j = 150 °C.
(2) T_j = 25 °C.
(3) T_j = −65 °C.

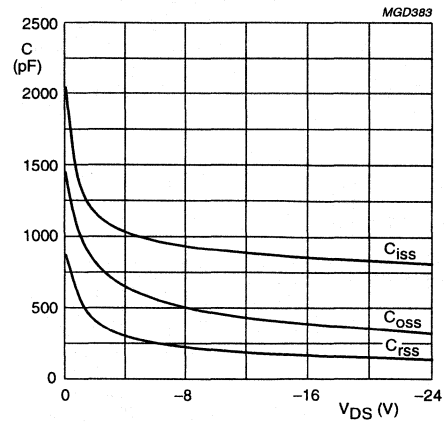
Fig.8 Source current as a function of source-drain diode forward voltage; typical values.



$V_{DS} \geq I_D \times R_{DSon}$; T_j = 25 °C.

(1) I_D = −100 mA.
(2) I_D = −500 mA.
(3) I_D = −1.25 A.
(4) I_D = −2.5 A.
(5) I_D = −5 A.
(6) I_D = −7 A.

Fig.9 Drain source on-state resistance as a function of gate-source voltage; typical values.



V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

Fig.10 Capacitance as a function of drain-source voltage; typical values.

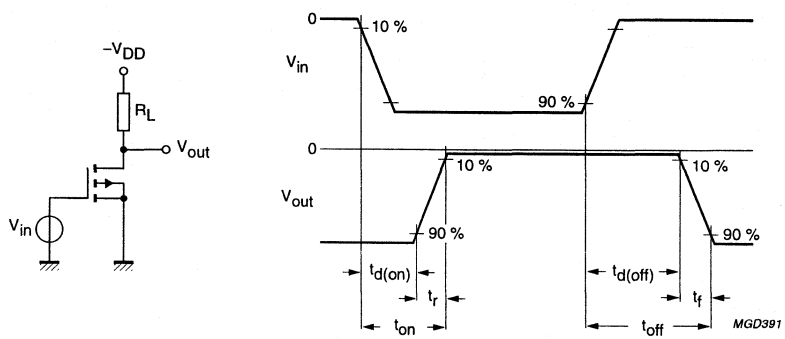
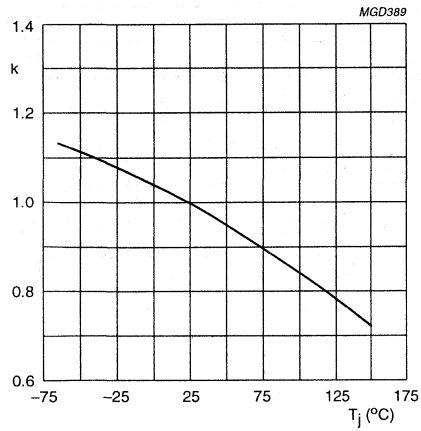


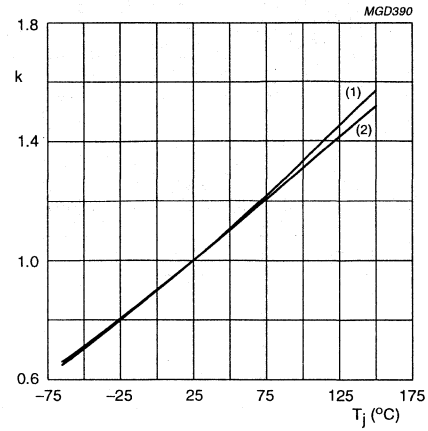
Fig.11 Switching times test circuit and input and output waveforms.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

V_{GSth} at $V_{DS} = V_{GS}$; $I_D = -1$ mA.

Fig.12 Temperature coefficient of gate-source threshold voltage as a function of junction temperature; typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

R_{DSon} at:

(1) $V_{GS} = -10$ V; $I_D = -2.5$ A.

(2) $V_{GS} = -4.5$ V; $I_D = -1.25$ A.

Fig.13 Temperature coefficient of drain-source on-resistance as a function of junction temperature; typical values.

P-channel enhancement mode MOS transistor

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FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

PINNING - SO8 (SOT96-1)

PIN	SYMBOL	DESCRIPTION
1	n.c.	not connected
2	s	source
3	s	source
4	g	gate
5	d	drain
6	d	drain
7	d	drain
8	d	drain

DESCRIPTION

P-channel enhancement mode MOS transistor in an 8-pin plastic SO8 (SOT96-1) package.

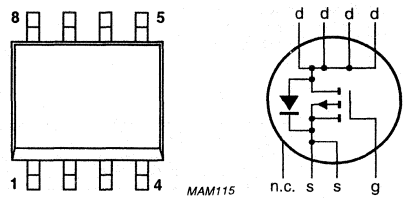


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{SD}	source-drain diode forward voltage	I_S = –1.25 A	–	–1.6	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = –1 mA; V_{DS} = V_{GS}	–1	–2.8	V
I_D	drain current (DC)	T_s = 80 °C	–	–2.5	A
R_{DSon}	drain-source on-state resistance	I_D = –1 A; V_{GS} = –10 V	–	0.25	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	2.8	W

P-channel enhancement mode MOS transistor

PHP125

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	–2.5	A
I_{DM}	peak drain current	note 2	–	–10	A
P_{tot}	total power dissipation	T_s = 80 °C	–	2.8	W
		T_{amb} = 25 °C; note 3	–	2.4	W
		T_{amb} = 25 °C; note 4	–	1.1	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–65	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	–2	A
I_{SM}	peak pulsed source current	note 2	–	–8	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Value based on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Value based on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

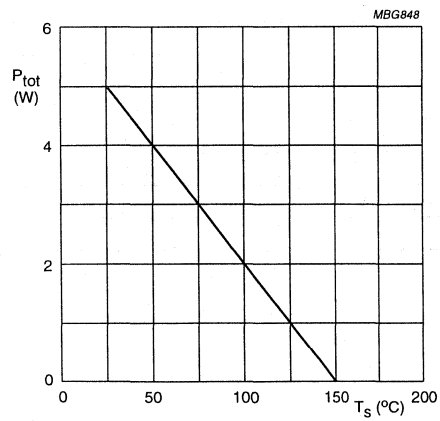
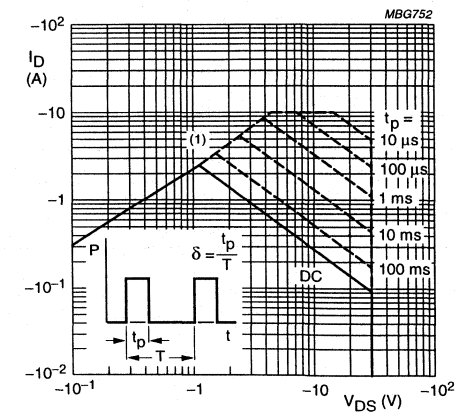


Fig.2 Power derating curve.



δ = 0.01; T_S = 80 °C.
(1) R_{DSon} limitation.

Fig.3 SOAR.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	25	K/W

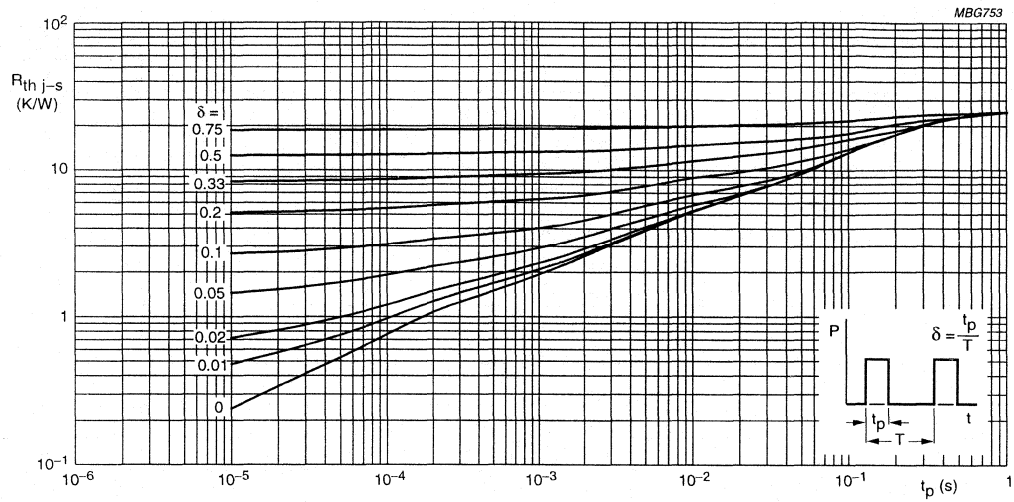


Fig.4 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

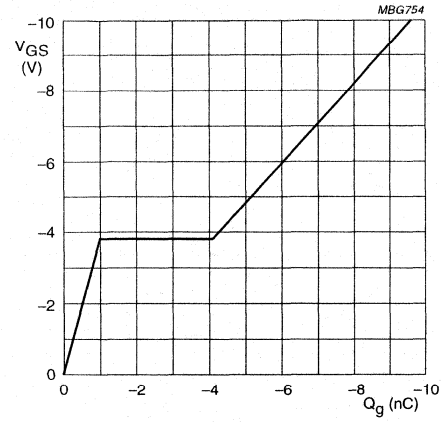
P-channel enhancement mode MOS transistor

PHP125

CHARACTERISTICS

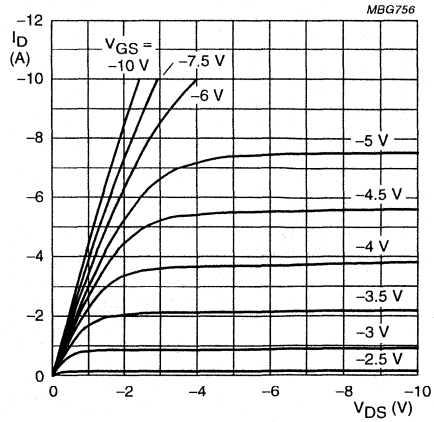
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−1	–	−2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −24 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = −4.5 V; I_D = −0.5 A	–	0.33	0.4	Ω
		V_{GS} = −10 V; I_D = −1 A	–	0.22	0.25	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	250	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	140	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	50	–	pF
Q_G	total gate charge	V_{GS} = −10 V; V_{DS} = −15 V; I_D = −1 A	–	10	25	nC
Q_{GS}	gate-source charge	V_{GS} = −10 V; V_{DS} = −15 V; I_D = −1 A	–	1	–	nC
Q_{GD}	gate-drain charge	V_{GS} = −10 V; V_{DS} = −15 V; I_D = −1 A	–	3	–	nC
Switching times (see Fig.11)						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to −10 V; V_{DD} = −15 V; I_D = −1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	4.5	–	ns
t_f	fall time		–	3.5	–	ns
t_{on}	turn-on switching time		–	8	16	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = −10 to 0 V; V_{DD} = −15 V; I_D = −1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	25	–	ns
t_r	rise time		–	15	–	ns
t_{off}	turn-off switching time		–	40	80	ns
Source-drain diode						
V_{SD}	source-drain forward voltage	V_{GD} = 0; I_S = −1.25 A	–	–	−1.6	V
t_{rr}	reverse recovery time	I_S = −1.25 A; di/dt = 100 A/μs	–	150	200	ns



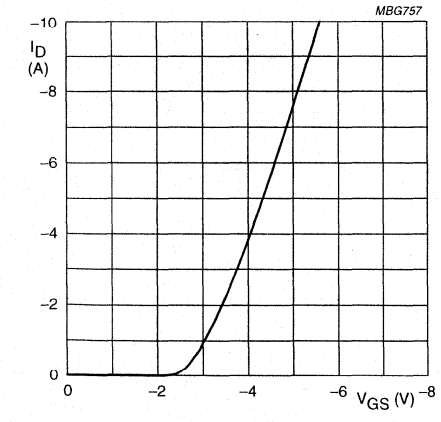
V_{DD} = −15 V; I_D = −1 A.

Fig.5 Gate-source voltage as a function of total gate charge; typical values.



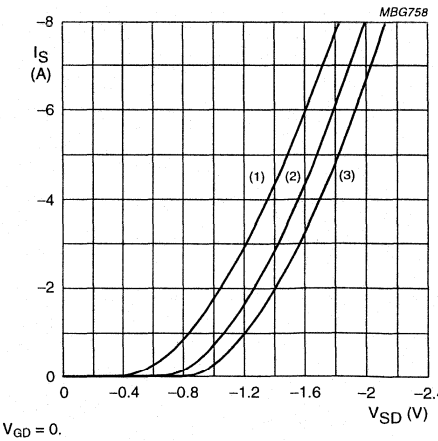
T_j = 25 °C.

Fig.6 Output characteristics; typical values.



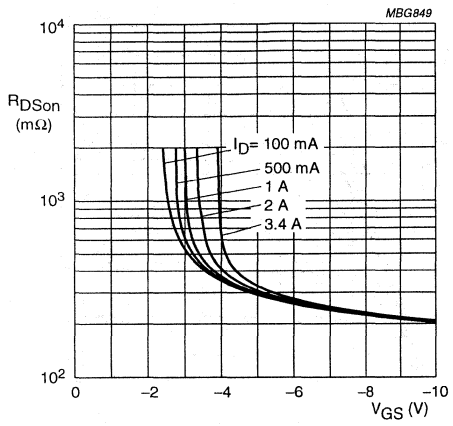
V_{DS} = −10 V; T_j = 25 °C.

Fig.7 Transfer characteristics; typical values.



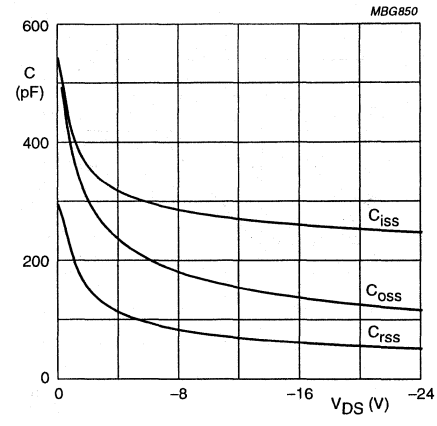
V_{GD} = 0.
(1) T_j = 150 °C.
(2) T_j = 25 °C.
(3) T_j = −65 °C.

Fig.8 Source current as a function of source-drain diode forward voltage; typical values.



$V_{DS} \geq I_D \times R_{DSon}$; T_j = 25 °C.

Fig.9 Drain source on-resistance as a function of gate-source voltage; typical values.



V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

Fig.10 Capacitance as a function of drain-source voltage; typical values.

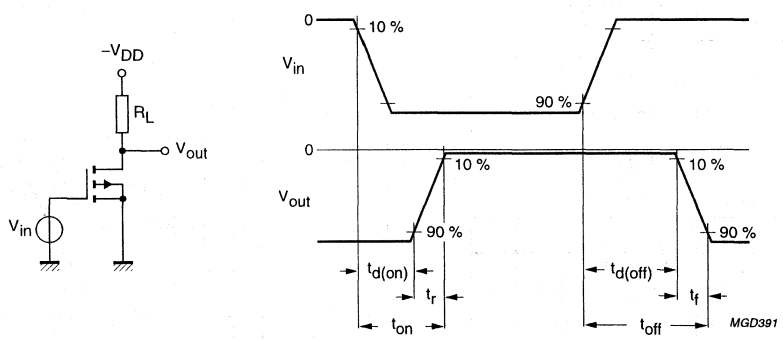
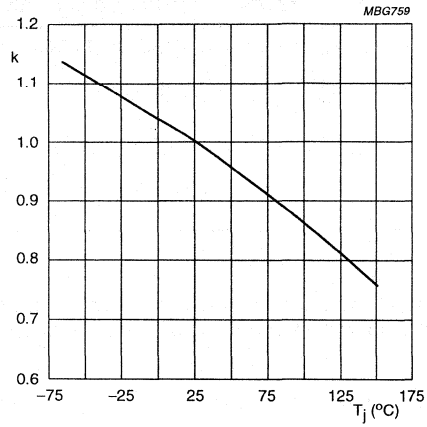


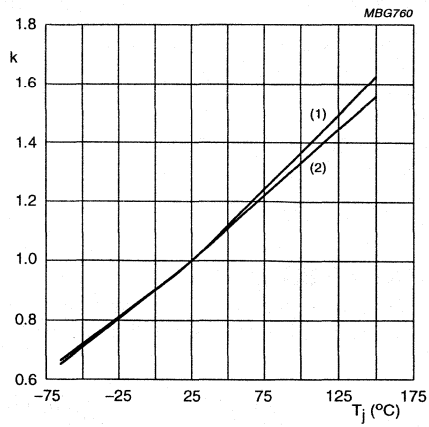
Fig.11 Switching time test circuit and input and output waveforms.



$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$ Typical V_{GSth} at:

(1) $I_D = -1$ mA; $V_{DS} = V_{GS}$.

Fig.12 Temperature coefficient of gate-source threshold voltage; typical values.



$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$ Typical R_{DSon} at:

(1) $I_D = -1$ A; $V_{GS} = -10$ V.

(2) $I_D = -0.5$ A; $V_{GS} = -4.5$ V.

Fig.13 Temperature coefficient of drain-source on-resistance; typical values.

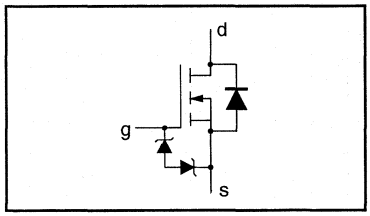
TrenchMOS™ transistor Logic level FET

PHP125N06LT, PHB125N06LT

FEATURES

- **'Trench'** technology
- Very low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 55 V

I_D = 75 A

$R_{DS(ON)} \leq 8\ m\Omega$ (V_{GS} = 5 V)

$R_{DS(ON)} \leq 6\ m\Omega$ (V_{GS} = 10 V)

GENERAL DESCRIPTION

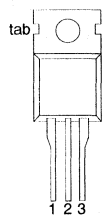
N-channel enhancement mode, logic level, field-effect power transistor in a plastic envelope using **'trench'** technology. The device has very low on-state resistance. It is intended for use in dc to dc converters and general purpose switching applications.

The PHP125N06LT is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHB125N06LT is supplied in the SOT404 surface mounting package.

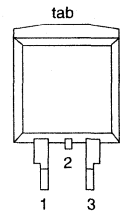
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

SOT78 (TO220AB)



SOT404



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 175°C	-	55	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 175°C; R_{GS} = 20 kΩ	-	55	V
V_{GS}	Gate-source voltage		-	± 13	V
I_D	Continuous drain current	T_{mb} = 25 °C	-	75	A
		T_{mb} = 100 °C	-	75	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	240	A
P_D	Total power dissipation	T_{mb} = 25 °C	-	250	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	175	°C

1 It is not possible to make connection to pin 2 of the SOT404 package.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	0.6	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	SOT78 package, in free air	60	-	K/W
		SOT404 package, pcb mounted, minimum footprint	50	-	K/W

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

ELECTRICAL CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	6.5	8	mΩ
		V_{GS} = 10 V; I_D = 25 A	-	4.5	6	mΩ
		T_j = 175˚C	-	-	17	mΩ
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	10	45	-	S
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	20	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
$Q_{g(tot)}$	Total gate charge	I_D = 50 A; V_{DD} = 44 V; V_{GS} = 5 V	-	84	-	nC
Q_{gs}	Gate-source charge		-	18	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	39	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	45	60	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω	-	120	170	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	225	300	ns
t_f	Turn-off fall time		-	100	135	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	5200	6900	pF
C_{oss}	Output capacitance		-	840	1000	pF
C_{rss}	Feedback capacitance		-	350	480	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)		-	-	75	A
I_{SM}	Pulsed source current (body diode)		-	-	240	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.85	1.2	V
		I_F = 75 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 75 A; -dI_F/dt = 100 A/µs;	-	65	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.18	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 75 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 ˚C	-	500	mJ

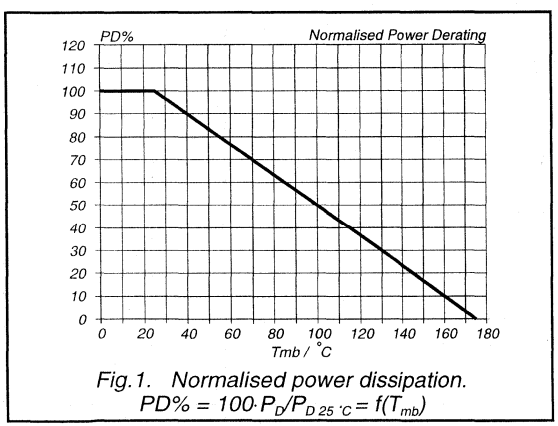


Fig.1. Normalised power dissipation.
PD% = 100·$P_D/P_{D\ 25\ ˚C}$ = f(T_{mb})

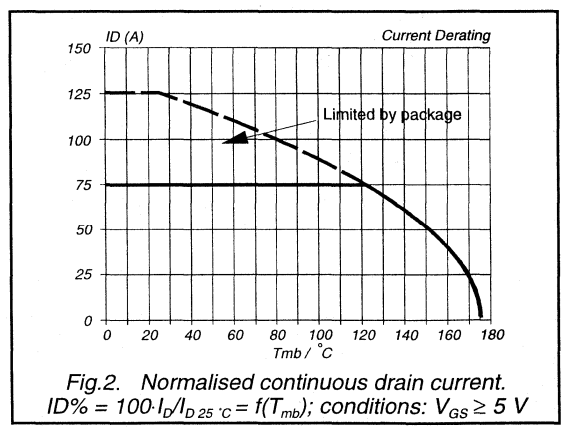


Fig.2. Normalised continuous drain current.
ID% = 100·$I_D/I_{D\ 25\ ˚C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

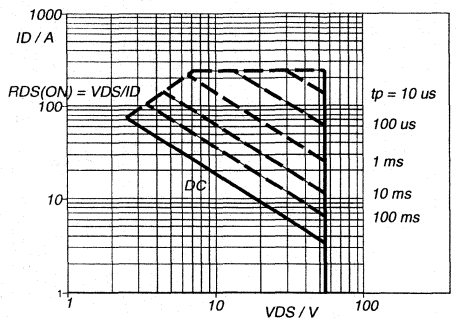


Fig.3. Safe operating area. T_{mb} = 25 ˚C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

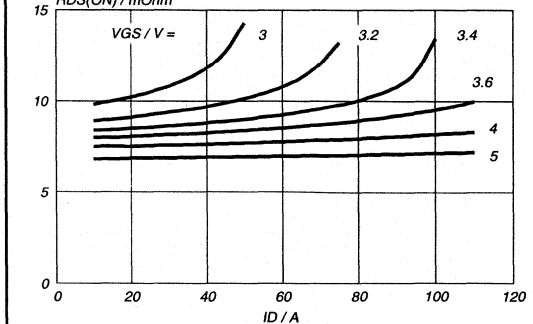


Fig.6. Typical on-state resistance, T_j = 25 ˚C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

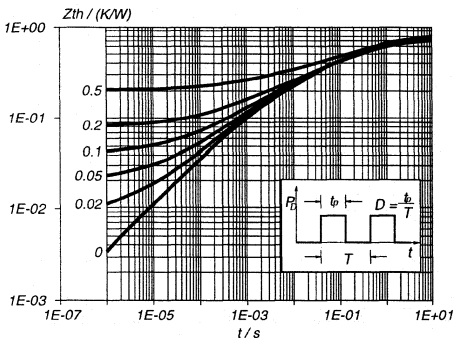


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

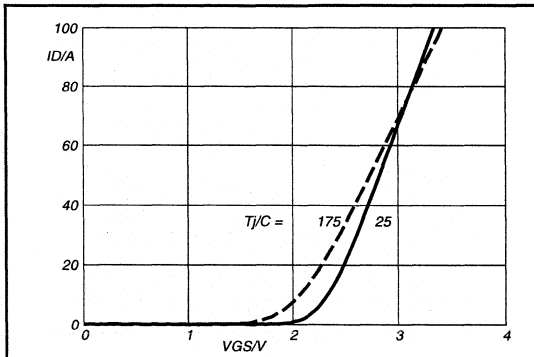


Fig.7. Typical transfer characteristics.
I_D = f(V_{GS}) ; conditions: V_{DS} = 25 V; parameter T_j

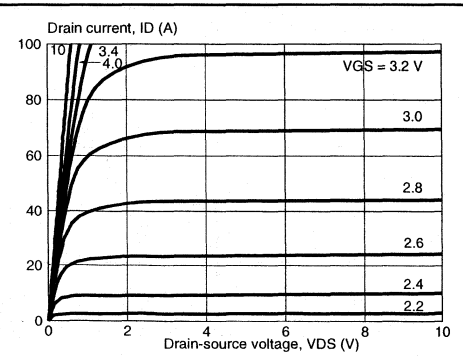


Fig.5. Typical output characteristics, T_j = 25 ˚C.
I_D = f(V_{DS}); parameter V_{GS}

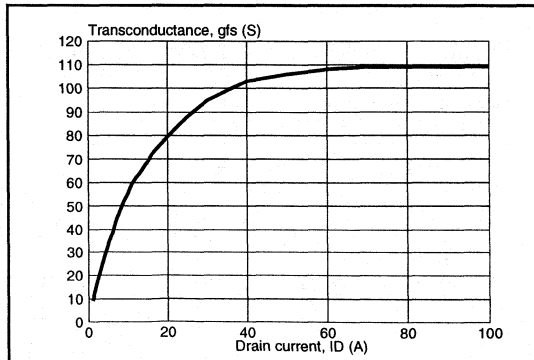


Fig.8. Typical transconductance, T_j = 25 ˚C.
g_{fs} = f(I_D); conditions: V_{DS} = 25 V

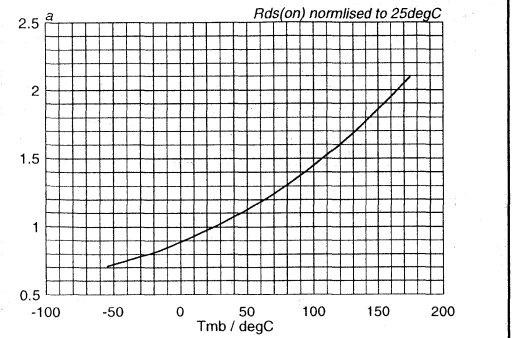


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

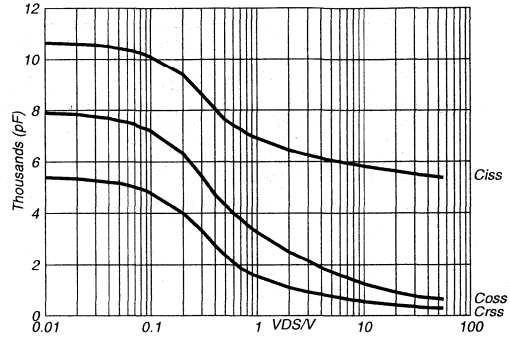


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

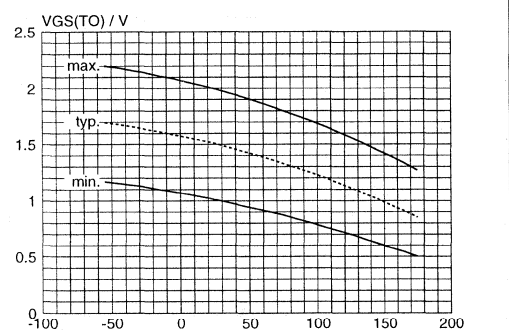


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

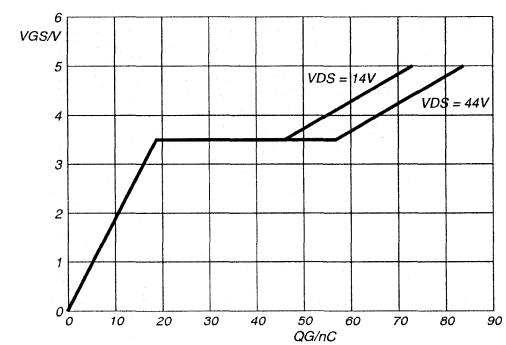


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 50 A; parameter V_{DS}

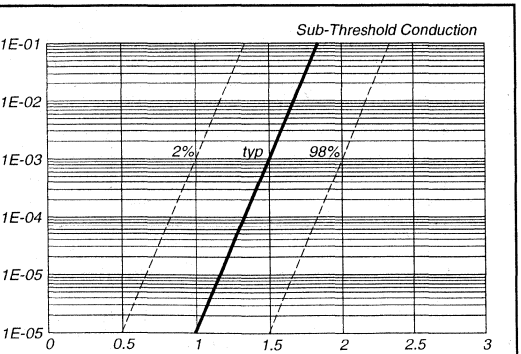


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

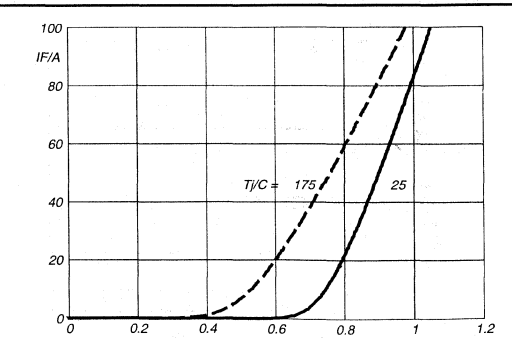


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

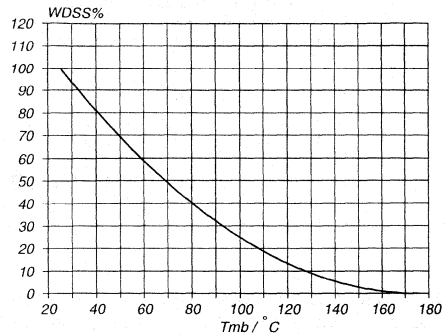


Fig.15. Normalised avalanche energy rating.
W_{DSS}% = f(T_{mb}); conditions: I_D = 75 A

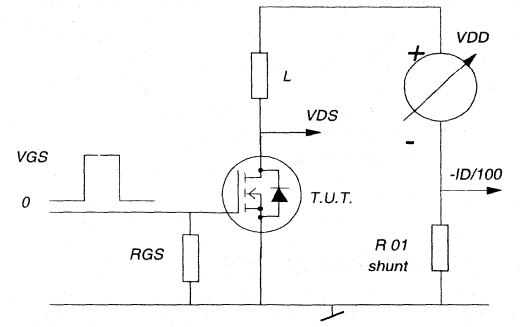


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

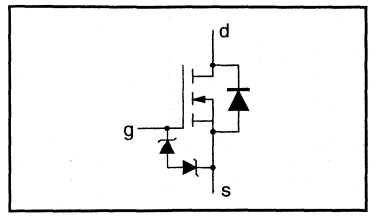
TrenchMOS™ transistor Logic level FET

PHP130N03LT, PHB130N03LT

FEATURES

- **'Trench'** technology
- Very low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 30 V

I_D = 75 A

$R_{DS(ON)} \leq 6\ m\Omega$ (V_{GS} = 5 V)

$R_{DS(ON)} \leq 5\ m\Omega$ (V_{GS} = 10 V)

GENERAL DESCRIPTION

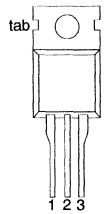
N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using **'trench'** technology. The device has very low on-state resistance. It is intended for use in dc to dc converters and general purpose switching applications.

The PHP130N03LT is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHB130N03LT is supplied in the SOT404 surface mounting package.

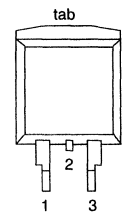
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

SOT78 (TO220AB)



SOT404



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 175°C	-	30	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 175°C; R_{GS} = 20 kΩ	-	30	V
V_{GS}	Gate-source voltage		-	± 13	V
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 5 V	-	75	A
		T_{mb} = 100 °C; V_{GS} = 5 V	-	75	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	240	A
P_D	Total power dissipation	T_{mb} = 25 °C	-	187	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	175	°C

1 It is not possible to make connection to pin 2 of the SOT404 package.

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	0.8	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	SOT78 package, in free air	-	60	-	K/W
		SOT404 package, pcb mounted, minimum footprint	-	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	30	-	-	V
		T_j = -55˚C	27	-	-	V
$V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = 1 mA	10	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	1.5	2	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	5	6	mΩ
		V_{GS} = 10 V; I_D = 25 A	-	4.5	5	mΩ
		V_{GS} = 5 V; I_D = 25 A; T_j = 175˚C	-	-	11	mΩ
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	20	40	-	S
I_{GSS}	Gate-source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V;	-	0.02	1	µA
		T_j = 175˚C	-	-	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 30 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
$Q_{g(tot)}$	Total gate charge	I_D = 75 A; V_{DD} = 24 V; V_{GS} = 5 V	-	92	-	nC
Q_{gs}	Gate-source charge		-	10	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	36	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 15 V; I_D = 25 A;	-	45	60	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 5 Ω	-	120	170	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	225	300	ns
t_f	Turn-off fall time		-	100	135	ns
L_d	Internal drain inductance	Measured tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	5000	-	pF
C_{oss}	Output capacitance		-	1150	-	pF
C_{rss}	Feedback capacitance		-	500	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)		-	-	75	A
I_{SM}	Pulsed source current (body diode)		-	-	240	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.85	1.2	V
		I_F = 75 A; V_{GS} = 0 V	-	1.0	-	
t_{rr}	Reverse recovery time	I_F = 75 A; -dI_F/dt = 100 A/µs;	-	100	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 25 V	-	0.6	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 75 A; $V_{DD} \leq$ 15 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 ˚C	-	500	mJ

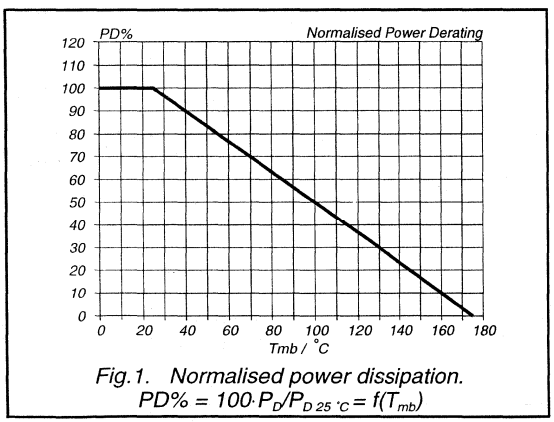


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ ˚C}$ = f(T_{mb})

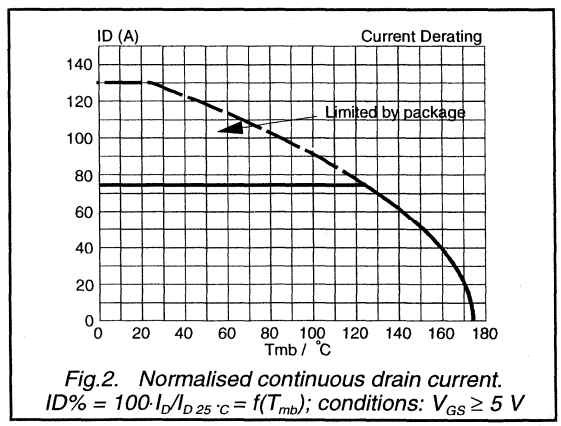


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ ˚C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

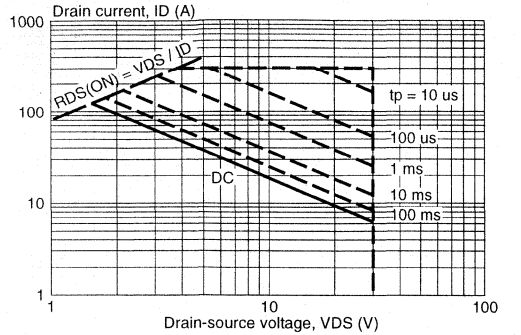


Fig.3. Safe operating area. T_{mb} = 25 ˚C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

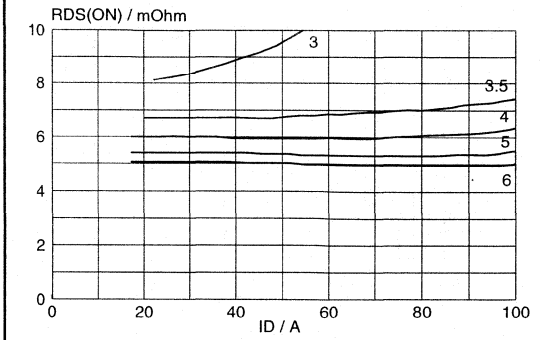


Fig.6. Typical on-state resistance, T_j = 25 ˚C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

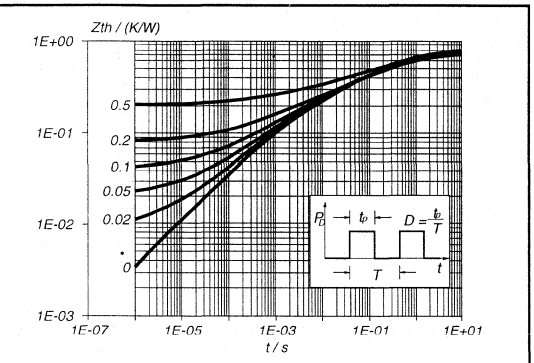


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

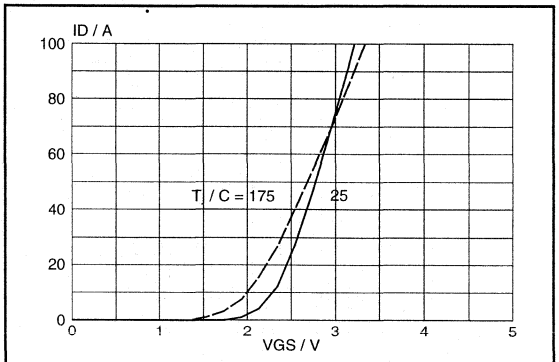


Fig.7. Typical transfer characteristics.
I_D = f(V_{GS}) ; conditions: V_{DS} = 25 V; parameter T_j

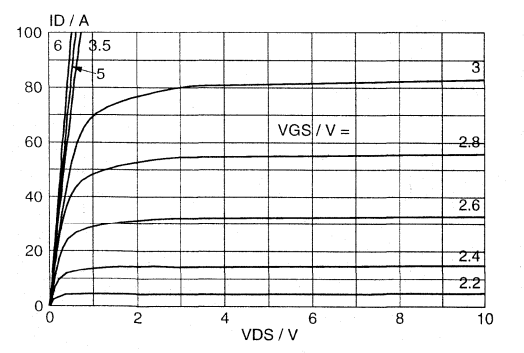


Fig.5. Typical output characteristics, T_j = 25 ˚C.
I_D = f(V_{DS}); parameter V_{GS}

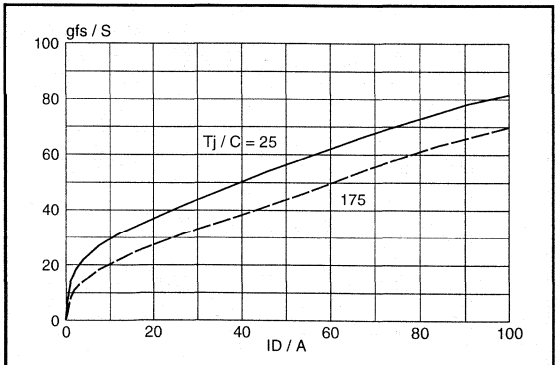


Fig.8. Typical transconductance, T_j = 25 ˚C.
g_{fs} = f(I_D); conditions: V_{DS} = 25 V

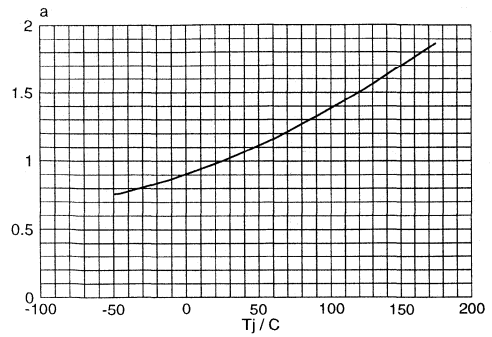


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

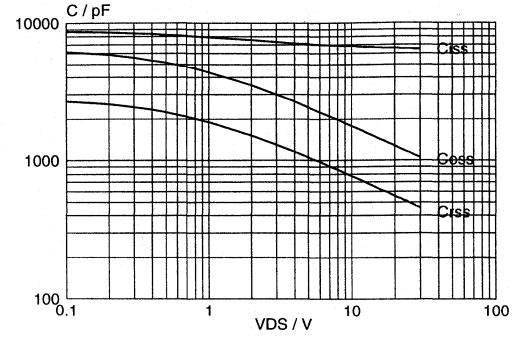


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

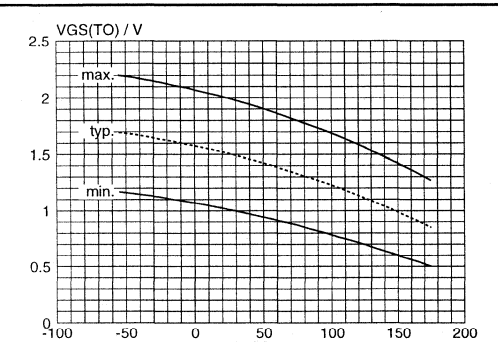


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

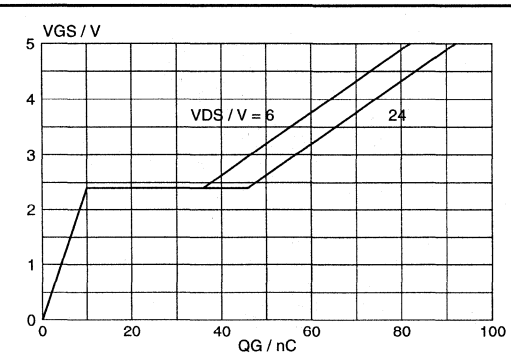


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 75 A; parameter V_{DS}

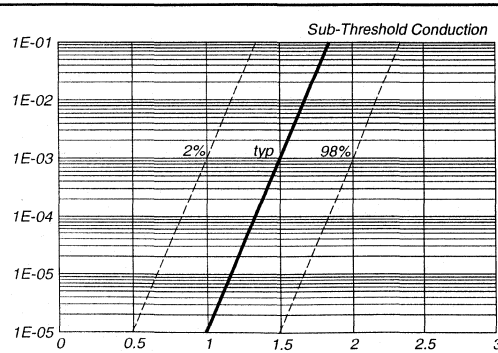


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

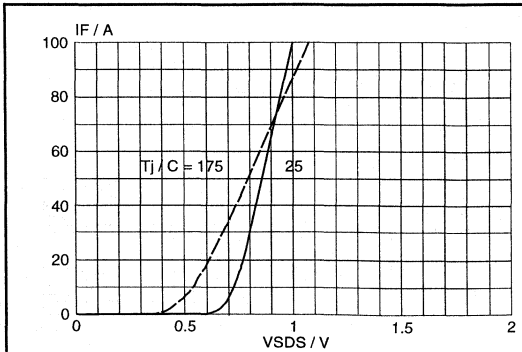


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

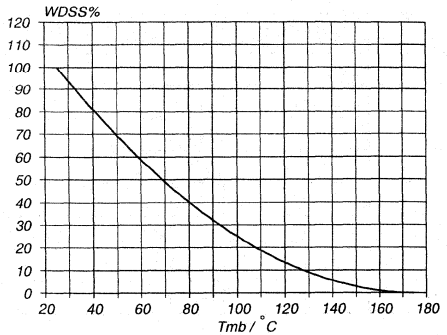


Fig.15. Normalised avalanche energy rating.
W_{DSS}% = f(T_{mb}); conditions: I_D = 75 A

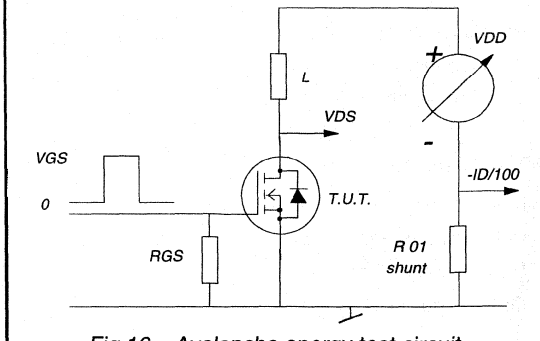


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

Dual P-channel enhancement mode MOS transistor

PHP206

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-state resistance.

APPLICATIONS

- Motor driver
- Power management
- DC-DC converters
- General purpose switching.

DESCRIPTION

Two P-channel enhancement mode MOS transistors in an 8-pin plastic SOT96-1 (SO8) package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s_1	source 1
2	g_1	gate 1
3	s_2	source 2
4	g_2	gate 2
5	d_2	drain 2
6	d_2	drain 2
7	d_1	drain 1
8	d_1	drain 1

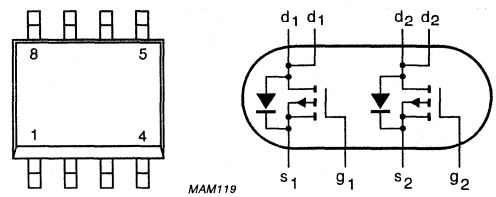


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per P-channel					
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = –1.25 A	–	–1.3	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = –1 mA	–1	–	V
I_D	drain current (DC)	T_s = 80 °C	–	–5.6	A
R_{DSon}	drain-source on-state resistance	V_{GS} = –10 V; I_D = –2.8 A	–	65	mΩ
P_{tot}	total power dissipation	T_s = 80 °C	–	3.5	W

OBJECTIVE
See Philips Semiconductors for Design-in information

Dual P-channel enhancement mode MOS transistor

PHP206

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per P-channel					
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	–5.6	A
I_{DM}	peak drain current	note 2	–	–22.5	A
P_{tot}	total power dissipation	T_s = 80 °C; note 3	–	3.5	W
		T_{amb} = 25 °C; note 4	–	2.63	W
		T_{amb} = 25 °C; note 5	–	1.14	W
		T_{amb} = 25 °C; note 6	–	1.56	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	–2.7	A
I_{SM}	peak pulsed source current	note 2	–	–10.8	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Maximum permissible dissipation per MOS transistor. Both devices may be loaded up to 3.5 Watt at the same time.
4. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
5. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.
6. Maximum permissible dissipation if only one MOS transistor dissipates. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	20	K/W

Dual P-channel enhancement mode MOS transistor

PHP206

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per P-channel						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−1	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −24 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = −4.5 V; I_D = −2.8 A	–	–	100	mΩ
		V_{GS} = −10 V; I_D = −5.6 A	–	–	65	mΩ
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	tbf	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	tbf	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	tbf	–	pF
Q_G	total gate charge	V_{GS} = −10 V; V_{DD} = −15 V; I_D = −1 A; T_{amb} = 25 °C	–	tbf	–	nC
Q_{GS}	gate-source charge	V_{DD} = −15 V; I_D = −1 A; T_{amb} = 25 °C	–	tbf	–	nC
Q_{GD}	gate-drain charge	V_{DD} = −15 V; I_D = −1 A; T_{amb} = 25 °C	–	tbf	–	nC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to −10 V; V_{DD} = −20 V; I_D = −1 A; R_{gen} = 6 Ω	–	tbf	–	ns
t_f	fall time	V_{GS} = 0 to −10 V; V_{DD} = −20 V; I_D = −1 A; R_{gen} = 6 Ω	–	tbf	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to −10 V; V_{DD} = −20 V; I_D = −1 A; R_{gen} = 6 Ω	–	tbf	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = −10 to 0 V; V_{DD} = −20 V; I_D = −1 A; R_{gen} = 6 Ω	–	tbf	–	ns
t_r	rise time	V_{GS} = −10 to 0 V; V_{DD} = −20 V; I_D = −1 A; R_{gen} = 6 Ω	–	tbf	–	ns
t_{off}	turn-off switching time	V_{GS} = −10 to 0 V; V_{DD} = −20 V; I_D = −1 A; R_{gen} = 6 Ω	–	tbf	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = −1.25 A	–	–	−1.3	V
t_{rr}	reverse recovery time	I_S = −1.25 A; di/dt = 100 A/μs	–	tbf	–	ns

Dual P-channel enhancement mode MOS transistor

PHP212

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-state resistance.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

DESCRIPTION

Two P-channel enhancement mode MOS transistors in an 8-pin plastic SOT96-1 (SO8) package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s_1	source 1
2	g_1	gate 1
3	s_2	source 2
4	g_2	gate 2
5	d_2	drain 2
6	d_2	drain 2
7	d_1	drain 1
8	d_1	drain 1

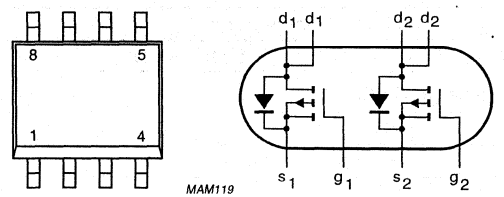


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{SD}	source-drain diode forward voltage	I_S = –1.25 A	–	–1.3	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = –1 mA; V_{DS} = V_{GS}	–1	–2.8	V
I_D	drain current (DC)	T_s = 80 °C	–	–4	A
R_{DSon}	drain-source on-state resistance	I_D = –2 A; V_{GS} = –10 V	–	0.12	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	3.5	W

Dual P-channel enhancement mode MOS transistor

PHP212

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per P-channel					
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	–4	A
I_{DM}	peak drain current	note 2	–	–16	A
P_{tot}	total power dissipation	T_s = 80 °C; note 3	–	3.5	W
		T_{amb} = 25 °C; note 4	–	2.6	W
		T_{amb} = 25 °C; note 5	–	1.1	W
		T_{amb} = 25 °C; note 6	–	1.5	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	–2.6	A
I_{SM}	peak pulsed source current	note 2	–	–10	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Maximum permissible dissipation per MOS transistor. Both devices may be loaded up to 3.5 W at the same time.
4. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
5. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.
6. Maximum permissible dissipation if only one MOS transistor dissipates. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	20	K/W

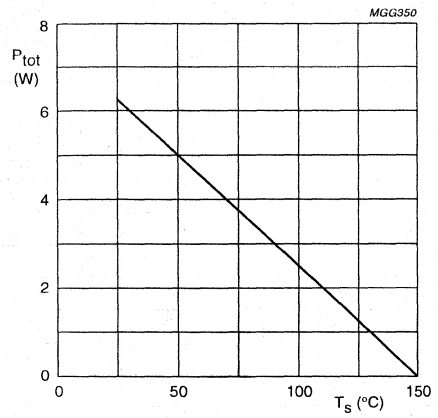
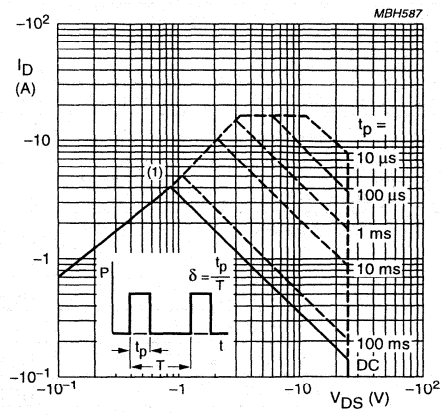


Fig.2 Power derating curve.



$\delta = 0.01$; $T_s = 80$ °C.
(1) R_{DSon} limitation.

Fig.3 SOAR.

Dual P-channel enhancement mode MOS transistor

PHP212

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per P-channel						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−1	–	−2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −24 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = −4.5 V; I_D = −1 A	–	–	0.25	Ω
		V_{GS} = −10 V; I_D = −2 A	–	–	0.12	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	450	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	200	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	100	–	pF
Q_G	total gate charge	V_{GS} = −10 V; V_{DD} = −15 V; I_D = −2 A	–	13	–	nC
Q_{GS}	gate-source charge	V_{GS} = −10 V; V_{DD} = −15 V; I_D = −2 A	–	1	–	nC
Q_{GD}	gate-drain charge	V_{GS} = −10 V; V_{DD} = −15 V; I_D = −2 A	–	4	–	nC
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to −10 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω; see Fig.4	–	6	–	ns
t_r	rise time	V_{GS} = 0 to −10 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω; see Fig.4	–	4	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to −10 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω; see Fig.4	–	10	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = −10 to 0 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω; see Fig.4	–	29	–	ns
t_f	fall time	V_{GS} = −10 to 0 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω; see Fig.4	–	16	–	ns
t_{off}	turn-off switching time	V_{GS} = −10 to 0 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω; see Fig.4	–	45	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = −1.25 A	–	–	−1.3	V
t_{rr}	reverse recovery time	I_S = −1.25 A; di/dt = 100 A/μs	–	75	–	ns

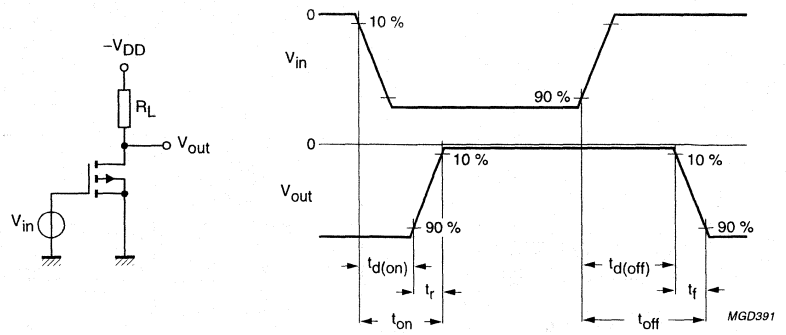
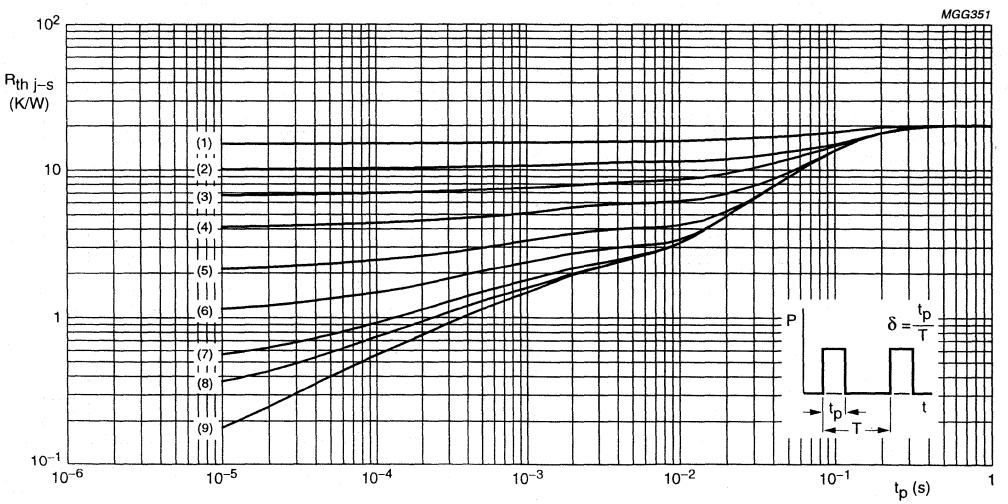
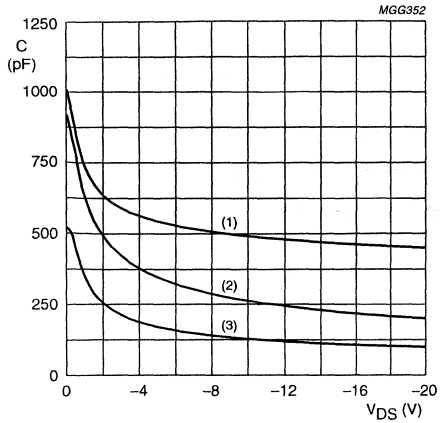


Fig.4 Switching times test circuit; input and output waveforms.



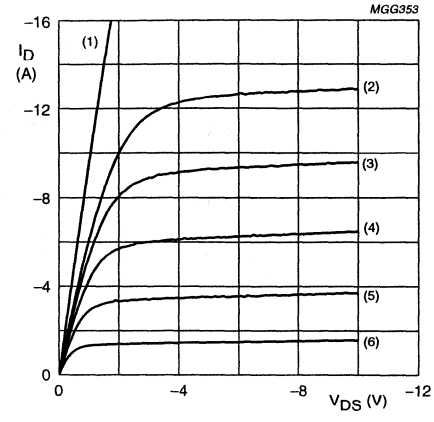
(1) δ = 0.75. (2) δ = 0.5. (3) δ = 0.33. (4) δ = 0.2.
(5) δ = 0.1. (6) δ = 0.05. (7) δ = 0.02. (8) δ = 0.01. (9) δ = 0.

Fig.5 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.



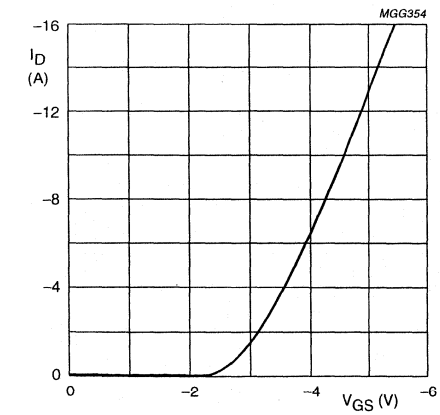
V_{GS} = 0; f = 1 MHz; T_j = 25 °C.
(1) C_{iss}.
(2) C_{oss}.
(3) C_{rss}.

Fig.6 Capacitance as a function of drain-source voltage; typical values.



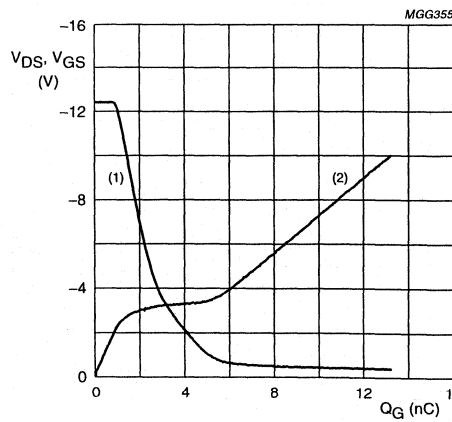
T_{amb} = 25 °C; t_p = 80 µs; δ = 0.
(1) V_{GS} = −10 V.
(2) V_{GS} = −5 V.
(3) V_{GS} = −4.5 V.
(4) V_{GS} = −4 V.
(5) V_{GS} = −3.5 V.
(6) V_{GS} = −3 V.

Fig.7 Output characteristics; typical values.



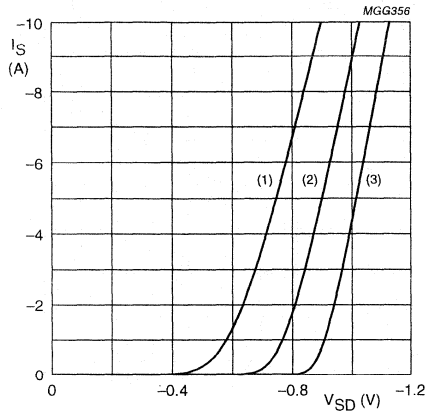
V_{DS} = −10 V; T_{amb} = 25 °C; t_p = 80 µs; δ = 0.

Fig.8 Transfer characteristic; typical value.



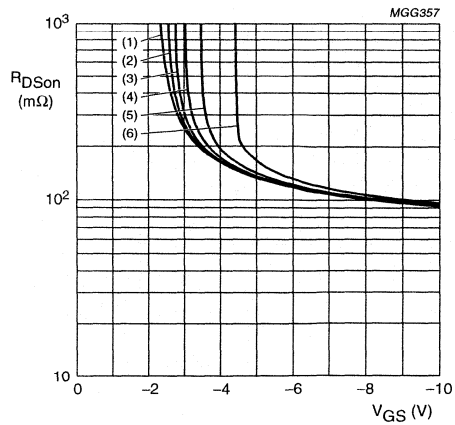
V_{DD} = −12.5 V; I_D = −2 A; T_{amb} = 25 °C.
(1) V_{DS}.
(2) V_{GS}.

Fig.9 Gate-source voltage and drain-source voltage as functions of total gate charge; typical values.



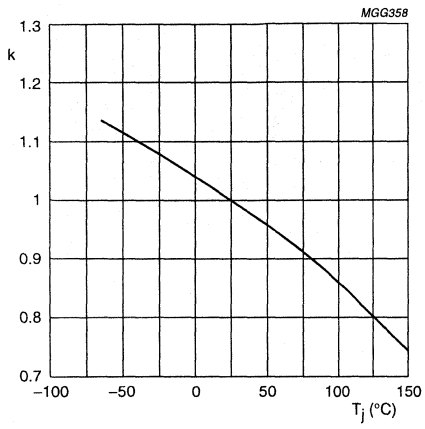
V_{GD} = 0.
(1) T_{amb} = 150 °C; t_p = 300 µs; δ = 0.
(2) T_{amb} = 25 °C; t_p = 300 µs; δ = 0.
(3) T_{amb} = −65 °C; t_p = 300 µs; δ = 0.

Fig.10 Source current as a function of source-drain diode forward voltage; typical values.



T_{amb} = 25 °C; t_p = 300 µs; δ = 0.
$V_{DS} \geq I_D \times R_{DSon}$.
(1) I_D = 0.1 A.
(2) I_D = 0.5 A.
(3) I_D = 1 A.
(4) I_D = 2 A.
(5) I_D = 4 A.
(6) I_D = 8 A.

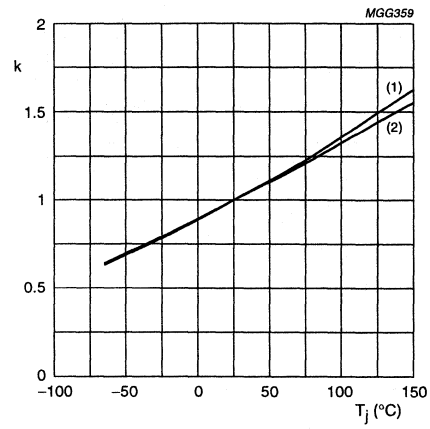
Fig.11 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

V_{GSth} at $V_{DS} = V_{GS}$; $I_D = -1$ mA.

Fig.12 Temperature coefficient of gate-source threshold voltage; typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

(1) R_{DSon} at $V_{GS} = -10$ V; $I_D = -2$ A.

(2) R_{DSon} at $V_{GS} = -4.5$ V; $I_D = -1$ A.

Fig.13 Temperature coefficient of drain-source on-state resistance; typical values.

Dual P-channel enhancement mode MOS transistor

PHP222

FEATURES

- Very low on-state resistance
- High-speed switching
- No secondary breakdown
- Low threshold.

APPLICATIONS

- Power management
- DC-DC converters
- General purpose switch.

DESCRIPTION

Two P-channel enhancement mode MOS transistors in an 8-pin SOT96-1 (SO8) SMD plastic package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s_1	source 1
2	g_1	gate 1
3	s_2	source 2
4	g_2	gate 2
5	d_2	drain 2
6	d_2	drain 2
7	d_1	drain 1
8	d_1	drain 1

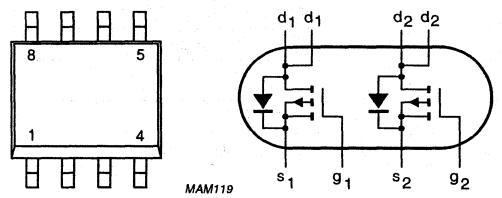


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{SD}	source-drain diode forward voltage	$I_S = -1.25$ A; $V_{GD} = 0$	–	–1.3	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±8	V
V_{GSth}	gate-source threshold voltage	$I_D = -1$ mA; $V_{DS} = V_{GS}$	–0.4	–	V
I_D	drain current (DC)	$T_s = 80$ °C	–	–3.2	A
R_{DSon}	drain-source on-state resistance	$I_D = -1.6$ A; $V_{GS} = -2.5$ V	–	220	mΩ
P_{tot}	total power dissipation	$T_s = 80$ °C	–	3.5	W

PRELIMINARY
See Philips Semiconductors for Design-in information

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per P-channel					
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±8	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	–3.2	A
I_{DM}	peak drain current	note 2	–	–12.8	A
P_{tot}	total power dissipation	T_s = 80 °C; note 3	–	3.5	W
		T_{amb} = 25 °C; note 4	–	2.63	W
		T_{amb} = 25 °C; note 5	–	1.14	W
		T_{amb} = 25 °C; note 6	–	1.56	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	–2.7	A
I_{SM}	peak pulsed source current	note 2	–	–10.8	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Maximum permissible dissipation per MOS transistor. Both devices may be loaded up to 3.5 W at the same time.
4. Maximum permissible dissipation per MOS transistor. Device mounted on a printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
5. Maximum permissible dissipation per MOS transistor. Device mounted on a printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.
6. Maximum permissible dissipation if only one MOS transistor dissipates. Device mounted on a printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	20	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per P-channel						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−0.4	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −24 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±8 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = −4.5 V; I_D = −1.6 A	–	–	200	mΩ
		V_{GS} = −2.5 V; I_D = −1.6 A	–	–	220	mΩ
		V_{GS} = −1.8 V; I_D = −0.8 A	–	–	250	mΩ
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	696	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	163	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	73	–	pF
Q_G	total gate charge	V_{GS} = −4.5 V; V_{DD} = −15 V; I_D = −1 A; T_{amb} = 25 °C	–	16	–	nC
Q_{GS}	gate-source charge	V_{DD} = −15 V; I_D = −1 A; T_{amb} = 25 °C	–	0.7	–	nC
Q_{GD}	gate-drain charge	V_{DD} = −15 V; I_D = −1 A; T_{amb} = 25 °C	–	4.1	–	nC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to −8 V; V_{DD} = −20 V; I_D = −1 A; R_{gen} = 6 Ω	–	3.5	–	ns
t_r	rise time		–	4	–	ns
t_{on}	turn-on switching time		–	7.5	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = −8 to 0 V; V_{DD} = −20 V; I_D = −1 A; R_{gen} = 6 Ω	–	90	–	ns
t_f	fall time		–	35	–	ns
t_{off}	turn-off switching time		–	125	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = −1.25 A	–	–	−1.3	V
t_{rr}	reverse recovery time	I_S = −1.25 A; di/dt = 100 A/μs	–	65	–	ns

Dual P-channel enhancement mode MOS transistor

PHP225

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

DESCRIPTION

Two P-channel enhancement mode MOS transistors in an 8-pin plastic SOT96-1 (SO8) package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s_1	source 1
2	g_1	gate 1
3	s_2	source 2
4	g_2	gate 2
5	d_2	drain 2
6	d_2	drain 2
7	d_1	drain 1
8	d_1	drain 1

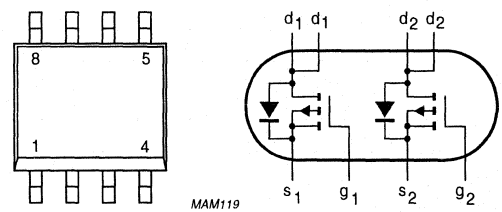


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per P-channel					
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{SD}	source-drain diode forward voltage	I_S = –1.25 A	–	–1.6	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = –1 mA; V_{DS} = V_{GS}	–1	–2.8	V
I_D	drain current (DC)		–	–2.3	A
R_{DSon}	drain-source on-state resistance	I_D = –1 A; V_{GS} = –10 V	–	0.25	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	2	W

Dual P-channel enhancement mode MOS transistor

PHP225

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per P-channel					
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)	$T_s \leq 80$ °C	–	–2.3	A
I_{DM}	peak drain current	note 1	–	–10	A
P_{tot}	total power dissipation	$T_s = 80$ °C; note 2	–	2	W
		$T_{amb} = 25$ °C; note 3	–	2	W
		$T_{amb} = 25$ °C; note 4	–	1	W
		$T_{amb} = 25$ °C; note 5	–	1.3	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C
Source-drain diode					
I_S	source current (DC)	$T_s \leq 80$ °C	–	–1.25	A
I_{SM}	peak pulsed source current	note 1	–	–5	A

Notes

1. Pulse width and duty cycle limited by maximum junction temperature.
2. Maximum permissible dissipation per MOS transistor. Both devices may be loaded up to 2 W at the same time.
3. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.
5. Maximum permissible dissipation if only one MOS transistor dissipates. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

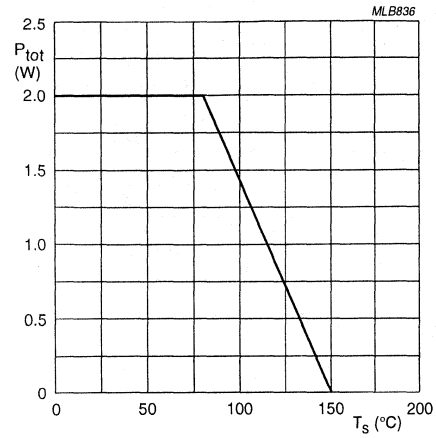
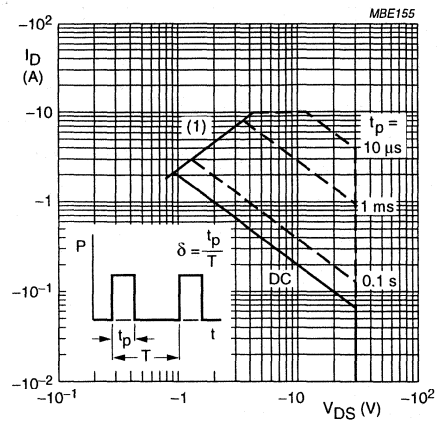


Fig.2 Power derating curve.



$\delta = 0.01$.
$T_s = 80$ °C.
(1) R_{DSon} limitation.

Fig.3 SOAR.

Dual P-channel enhancement mode MOS transistor

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	35	K/W

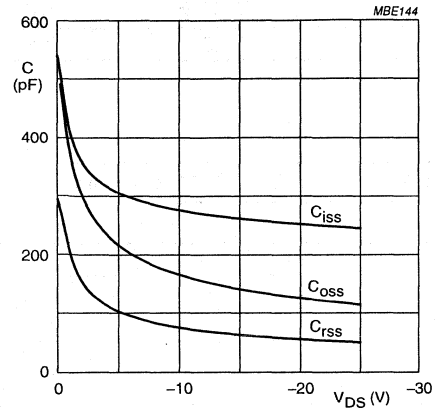
CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per P-channel						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−1	–	−2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −24 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
I_{Don}	on-state drain current	V_{GS} = −10 V; V_{DS} = −1 V	−2.3	–	–	A
		V_{GS} = −4.5 V; V_{DS} = −5 V	−1	–	–	A
R_{DSon}	drain-source on-state resistance	V_{GS} = −4.5 V; I_D = −0.5 A	–	0.33	0.4	Ω
		V_{GS} = −10 V; I_D = −1 A	–	0.22	0.25	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = −20 V; I_D = −1 A	1	2	–	S
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −20 V; f = 1 MHz	–	250	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −20 V; f = 1 MHz	–	140	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −20 V; f = 1 MHz	–	50	–	pF
Q_G	total gate charge	V_{GS} = −10 V; V_{DS} = −15 V; I_D = −2.3 A	–	10	25	nC
Q_{GS}	gate-source charge	V_{GS} = −10 V; V_{DS} = −15 V; I_D = −2.3 A	–	1	–	nC
Q_{GD}	gate-drain charge	V_{GS} = −10 V; V_{DS} = −15 V; I_D = −2.3 A	–	3	–	nC
Switching times						
t_{on}	turn-on time	V_{GD} = 0 to −10 V; V_{DD} = −20 V; I_D = −1 A; R_L = 20 Ω	–	20	80	ns
t_{off}	turn-off time	V_{GS} = −10 to 0 V; V_{DD} = −20 V; I_D = −1 A; R_L = 20 Ω	–	50	140	ns
Source-drain diode						
V_{DS}	source drain diode forward voltage	V_{GD} = 0; I_S = −1.25 A	–	–	−1.6	V
t_{rr}	reverse recovery time	I_S = −1.25 A; di/dt = 100 A/μs	–	150	200	ns

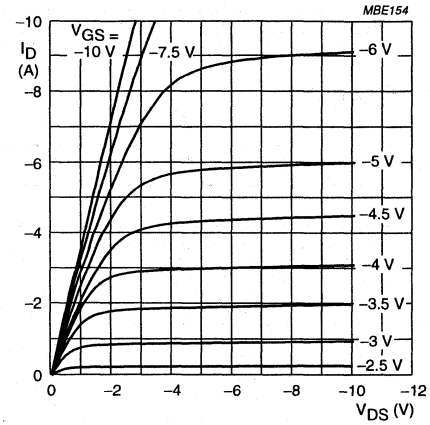
Dual P-channel enhancement mode MOS transistor

PHP225



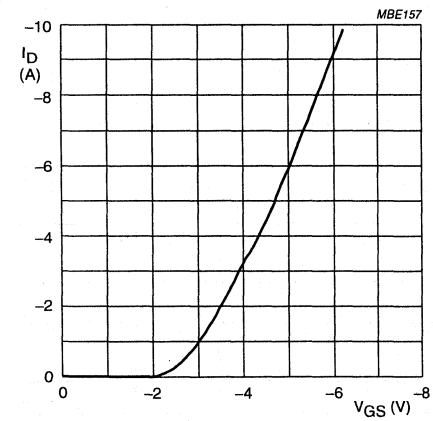
V_{GS} = 0.
T_j = 25 °C.

Fig.4 Capacitance as a function of drain-source voltage; typical values.



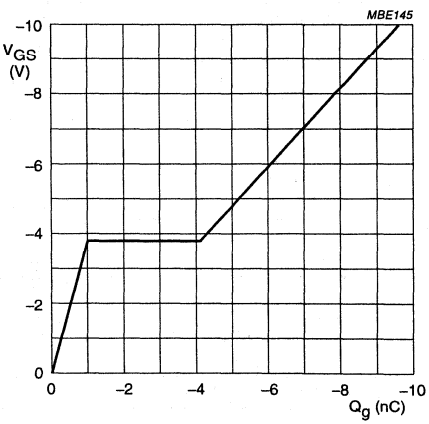
T_j = 25 °C.

Fig.5 Output characteristics; typical values.



V_{DS} = −10 V.
T_j = 25 °C.

Fig.6 Transfer characteristic; typical values.



V_{DD} = −15 V.
I_D = −2.3 A.

Fig.7 Gate-source voltage as a function of total gate charge.

Dual P-channel enhancement mode MOS transistor

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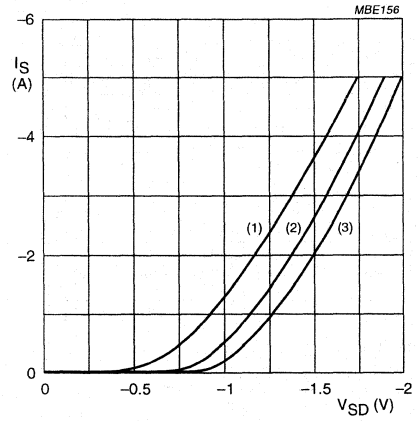
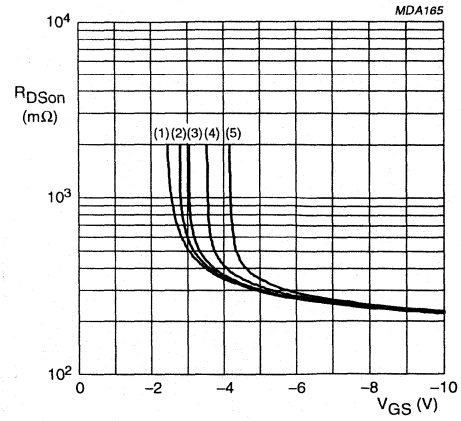


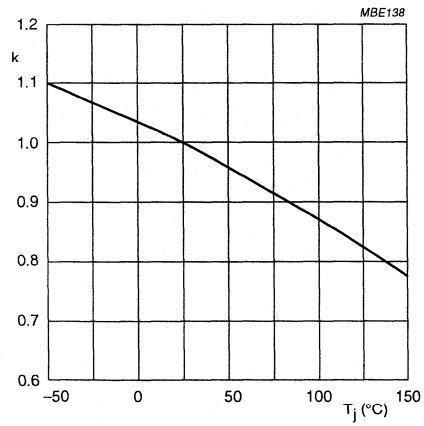
V_{GD} = 0.
(1) T_j = 150 °C.
(2) T_j = 25 °C.
(3) T_j = −55 °C.

Fig.8 Source current as a function of source-drain diode forward voltage.



$-V_{DS} \geq -I_D \times R_{DSon}$; T_j = 25 °C.
(1) I_D = −0.1 A.
(2) I_D = −0.5 A.
(3) I_D = −1 A.
(4) I_D = −2.3 A.
(5) I_D = −4.5 A.

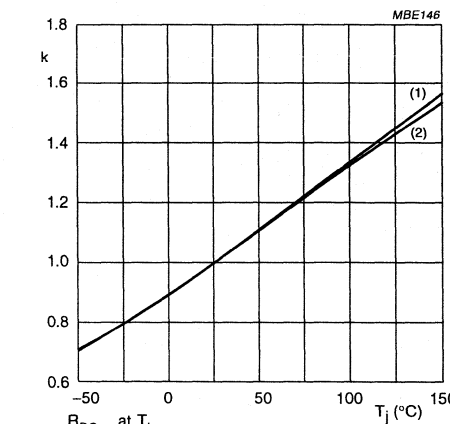
Fig.9 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

Typical V_{GSth} at I_D = 1 mA; V_{DS} = V_{GS} = V_{GSth}.

Fig.10 Temperature coefficient of gate-source threshold voltage.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

Typical R_{DSon} at:
(1) I_D = −1 A; V_{GS} = −10 V.
(2) I_D = −0.5 A; V_{GS} = −4.5 V.

Fig.11 Temperature coefficient of drain-source on-resistance.

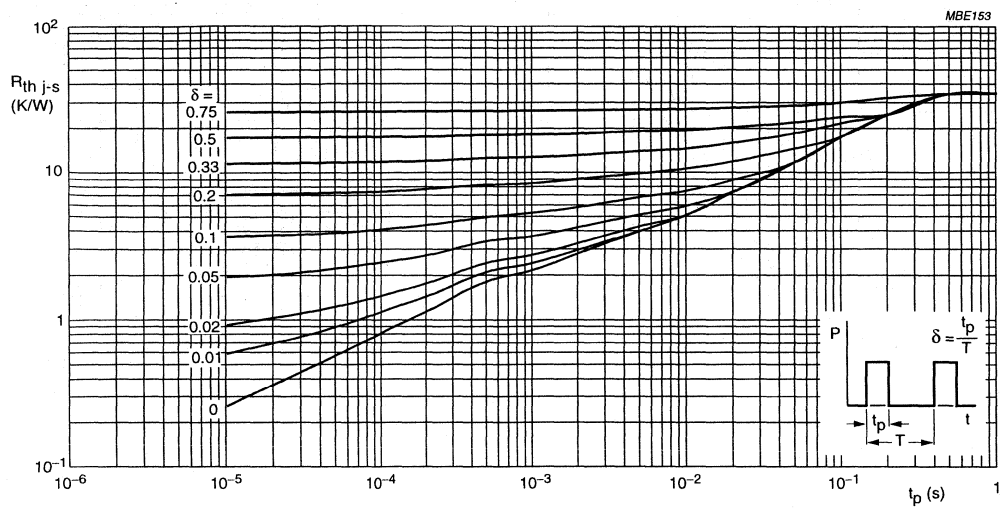


Fig.12 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

P-channel enhancement mode MOS transistor

PHP1025

FEATURES

- Very low R_{DSon} at low threshold
- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL, etc.

APPLICATIONS

- Power management
- DC-DC converters
- General purpose switch.

DESCRIPTION

P-channel enhancement mode MOS transistor in an 8-pin SOT96-1 (SO8) SMD plastic package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s	source
2	s	source
3	s	source
4	g	gate
5	d	drain
6	d	drain
7	d	drain
8	d	drain

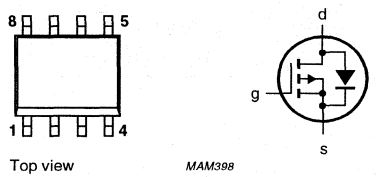


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–12	V
V_{SD}	source-drain diode forward voltage	I_S = –1.25 A; V_{GD} = 0	–	–1.3	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±8	V
V_{GSth}	gate-source threshold voltage	I_D = –1 mA; V_{DS} = V_{GS}	–0.4	–	V
I_D	drain current (DC)	T_s = 80 °C	–	–10	A
R_{DSon}	drain-source on-state resistance	I_D = –5 A; V_{GS} = –2.5 V	–	25	mΩ
P_{tot}	total power dissipation	T_s = 80 °C	–	4	W

P-channel enhancement mode MOS transistor

PHP1025

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–12	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±8	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	–10	A
I_{DM}	peak drain current	note 2	–	–40	A
P_{tot}	total power dissipation	T_s = 80 °C	–	4	W
		T_{amb} = 25 °C; note 3	–	2.78	W
		T_{amb} = 25 °C; note 4	–	1.16	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	–3	A
I_{SM}	peak pulsed source current	note 2	–	–12	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	17.5	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−12	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−0.4	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −9.6 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±8 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = −4.5 V; I_D = −5 A	–	–	23	mΩ
		V_{GS} = −2.5 V; I_D = −5 A	–	–	25	mΩ
		V_{GS} = −1.8 V; I_D = −2.5 A	–	–	29	mΩ
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −9.6 V; f = 1 MHz	–	tbf	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −9.6 V; f = 1 MHz	–	tbf	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −9.6 V; f = 1 MHz	–	tbf	–	pF
Q_G	total gate charge	V_{GS} = −6 V; V_{DD} = −6 V; I_D = −5 A; T_{amb} = 25 °C	–	tbf	–	pC
Q_{GS}	gate-source charge	V_{DD} = −6 V; I_D = −5 A T_{amb} = 25 °C	–	tbf	–	pC
Q_{GD}	gate-drain charge	V_{DD} = −6 V; I_D = −5 A T_{amb} = 25 °C	–	tbf	–	pC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to −6 V; V_{DD} = −6 V; I_D = −1 A; R_{gen} = 6 Ω	–	tbf	–	ns
t_f	fall time		–	tbf	–	ns
t_{on}	turn-on switching time		–	tbf	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = −6 to 0 V; V_{DD} = −6 V; I_D = −1 A; R_{gen} = 6 Ω	–	tbf	–	ns
t_r	rise time		–	tbf	–	ns
t_{off}	turn-off switching time		–	tbf	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = −1.25 A	–	–	−1.3	V
t_{rr}	reverse recovery time	I_S = −1.25 A; di/dt = 100 A/μs	–	tbf	–	ns

P-channel enhancement mode MOS transistor

PHP1035

FEATURES

- Very low R_{DSon}
- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL, etc.

APPLICATIONS

- Power management
- DC-DC converters
- General purpose switch.

DESCRIPTION

P-channel enhancement mode MOS transistor in an 8-pin SOT96-1 (SO8) SMD plastic package.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s	source
2	s	source
3	s	source
4	g	gate
5	d	drain
6	d	drain
7	d	drain
8	d	drain

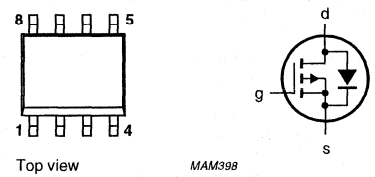


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{SD}	source-drain diode forward voltage	$I_S = -1.25$ A; $V_{GD} = 0$	–	–1.3	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	$I_D = -1$ mA; $V_{DS} = V_{GS}$	–1	–	V
I_D	drain current (DC)	$T_s = 80$ °C	–	–8	A
R_{DSon}	drain-source on-state resistance	$I_D = -4$ A; $V_{GS} = -10$ V	–	35	mΩ
P_{tot}	total power dissipation	$T_s = 80$ °C	–	4	W

P-channel enhancement mode MOS transistor

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	–8	A
I_{DM}	peak drain current	note 2	–	–32	A
P_{tot}	total power dissipation	T_s = 80 °C	–	4	W
		T_{amb} = 25 °C; note 3	–	2.78	W
		T_{amb} = 25 °C; note 4	–	1.16	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	–3	A
I_{SM}	peak pulsed source current	note 2	–	–12	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	17.5	K/W

P-channel enhancement mode MOS transistor

PHP1035

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−1	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −24 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = −4.5 V; I_D = 2 A	–	–	50	mΩ
		V_{GS} = −10 V; I_D = −4 A	–	–	35	mΩ
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −25 V; f = 1 MHz	–	tbf	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	tbf	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	tbf	–	pF
Q_G	total gate charge	V_{GS} = −10 V; V_{DD} = −15 V; I_D = −4 A; T_{amb} = 25 °C	–	tbf	–	pC
Q_{GS}	gate-source charge	V_{DD} = −15 V; I_D = −4 A; T_{amb} = 25 °C	–	tbf	–	pC
Q_{GD}	gate-drain charge	V_{DD} = −15 V; I_D = −4 A; T_{amb} = 25 °C	–	tbf	–	nC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to −10 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω	–	tbf	–	ns
t_f	fall time		–	tbf	–	ns
t_{on}	turn-on switching time		–	tbf	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = −10 to 0 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω	–	tbf	–	ns
t_r	rise time		–	tbf	–	ns
t_{off}	turn-off switching time		–	tbf	–	ns
Source-drain diode						
V_{SD}	source-drain forward voltage	V_{GD} = 0; I_S = −1.25 A	–	–	−1.3	V
t_{rr}	reverse recovery time	I_S = −1.25 A; di/dt = −100 A/μs	–	tbf	–	ns

PowerMOS transistor PHP3055E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

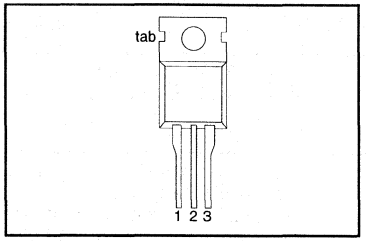
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	12	A
P_{tot}	Total power dissipation	50	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.15	Ω

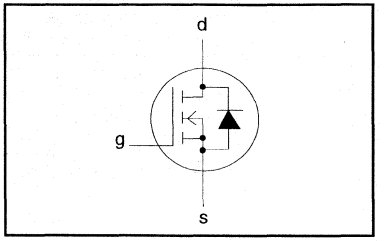
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	12	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	9	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	48	A
P_D	Total dissipation	T_{mb} = 25 °C	-	50	W
$\Delta P_D/\Delta T_{mb}$	Linear derating factor	T_{mb} > 25 °C	-	0.33	W/K
V_{GS}	Gate-source voltage		-	± 30	V
E_{AS}	Single pulse avalanche energy	$V_{DD} \leq 50$ V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	25	mJ
I_{AS}	Peak avalanche current	$V_{DD} \leq 50$ V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	6	A
T_j, T_{stg}	Operating junction and storage temperature range		- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	3	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.08	-	V/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 6 A	-	0.1	0.15	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 50 V; I_D = 6 A	2.4	4.0	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 60 V; V_{GS} = 0 V	-	0.1	25	µA
		V_{DS} = 48 V; V_{GS} = 0 V; T_j = 150 °C	-	1	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$Q_{g(tot)}$	Total gate charge	I_D = 10 A; V_{DD} = 48 V; V_{GS} = 10 V	-	10	12	nC
Q_{gs}	Gate-source charge		-	2	3	nC
Q_{gd}	Gate-drain (Miller) charge		-	5.6	7	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 30 V; I_D = 10 A;	-	8	-	ns
t_r	Turn-on rise time	R_G = 24 Ω; R_D = 2.7 Ω	-	55	-	ns
$t_{d(off)}$	Turn-off delay time		-	25	-	ns
t_f	Turn-off fall time		-	22	-	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	220	-	pF
C_{oss}	Output capacitance		-	108	-	pF
C_{rss}	Feedback capacitance		-	48	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	12	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	48	A
V_{SD}	Diode forward voltage	I_S = 10 A; V_{GS} = 0 V	-	-	1.5	V
t_{rr}	Reverse recovery time	I_S = 10 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	38	-	ns
Q_{rr}	Reverse recovery charge		-	0.1	-	µC

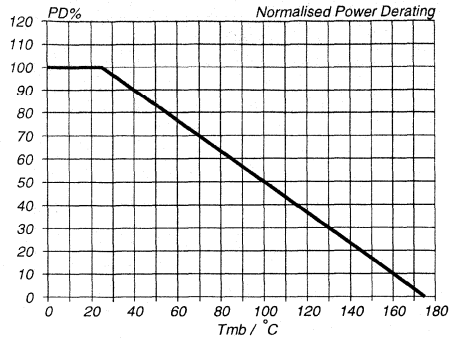


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

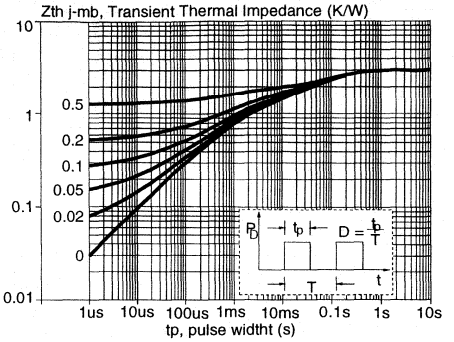


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

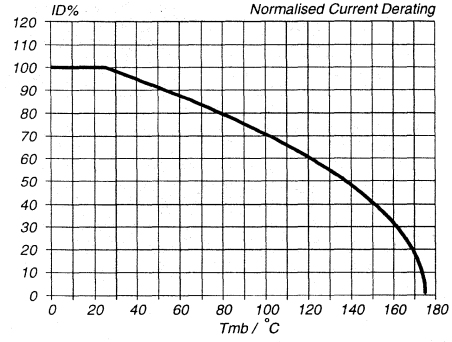


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

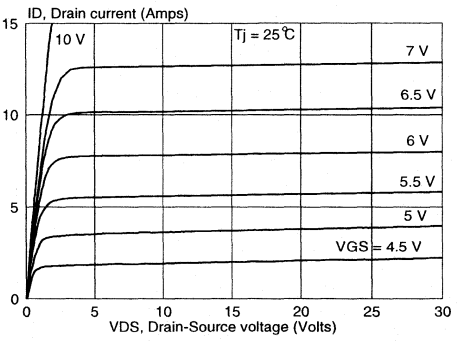


Fig.5. Typical output characteristics.
I_D = f(V_{DS}); parameter V_{GS}

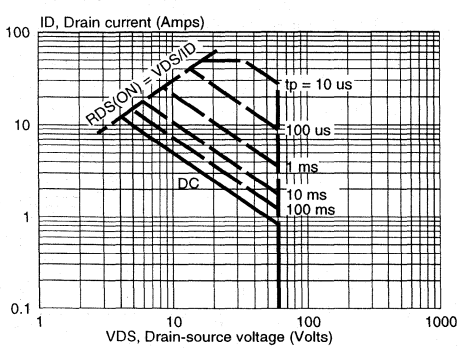


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

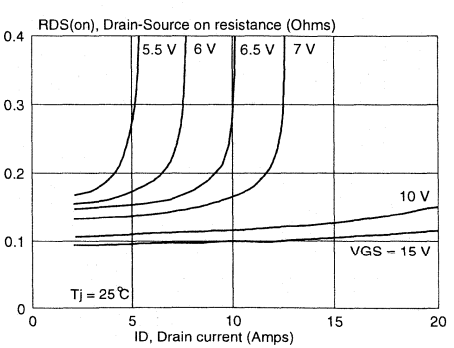


Fig.6. Typical on-state resistance.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

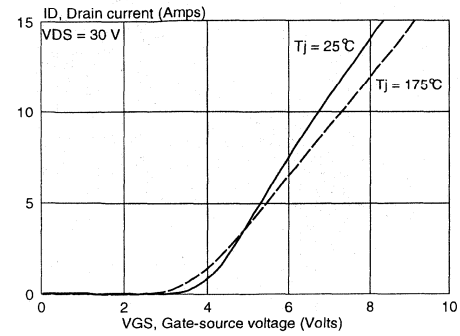


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; parameter T_j

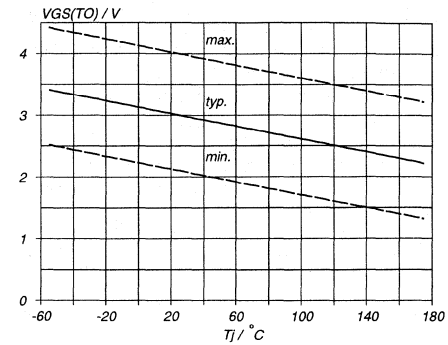


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

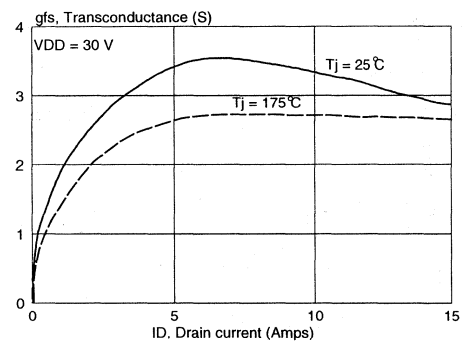


Fig.8. Typical transconductance. $g_{fs} = f(I_D)$; parameter T_j

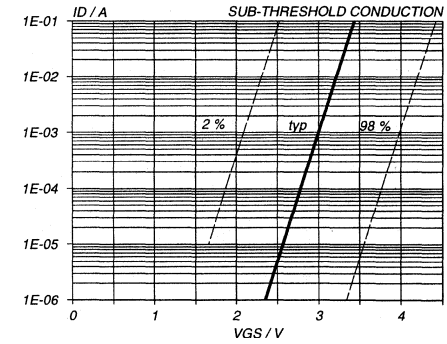


Fig.11. Sub-threshold drain current. $I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

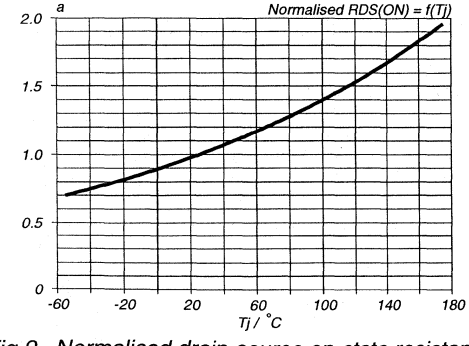


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,^{\circ}C} = f(T_j)$; I_D = 10 A; V_{GS} = 10 V

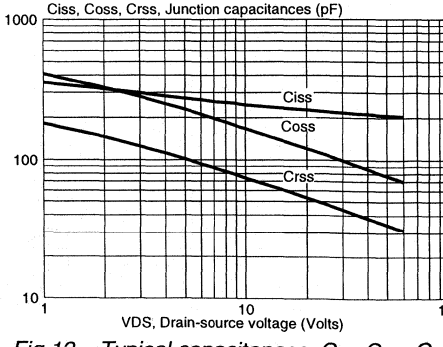


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

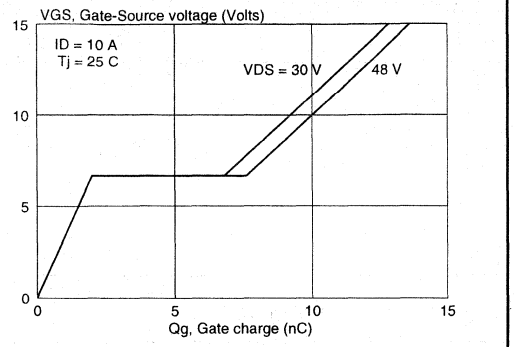


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; *parameter* V_{DS}

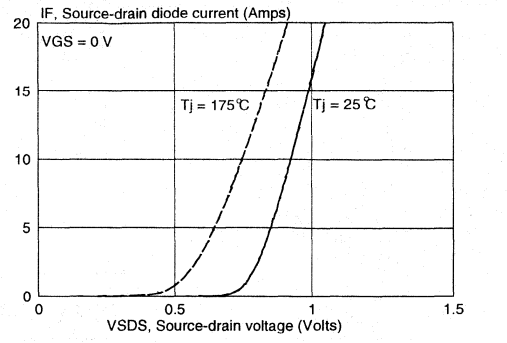


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; *parameter* T_j

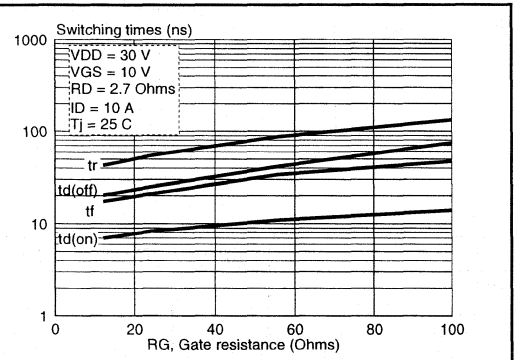


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

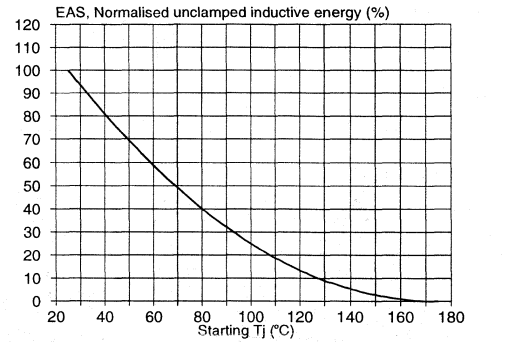


Fig.17. Normalised unclamped inductive energy.
$E_{AS}\% = f(T_j)$

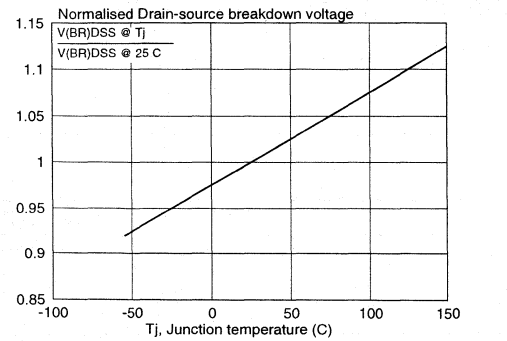


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ ^\circ C} = f(T_j)$

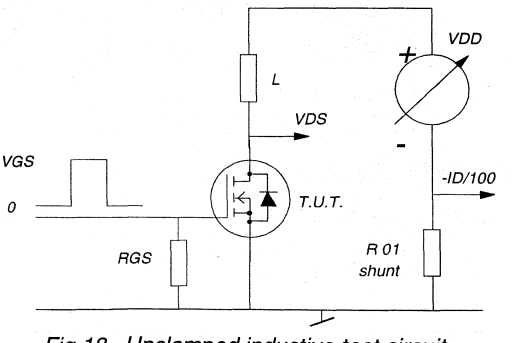


Fig.18. Unclamped inductive test circuit.
$E_{AS} = 0.5 \cdot LI_D^2 \cdot V_{(BR)DSS}/(V_{(BR)DSS} - V_{DD})$

PowerMOS transistor Logic level FET

PHP3055L

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

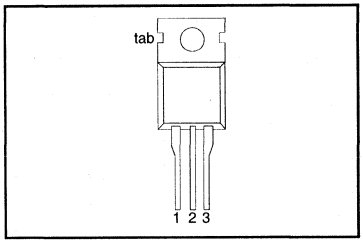
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	12	A
P_{tot}	Total power dissipation	50	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.18	Ω

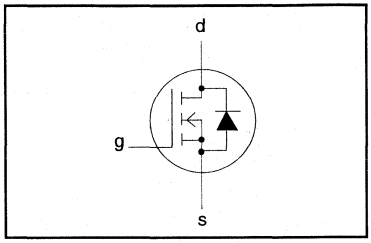
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	12	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	9	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	48	A
P_D	Total dissipation	T_{mb} = 25 °C	-	50	W
$\Delta P_D/\Delta T_{mb}$	Linear derating factor	T_{mb} > 25 °C	-	0.33	W/K
V_{GS}	Gate-source voltage		-	± 15	V
V_{GSM}	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	± 20	V
E_{AS}	Single pulse avalanche energy	$V_{DD} \leq 50$ V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 5 V	-	25	mJ
I_{AS}	Peak avalanche current	$V_{DD} \leq 50$ V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 5 V	-	6	A
T_j, T_{stg}	Operating junction and storage temperature range		- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	3	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.08	-	V/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 5 V; I_D = 6 A	-	0.13	0.18	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	1.0	1.5	2.0	V
g_{fs}	Forward transconductance	V_{DS} = 50 V; I_D = 6 A	3.5	5.5	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 60 V; V_{GS} = 0 V	-	0.1	25	µA
		V_{DS} = 48 V; V_{GS} = 0 V; T_j = 150 °C	-	1	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$Q_{g(tot)}$	Total gate charge	I_D = 10 A; V_{DD} = 48 V; V_{GS} = 5 V	-	7.5	10	nC
Q_{gs}	Gate-source charge		-	1.9	3	nC
Q_{gd}	Gate-drain (Miller) charge		-	5.5	7	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 30 V; I_D = 10 A;	-	12	-	ns
t_r	Turn-on rise time	R_G = 24 Ω; R_D = 2.7 Ω	-	105	-	ns
$t_{d(off)}$	Turn-off delay time		-	26	-	ns
t_f	Turn-off fall time		-	35	-	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	290	-	pF
C_{oss}	Output capacitance		-	103	-	pF
C_{rss}	Feedback capacitance		-	40	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	12	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	48	A
V_{SD}	Diode forward voltage	I_S = 10 A; V_{GS} = 0 V	-	-	1.5	V
t_{rr}	Reverse recovery time	I_S = 10 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	40	-	ns
Q_{rr}	Reverse recovery charge		-	0.1	-	µC

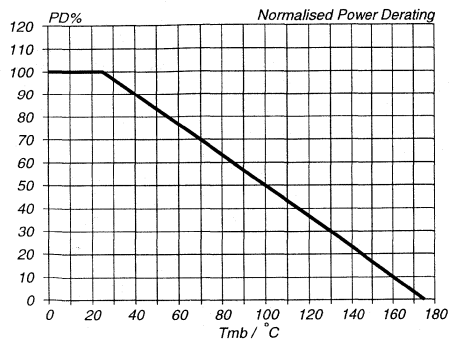


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

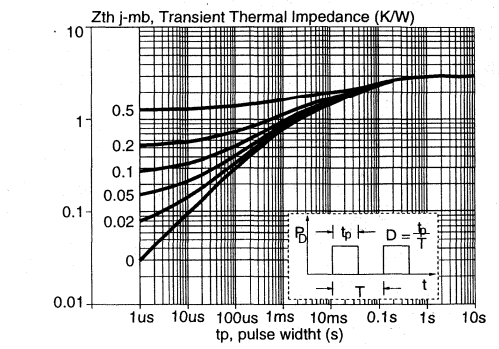


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

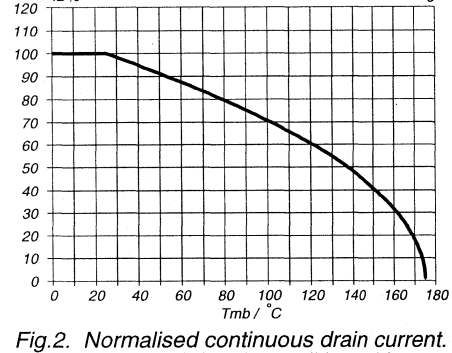


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

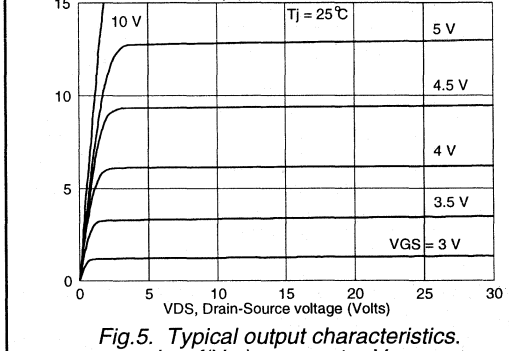


Fig.5. Typical output characteristics.
I_D = f(V_{DS}); parameter V_{GS}

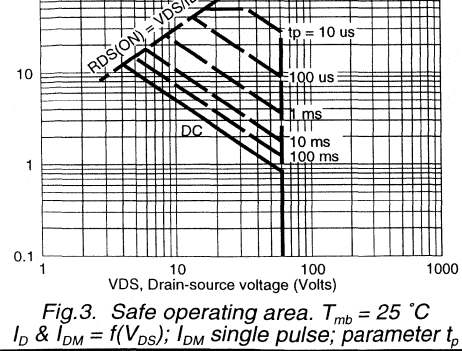


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

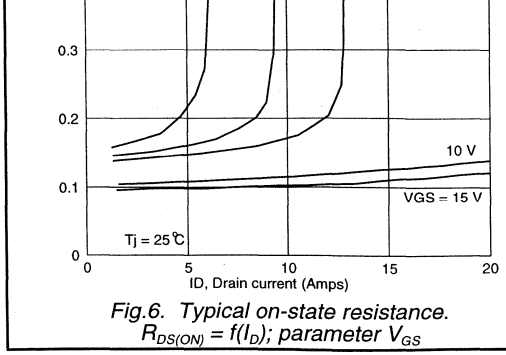


Fig.6. Typical on-state resistance.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

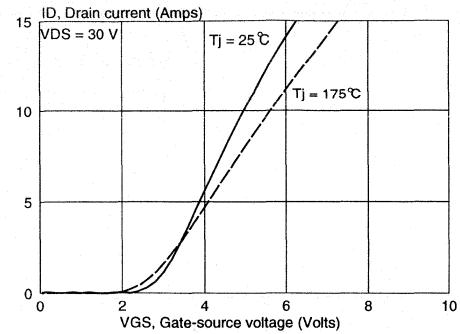


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; parameter T_j

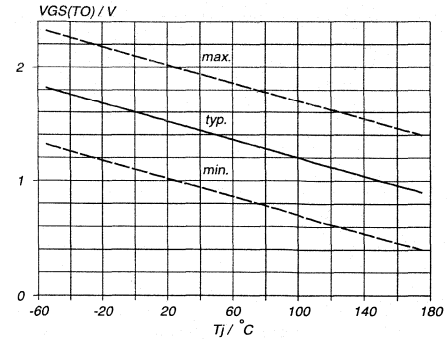


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

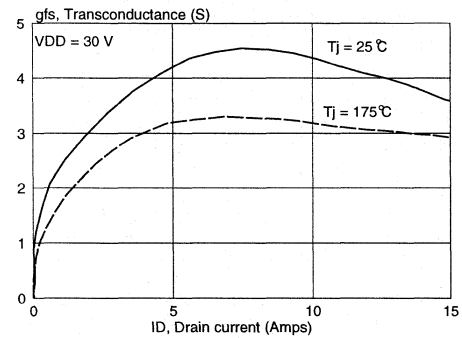


Fig.8. Typical transconductance. $g_{fs} = f(I_D)$; parameter T_j

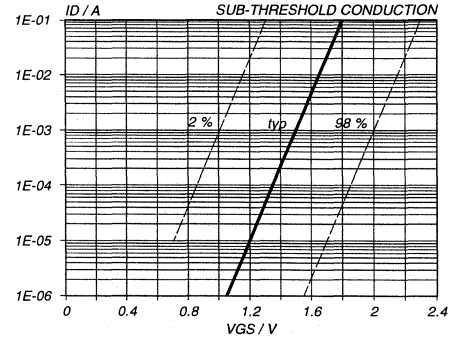


Fig.11. Sub-threshold drain current. $I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

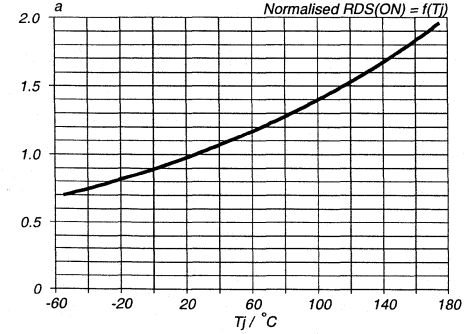


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\ ^\circ C} = f(T_j)$; I_D = 10 A; V_{GS} = 10 V

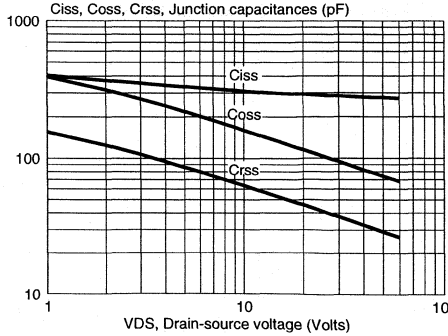


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

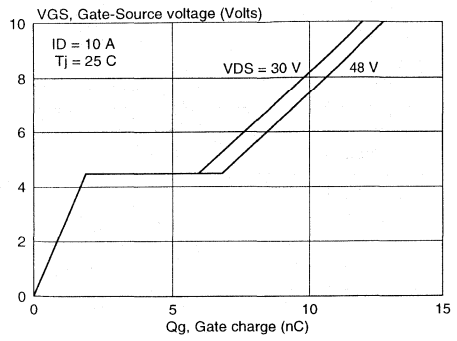


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; *parameter* V_{DS}

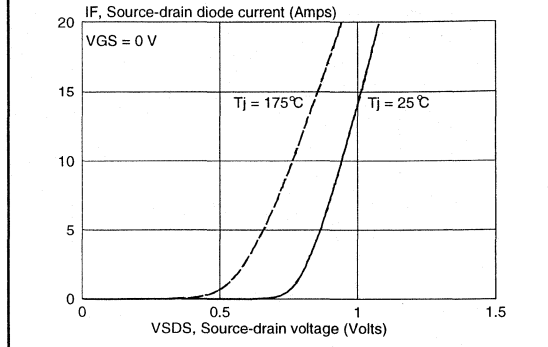


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; *parameter* T_j

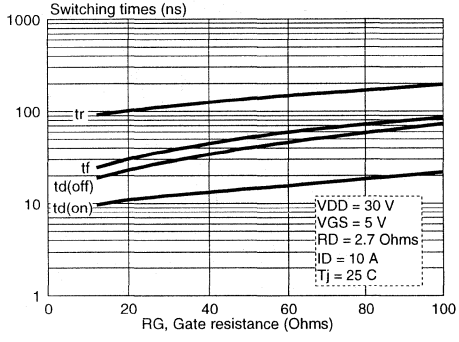


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

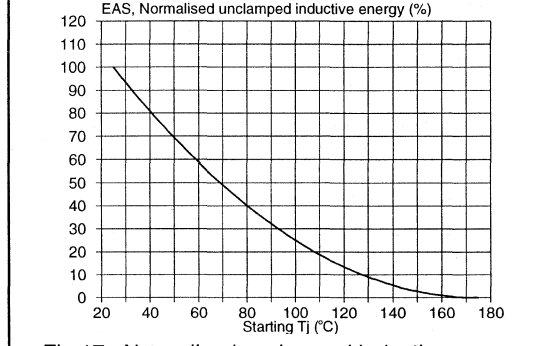


Fig.17. Normalised unclamped inductive energy.
$E_{AS}\% = f(T_j)$

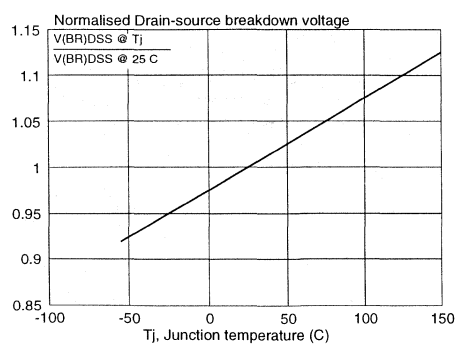


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ ^\circ C} = f(T_j)$

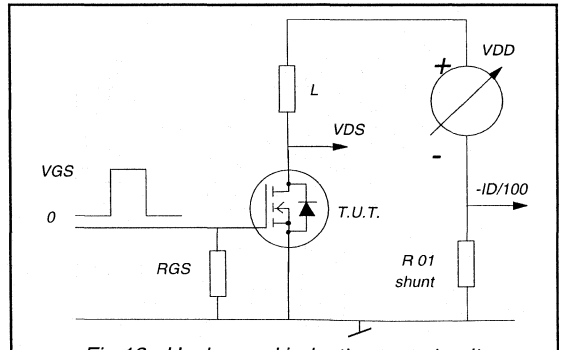


Fig.18. Unclamped inductive test circuit.
$E_{AS} = 0.5 \cdot LI_D^2 \cdot V_{(BR)DSS}/(V_{(BR)DSS} - V_{DD})$

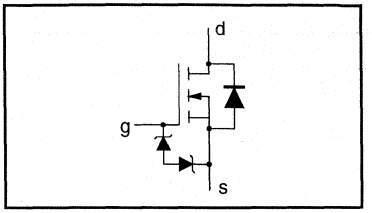
TrenchMOS™ transistor Logic level FET

PHT6N03LT

FEATURES

- **'Trench'** technology
- Very low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Surface mounting package

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 30 V

I_D = 5.9 A

$R_{DS(ON)} \leq 30\ m\Omega$ (V_{GS} = 5 V)

$R_{DS(ON)} \leq 28\ m\Omega$ (V_{GS} = 10 V)

GENERAL DESCRIPTION

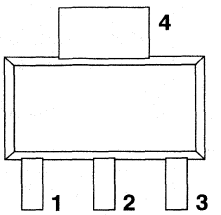
N-channel enhancement mode logic level field-effect power transistor using **'trench'** technology. The device has very low on-state resistance. It is intended for use in dc to dc converters and general purpose switching applications.

The PHT6N03LT is supplied in the SOT223 surface mounting package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

SOT223



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	30	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	30	V
V_{GS}	Gate-source voltage		-	± 13	V
I_D	Continuous drain current	T_{amb} = 25 °C; V_{GS} = 10 V	-	5.9	A
		T_{amb} = 100 °C; V_{GS} = 10 V	-	4.1	A
I_{DM}	Pulsed drain current		-	23.6	A
P_D	Total power dissipation	T_{amb} = 25 °C	-	1.8	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	150	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}sp}$	Thermal resistance junction to solder point	mounted on any pcb	-	-	15	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	mounted on test pcb of fig:17	-	70	-	K/W

ELECTRICAL CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	30	-	-	V
		T_j = -55˚C	27	-	-	V
$V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = 1 mA	10	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	1.5	2	V
		T_j = 150˚C	0.6	-	-	V
		T_j = -55˚C	-	-	2.3	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 3.2 A	-	24	30	mΩ
		V_{GS} = 10 V; I_D = 3.2 A	-	18	28	mΩ
		V_{GS} = 5 V; I_D = 3.2 A; T_j = 150˚C	-	-	51	mΩ
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5.9 A	8	14	-	S
I_{DSS}	Zero gate voltage drain current	V_{DS} = 30 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 150˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 150˚C	-	-	10	µA
$Q_{g(tot)}$	Total gate charge	I_D = 5.9 A; V_{DD} = 24 V; V_{GS} = 5 V	-	24	-	nC
Q_{gs}	Gate-source charge		-	3	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	11	-	nC
$t_{d\,on}$	Turn-on delay time	V_{DD} = 15 V; I_D = 5.9 A;	-	30	45	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 5 Ω	-	80	130	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	95	135	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die	-	3.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1050	-	pF
C_{oss}	Output capacitance		-	270	-	pF
C_{rss}	Feedback capacitance		-	140	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)		-	-	5.9	A
I_{SM}	Pulsed source current (body diode)		-	-	10	A
V_{SD}	Diode forward voltage	I_F = 5.9 A; V_{GS} = 0 V	-	0.75	1.2	V
t_{rr}	Reverse recovery time	I_F = 5.9 A; -dI_F/dt = 100 A/µs;	-	100	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 25 V	-	0.4	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 5.9 A; $V_{DD} \leq$ 15 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{amb} = 25 °C	-	60	mJ

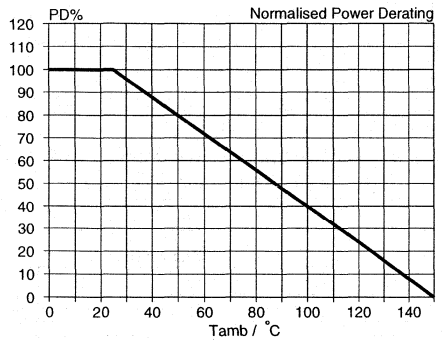


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{amb})

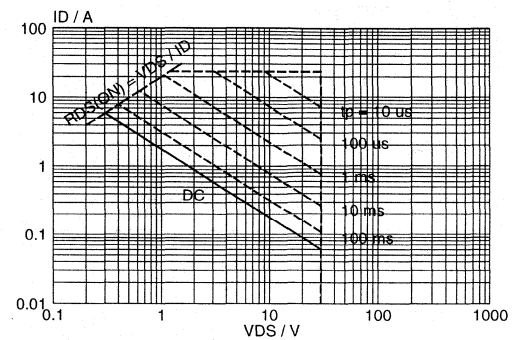


Fig.3. Safe operating area. T_{amb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

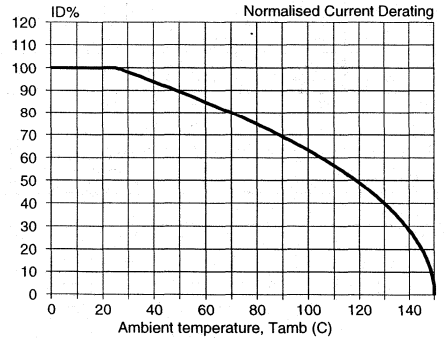


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{amb}); conditions: $V_{GS} \geq$ 5 V

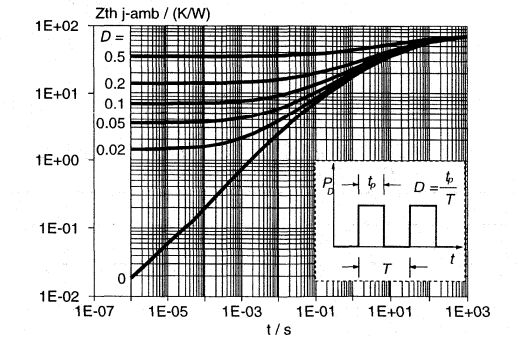


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}amb}$ = f(t); parameter D = t_p/T

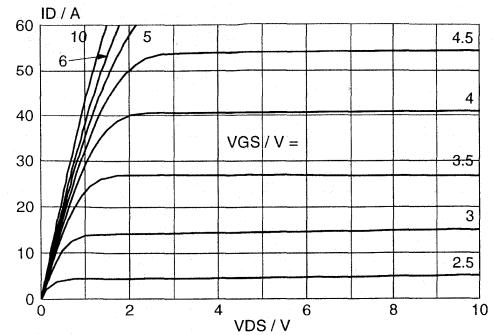


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

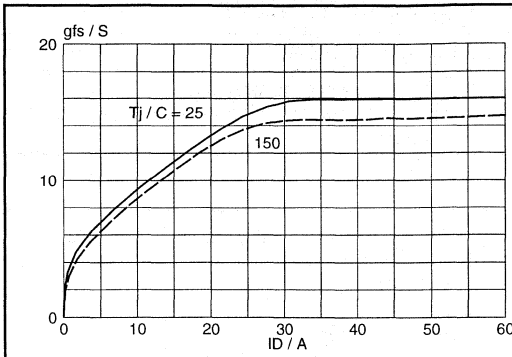


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

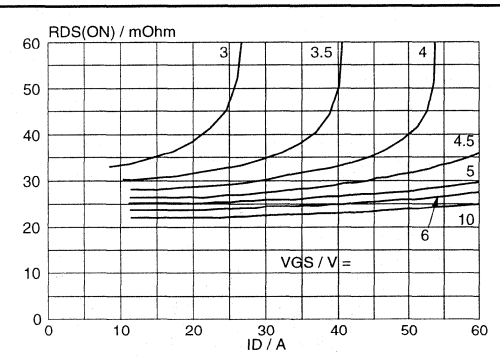


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

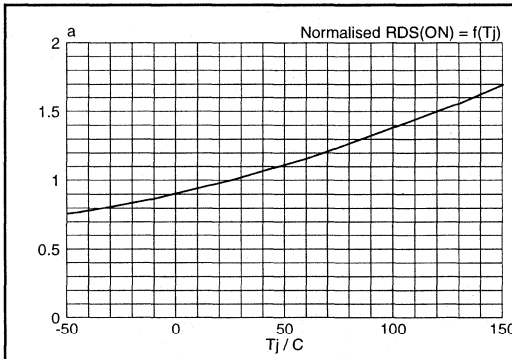


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,˚C} = f(T_j)$; I_D = 3.2 A; V_{GS} = 5 V

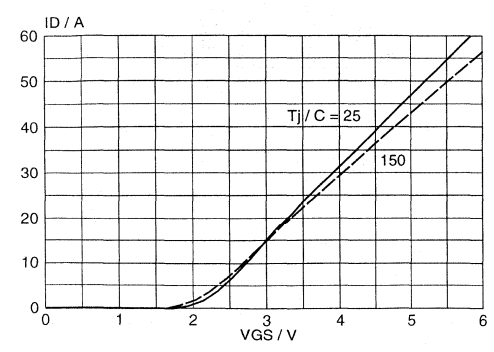


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

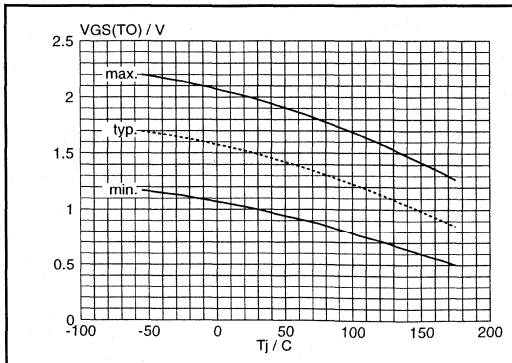


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

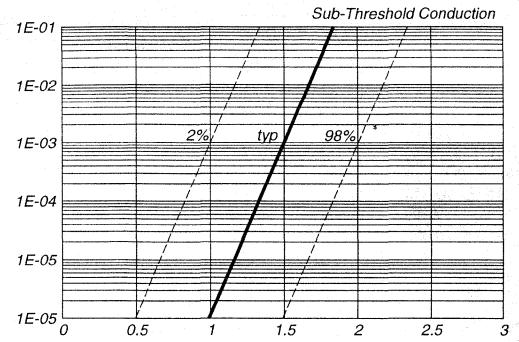


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

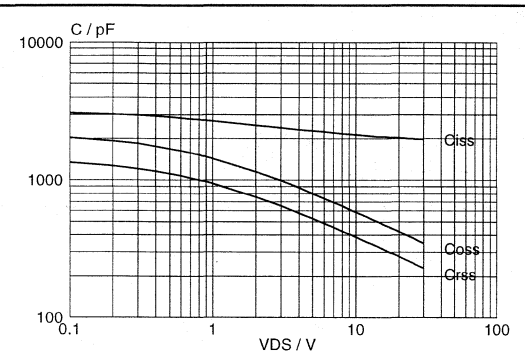


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

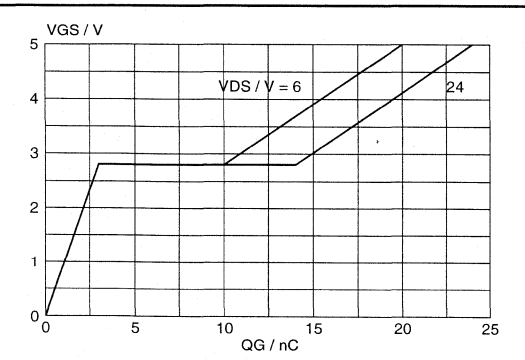


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 5.9$ A; parameter V_{DS}

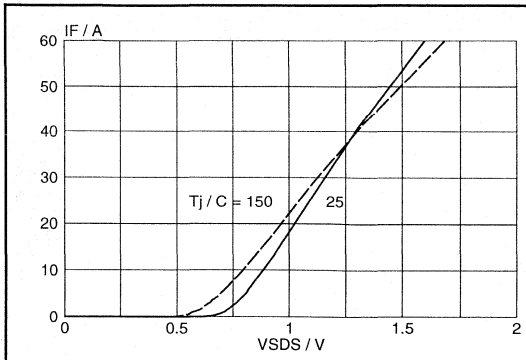


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

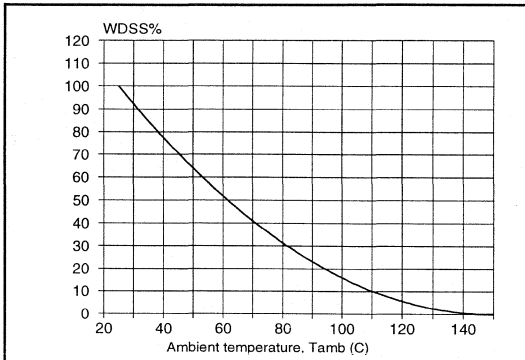


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{amb})$; conditions: $I_D = 5.9$ A

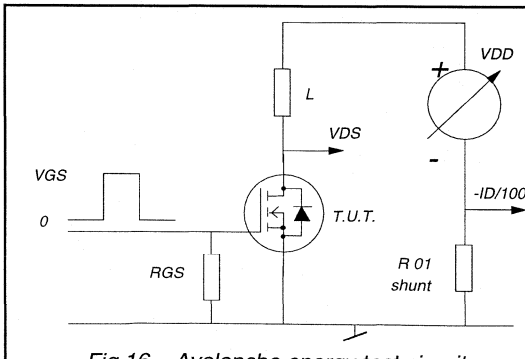


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PRINTED CIRCUIT BOARD

Dimensions in mm.

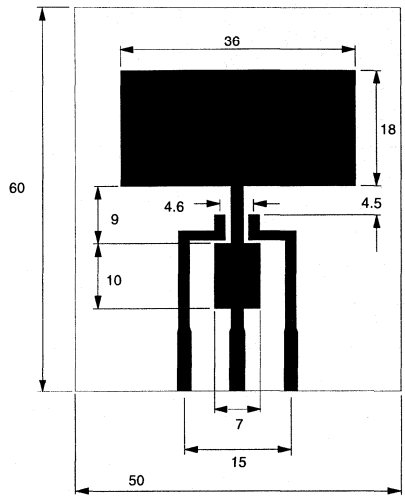


Fig.17. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).

TrenchMOS™ transistor
Logic level FET

PHT6N06LT

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting. The device features very low on-state resistance and has integral zener diodes giving ESD protection. It is intended for use in DC-DC converters and general purpose switching applications.

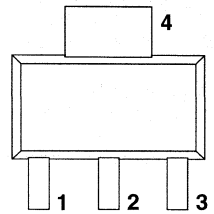
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC) T_{sp} = 25 °C	5.5	A
	Drain current (DC) T_{amb} = 25 °C	2.5	A
P_{tot}	Total power dissipation	8.3	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	150	mΩ

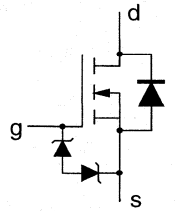
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
V_{GS}	Gate-source voltage	-	-	±13	V
I_D	Drain current (DC)	T_{sp} = 25 °C	-	5.5	A
		T_{amb} = 25 °C	-	2.5	A
I_D	Drain current (DC)	T_{sp} = 100 °C	-	3.8	A
		T_{amb} = 100 °C	-	1.75	A
I_{DM}	Drain current (pulse peak value)	T_{sp} = 25 °C	-	22	A
		T_{amb} = 25 °C	-	10	A
P_{tot}	Total power dissipation	T_{sp} = 25 °C	-	8.3	W
		T_{amb} = 25 °C	-	1.8	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	150	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}sp}$	From junction to solder point	Mounted on any PCB	12	15	K/W
$R_{th\ j\text{-}amb}$	From junction to ambient	Mounted on PCB of Fig.17	-	70	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
		T_j = 150˚C	0.6	-	-	V
		T_j = -55˚C	-	-	2.3	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 150˚C	-	-	100	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V	-	0.02	1	µA
		T_j = 150˚C	-	-	5	µA
$\pm V_{(BR)GSS}$	Gate source breakdown voltage	V_{GS} = ±1 mA	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 5 A	-	120	150	mΩ
		T_j = 150˚C	-	-	277	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5 A; T_j = 25˚C	3	5	-	S
$Q_{g(tot)}$	Total gate charge	I_D = 5 A; V_{DD} = 44 V; V_{GS} = 5 V	-	4.5	-	nC
Q_{gs}	Gate-source charge		-	1	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	2.5	-	nC
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	250	330	pF
C_{oss}	Output capacitance		-	65	80	pF
C_{rss}	Feedback capacitance		-	35	50	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 5 A;	-	11	17	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω;	-	38	60	ns
$t_{d\ off}$	Turn-off delay time		-	25	38	ns
t_f	Turn-off fall time	T_j = 25˚C	-	20	38	ns

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = -55 to 175˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{sp} = 25˚C	-	-	5.5	A
I_{DRM}	Pulsed reverse drain current	T_{sp} = 25˚C	-	-	30	A
V_{SD}	Diode forward voltage	I_F = 2 A; V_{GS} = 0 V	-	0.85	1.1	V
t_{rr}	Reverse recovery time	I_F = 2 A; -dI_F/dt = 100 A/µs;	-	43	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.16	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 1.9 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{sp} = 25 °C	-	-	15	mJ

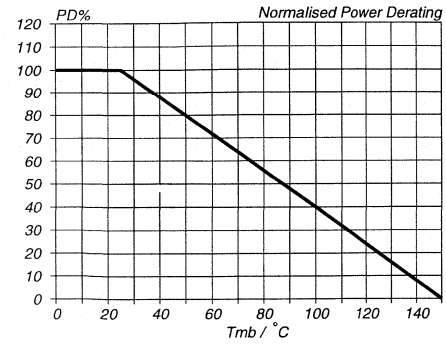


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{sp})

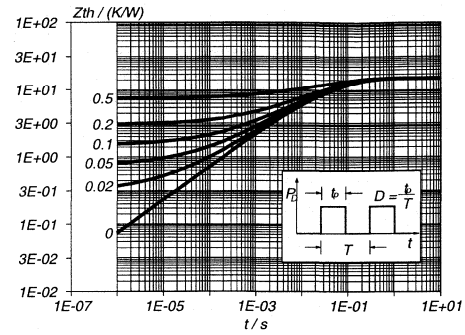


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}sp}$ = f(t); parameter D = t_p/T

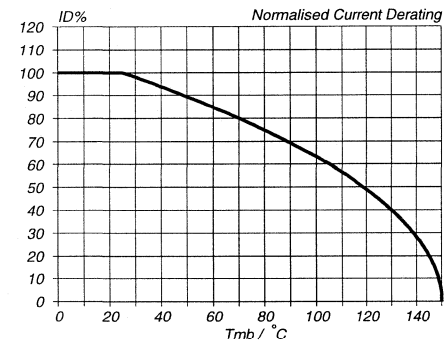


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{sp}); conditions: V_{GS} ≥ 5 V

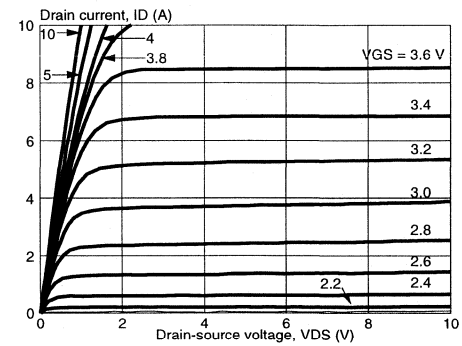


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

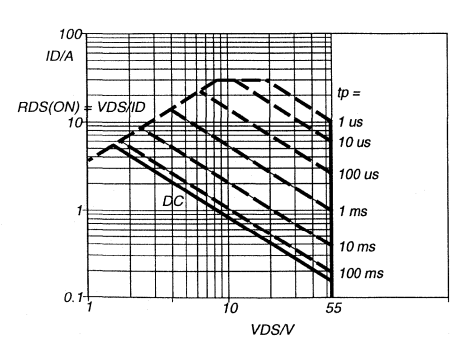


Fig.3. Safe operating area. T_{sp} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

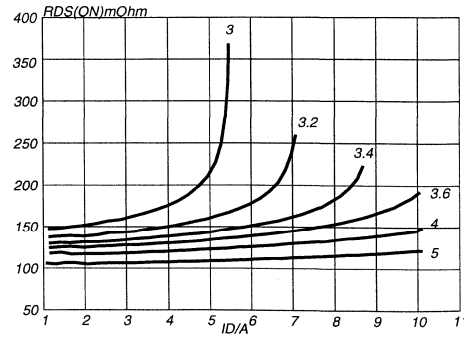


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

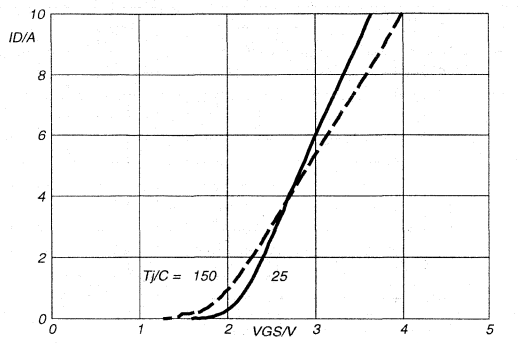


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

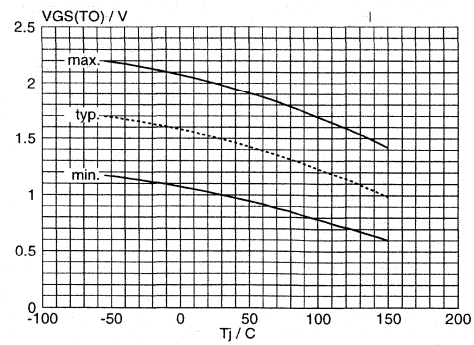


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

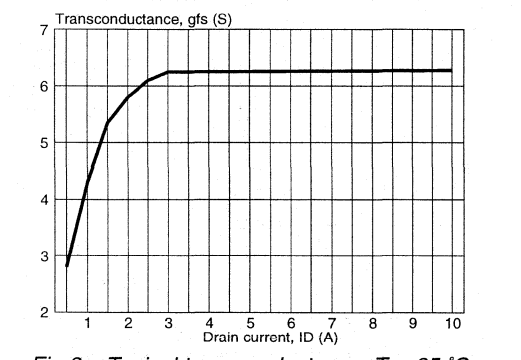


Fig.8. Typical transconductance, $T_j = 25$ °C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

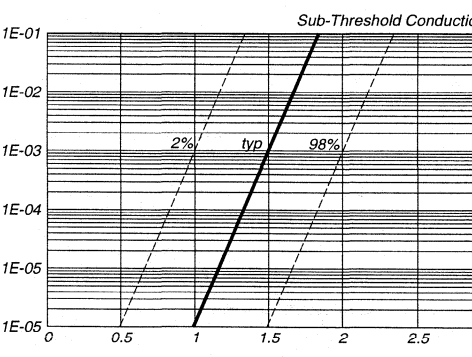


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

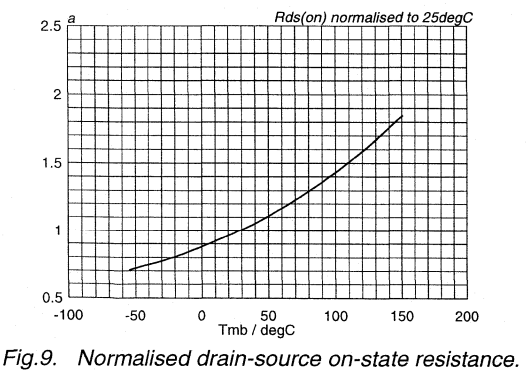


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ °C} = f(T_j)$; $I_D = 5$ A; $V_{GS} = 5$ V

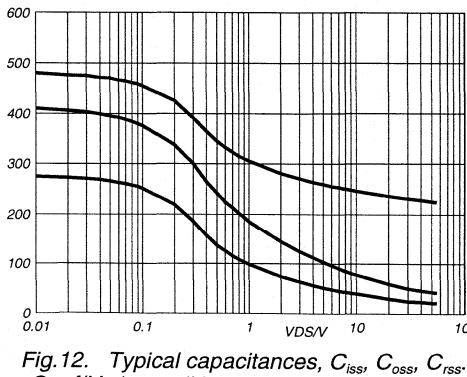


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

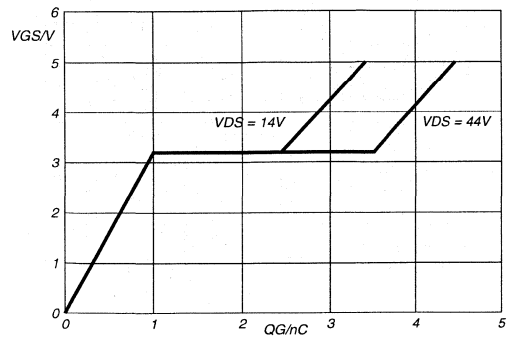


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 5$ A; parameter V_{DS}

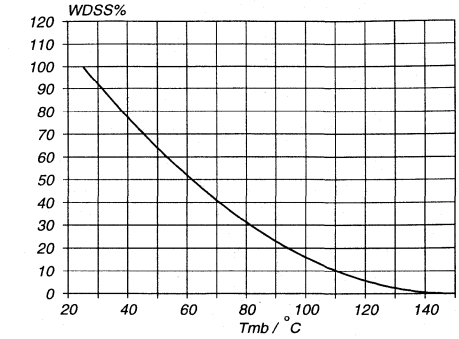


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{sp})$; conditions: $I_D = 1.9$ A

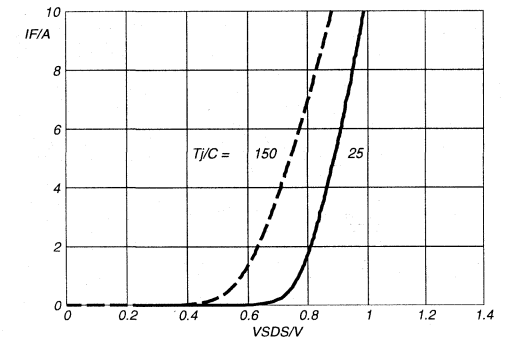


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

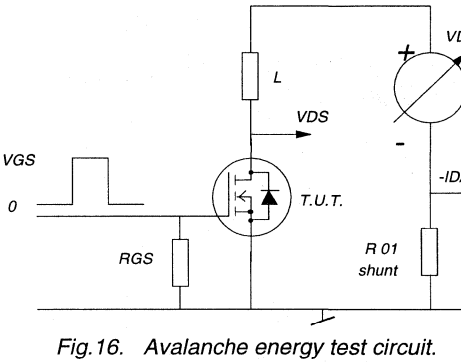


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PRINTED CIRCUIT BOARD

Dimensions in mm.

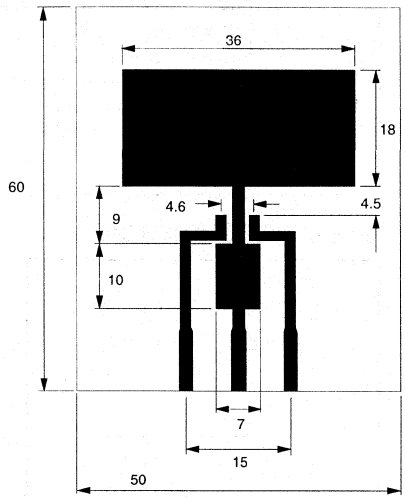


Fig.17. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).

TrenchMOS™ transistor Logic level FET

PHT8N06LT

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting. The device features very low on-state resistance and has integral zener diodes giving ESD protection. It is intended for use in DC-DC converters and general purpose switching applications.

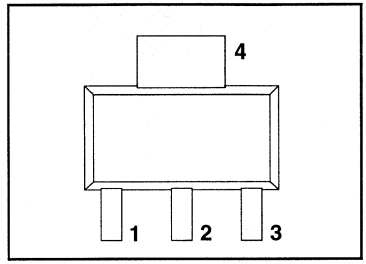
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current	7.5	A
P_{tot}	Total power dissipation	1.8	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	80	mΩ

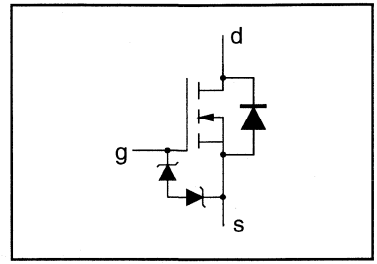
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	13	V
I_D	Drain current (DC)	T_{sp} = 25 °C	-	7.5	A
I_D	Drain current (DC)	On PCB in Fig.2 T_{amb} = 25 °C	-	3.5	A
I_D	Drain current (DC)	On PCB in Fig.2 T_{amb} = 100 °C	-	2.2	A
I_{DM}	Drain current (pulse peak value)	T_{sp} = 25 °C	-	40	A
P_{tot}	Total power dissipation	T_{sp} = 25 °C	-	8.3	W
P_{tot}	Total power dissipation	On PCB in Fig.2 T_{amb} = 25 °C	-	1.8	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	150	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}sp}$	From junction to solder point	Mounted on any PCB	12	15	K/W
$R_{th\ j\text{-}amb}$	From junction to ambient	Mounted on PCB of Fig.17	-	70	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
		T_j = 150˚C	0.6	-	-	V
		T_j = -55˚C	-	-	2.3	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 150˚C	-	-	100	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V	-	0.02	1	µA
		T_j = 150˚C	-	-	5	µA
$\pm V_{(BR)GSS}$	Gate source breakdown voltage	I_G = ±1 mA	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 5 A	-	65	80	mΩ
		T_j = 150˚C	-	-	148	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5 A; T_j = 25˚C	4	-	-	S
$Q_{g(tot)}$	Total gate charge	I_D = 7 A; V_{DD} = 44 V; V_{GS} = 5 V	-	11.2	-	nC
Q_{gs}	Gate-source charge		-	2.2	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	5	-	nC
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	500	650	pF
C_{oss}	Output capacitance		-	110	135	pF
C_{rss}	Feedback capacitance		-	60	85	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 7 A;	-	10	15	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω;	-	30	50	ns
$t_{d\ off}$	Turn-off delay time		-	30	45	ns
t_f	Turn-off fall time	T_j = 25˚C	-	30	40	ns

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = -55 to 175˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{sp} = 25˚C	-	-	7.5	A
I_{DRM}	Pulsed reverse drain current	T_{sp} = 25˚C	-	-	40	A
V_{SD}	Diode forward voltage	I_F = 5 A; V_{GS} = 0 V	-	0.85	1.1	V
t_{rr}	Reverse recovery time	I_F = 5 A; -dI_F/dt = 100 A/µs;	-	38	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.2	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 2.5 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{sp} = 25 °C	-	-	30	mJ

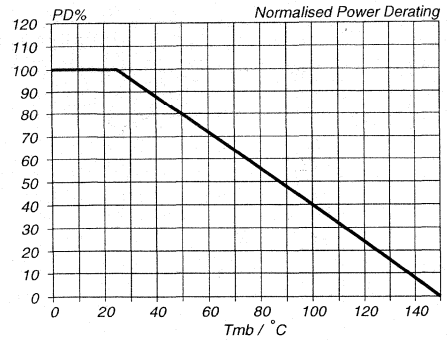


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{sp})

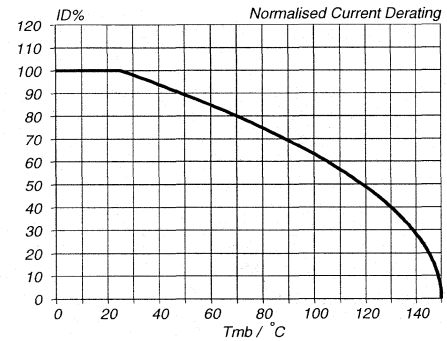


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{sp}); conditions: V_{GS} ≥ 5 V

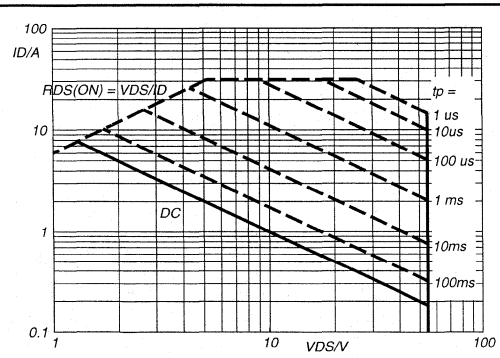


Fig.3. Safe operating area. T_{sp} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

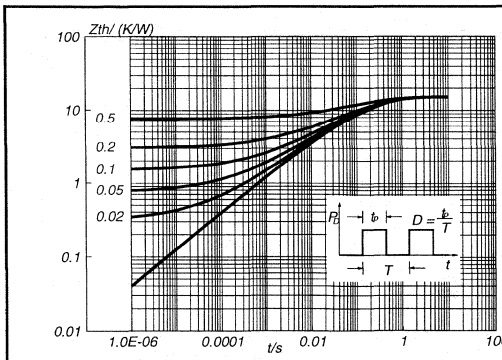


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}sp}$ = f(t); parameter D = t_p/T

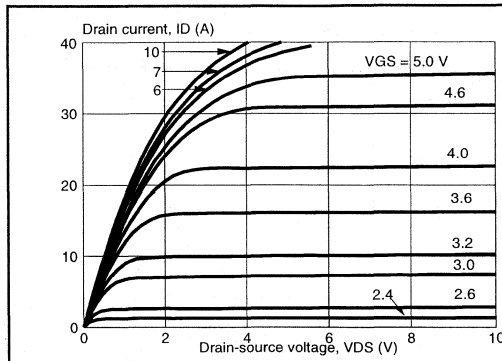


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

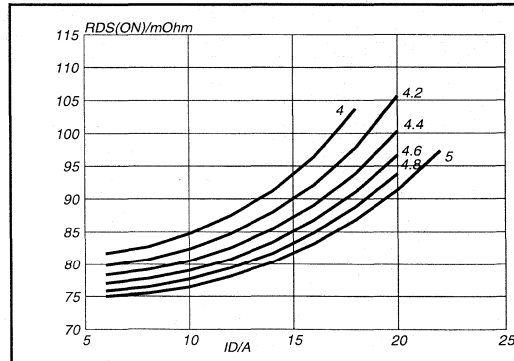


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

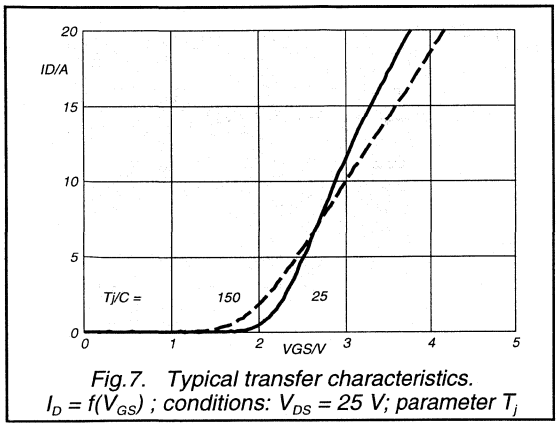


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

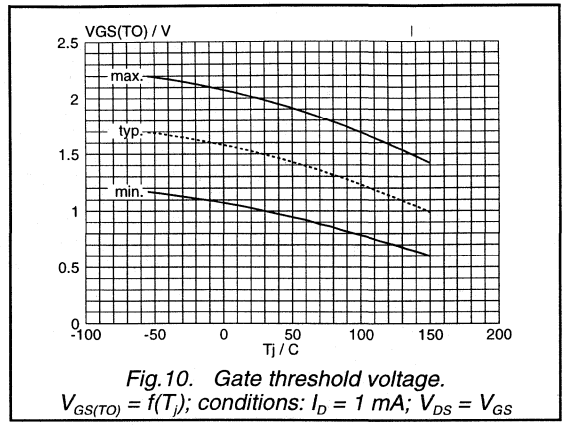


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

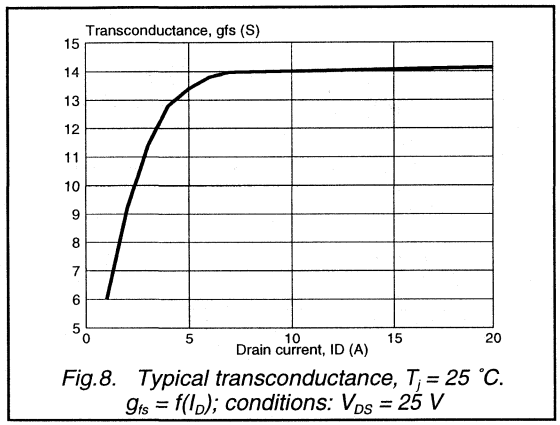


Fig.8. Typical transconductance, T_j = 25 ˚C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

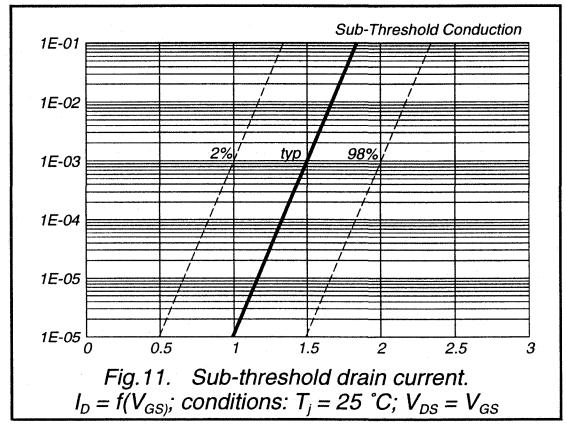


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

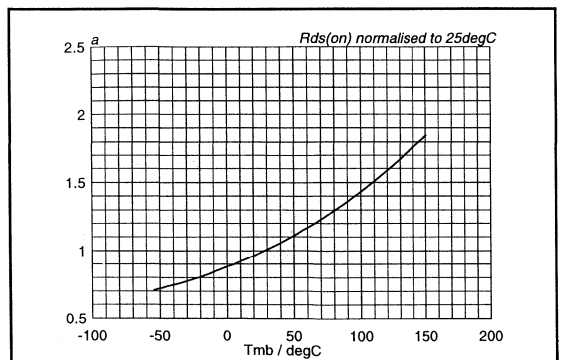


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,^{\circ}C} = f(T_j)$; I_D = 5 A; V_{GS} = 5 V

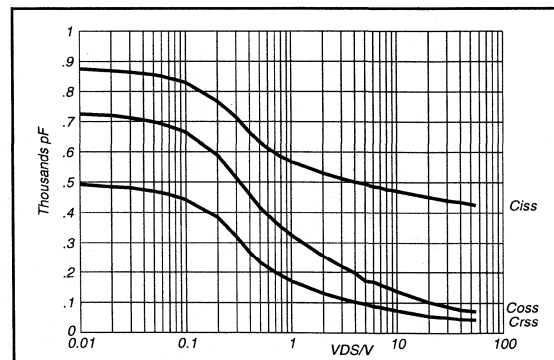


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

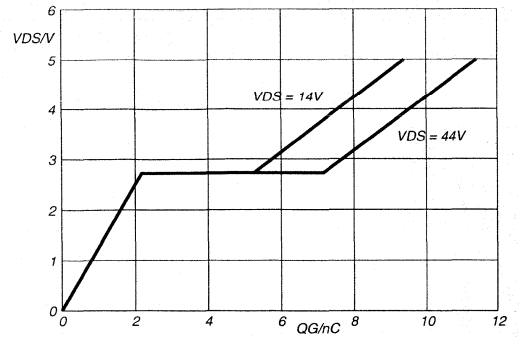


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 7$ A; parameter V_{DS}

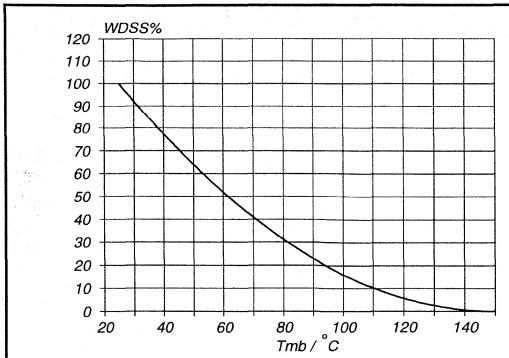


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{sp})$; conditions: $I_D = 2.5$ A

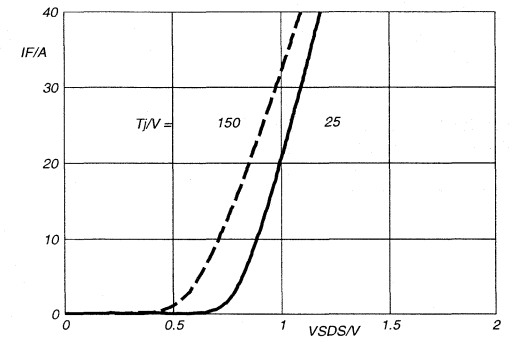


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

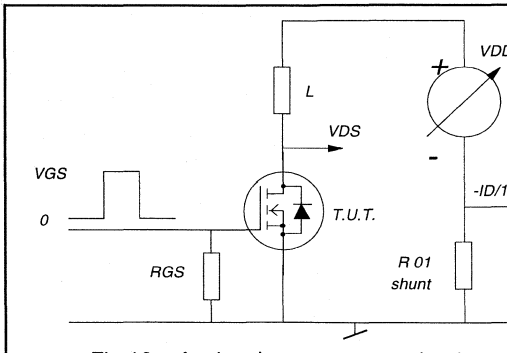


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PRINTED CIRCUIT BOARD

Dimensions in mm.

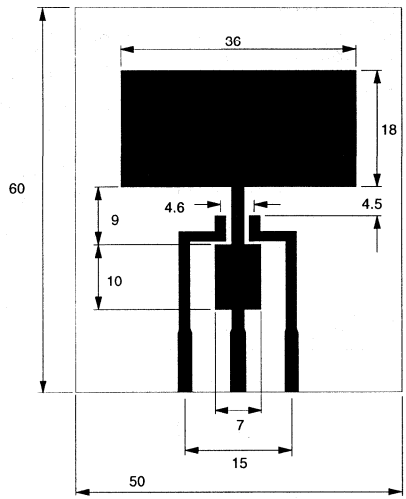


Fig.17. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).

TrenchMOS™ transistor Logic level FET

PHT11N06LT

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting. The device features very low on-state resistance and has integral zener diodes giving ESD protection. It is intended for use in DC-DC converters and general purpose switching applications.

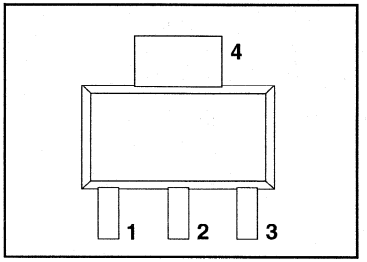
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC) T_{sp} = 25 °C	10.7	A
	Drain current (DC) T_{amb} = 25 °C	4.9	A
P_{tot}	Total power dissipation	8.3	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	40	mΩ

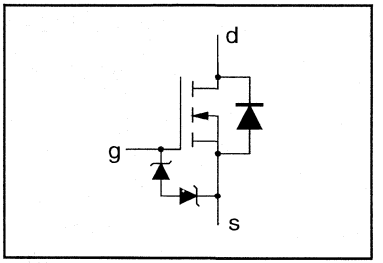
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	13	V
I_D	Drain current (DC)	T_{sp} = 25 °C	-	10.7	A
		T_{amb} = 25 °C	-	4.9	A
I_D	Drain current (DC)	T_{sp} = 100 °C	-	7.5	A
		T_{amb} = 100 °C	-	3.4	A
I_{DM}	Drain current (pulse peak value)	T_{sp} = 25 °C	-	42	A
		T_{amb} = 25 °C	-	19	A
P_{tot}	Total power dissipation	T_{sp} = 25 °C	-	8.3	W
		T_{amb} = 25 °C	-	1.8	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	150	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}sp}$	From junction to solder point	Mounted on any PCB	12	15	K/W
$R_{th\ j\text{-}amb}$	From junction to ambient	Mounted on PCB of Fig.18	-	70	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
		T_j = 150˚C	0.6	-	-	V
		T_j = -55˚C	-	-	2.3	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 150˚C	-	-	100	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V	-	0.02	1	µA
		T_j = 150˚C	-	-	5	µA
$\pm V_{(BR)GSS}$	Gate source breakdown voltage	I_G = ±1 mA	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 5 A	-	30	40	mΩ
		T_j = 150˚C	-	-	74	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5 A; T_j = 25˚C	11	19	-	S
$Q_{g(tot)}$	Total gate charge	I_D = 9 A; V_{DD} = 44 V; V_{GS} = 5 V	-	17	-	nC
Q_{gs}	Gate-source charge		-	3.5	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	10	-	nC
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1050	1400	pF
C_{oss}	Output capacitance		-	205	245	pF
C_{rss}	Feedback capacitance		-	110	150	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 9 A;	-	17	25	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω;	-	65	100	ns
$t_{d\ off}$	Turn-off delay time		-	70	105	ns
t_f	Turn-off fall time	T_j = 25˚C	-	70	105	ns

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = -55 to 175˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{sp} = 25˚C	-	-	10.7	A
I_{DRM}	Pulsed reverse drain current	T_{sp} = 25˚C	-	-	40	A
V_{SD}	Diode forward voltage	I_F = 5 A; V_{GS} = 0 V	-	0.85	1.1	V
t_{rr}	Reverse recovery time	I_F = 5 A; -dI_F/dt = 100 A/µs;	-	45	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	.3	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 3.6 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{sp} = 25 °C	-	-	60	mJ

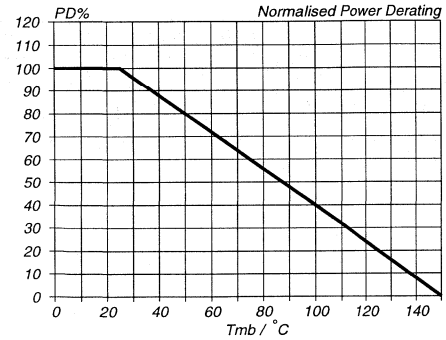


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{sp})

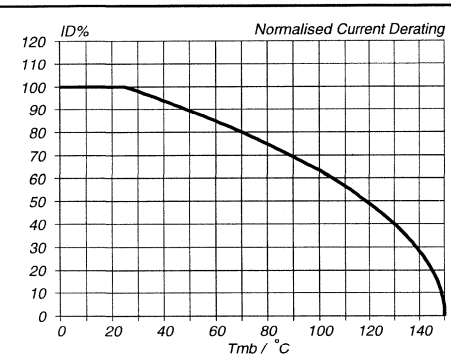


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{sp}); conditions: V_{GS} ≥ 5 V

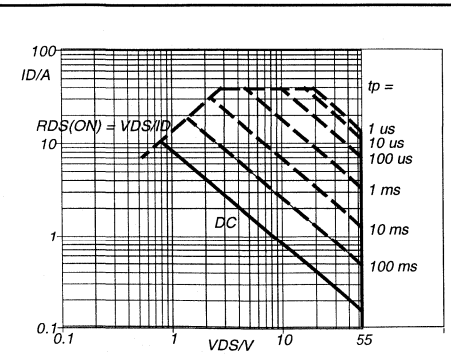


Fig.3. Safe operating area. T_{sp} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

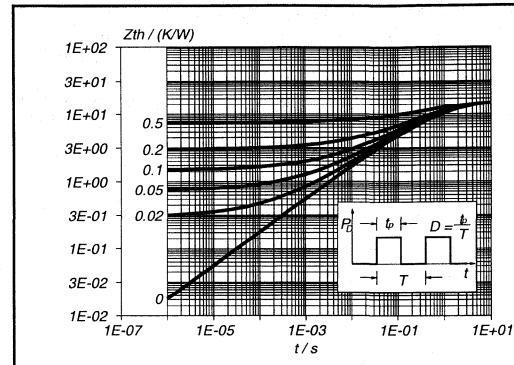


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}sp}$ = f(t); parameter D = t_p/T

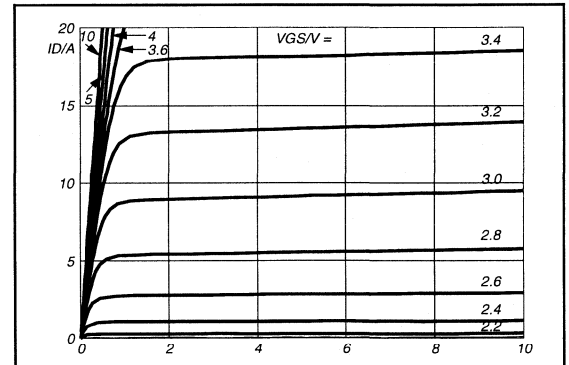


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

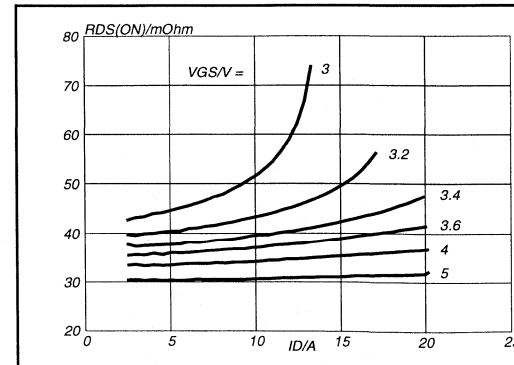


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

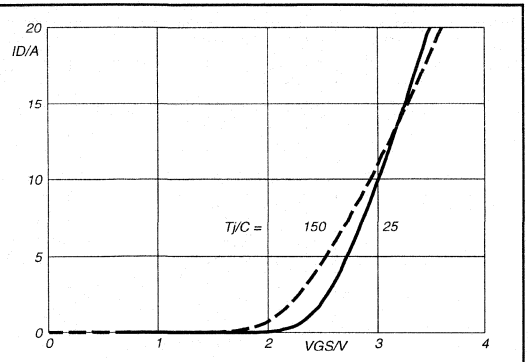


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

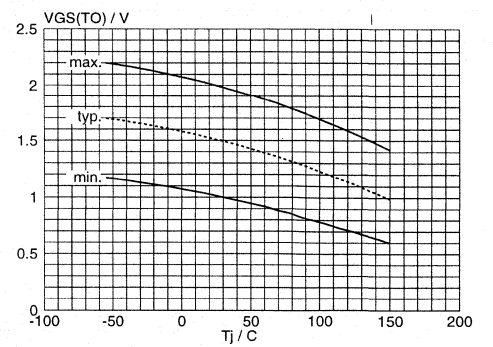


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

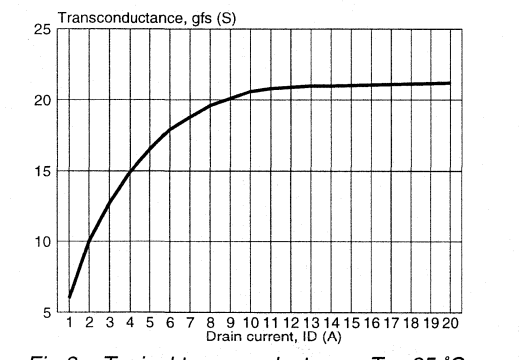


Fig.8. Typical transconductance, $T_j = 25$ °C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

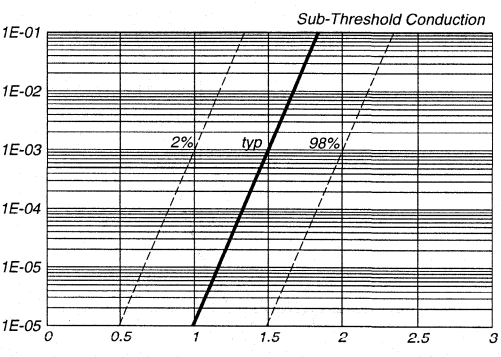


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

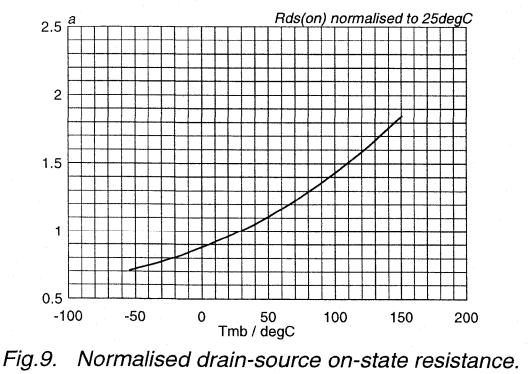


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ °C} = f(T_j)$; $I_D = 5$ A; $V_{GS} = 5$ V

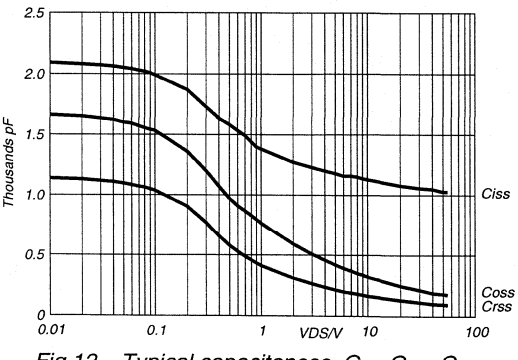


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

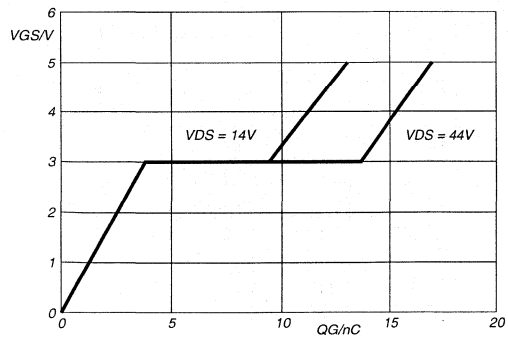


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 9$ A; parameter V_{DS}

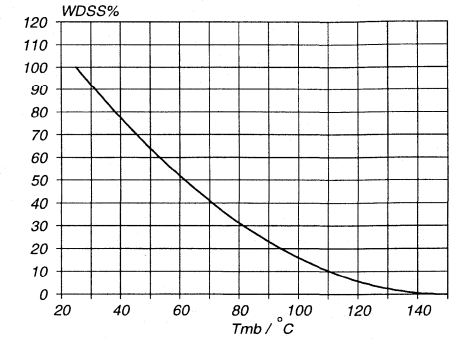


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{sp})$; conditions: $I_D = 3.6$ A

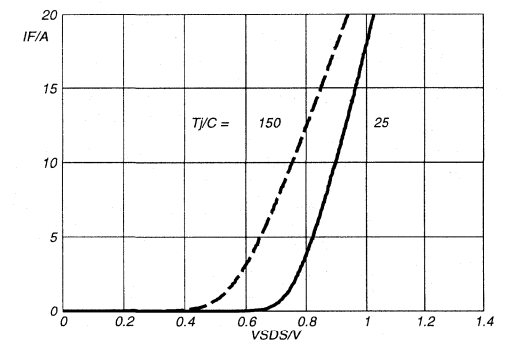


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

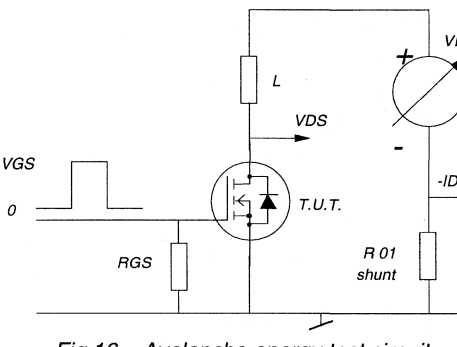


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PRINTED CIRCUIT BOARD

Dimensions in mm.

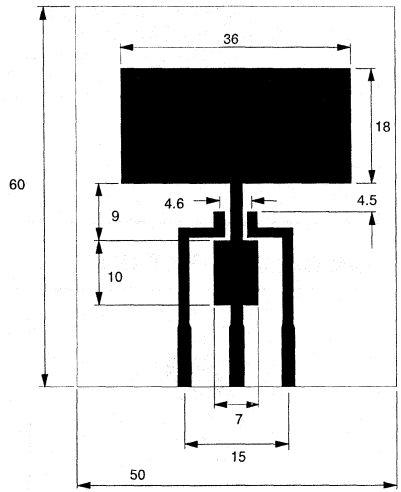


Fig.17. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).

PowerMOS transistor PHW7N60

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope featuring high avalanche energy capability, stable off-state characteristics, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

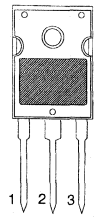
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	600	V
I_D	Drain current (DC)	7	A
P_{tot}	Total power dissipation	147	W
$R_{DS(ON)}$	Drain-source on-state resistance	1.2	Ω

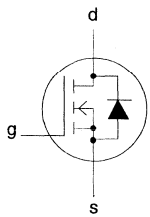
PINNING - SOT429 (TO247)

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	7	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	4.5	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	28	A
P_D	Total dissipation	T_{mb} = 25 °C	-	147	W
$\Delta P_D/\Delta T_{mb}$	Linear derating factor	T_{mb} > 25 °C	-	1.176	W/K
V_{GS}	Gate-source voltage		-	± 30	V
E_{AS}	Single pulse avalanche energy	$V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	570	mJ
I_{AS}	Peak avalanche current	$V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	7	A
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	0.85	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	45	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	600	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.7	-	V/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 4.1 A	-	0.9	1.2	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 4.1 A	3	4.5	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 600 V; V_{GS} = 0 V	-	2	100	μA
		V_{DS} = 480 V; V_{GS} = 0 V; T_j = 125 °C	-	50	500	μA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 6.2 A; V_{DD} = 360 V; V_{GS} = 10 V	-	90	110	nC
Q_{gs}	Gate-source charge		-	6	7	nC
Q_{gd}	Gate-drain (Miller) charge		-	44	60	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V; I_D = 6.2 A;	-	17	-	ns
t_r	Turn-on rise time	R_G = 9.1 Ω; R_D = 47 Ω	-	43	-	ns
$t_{d(off)}$	Turn-off delay time		-	118	-	ns
t_f	Turn-off fall time		-	50	-	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	12.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1100	-	pF
C_{oss}	Output capacitance		-	140	-	pF
C_{rss}	Feedback capacitance		-	80	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	7	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	28	A
V_{SD}	Diode forward voltage	I_S = 7 A; V_{GS} = 0 V	-	-	1.5	V
t_{rr}	Reverse recovery time	I_S = 6.2 A; V_{GS} = 0 V; dI/dt = 100 A/μs	-	530	-	ns
Q_{rr}	Reverse recovery charge		-	6.7	-	μC

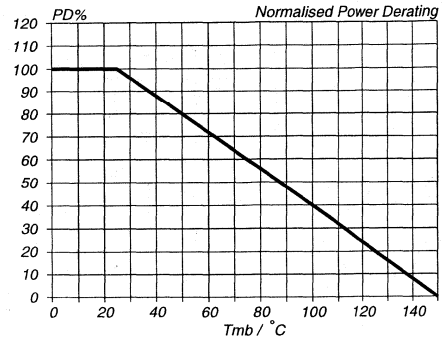


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

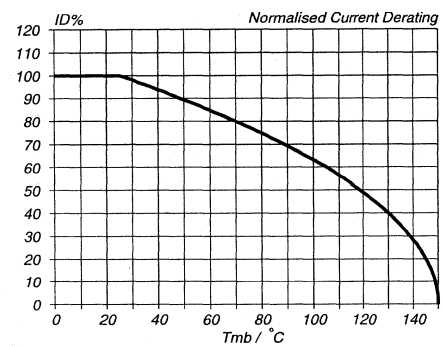


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq 10$ V

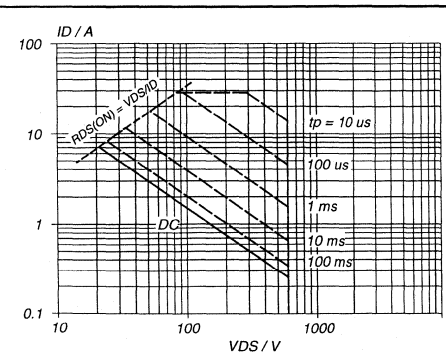


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

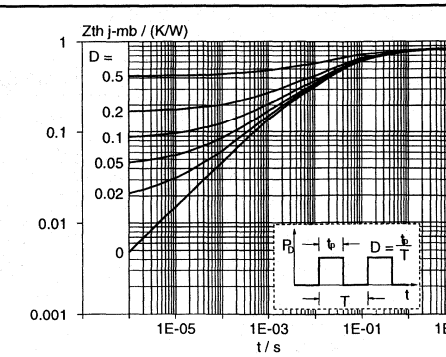


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

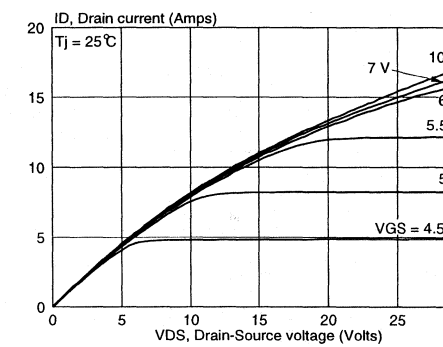


Fig.5. Typical output characteristics.
I_D = f(V_{DS}); parameter V_{GS}

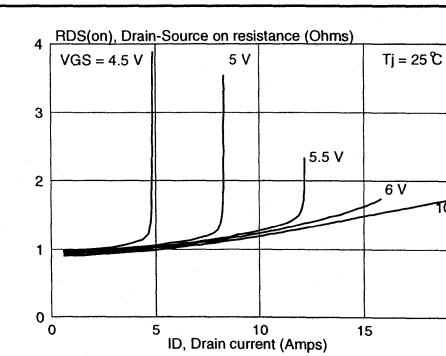


Fig.6. Typical on-state resistance.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

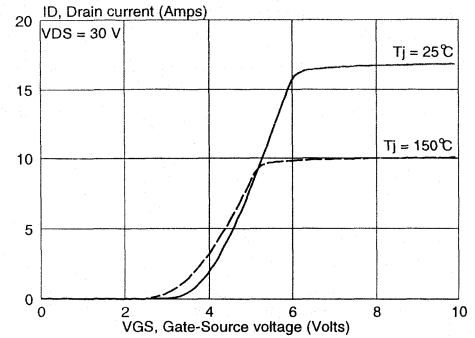


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; parameter T_j

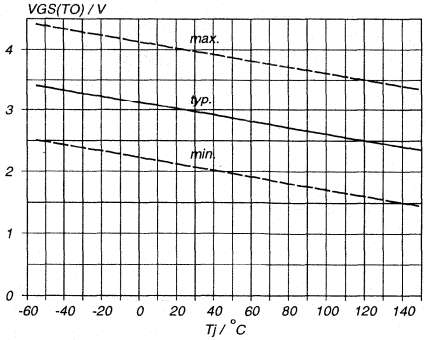


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: $I_D = 0.25$ mA; $V_{DS} = V_{GS}$

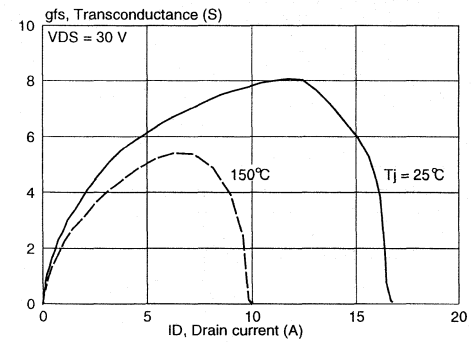


Fig.8. Typical transconductance. $g_{fs} = f(I_D)$; parameter T_j

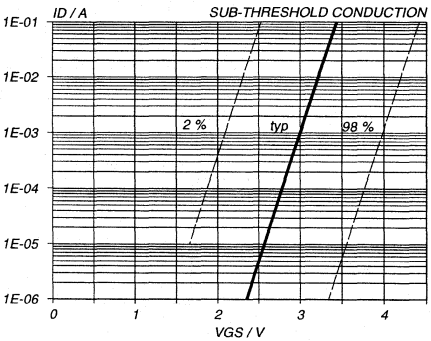


Fig.11. Sub-threshold drain current. $I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

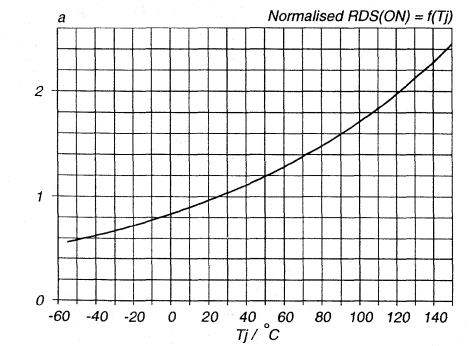


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 6.2$ A; $V_{GS} = 10$ V

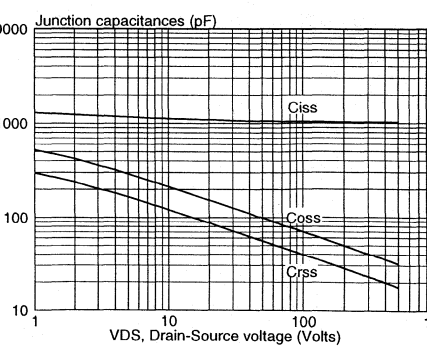


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

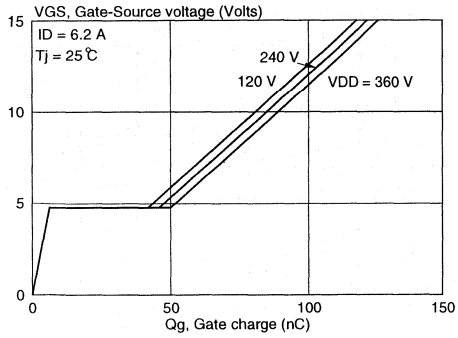


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; *parameter* V_{DS}

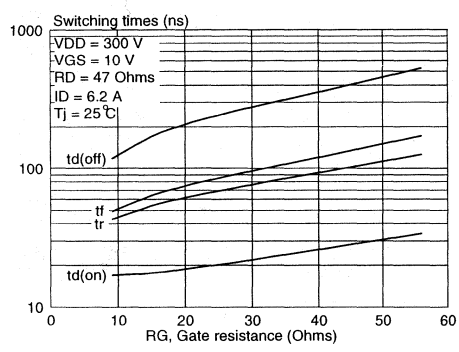


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

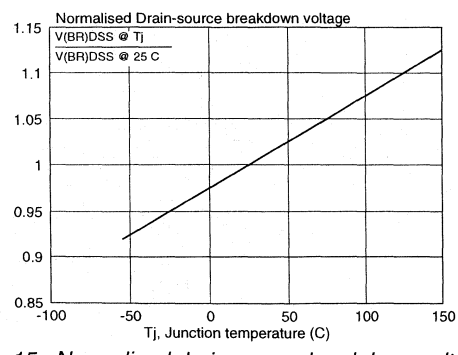


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ ^\circ C} = f(T_j)$

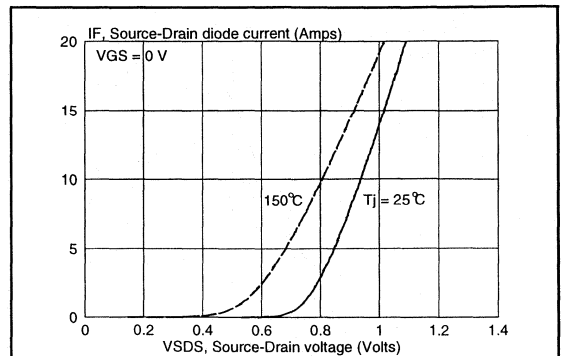


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; *parameter* T_j

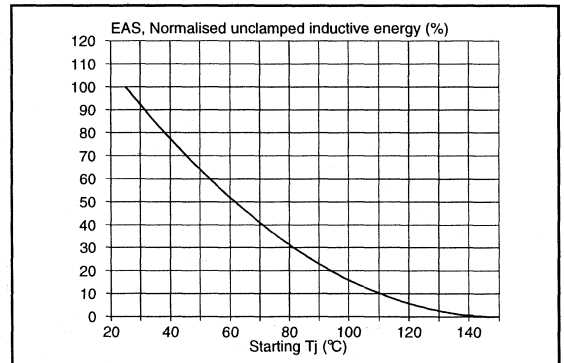


Fig.17. Normalised unclamped inductive energy.
$E_{AS}\% = f(T_j)$

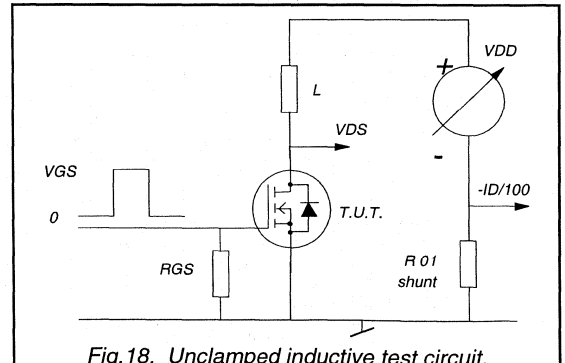


Fig.18. Unclamped inductive test circuit.
$E_{AS} = 0.5 \cdot LI_D^2 \cdot V_{(BR)DSS}/(V_{(BR)DSS} - V_{DD})$

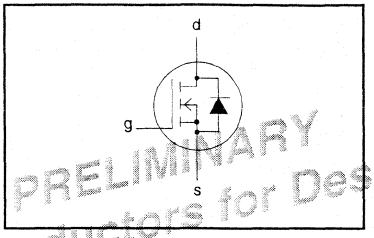
PowerMOS transistors
Avalanche energy rated

PHW14N50E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 500 V

I_D = 14 A

$R_{DS(ON)} \leq 0.4\ \Omega$

PRELIMINARY
Philips Semiconductors for Design-in information

GENERAL DESCRIPTION

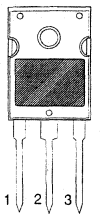
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHW14N50E is supplied in the SOT429 (TO247) conventional leaded package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

SOT429 (TO247)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	500	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	500	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	14	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	9	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	56	A
P_D	Total dissipation	T_{mb} = 25 °C	-	192	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 14 A; $V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	910	mJ
E_{AR}	Repetitive avalanche energy[1]		-	23	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	14	A

1 pulse width and repetition rate limited by T_j max.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	0.65	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	SOT78 package, in free air	-	60	-	K/W
		SOT429 package, in free air	-	45	-	K/W
		SOT404 package, pcb mounted, minimum footprint	-	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	500	-	-	V
$\Delta V_{(BR)DSS} / \Delta T_j$	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 7 A	-	0.35	0.4	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 7 A	9	12	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 500 V; V_{GS} = 0 V	-	1	20	µA
		V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 °C	-	50	500	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 14 A; V_{DD} = 400 V; V_{GS} = 10 V	-	170	220	nC
Q_{gs}	Gate-source charge		-	5	15	nC
Q_{gd}	Gate-drain (Miller) charge		-	95	130	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 250 V; R_D = 18 Ω;	-	35	-	ns
t_r	Turn-on rise time	R_G = 4.7 Ω	-	105	-	ns
$t_{d(off)}$	Turn-off delay time		-	200	-	ns
t_f	Turn-off fall time		-	120	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	2000	-	pF
C_{oss}	Output capacitance		-	325	-	pF
C_{rss}	Feedback capacitance		-	180	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	14	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	56	A
V_{SD}	Diode forward voltage	I_S = 14 A; V_{GS} = 0 V	-	-	1.5	V
t_{rr}	Reverse recovery time	I_S = 14 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	600	-	ns
Q_{rr}	Reverse recovery charge		-	10	-	µC

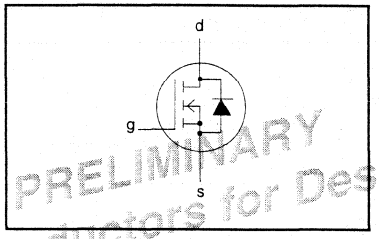
PowerMOS transistors Avalanche energy rated

PHW20N50E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 500 V

I_D = 20 A

$R_{DS(ON)} \leq 0.27\ \Omega$

PRELIMINARY
Philips Semiconductors for Design-in information

GENERAL DESCRIPTION

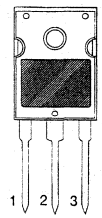
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHW20N50E is supplied in the SOT429 (TO247) conventional leaded package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

SOT429 (TO247)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	500	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	500	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	20	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	12.4	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	80	A
P_D	Total dissipation	T_{mb} = 25 °C	-	250	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 20 A; $V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	1300	mJ
E_{AR}	Repetitive avalanche energy[1]		-	32.5	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	20	A

1 pulse width and repetition rate limited by T_j max.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	0.5	K/W
$R_{th\ j\text{-}a$	Thermal resistance junction to ambient	SOT78 package, in free air	-	60	-	K/W
		SOT429 package, in free air	-	45	-	K/W
		SOT404 package, pcb mounted, minimum footprint	-	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	500	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 10 A	-	0.2	0.27	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 10 A	13	15	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 500 V; V_{GS} = 0 V	-	2	50	μA
		V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 °C	-	100	1000	μA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 20 A; V_{DD} = 400 V; V_{GS} = 10 V	-	250	330	nC
Q_{gs}	Gate-source charge		-	7	22	nC
Q_{gd}	Gate-drain (Miller) charge		-	140	190	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 250 V; R_D = 12 Ω;	-	48	-	ns
t_r	Turn-on rise time	R_G = 3.9 Ω	-	155	-	ns
$t_{d(off)}$	Turn-off delay time		-	300	-	ns
t_f	Turn-off fall time		-	180	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	3000	-	pF
C_{oss}	Output capacitance		-	480	-	pF
C_{rss}	Feedback capacitance		-	270	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	20	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	80	A
V_{SD}	Diode forward voltage	I_S = 20 A; V_{GS} = 0 V	-	-	1.5	V
t_{rr}	Reverse recovery time	I_S = 20 A; V_{GS} = 0 V; dI/dt = 100 A/μs	-	900	-	ns
Q_{rr}	Reverse recovery charge		-	15	-	μC

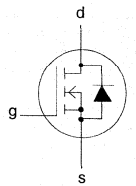
PowerMOS transistors
Avalanche energy rated

PHX2N50E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Isolated package

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 500 V

I_D = 1.4 A

$R_{DS(ON)} \leq 5\ \Omega$

GENERAL DESCRIPTION

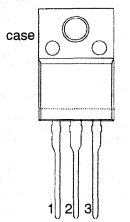
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHX2N50E is supplied in the SOT186A full pack, isolated package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

SOT186A



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	500	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	500	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{hs} = 25 °C; V_{GS} = 10 V	-	1.4	A
		T_{hs} = 100 °C; V_{GS} = 10 V	-	0.9	A
I_{DM}	Pulsed drain current	T_{hs} = 25 °C	-	8	A
P_D	Total dissipation	T_{hs} = 25 °C	-	25	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 2 A; $V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	130	mJ
E_{AR}	Repetitive avalanche energy[1]		-	3.6	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	2	A

1 pulse width and repetition rate limited by T_j max.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	500	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 1 A	-	3.1	5	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 1 A	0.5	1.3	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 500 V; V_{GS} = 0 V	-	1	25	µA
		V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 °C	-	30	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 2 A; V_{DD} = 400 V; V_{GS} = 10 V	-	20	25	nC
Q_{gs}	Gate-source charge		-	2	3	nC
Q_{gd}	Gate-drain (Miller) charge		-	12	15	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 250 V; R_D = 120 Ω;	-	10	-	ns
t_r	Turn-on rise time	R_G = 24 Ω	-	20	-	ns
$t_{d(off)}$	Turn-off delay time		-	60	-	ns
t_f	Turn-off fall time		-	20	-	ns
L_d	Internal drain inductance	Measured from drain lead to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	236	-	pF
C_{oss}	Output capacitance		-	40	-	pF
C_{rss}	Feedback capacitance		-	22	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{hs} = 25°C	-	-	2	A
I_{SM}	Pulsed source current (body diode)	T_{hs} = 25°C	-	-	8	A
V_{SD}	Diode forward voltage	I_S = 2 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 2 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	300	-	ns
Q_{rr}	Reverse recovery charge		-	2.1	-	µC

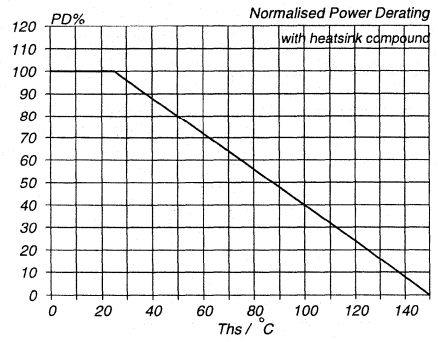


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{hs})

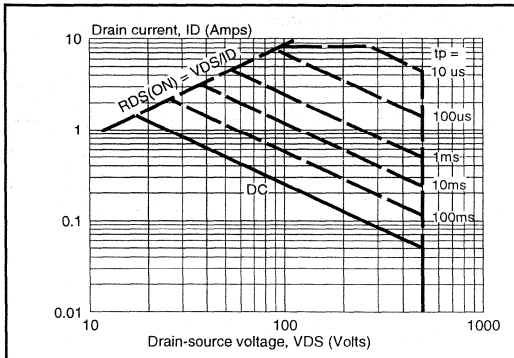


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

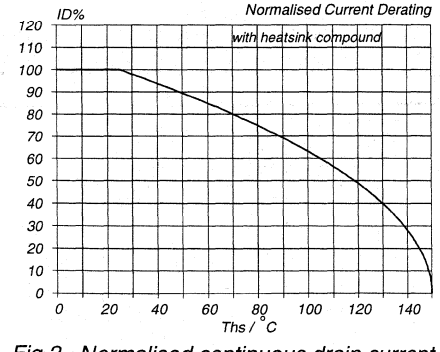


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{hs}); conditions: V_{GS} ≥ 10 V

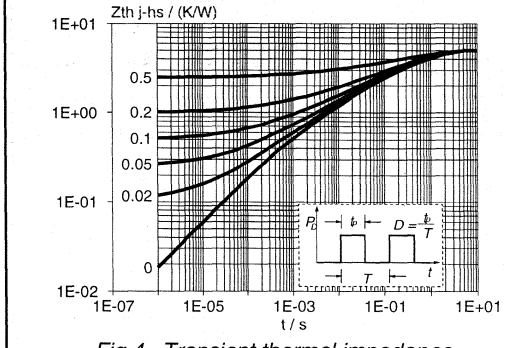


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}hs}$ = f(t); parameter D = t_p/T

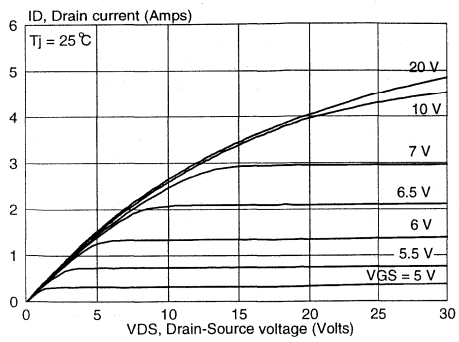


Fig.5. Typical output characteristics.
$I_D = f(V_{DS})$; parameter V_{GS}

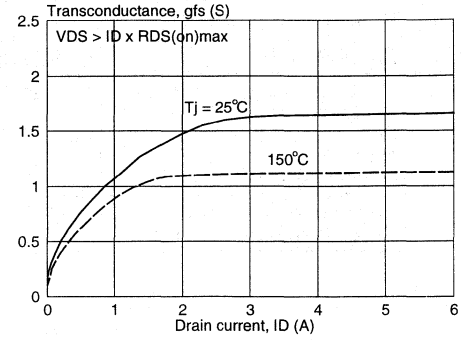


Fig.8. Typical transconductance.
$g_{fs} = f(I_D)$; parameter T_j

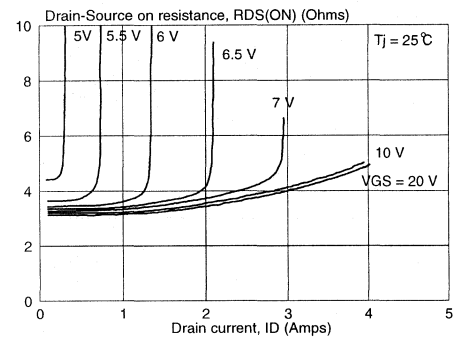


Fig.6. Typical on-state resistance.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

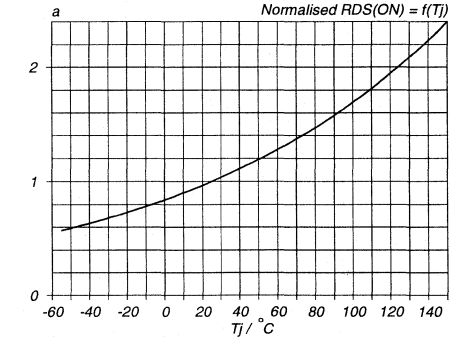


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 1 A; V_{GS} = 10 V

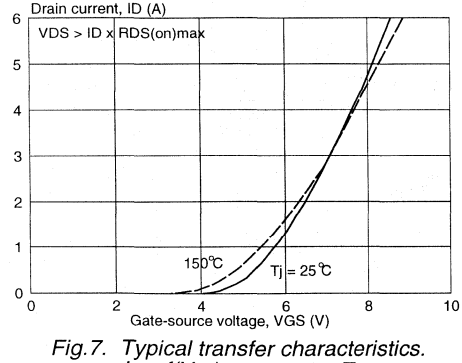


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

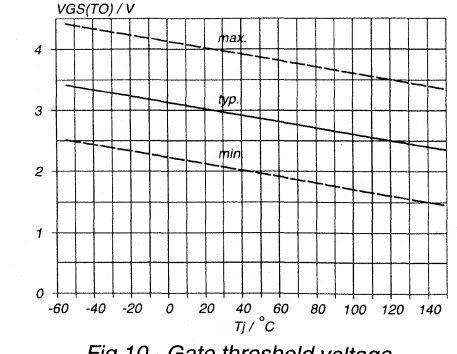


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

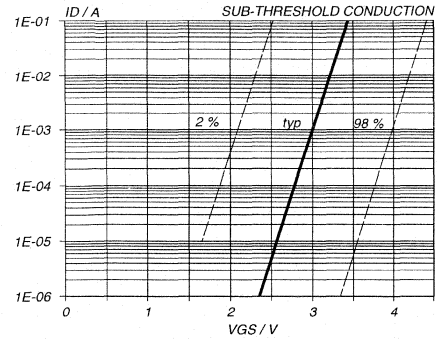


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

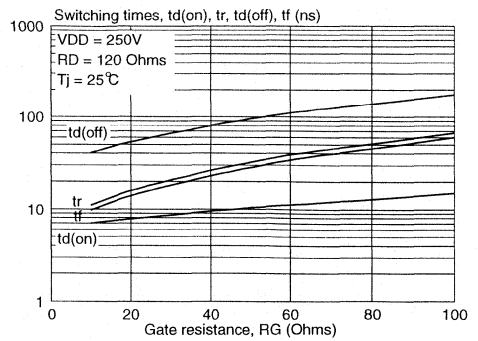


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

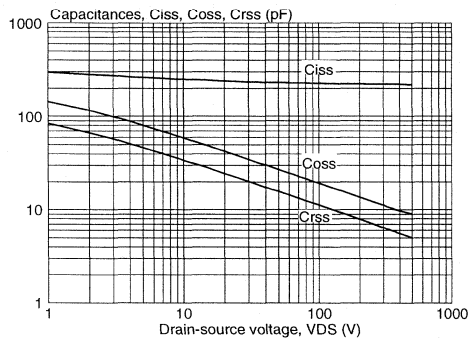


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

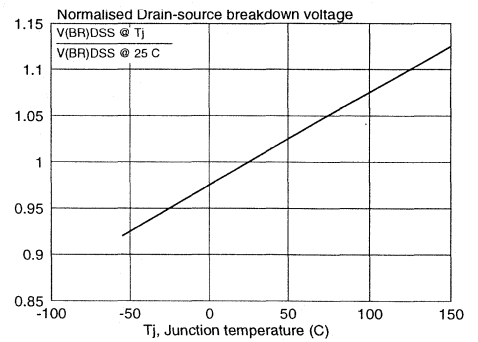


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ ^\circ C} = f(T_j)$

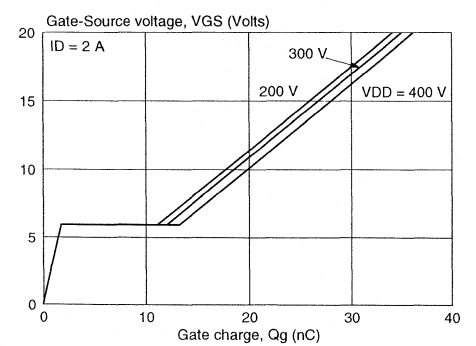


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

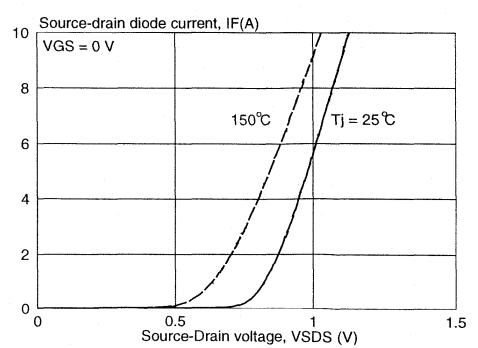


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

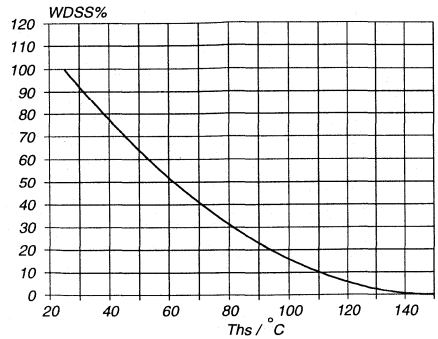


Fig.17. Normalised non-repetitive avalanche energy rating.
$E_{AS}\% = f(T_{hs})$

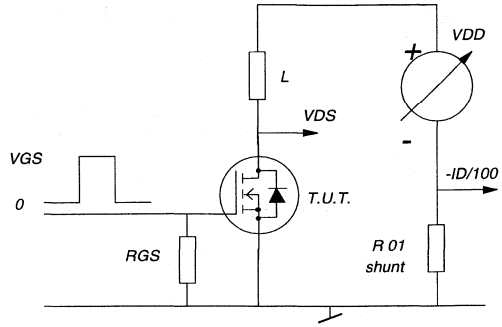


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot \frac{V_{(BR)DSS}}{(V_{(BR)DSS} - V_{DD})}$$

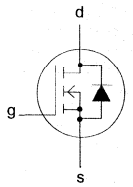
PowerMOS transistors Avalanche energy rated

PHX2N60E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Isolated package

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 600 V

I_D = 1.3 A

$R_{DS(ON)} \leq 6\ \Omega$

GENERAL DESCRIPTION

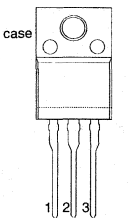
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHX2N60E is supplied in the SOT186A full pack, isolated package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

SOT186A



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	600	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	600	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{hs} = 25 °C; V_{GS} = 10 V	-	1.3	A
		T_{hs} = 100 °C; V_{GS} = 10 V	-	0.83	A
I_{DM}	Pulsed drain current	T_{hs} = 25 °C	-	7.6	A
P_D	Total dissipation	T_{hs} = 25 °C	-	25	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 1.9 A; $V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	144	mJ
E_{AR}	Repetitive avalanche energy[1]		-	3.6	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	1.9	A

1 pulse width and repetition rate limited by T_j max.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	600	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 1 A	-	4.6	6	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 1 A	0.5	1.4	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 600 V; V_{GS} = 0 V	-	1	100	µA
		V_{DS} = 480 V; V_{GS} = 0 V; T_j = 125 °C	-	50	500	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 2 A; V_{DD} = 480 V; V_{GS} = 10 V	-	20	25	nC
Q_{gs}	Gate-source charge		-	2	3	nC
Q_{gd}	Gate-drain (Miller) charge		-	9	15	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V; R_D = 150 Ω;	-	10	-	ns
t_r	Turn-on rise time	R_G = 24 Ω	-	20	-	ns
$t_{d(off)}$	Turn-off delay time		-	60	-	ns
t_f	Turn-off fall time		-	20	-	ns
L_d	Internal drain inductance	Measured from drain lead to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	236	-	pF
C_{oss}	Output capacitance		-	34	-	pF
C_{rss}	Feedback capacitance		-	20	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{hs} = 25°C	-	-	1.9	A
I_{SM}	Pulsed source current (body diode)	T_{hs} = 25°C	-	-	7.6	A
V_{SD}	Diode forward voltage	I_S = 2 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 2 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	360	-	ns
Q_{rr}	Reverse recovery charge		-	2.4	-	µC

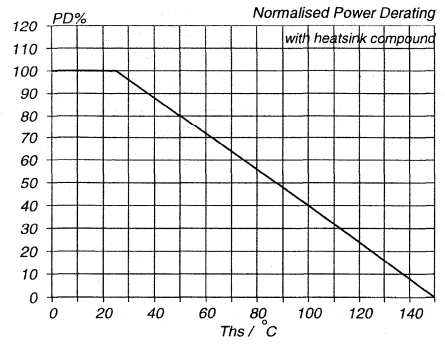


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{hs})

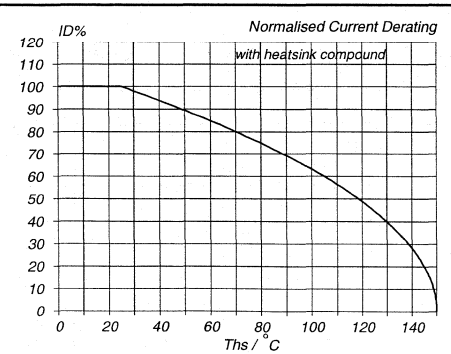


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{hs}); conditions: V_{GS} ≥ 10 V

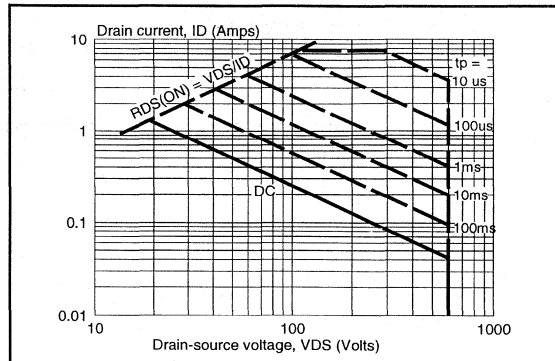


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

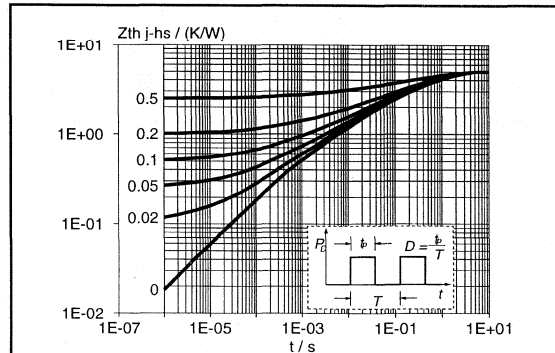


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}hs}$ = f(t); parameter D = t_p/T

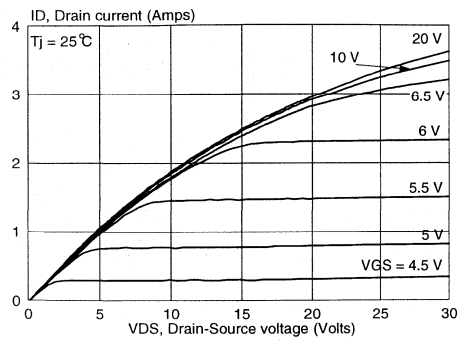


Fig.5. Typical output characteristics.
$I_D = f(V_{DS})$; parameter V_{GS}

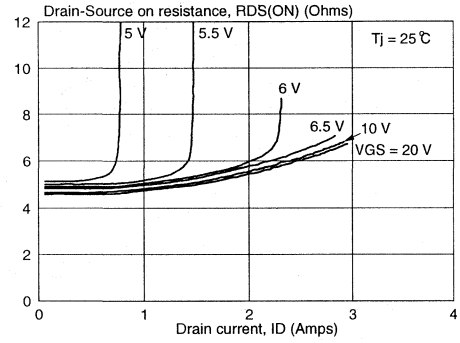


Fig.6. Typical on-state resistance.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

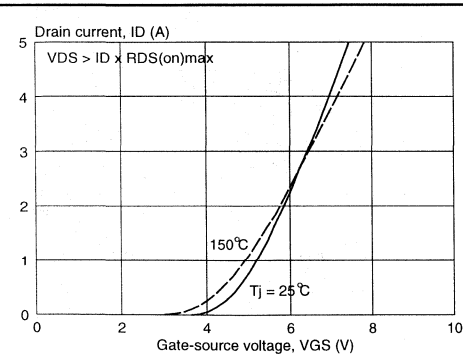


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

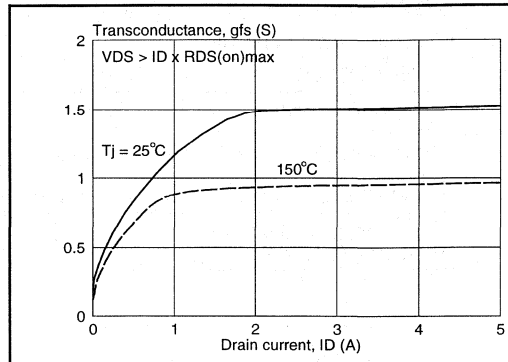


Fig.8. Typical transconductance.
$g_{fs} = f(I_D)$; parameter T_j

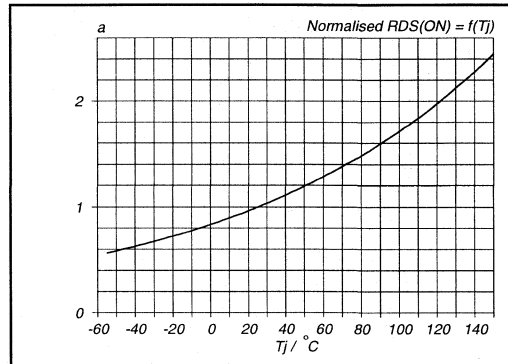


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 1 A; V_{GS} = 10 V

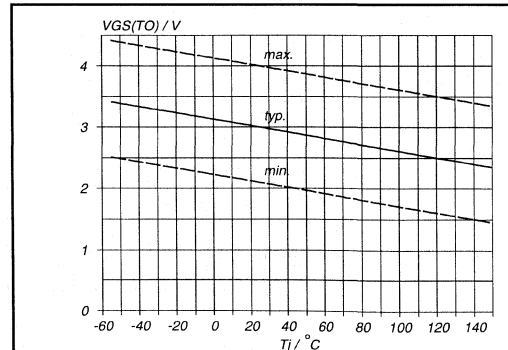


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

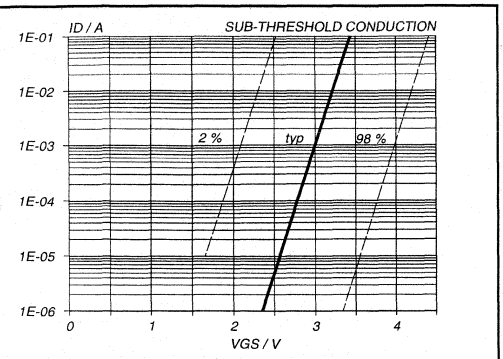


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

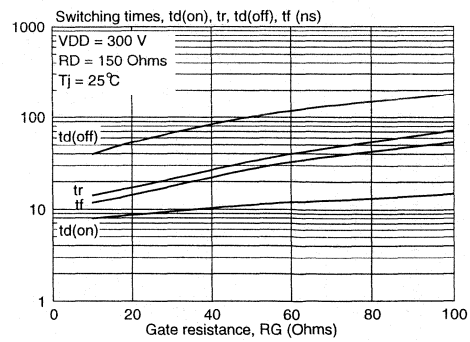


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

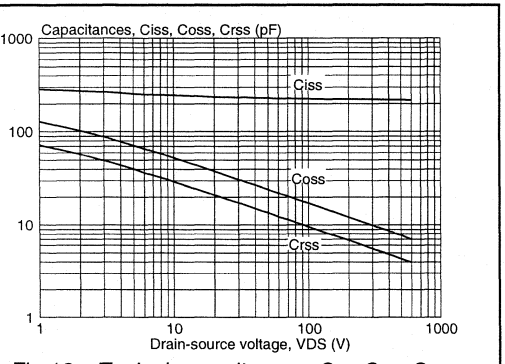


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

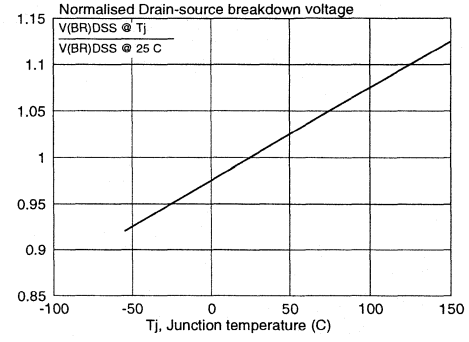


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

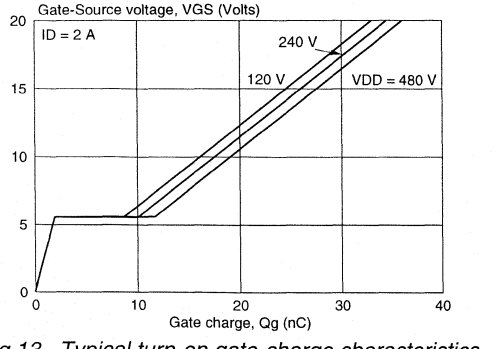


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

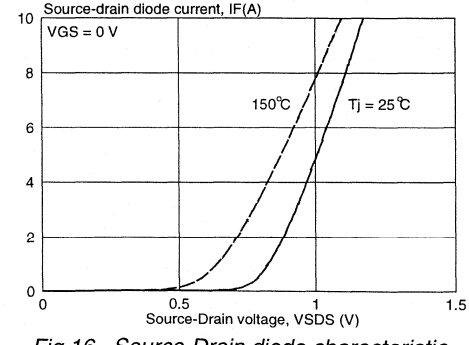


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

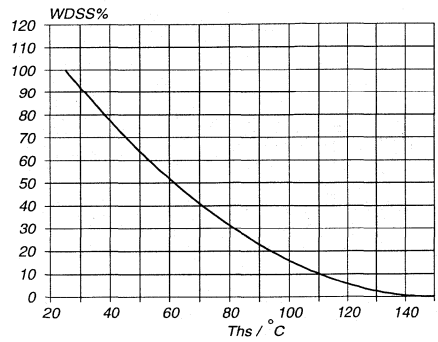


Fig.17. Normalised non-repetitive avalanche energy rating.
$E_{AS}\% = f(T_{hs})$

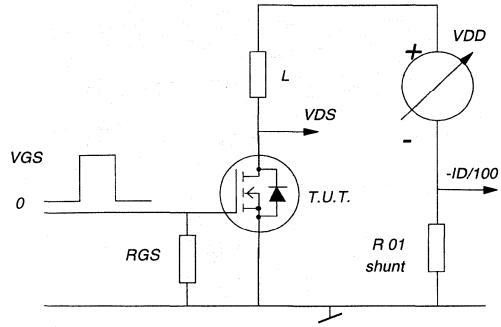


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot \frac{V_{(BR)DSS}}{(V_{(BR)DSS} - V_{DD})}$$

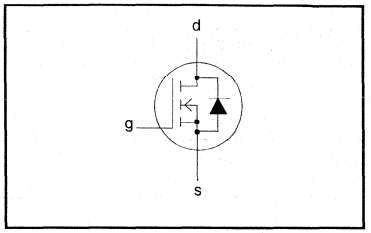
PowerMOS transistors Avalanche energy rated

PHX3N40E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Isolated package

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 400 V

I_D = 1.7 A

$R_{DS(ON)} \leq 3.5\ \Omega$

GENERAL DESCRIPTION

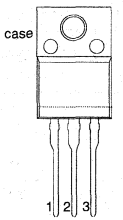
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHX3N40E is supplied in the SOT186A full pack, isolated package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

SOT186A



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	400	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	400	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{hs} = 25 °C; V_{GS} = 10 V	-	1.7	A
		T_{hs} = 100 °C; V_{GS} = 10 V	-	1.1	A
I_{DM}	Pulsed drain current	T_{hs} = 25 °C	-	10	A
P_D	Total dissipation	T_{hs} = 25 °C	-	25	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 2 A; $V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	120	mJ
E_{AR}	Repetitive avalanche energy[1]		-	3.6	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	2	A

1 pulse width and repetition rate limited by T_j max.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	400	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 1.25 A	-	2	3.5	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 1.25 A	0.5	1.5	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 400 V; V_{GS} = 0 V	-	1	25	µA
		V_{DS} = 320 V; V_{GS} = 0 V; T_j = 125 °C	-	30	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 2.5 A; V_{DD} = 320 V; V_{GS} = 10 V	-	20	25	nC
Q_{gs}	Gate-source charge		-	2	3	nC
Q_{gd}	Gate-drain (Miller) charge		-	8	12	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 200 V; R_D = 82 Ω;	-	10	-	ns
t_r	Turn-on rise time	R_G = 24 Ω	-	25	-	ns
$t_{d(off)}$	Turn-off delay time		-	46	-	ns
t_f	Turn-off fall time		-	25	-	ns
L_d	Internal drain inductance	Measured from drain lead to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	240	-	pF
C_{oss}	Output capacitance		-	44	-	pF
C_{rss}	Feedback capacitance		-	26	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{hs} = 25°C	-	-	2.5	A
I_{SM}	Pulsed source current (body diode)	T_{hs} = 25°C	-	-	10	A
V_{SD}	Diode forward voltage	I_S = 2.5 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 2.5 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	200	-	ns
Q_{rr}	Reverse recovery charge		-	2	-	µC

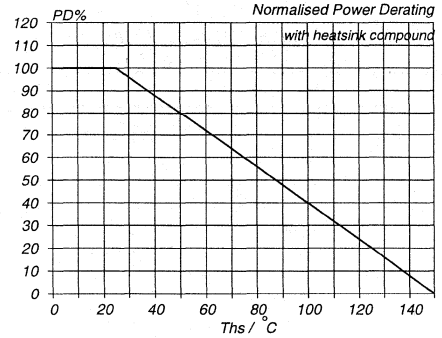


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{hs})

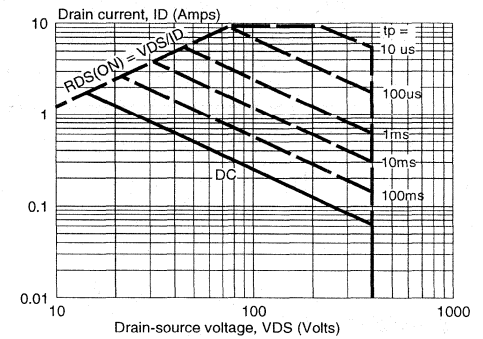


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

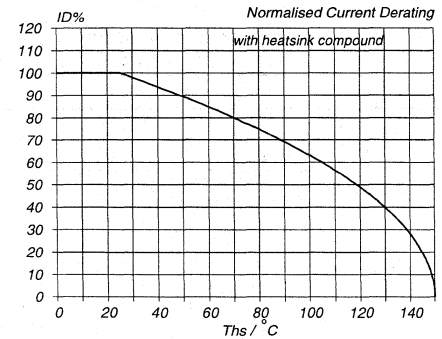


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{hs}); conditions: V_{GS} ≥ 10 V

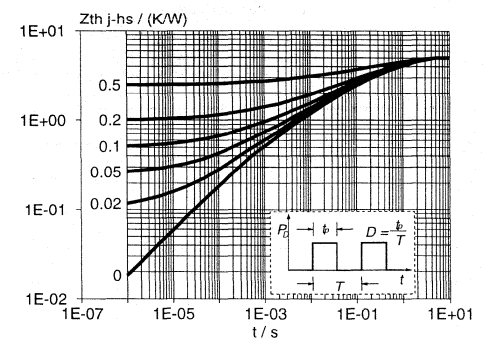


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}hs}$ = f(t); parameter D = t_p/T

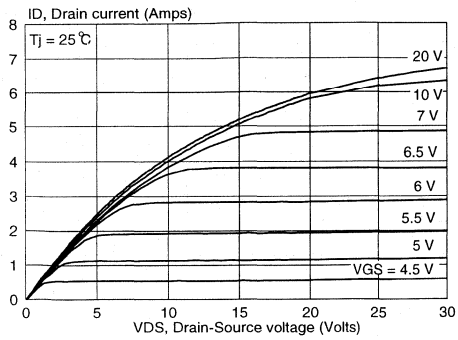


Fig.5. Typical output characteristics.
$I_D = f(V_{DS})$; parameter V_{GS}

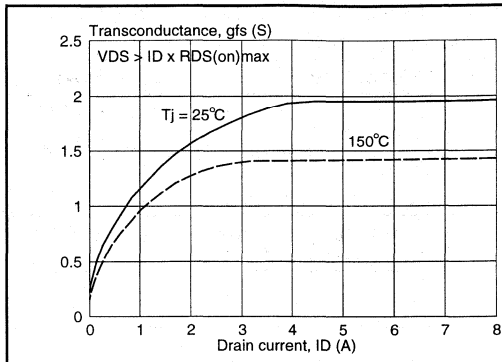


Fig.8. Typical transconductance.
$g_{fs} = f(I_D)$; parameter T_j

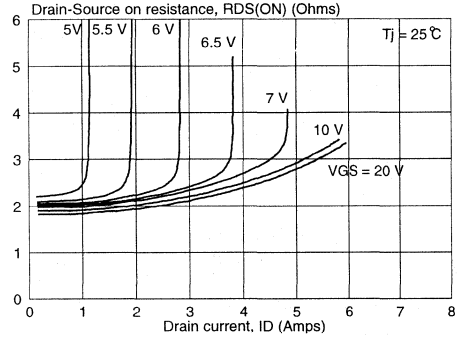


Fig.6. Typical on-state resistance.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

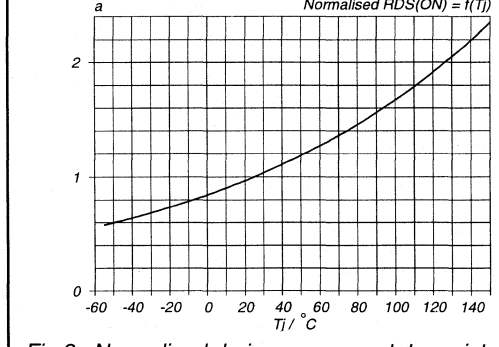


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 1.25 A; V_{GS} = 10 V

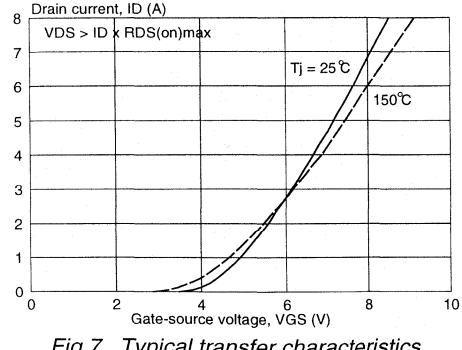


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

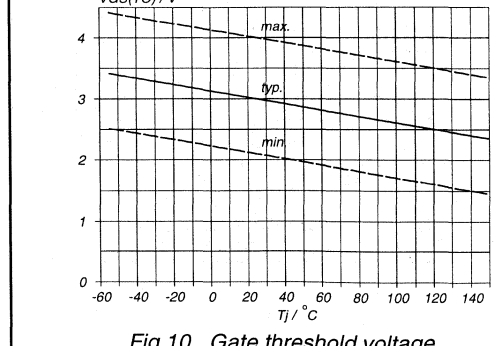


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

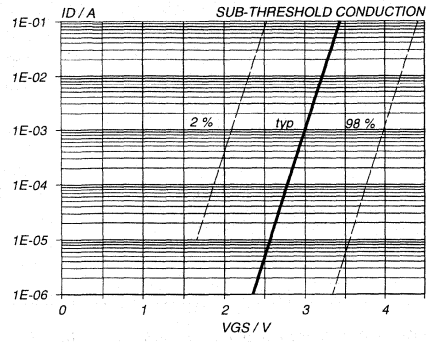


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

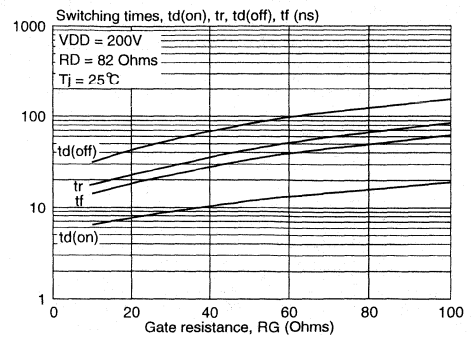


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

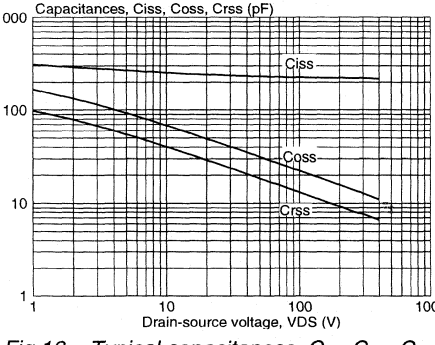


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

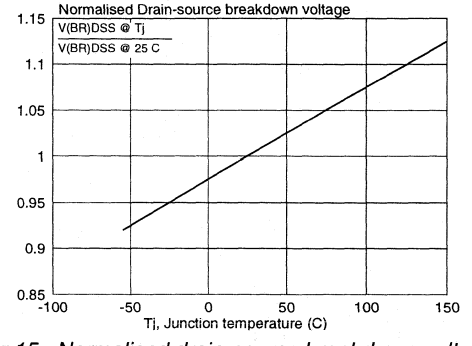


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

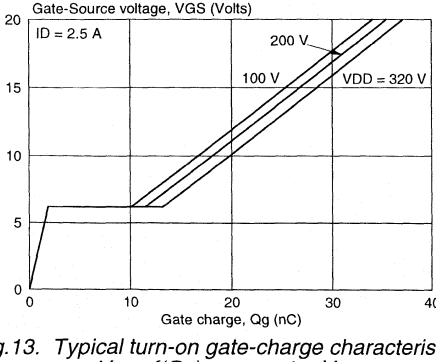


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

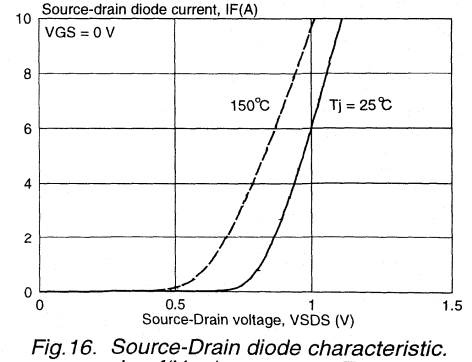


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

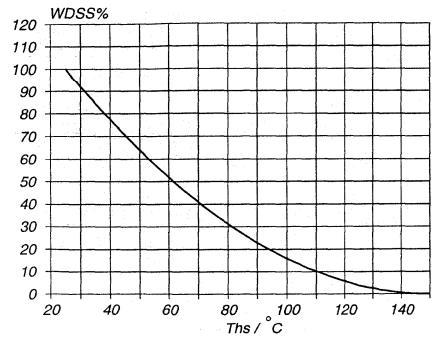


Fig.17. Normalised non-repetitive avalanche energy rating.
$E_{AS}\% = f(T_{hs})$

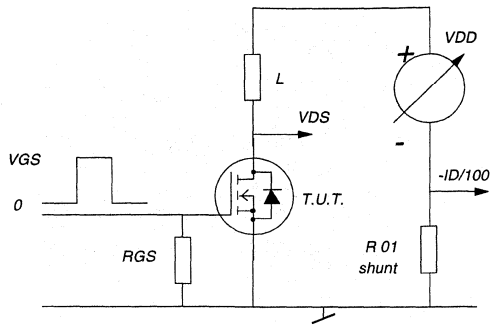


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot \frac{V_{(BR)DSS}}{(V_{(BR)DSS} - V_{DD})}$$

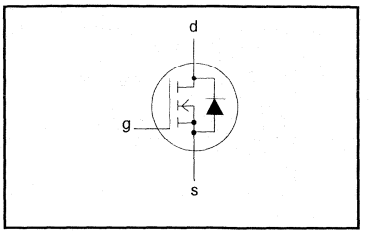
PowerMOS transistors
Avalanche energy rated

PHX3N50E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Isolated package

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 500 V

I_D = 2.1 A

$R_{DS(ON)} \leq 3\ \Omega$

GENERAL DESCRIPTION

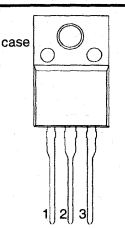
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHX3N50E is supplied in the SOT186A full pack, isolated package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

SOT186A



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	500	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	500	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{hs} = 25 °C; V_{GS} = 10 V	-	2.1	A
		T_{hs} = 100 °C; V_{GS} = 10 V	-	1.3	A
I_{DM}	Pulsed drain current	T_{hs} = 25 °C	-	14	A
P_D	Total dissipation	T_{hs} = 25 °C	-	30	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 2.5 A; $V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	210	mJ
E_{AR}	Repetitive avalanche energy[1]		-	5	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	2.5	A

[1] pulse width and repetition rate limited by T_j max.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	4.1	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	500	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 1.7 A	-	2.5	3	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 1.7 A	1	2	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 500 V; V_{GS} = 0 V	-	1	25	µA
		V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 °C	-	30	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 3.4 A; V_{DD} = 400 V; V_{GS} = 10 V	-	26	30	nC
Q_{gs}	Gate-source charge		-	2	3	nC
Q_{gd}	Gate-drain (Miller) charge		-	13	17	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 250 V; R_D = 68 Ω;	-	10	-	ns
t_r	Turn-on rise time	R_G = 18 Ω	-	29	-	ns
$t_{d(off)}$	Turn-off delay time		-	66	-	ns
t_f	Turn-off fall time		-	32	-	ns
L_d	Internal drain inductance	Measured from drain lead to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	310	-	pF
C_{oss}	Output capacitance		-	50	-	pF
C_{rss}	Feedback capacitance		-	28	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{hs} = 25°C	-	-	3.4	A
I_{SM}	Pulsed source current (body diode)	T_{hs} = 25°C	-	-	14	A
V_{SD}	Diode forward voltage	I_S = 3.4 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 3.4 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	370	-	ns
Q_{rr}	Reverse recovery charge		-	2.7	-	µC

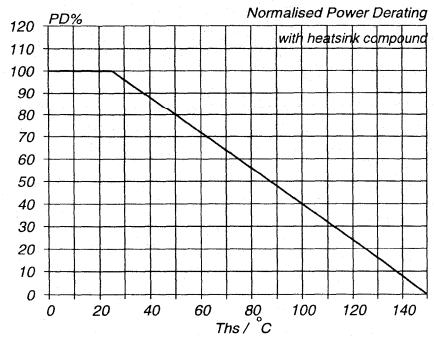


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{hs})

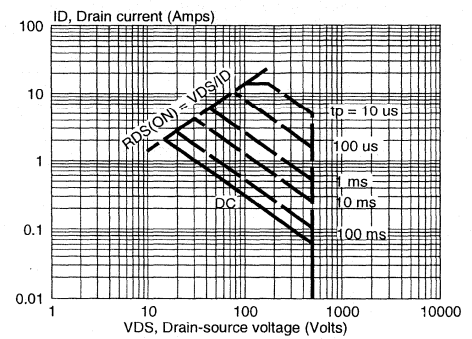


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

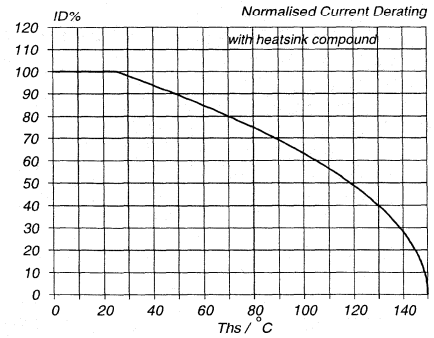


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{hs}); conditions: V_{GS} ≥ 10 V

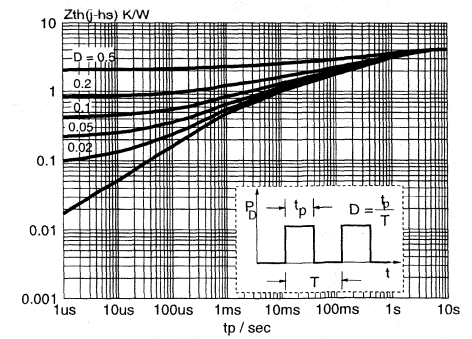


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}hs}$ = f(t); parameter D = t_p/T

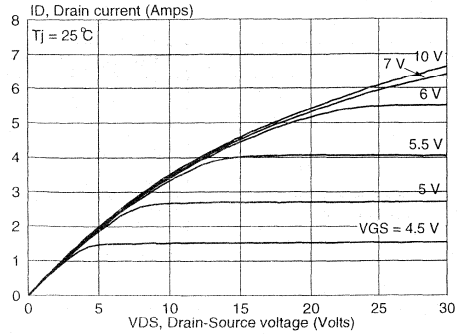


Fig.5. Typical output characteristics.
$I_D = f(V_{DS})$; parameter V_{GS}

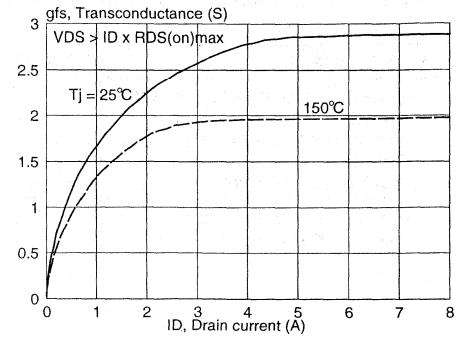


Fig.8. Typical transconductance.
$g_{fs} = f(I_D)$; parameter T_j

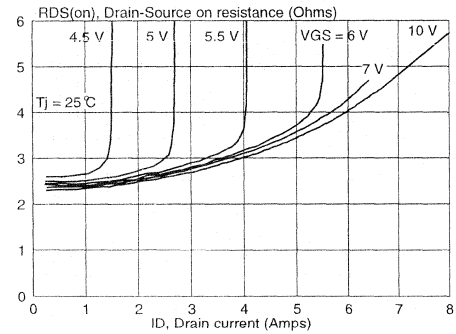


Fig.6. Typical on-state resistance.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

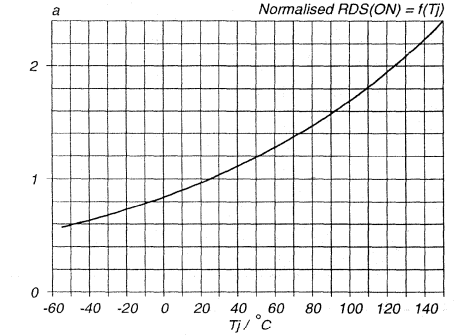


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 1.7 A; V_{GS} = 10 V

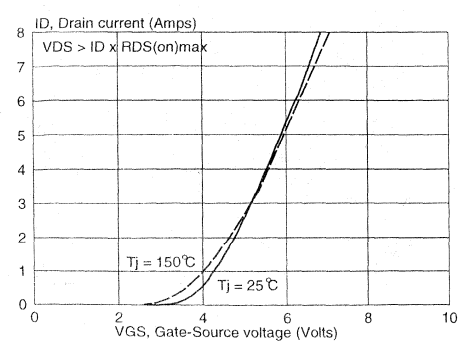


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

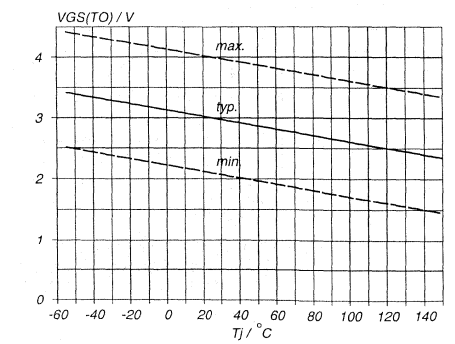


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

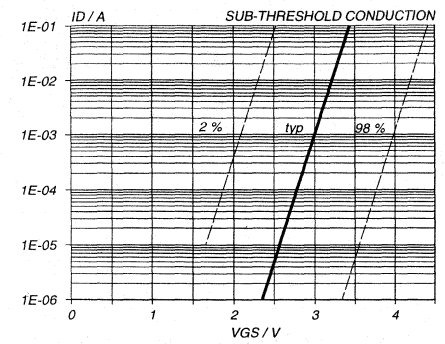


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

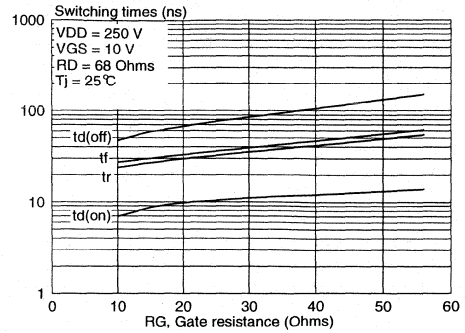


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

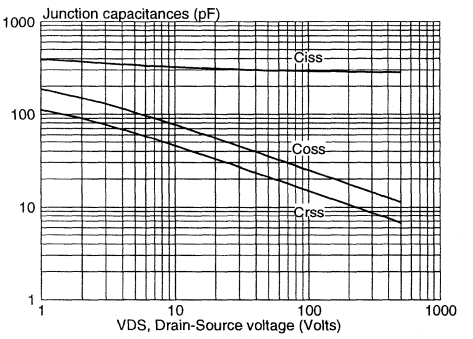


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

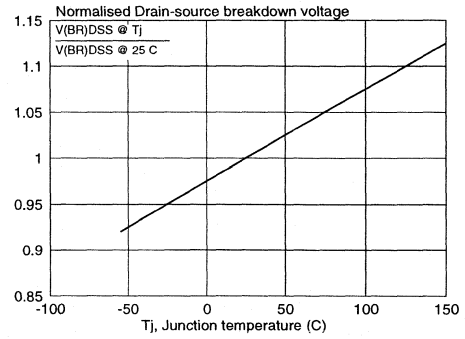


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

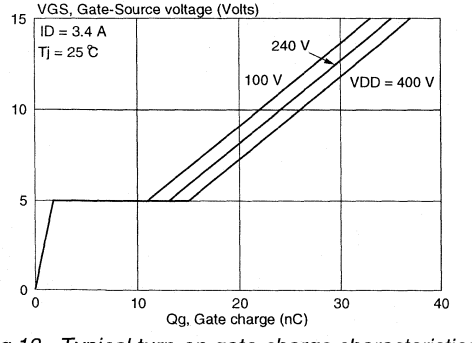


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

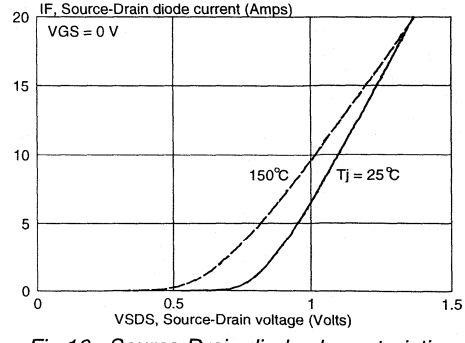


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

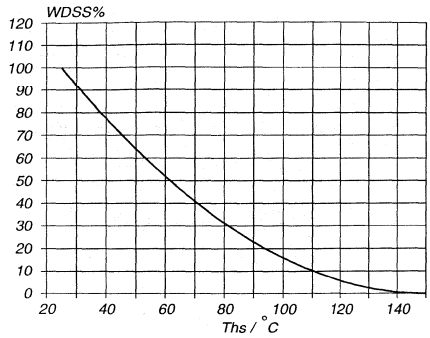


Fig.17. Normalised non-repetitive avalanche energy rating.
$E_{AS}\% = f(T_{hs})$

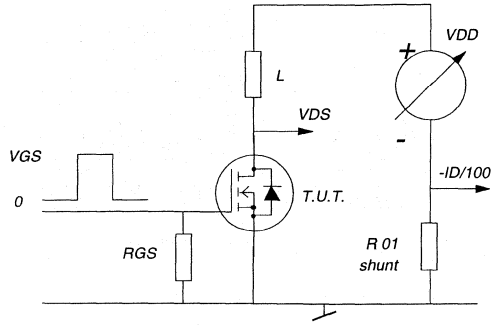


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot \frac{V_{(BR)DSS}}{(V_{(BR)DSS} - V_{DD})}$$

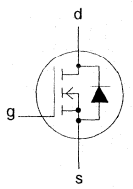
PowerMOS transistors Avalanche energy rated

PHX3N60E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Isolated package

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 600 V

I_D = 1.7 A

$R_{DS(ON)} \leq 4.4\ \Omega$

GENERAL DESCRIPTION

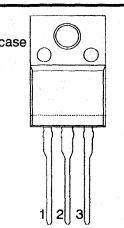
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHX3N60E is supplied in the SOT186A full pack, isolated package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

SOT186A



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	600	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	600	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{hs} = 25 °C; V_{GS} = 10 V	-	1.7	A
		T_{hs} = 100 °C; V_{GS} = 10 V	-	1.1	A
I_{DM}	Pulsed drain current	T_{hs} = 25 °C	-	11	A
P_D	Total dissipation	T_{hs} = 25 °C	-	30	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 2.2 A; $V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	171	mJ
E_{AR}	Repetitive avalanche energy[1]		-	5	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	2.2	A

[1] pulse width and repetition rate limited by T_j max.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	4.1	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	600	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 1.4 A	-	4	4.4	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 1.4 A	0.7	1.7	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 600 V; V_{GS} = 0 V	-	1	100	µA
		V_{DS} = 480 V; V_{GS} = 0 V; T_j = 125 °C	-	50	500	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 2.8 A; V_{DD} = 480 V; V_{GS} = 10 V	-	25	30	nC
Q_{gs}	Gate-source charge		-	2	3	nC
Q_{gd}	Gate-drain (Miller) charge		-	12	15	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V; R_D = 100 Ω;	-	10	-	ns
t_r	Turn-on rise time	R_G = 18 Ω	-	26	-	ns
$t_{d(off)}$	Turn-off delay time		-	66	-	ns
t_f	Turn-off fall time		-	30	-	ns
L_d	Internal drain inductance	Measured from drain lead to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	300	-	pF
C_{oss}	Output capacitance		-	43	-	pF
C_{rss}	Feedback capacitance		-	25	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{hs} = 25°C	-	-	2.8	A
I_{SM}	Pulsed source current (body diode)	T_{hs} = 25°C	-	-	11	A
V_{SD}	Diode forward voltage	I_S = 2.8 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 2.8 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	500	-	ns
Q_{rr}	Reverse recovery charge		-	3	-	µC

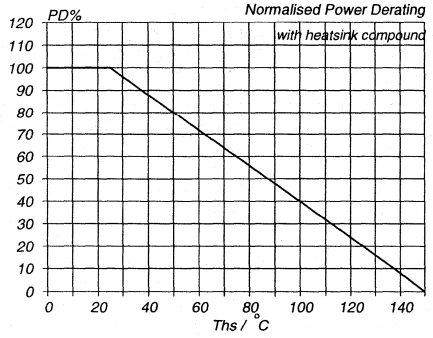


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{hs})

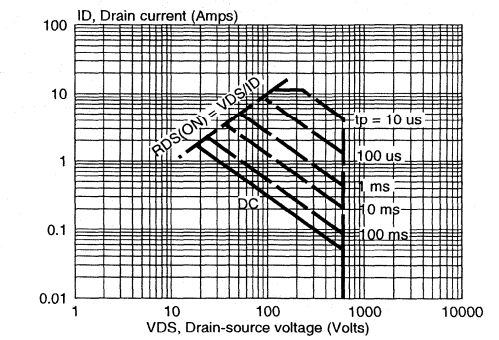


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

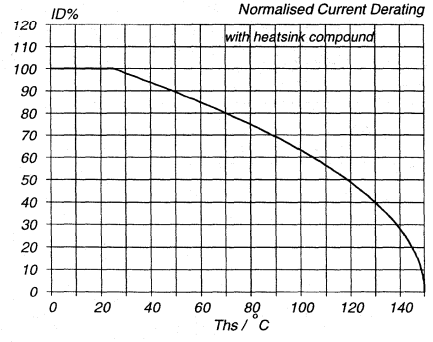


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{hs}); conditions: V_{GS} ≥ 10 V

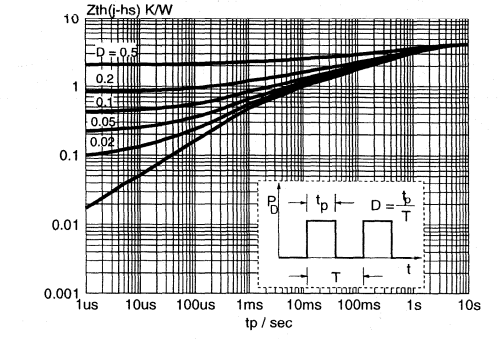


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}hs}$ = f(t); parameter D = t_p/T

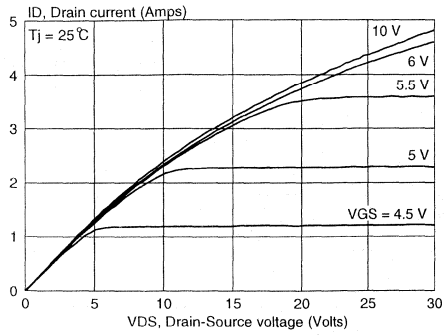


Fig.5. Typical output characteristics.
$I_D = f(V_{DS})$; parameter V_{GS}

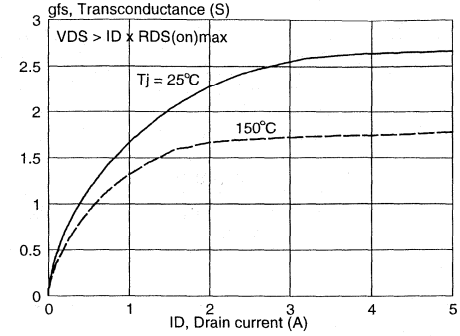


Fig.8. Typical transconductance.
$g_{fs} = f(I_D)$; parameter T_j

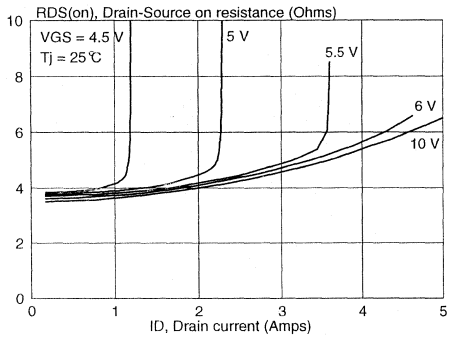


Fig.6. Typical on-state resistance.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

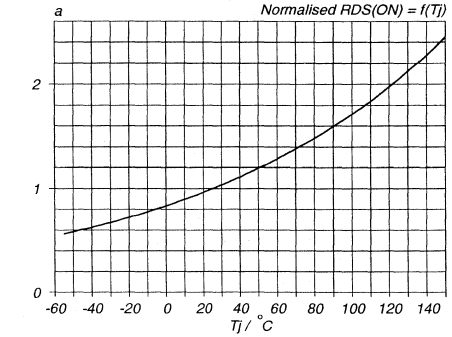


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 1.4 A; V_{GS} = 10 V

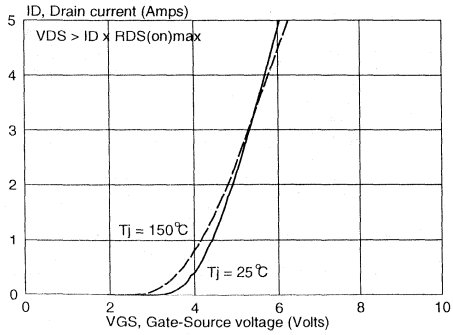


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

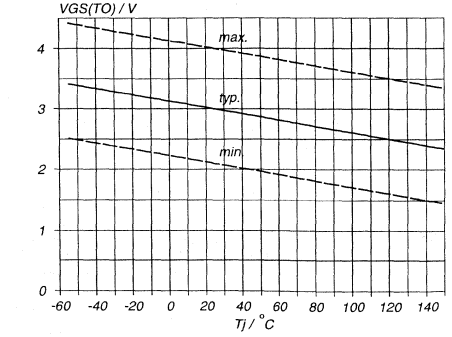


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

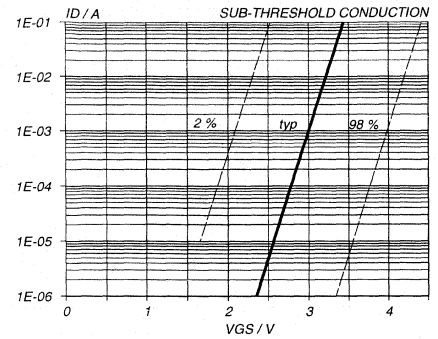


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

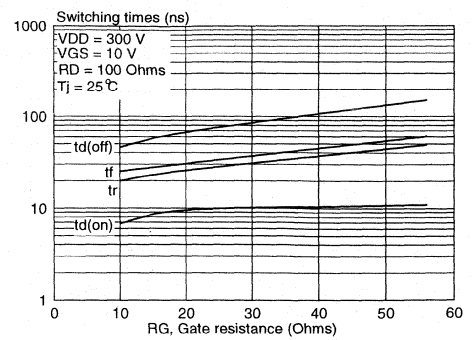


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

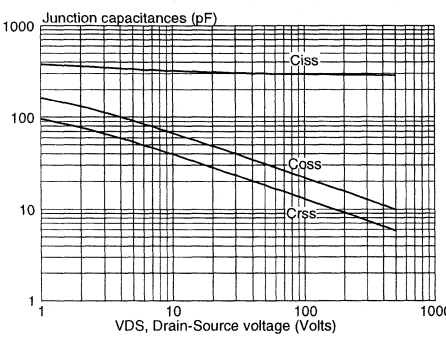


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

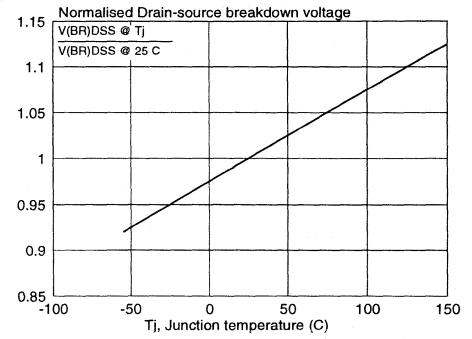


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

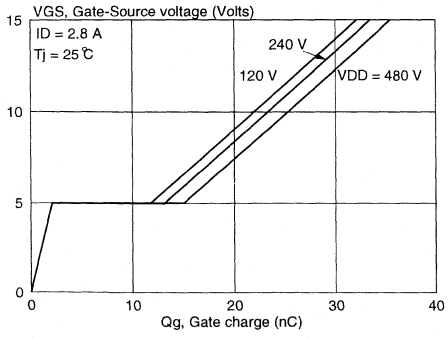


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

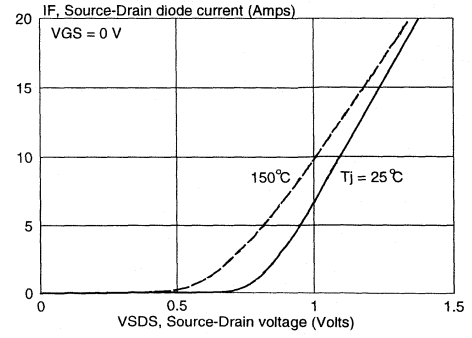


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

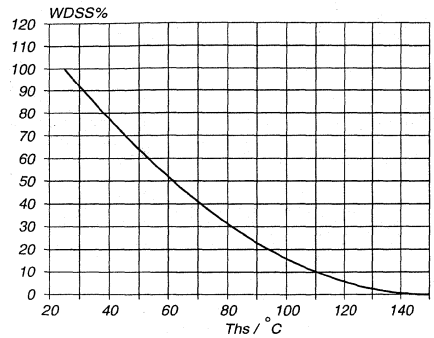


Fig.17. Normalised non-repetitive avalanche energy rating.
$E_{AS}\% = f(T_{hs})$

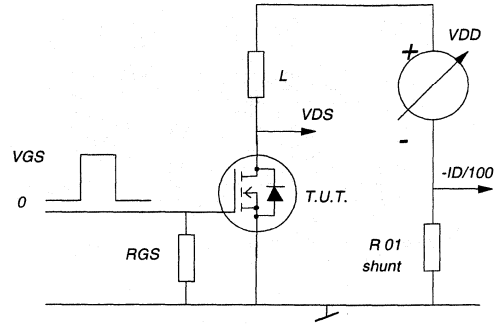


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot \frac{V_{(BR)DSS}}{(V_{(BR)DSS} - V_{DD})}$$

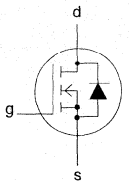
PowerMOS transistors
Avalanche energy rated

PHX4N40E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Isolated package

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 400 V

I_D = 2.7 A

$R_{DS(ON)} \leq 1.8\ \Omega$

GENERAL DESCRIPTION

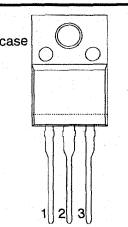
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHX4N40E is supplied in the SOT186A full pack isolated package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

SOT186A



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	400	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	400	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{hs} = 25 °C; V_{GS} = 10 V	-	2.7	A
		T_{hs} = 100 °C; V_{GS} = 10 V	-	1.7	A
I_{DM}	Pulsed drain current	T_{hs} = 25 °C	-	18	A
P_D	Total dissipation	T_{hs} = 25 °C	-	30	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 3.3 A; $V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	190	mJ
E_{AR}	Repetitive avalanche energy[1]		-	5	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	3.3	A

1 pulse width and repetition rate limited by T_j max.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	4.1	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	400	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 2.2 A	-	1.3	1.8	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 2.2 A	1.3	2.2	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 400 V; V_{GS} = 0 V	-	1	25	µA
		V_{DS} = 320 V; V_{GS} = 0 V; T_j = 125 °C	-	30	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 4.4 A; V_{DD} = 320 V; V_{GS} = 10 V	-	26	30	nC
Q_{gs}	Gate-source charge		-	2	4	nC
Q_{gd}	Gate-drain (Miller) charge		-	14	17	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 200 V; R_D = 47 Ω;	-	10	-	ns
t_r	Turn-on rise time	R_G = 18 Ω	-	30	-	ns
$t_{d(off)}$	Turn-off delay time		-	55	-	ns
t_f	Turn-off fall time		-	38	-	ns
L_d	Internal drain inductance	Measured from drain lead to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	310	-	pF
C_{oss}	Output capacitance		-	60	-	pF
C_{rss}	Feedback capacitance		-	36	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{hs} = 25°C	-	-	4.4	A
I_{SM}	Pulsed source current (body diode)	T_{hs} = 25°C	-	-	18	A
V_{SD}	Diode forward voltage	I_S = 4.4 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 4.4 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	250	-	ns
Q_{rr}	Reverse recovery charge		-	2.2	-	µC

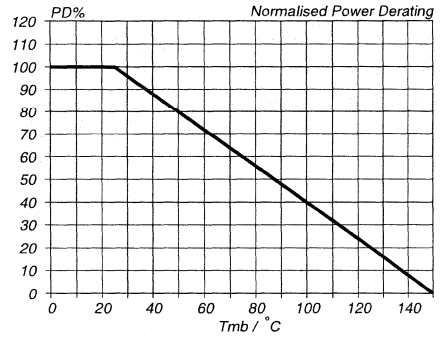


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

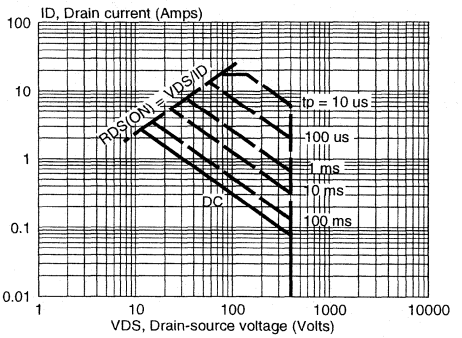


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

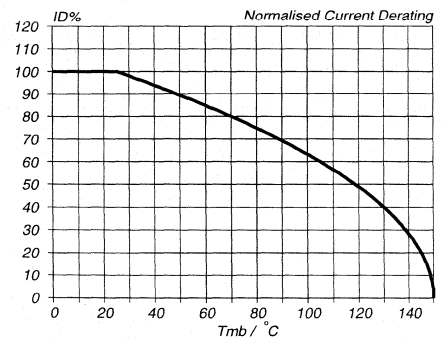


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 10 V

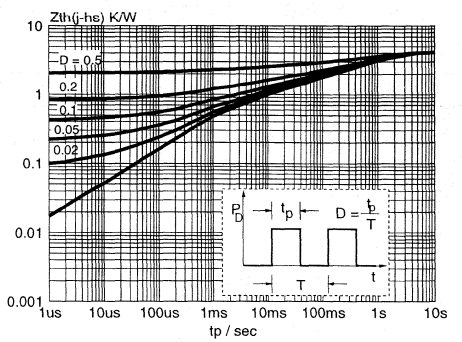


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}hs}$ = f(t); parameter D = t_p/T

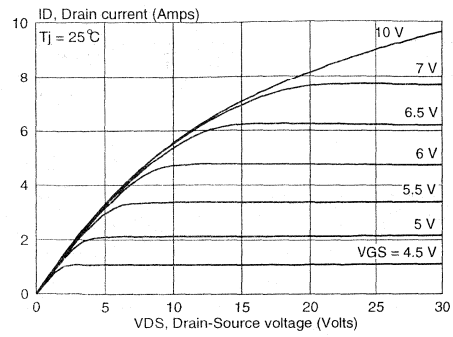


Fig.5. Typical output characteristics.
$I_D = f(V_{DS})$; parameter V_{GS}

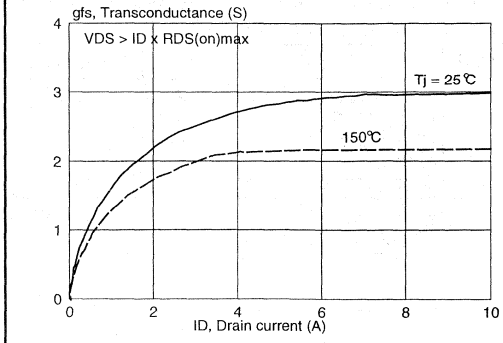


Fig.8. Typical transconductance.
$g_{fs} = f(I_D)$; parameter T_j

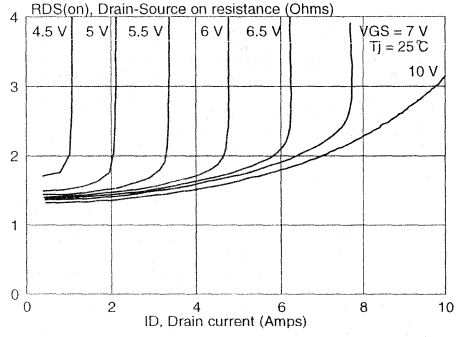


Fig.6. Typical on-state resistance.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

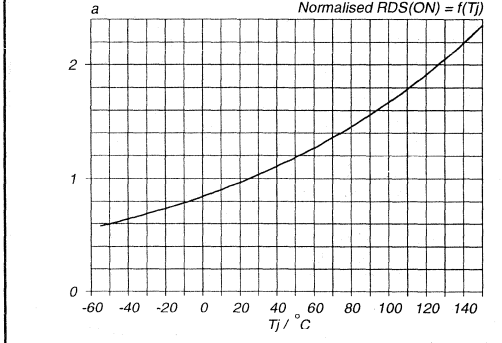


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 2.2 A; V_{GS} = 10 V

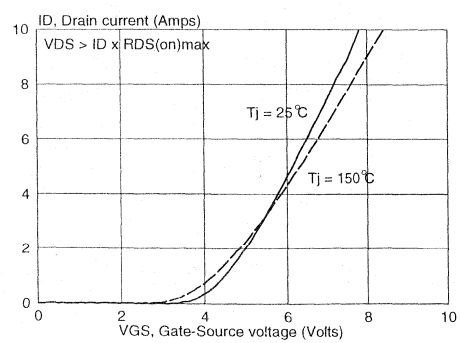


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

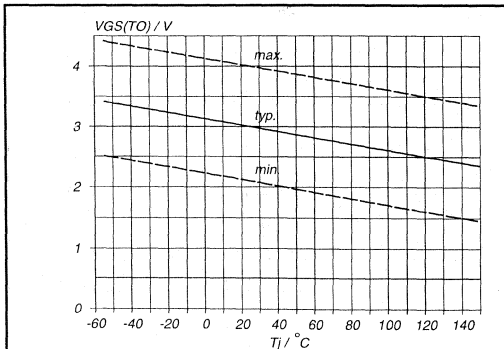


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

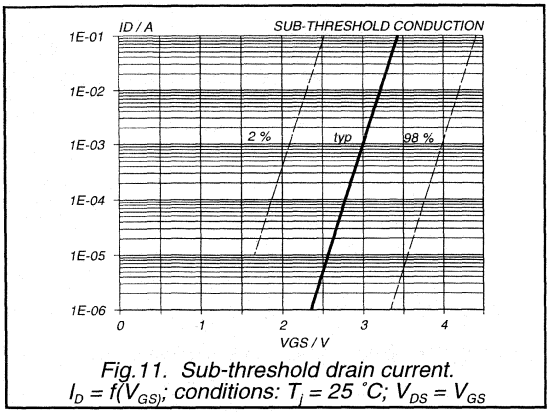


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

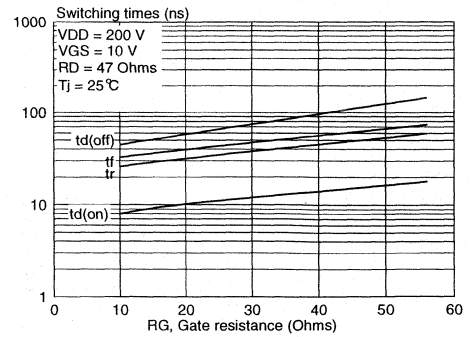


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

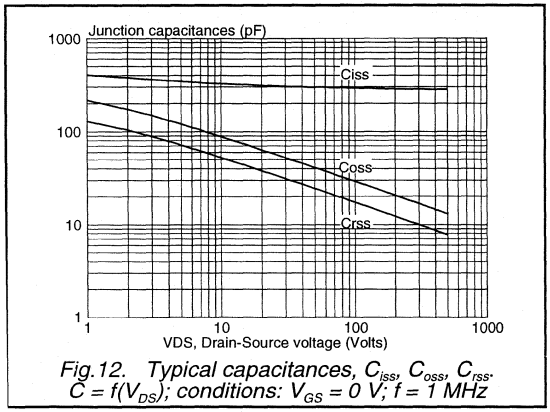


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

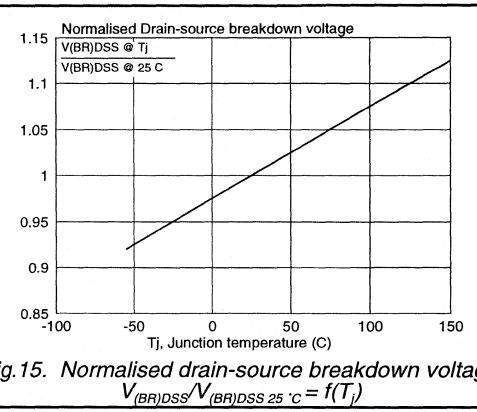


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

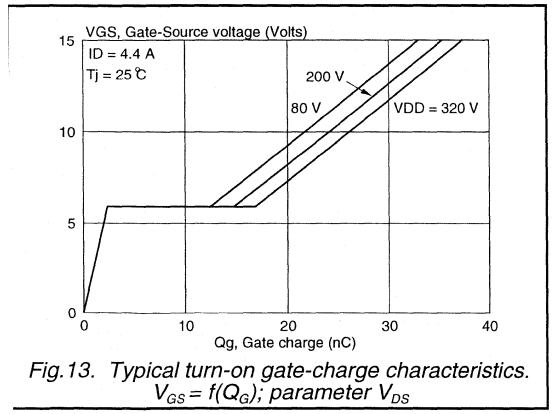


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

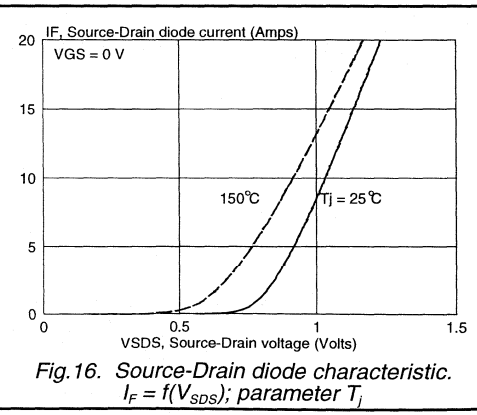


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

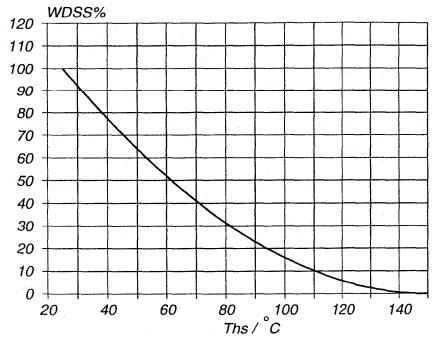


Fig.17. Normalised non-repetitive avalanche energy rating.
$E_{AS}\% = f(T_{hs})$

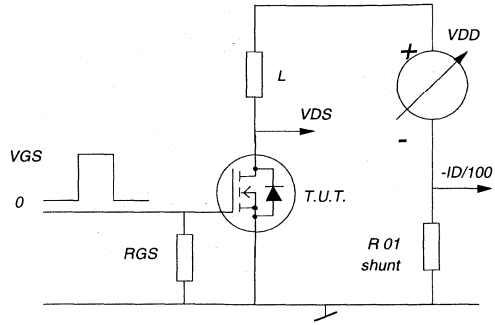


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot \frac{V_{(BR)DSS}}{(V_{(BR)DSS} - V_{DD})}$$

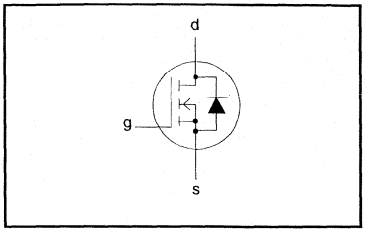
PowerMOS transistors Avalanche energy rated

PHX4N60E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Isolated package

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 600 V

I_D = 2.4 A

$R_{DS(ON)} \leq 2.5\ \Omega$

GENERAL DESCRIPTION

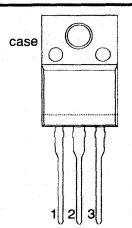
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHX4N60E is supplied in the SOT186A full pack, isolated package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

SOT186A



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	600	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	600	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{hs} = 25 °C; V_{GS} = 10 V	-	2.4	A
		T_{hs} = 100 °C; V_{GS} = 10 V	-	1.5	A
I_{DM}	Pulsed drain current	T_{hs} = 25 °C	-	18	A
P_D	Total dissipation	T_{hs} = 25 °C	-	35	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 3.6 A; $V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	290	mJ
E_{AR}	Repetitive avalanche energy[1]		-	7.4	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	3.6	A

pulse width and repetition rate limited by T_j max.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	3.6	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	600	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 2.25 A	-	2.1	2.5	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 2.25 A	2	3.4	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 600 V; V_{GS} = 0 V	-	2	100	µA
		V_{DS} = 480 V; V_{GS} = 0 V; T_j = 125 °C	-	50	500	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 4.5 A; V_{DD} = 480 V; V_{GS} = 10 V	-	48	60	nC
Q_{gs}	Gate-source charge		-	4	6	nC
Q_{gd}	Gate-drain (Miller) charge		-	24	30	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V; R_D = 68 Ω;	-	12	-	ns
t_r	Turn-on rise time	R_G = 12 Ω	-	33	-	ns
$t_{d(off)}$	Turn-off delay time		-	82	-	ns
t_f	Turn-off fall time		-	36	-	ns
L_d	Internal drain inductance	Measured from drain lead to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	600	-	pF
C_{oss}	Output capacitance		-	80	-	pF
C_{rss}	Feedback capacitance		-	46	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{hs} = 25°C	-	-	4.5	A
I_{SM}	Pulsed source current (body diode)	T_{hs} = 25°C	-	-	18	A
V_{SD}	Diode forward voltage	I_S = 4.5 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 4.5 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	480	-	ns
Q_{rr}	Reverse recovery charge		-	4	-	µC

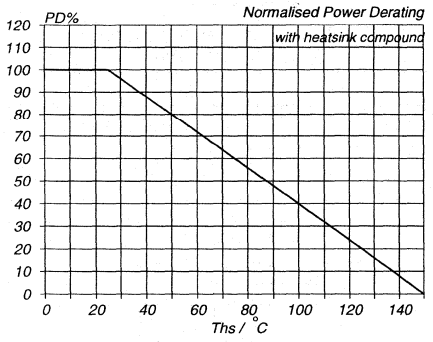


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{hs})

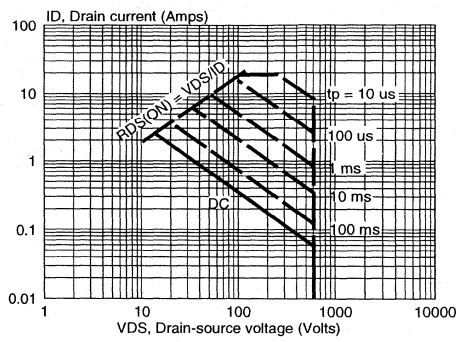


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

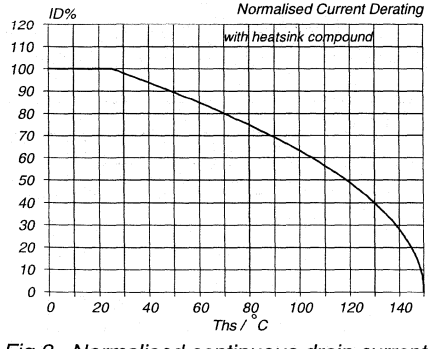


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{hs}); conditions: V_{GS} ≥ 10 V

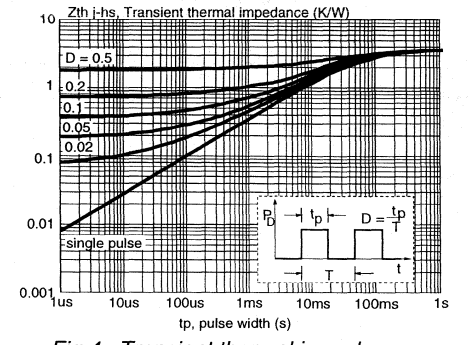


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}hs}$ = f(t); parameter D = t_p/T

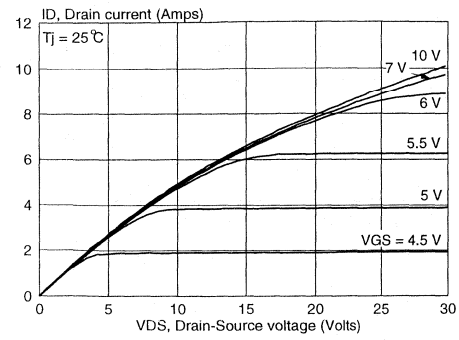


Fig.5. Typical output characteristics.
$I_D = f(V_{DS})$; parameter V_{GS}

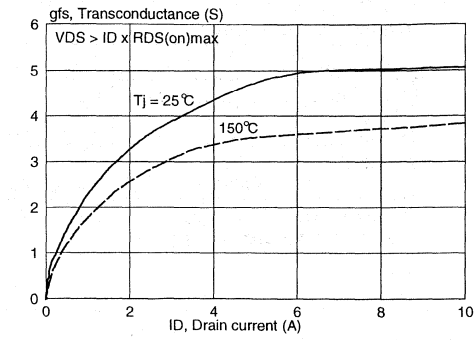


Fig.8. Typical transconductance.
$g_{fs} = f(I_D)$; parameter T_j

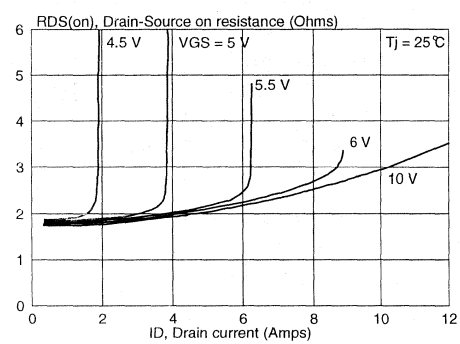


Fig.6. Typical on-state resistance.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

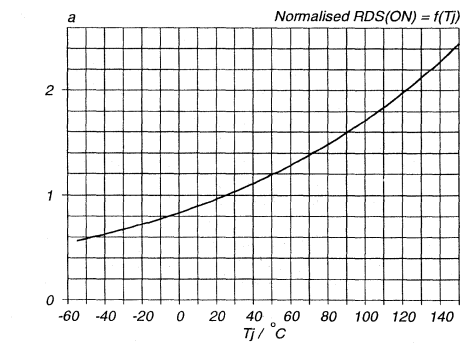


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 2.25 A; V_{GS} = 10 V

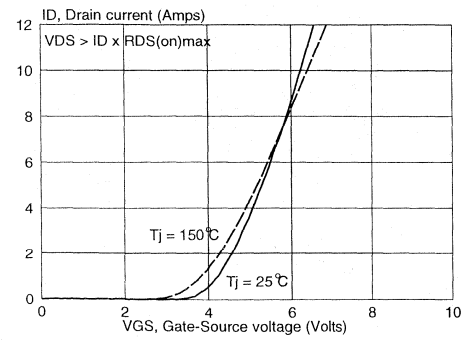


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

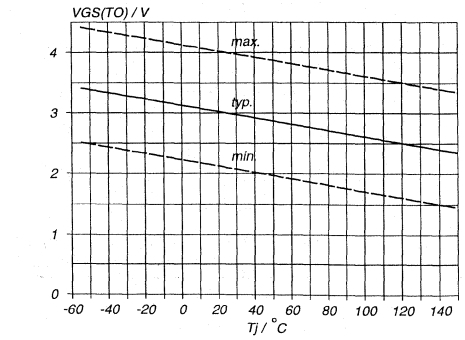


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

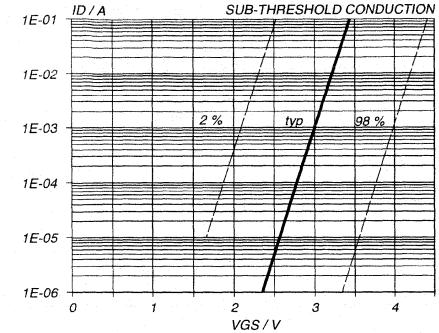


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

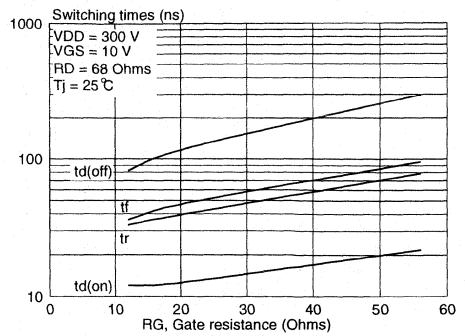


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

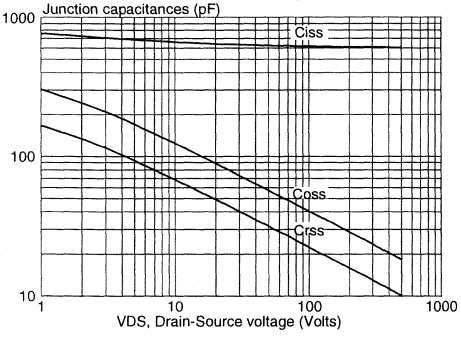


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

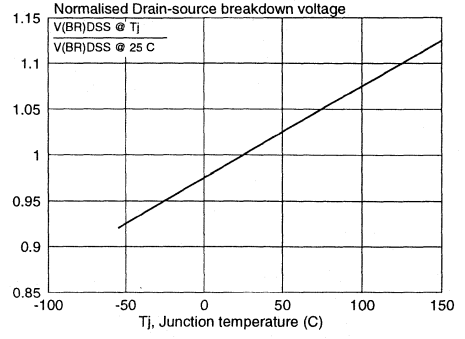


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

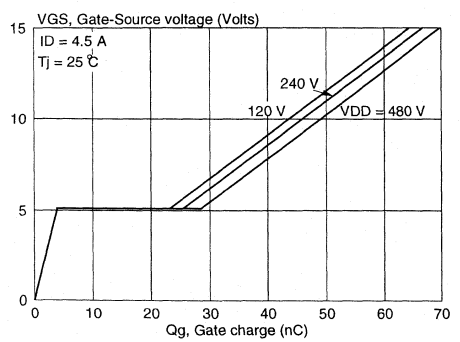


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

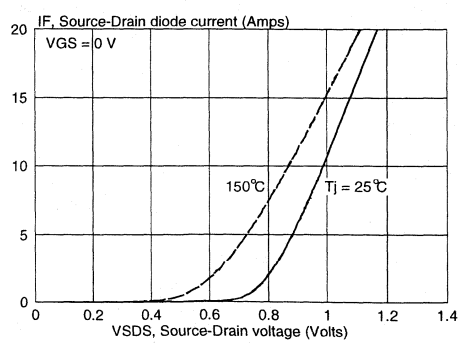


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

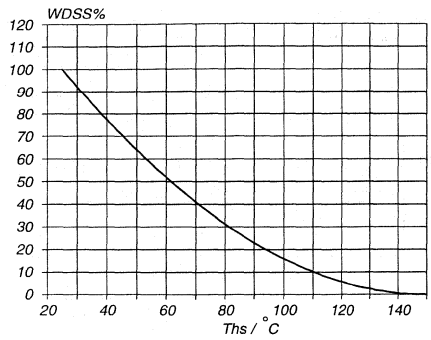


Fig.17. Normalised non-repetitive avalanche energy rating.
$E_{AS}\% = f(T_{hs})$

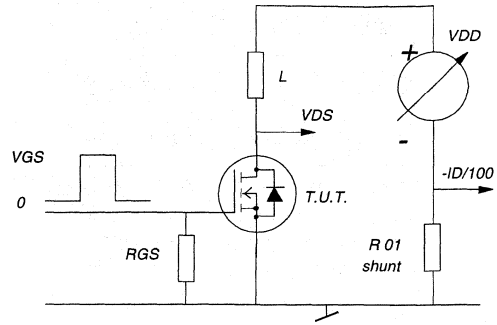


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot \frac{V_{(BR)DSS}}{(V_{(BR)DSS} - V_{DD})}$$

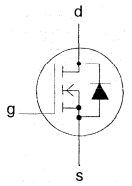
PowerMOS transistors FREDFET, Avalanche energy rated

PHX4ND40E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Isolated package
- Fast reverse recovery diode

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 400 V

I_D = 2.7 A

$R_{DS(ON)} \leq 1.8\ \Omega$

t_{rr} = 180 ns

GENERAL DESCRIPTION

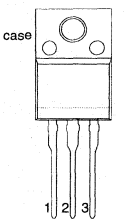
N-channel, enhancement mode field-effect power transistor, incorporating a **F**ast **R**ecovery **E**pitaxial **D**iode (FRED). This gives improved switching performance in half bridge and full bridge converters making this device particularly suitable for inverters, lighting ballasts and motor control circuits.

The PHX4ND40E is supplied in the SOT186A full pack isolated package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

SOT186A



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	400	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	400	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{hs} = 25 °C; V_{GS} = 10 V	-	2.7	A
		T_{hs} = 100 °C; V_{GS} = 10 V	-	1.7	A
I_{DM}	Pulsed drain current[1]	T_{hs} = 25 °C	-	18	A
P_D	Total dissipation	T_{hs} = 25 °C	-	30	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 3.3 A; $V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	190	mJ
E_{AR}	Repetitive avalanche energy[1]		-	5	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	3.3	A

[1] pulse width and repetition rate limited by T_j max.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	4.1	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	400	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 2.2 A	-	1.3	1.8	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 2.2 A	1.3	2.2	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 400 V; V_{GS} = 0 V	-	1	25	µA
		V_{DS} = 320 V; V_{GS} = 0 V; T_j = 125 °C	-	30	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 4.4 A; V_{DD} = 320 V; V_{GS} = 10 V	-	26	30	nC
Q_{gs}	Gate-source charge		-	2	4	nC
Q_{gd}	Gate-drain (Miller) charge		-	14	17	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 200 V; R_D = 47 Ω;	-	10	-	ns
t_r	Turn-on rise time	R_G = 18 Ω	-	30	-	ns
$t_{d(off)}$	Turn-off delay time		-	55	-	ns
t_f	Turn-off fall time		-	38	-	ns
L_d	Internal drain inductance	Measured from drain lead to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	310	-	pF
C_{oss}	Output capacitance		-	60	-	pF
C_{rss}	Feedback capacitance		-	36	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{hs} = 25°C	-	-	4.4	A
I_{SM}	Pulsed source current (body diode)	T_{hs} = 25°C	-	-	18	A
V_{SD}	Diode forward voltage	I_S = 4.4 A; V_{GS} = 0 V	-	-	1.5	V
t_{rr}	Reverse recovery time	I_S = 4.4 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	180	-	ns
		I_S = 4.4 A; V_{GS} = 0 V; dI/dt = 100 A/µs; 125°C	-	220	-	ns
Q_{rr}	Reverse recovery charge	I_S = 4.4 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	0.65	-	µC
		I_S = 4.4 A; V_{GS} = 0 V; dI/dt = 100 A/µs; 125°C	-	2.6	-	µC
I_{rrm}	Peak reverse recovery current	I_S = 4.4 A; V_{GS} = 0 V; dI/dt = 100 A/µs; 125°C	-	15	-	A

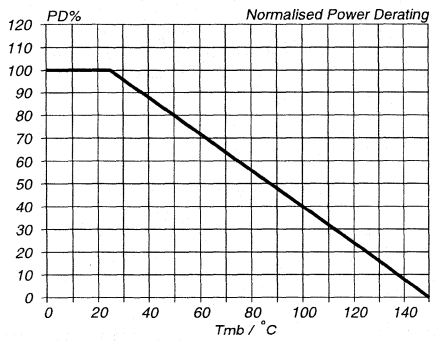


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

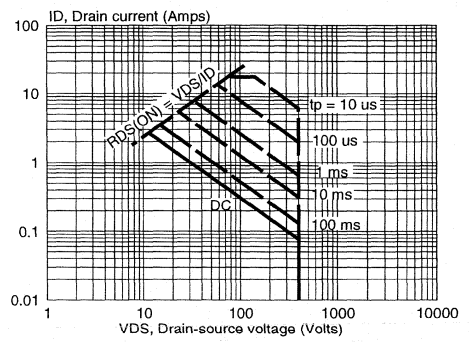


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

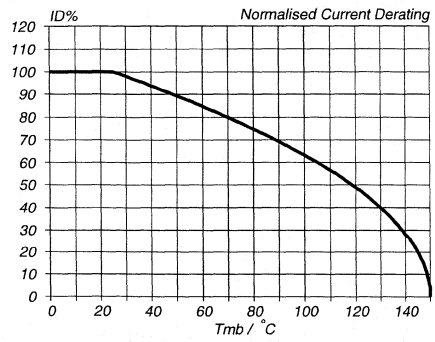


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

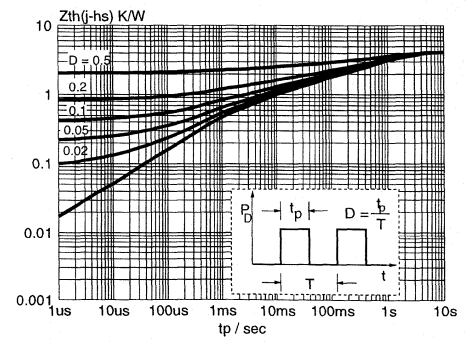


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}hs}$ = f(t); parameter D = t_p/T

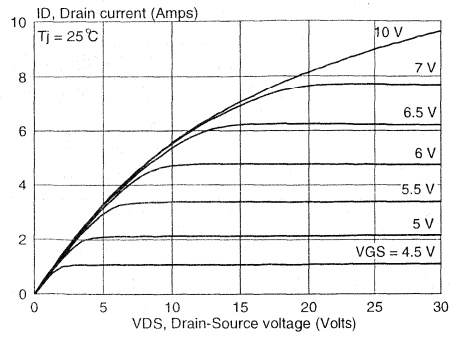


Fig.5. Typical output characteristics.
$I_D = f(V_{DS})$; parameter V_{GS}

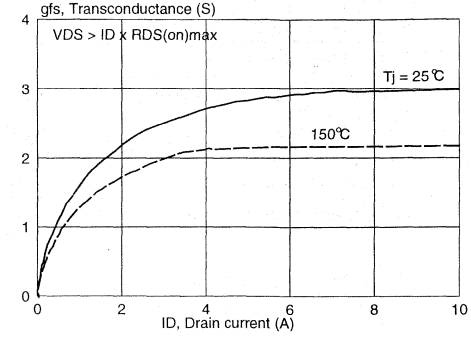


Fig.8. Typical transconductance.
$g_{fs} = f(I_D)$; parameter T_j

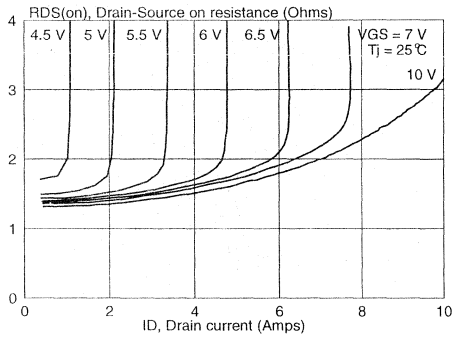


Fig.6. Typical on-state resistance.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

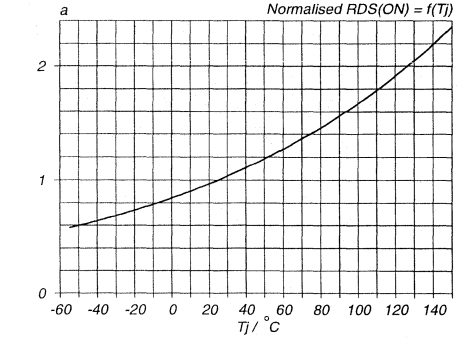


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 2.2$ A; $V_{GS} = 10$ V

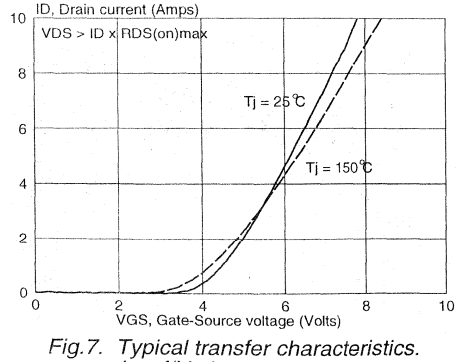


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

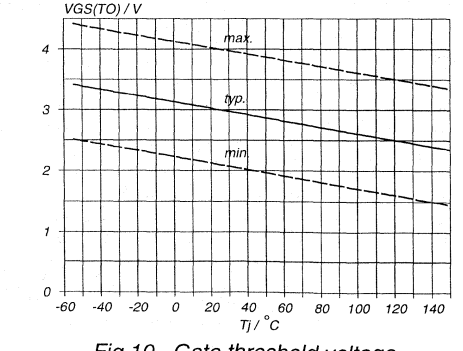


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 0.25$ mA; $V_{DS} = V_{GS}$

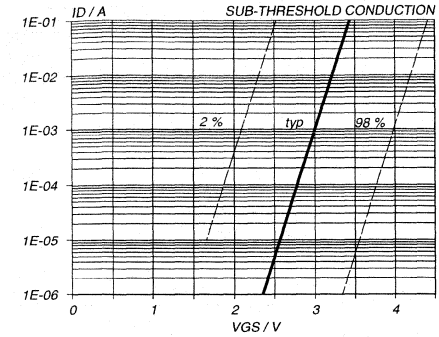


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

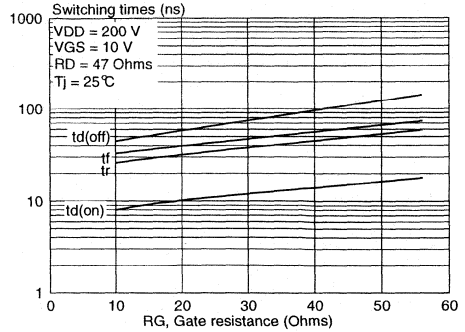


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

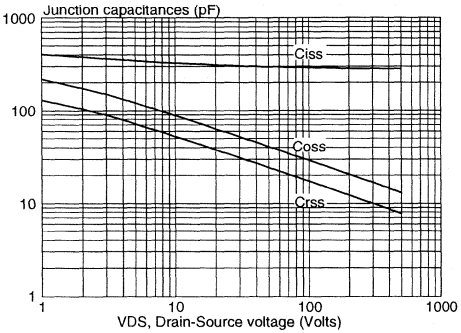


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

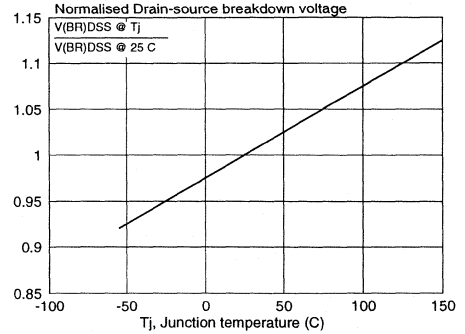


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

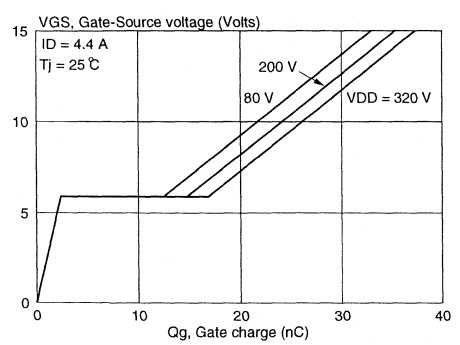


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

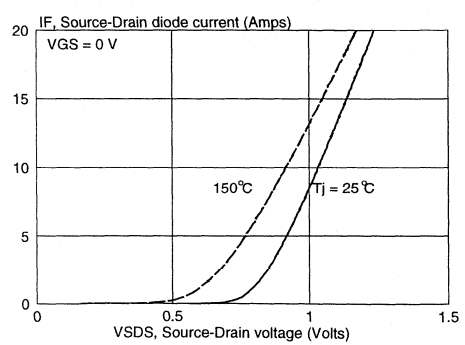


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

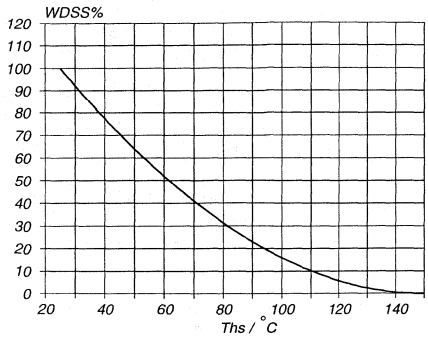


Fig.17. Normalised non-repetitive avalanche energy rating.
$E_{AS}\% = f(T_{hs})$

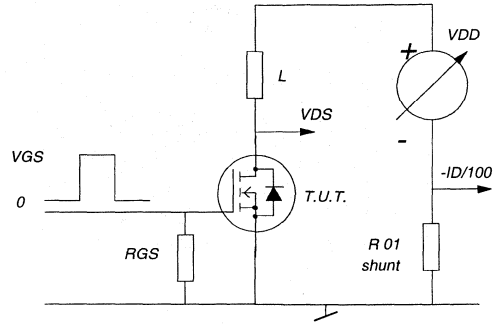


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot \frac{V_{(BR)DSS}}{(V_{(BR)DSS} - V_{DD})}$$

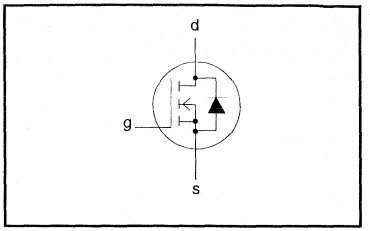
PowerMOS transistors Avalanche energy rated

PHX6N50E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Isolated package

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 500 V

I_D = 3.1 A

$R_{DS(ON)} \leq 1.5\ \Omega$

GENERAL DESCRIPTION

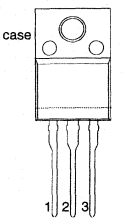
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHX6N50E is supplied in the SOT186A full pack, isolated package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

SOT186A



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	500	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	500	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{hs} = 25 °C; V_{GS} = 10 V	-	3.1	A
		T_{hs} = 100 °C; V_{GS} = 10 V	-	2	A
I_{DM}	Pulsed drain current	T_{hs} = 25 °C	-	24	A
P_D	Total dissipation	T_{hs} = 25 °C	-	35	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 4.5 A; $V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	280	mJ
E_{AR}	Repetitive avalanche energy[1]		-	7.4	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	4.5	A

[1] pulse width and repetition rate limited by T_j max.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	3.6	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	500	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 3 A	-	1.2	1.5	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 3 A	2	3.6	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 500 V; V_{GS} = 0 V	-	1	25	µA
		V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 °C	-	30	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 6 A; V_{DD} = 400 V; V_{GS} = 10 V	-	53	64	nC
Q_{gs}	Gate-source charge		-	4	6	nC
Q_{gd}	Gate-drain (Miller) charge		-	28	34	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 250 V; R_D = 39 Ω;	-	10	-	ns
t_r	Turn-on rise time	R_G = 12 Ω	-	33	-	ns
$t_{d(off)}$	Turn-off delay time		-	92	-	ns
t_f	Turn-off fall time		-	40	-	ns
L_d	Internal drain inductance	Measured from drain lead to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	610	-	pF
C_{oss}	Output capacitance		-	96	-	pF
C_{rss}	Feedback capacitance		-	54	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{hs} = 25°C	-	-	5.9	A
I_{SM}	Pulsed source current (body diode)	T_{hs} = 25°C	-	-	24	A
V_{SD}	Diode forward voltage	I_S = 6 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 6 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	390	-	ns
Q_{rr}	Reverse recovery charge		-	4	-	µC

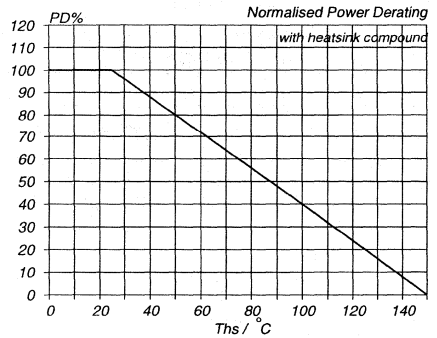


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{hs})

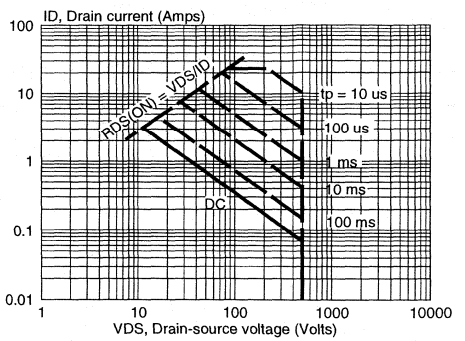


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

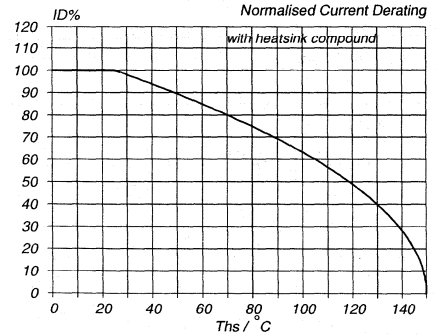


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{hs}); conditions: V_{GS} ≥ 10 V

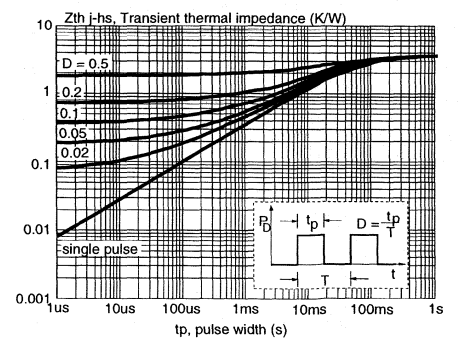


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}hs}$ = f(t); parameter D = t_p/T

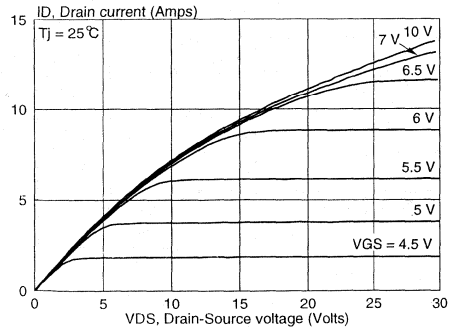


Fig.5. Typical output characteristics.
$I_D = f(V_{DS})$; parameter V_{GS}

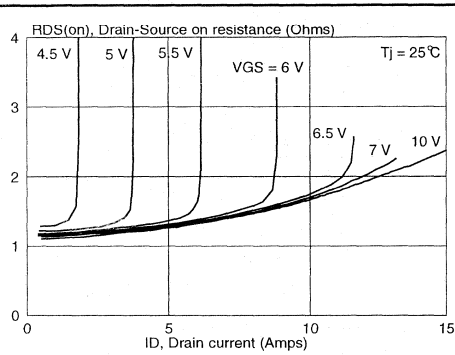


Fig.6. Typical on-state resistance.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

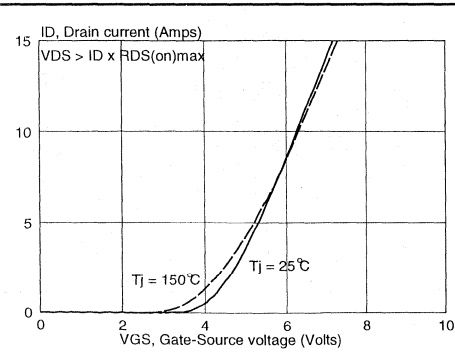


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

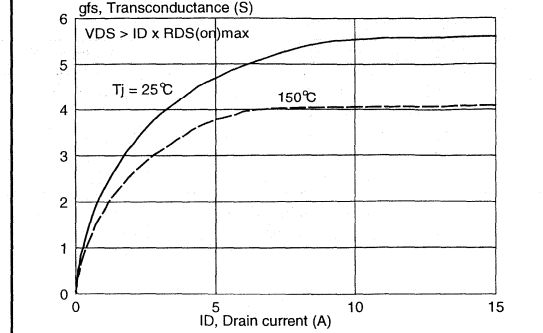


Fig.8. Typical transconductance.
$g_{fs} = f(I_D)$; parameter T_j

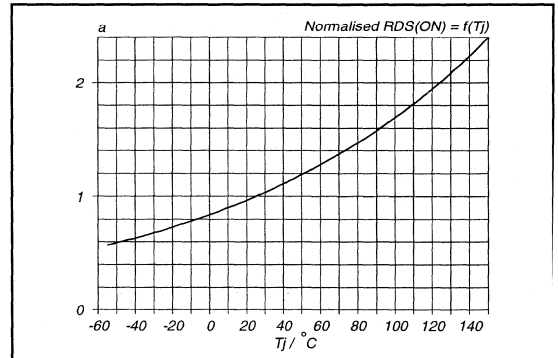


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 3 A; V_{GS} = 10 V

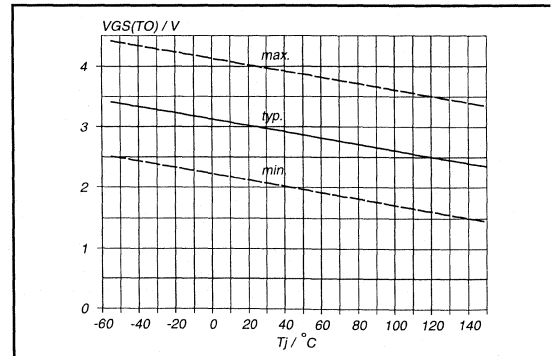


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

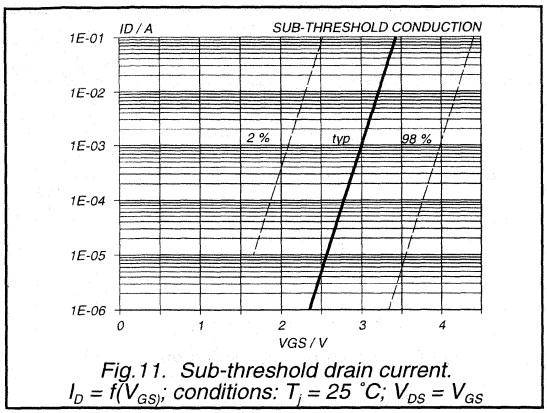


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

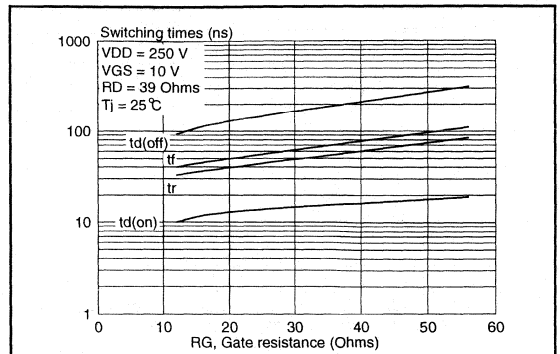


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

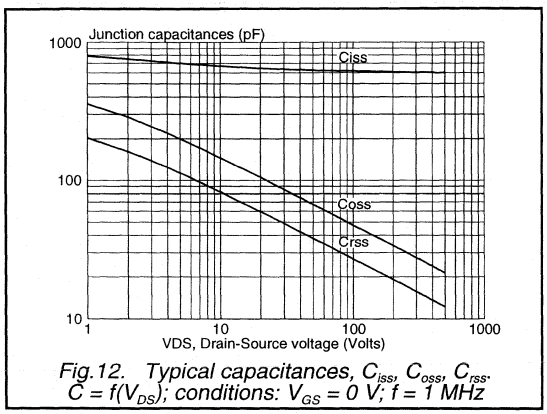


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

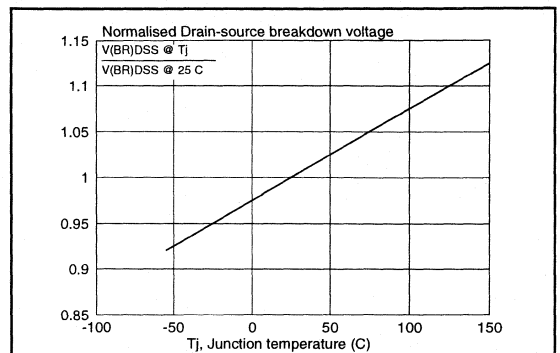


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

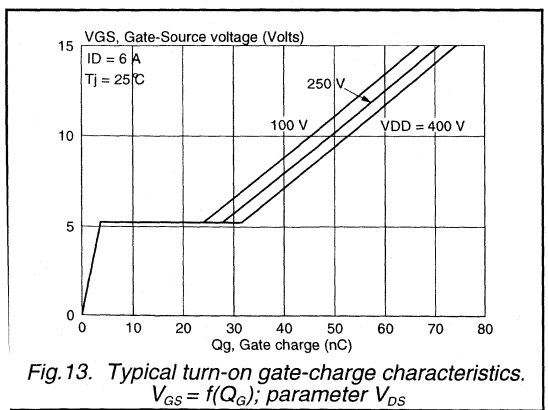


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

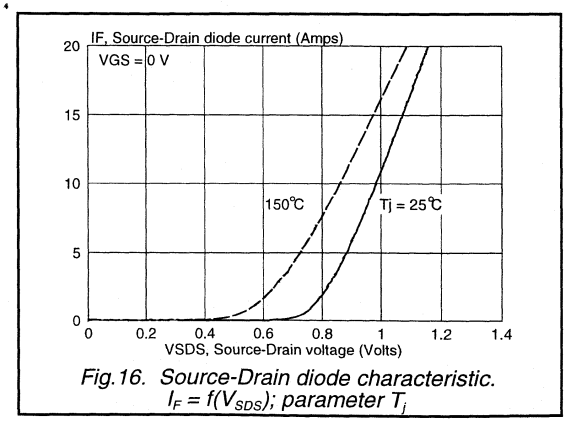


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

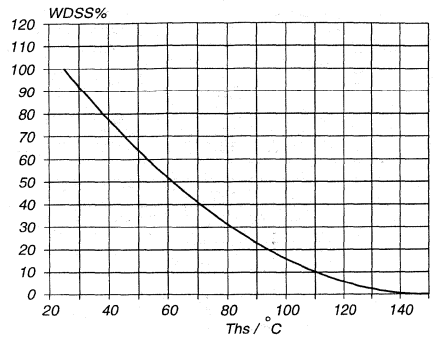


Fig.17. Normalised non-repetitive avalanche energy rating.
$E_{AS}\% = f(T_{hs})$

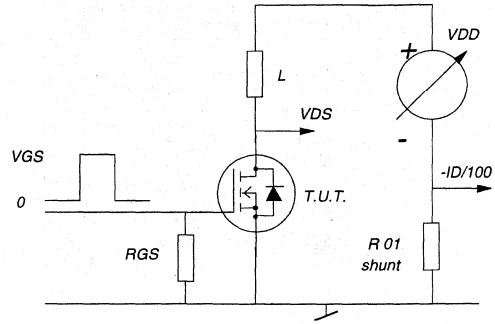


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot \frac{V_{(BR)DSS}}{(V_{(BR)DSS} - V_{DD})}$$

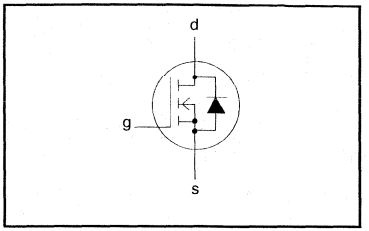
PowerMOS transistors Avalanche energy rated

PHX6N60E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Isolated package

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 600 V

I_D = 2.8 A

$R_{DS(ON)} \leq 1.8\ \Omega$

GENERAL DESCRIPTION

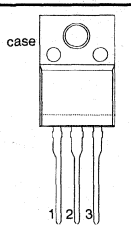
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHX6N60E is supplied in the SOT186A full pack, isolated package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

SOT186A



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	600	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	600	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{hs} = 25 °C; V_{GS} = 10 V	-	2.8	A
		T_{hs} = 100 °C; V_{GS} = 10 V	-	1.8	A
I_{DM}	Pulsed drain current	T_{hs} = 25 °C	-	21	A
P_D	Total dissipation	T_{hs} = 25 °C	-	35	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Single pulse avalanche energy	$V_{DD} \leq$ 50 V; starting T_j = 25°C	-	350	mJ
E_{AR}	Repetitive avalanche energy[1]	R_{GS} = 50 Ω; V_{GS} = 10 V	-	10	mJ
I_{AR}	Avalanche current		-	5.4	A

1 pulse width and repetition rate limited by T_j max.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	3.6	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	600	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 2.7 A	-	1.5	1.8	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 2.7 A	2	3.4	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 600 V; V_{GS} = 0 V	-	2	100	µA
		V_{DS} = 480 V; V_{GS} = 0 V; T_j = 125 °C	-	50	500	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 5.4 A; V_{DD} = 480 V; V_{GS} = 10 V	-	50	65	nC
Q_{gs}	Gate-source charge		-	5	8	nC
Q_{gd}	Gate-drain (Miller) charge		-	26	35	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V; R_D = 56 Ω;	-	15	-	ns
t_r	Turn-on rise time	R_G = 12 Ω	-	35	-	ns
$t_{d(off)}$	Turn-off delay time		-	90	-	ns
t_f	Turn-off fall time		-	40	-	ns
L_d	Internal drain inductance	Measured from drain lead to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	650	-	pF
C_{oss}	Output capacitance		-	85	-	pF
C_{rss}	Feedback capacitance		-	50	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{hs} = 25°C	-	-	5.4	A
I_{SM}	Pulsed source current (body diode)	T_{hs} = 25°C	-	-	21	A
V_{SD}	Diode forward voltage	I_S = 5.4 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 5.4 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	480	-	ns
Q_{rr}	Reverse recovery charge		-	4	-	µC

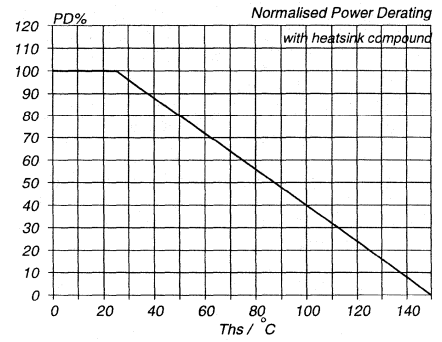


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{hs})

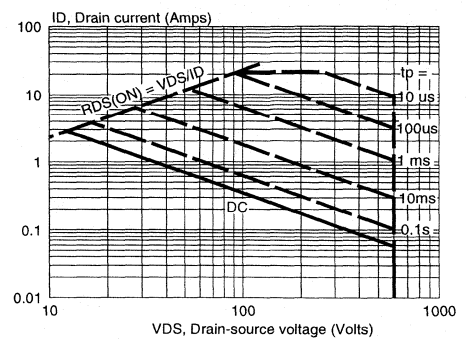


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

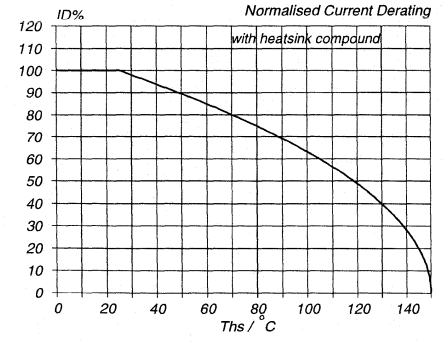


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{hs}); conditions: $V_{GS} \geq$ 10 V

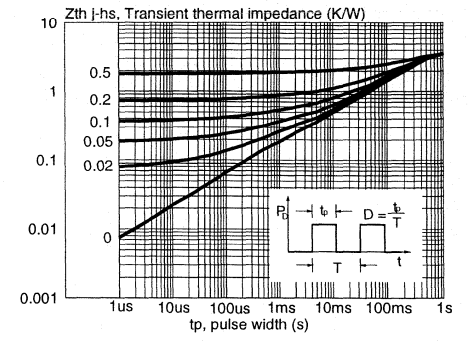


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}hs}$ = f(t); parameter D = t_p/T

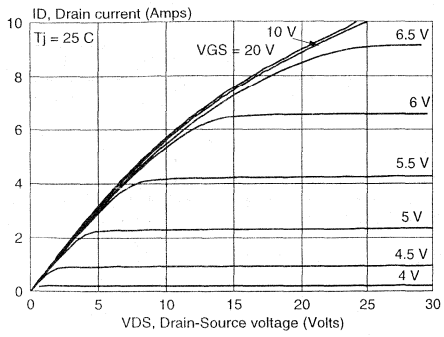


Fig.5. Typical output characteristics.
$I_D = f(V_{DS})$; parameter V_{GS}

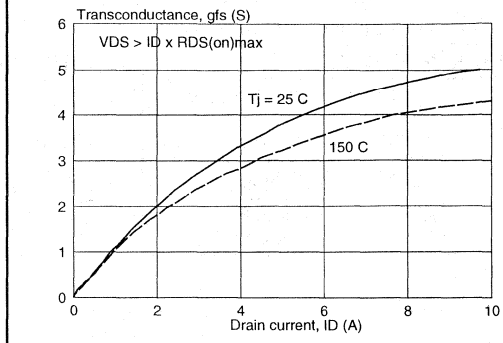


Fig.8. Typical transconductance.
$g_{fs} = f(I_D)$; parameter T_j

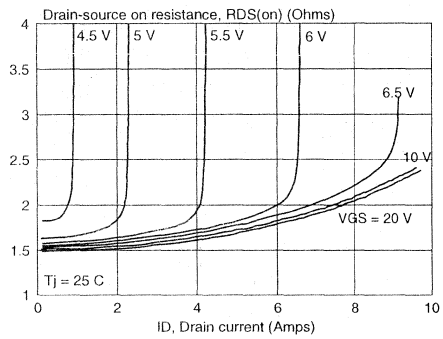


Fig.6. Typical on-state resistance.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

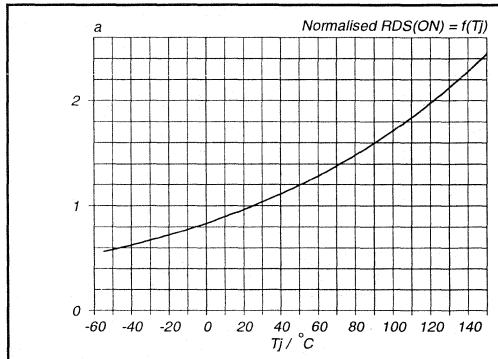


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 2.7 A; V_{GS} = 10 V

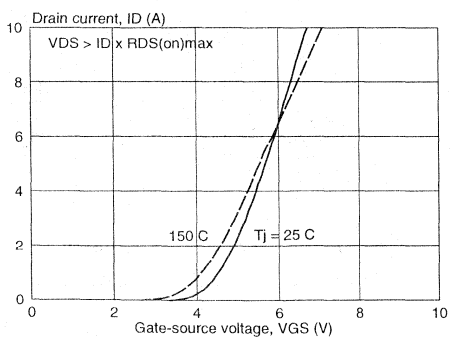


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

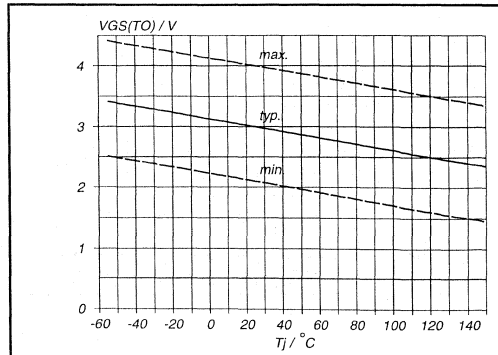


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

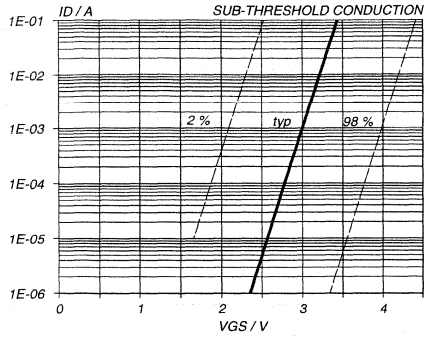


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

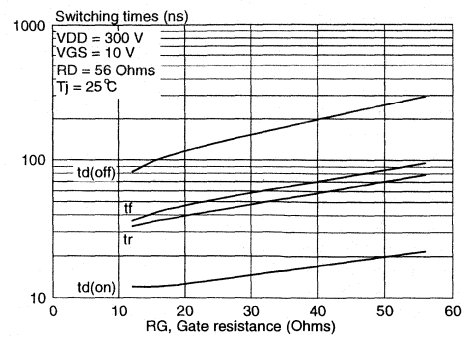


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

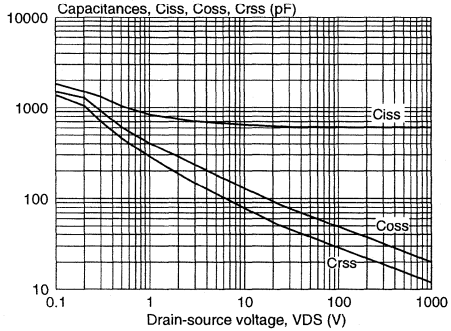


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

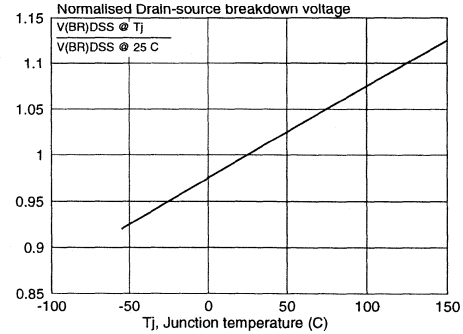


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

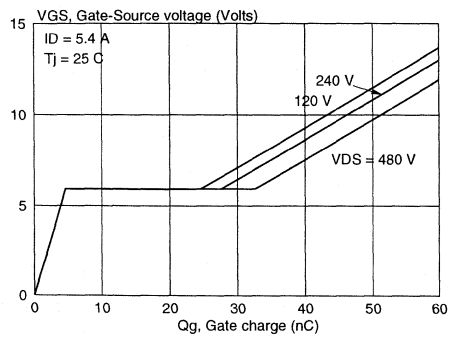


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

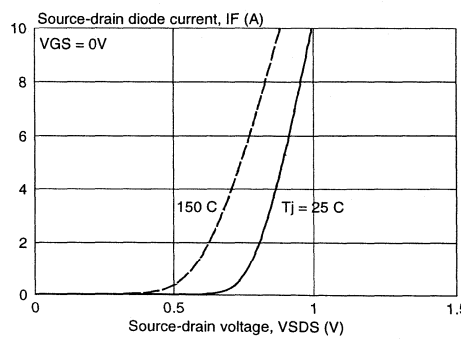


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

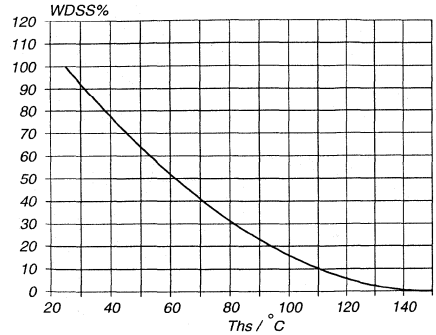


Fig.17. Normalised non-repetitive avalanche energy rating.
$E_{AS}\% = f(T_{hs})$

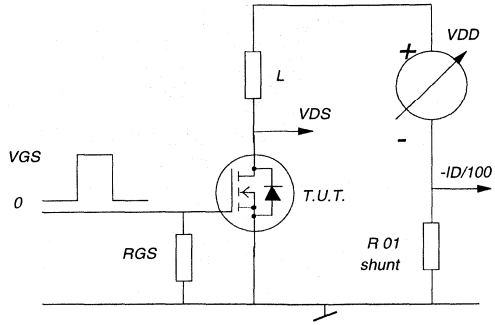


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot \frac{V_{(BR)DSS}}{(V_{(BR)DSS} - V_{DD})}$$

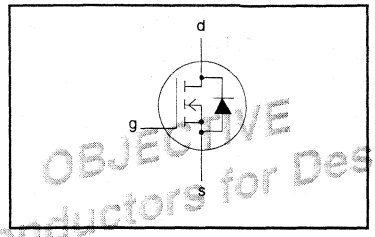
PowerMOS transistors
Low capacitance
Avalanche energy rated

PHX6NA60E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Low feedback capacitance
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 600 V

I_D = 3.9 A

$R_{DS(ON)} \leq 1.2\ \Omega$

OBJECTIVE
Philips Semiconductors for Design-in information

GENERAL DESCRIPTION

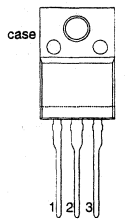
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHX6NA60E is supplied in the SOT186A full pack, isolated package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

SOT186A



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	600	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	600	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{hs} = 25 °C; V_{GS} = 10 V	-	3.9	A
		T_{hs} = 100 °C; V_{GS} = 10 V	-	2.6	A
I_{DM}	Pulsed drain current	T_{hs} = 25 °C	-	26	A
P_D	Total dissipation	T_{hs} = 25 °C	-	45	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Single pulse avalanche energy	Unclamped inductive load, ID = 6.5A; $V_{DD} \leq 50$ V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	570	mJ
E_{AR}	Repetitive avalanche energy[1]		-	9.5	mJ
I_{AS}, I_{AR}	Avalanche current		-	6.5	A

pulse width and repetition rate limited by T_j max.

PowerMOS transistors
Low capacitance
Avalanche energy rated

PHX6NA60E

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	2.78	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	600	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 3.25 A	-	-	1.2	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 3.25 A	3	4.5	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 600 V; V_{GS} = 0 V	-	2	100	µA
		V_{DS} = 480 V; V_{GS} = 0 V; T_j = 125 °C	-	50	500	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 6.5 A; V_{DD} = 480 V; V_{GS} = 10 V	-	-	75	nC
Q_{gs}	Gate-source charge		-	7	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	23	-	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V; R_D = 56 Ω;	-	-	50	ns
t_r	Turn-on rise time	R_G = 9.1 Ω	-	-	125	ns
$t_{d(off)}$	Turn-off delay time		-	-	110	ns
t_f	Turn-off fall time		-	-	30	ns
L_d	Internal drain inductance	Measured from drain lead to centre of die	-	3.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	-	1550	pF
C_{oss}	Output capacitance		-	140	-	pF
C_{rss}	Feedback capacitance		-	40	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{hs} = 25°C	-	-	6.5	A
I_{SM}	Pulsed source current (body diode)	T_{hs} = 25°C	-	-	26	A
V_{SD}	Diode forward voltage	I_S = 6.5 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 6.5 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	530	-	ns
Q_{rr}	Reverse recovery charge		-	6.7	-	µC

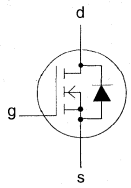
PowerMOS transistors FREDFET, Avalanche energy rated

PHX6ND50E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Isolated package
- Fast reverse recovery diode

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 500 V

I_D = 3.1 A

$R_{DS(ON)} \leq 1.5\ \Omega$

t_{rr} = 180 ns

GENERAL DESCRIPTION

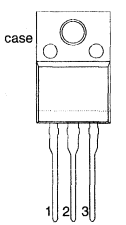
N-channel, enhancement mode field-effect power transistor, incorporating a **F**ast **R**ecovery **E**pitaxial **D**iode (FRED). This gives improved switching performance in half bridge and full bridge converters making this device particularly suitable for inverters, lighting ballasts and motor control circuits.

The PHX6ND50E is supplied in the SOT186A full pack, isolated package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

SOT186A



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	500	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	500	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{hs} = 25 °C; V_{GS} = 10 V	-	3.1	A
		T_{hs} = 100 °C; V_{GS} = 10 V	-	2	A
I_{DM}	Pulsed drain current[1]	T_{hs} = 25 °C	-	24	A
P_D	Total dissipation	T_{hs} = 25 °C	-	35	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 4.5 A; $V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	280	mJ
E_{AR}	Repetitive avalanche energy[1]		-	7.4	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	4.5	A

1 pulse width and repetition rate limited by T_j max.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	3.6	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	500	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 3 A	-	1.2	1.5	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 3 A	2	3.6	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 500 V; V_{GS} = 0 V	-	1	25	µA
		V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 °C	-	30	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 6 A; V_{DD} = 400 V; V_{GS} = 10 V	-	53	64	nC
Q_{gs}	Gate-source charge		-	4	6	nC
Q_{gd}	Gate-drain (Miller) charge		-	28	34	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 250 V; R_D = 39 Ω;	-	10	-	ns
t_r	Turn-on rise time	R_G = 12 Ω	-	33	-	ns
$t_{d(off)}$	Turn-off delay time		-	92	-	ns
t_f	Turn-off fall time		-	40	-	ns
L_d	Internal drain inductance	Measured from drain lead to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	610	-	pF
C_{oss}	Output capacitance		-	96	-	pF
C_{rss}	Feedback capacitance		-	54	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{hs} = 25°C	-	-	5.9	A
I_{SM}	Pulsed source current (body diode)	T_{hs} = 25°C	-	-	24	A
V_{SD}	Diode forward voltage	I_S = 6 A; V_{GS} = 0 V	-	-	1.5	V
t_{rr}	Reverse recovery time	I_S = 6 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	180	-	ns
		I_S = 6 A; V_{GS} = 0 V; dI/dt = 100 A/µs; 125°C	-	220	-	ns
Q_{rr}	Reverse recovery charge	I_S = 6 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	0.65	-	µC
		I_S = 6 A; V_{GS} = 0 V; dI/dt = 100 A/µs; 125°C	-	2.6	-	µC
I_{rrm}	Peak reverse recovery current	I_S = 6 A; V_{GS} = 0 V; dI/dt = 100 A/µs; 125°C	-	15	-	A

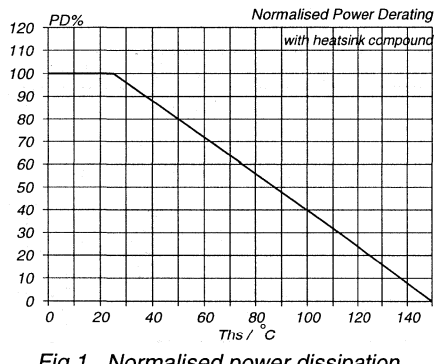


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{hs})

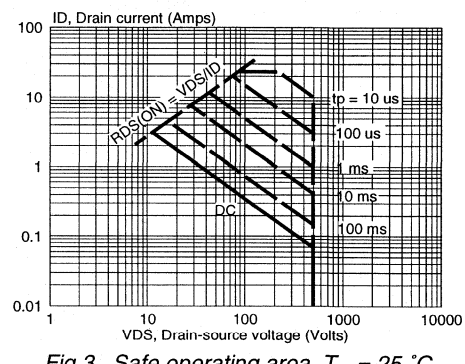


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

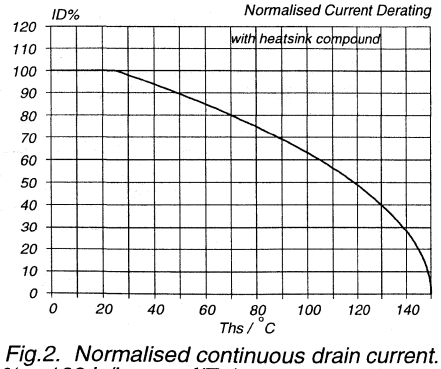


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{hs}); conditions: $V_{GS} \geq$ 10 V

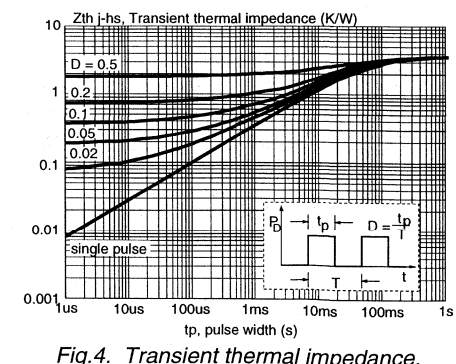


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}hs}$ = f(t); parameter D = t_p/T

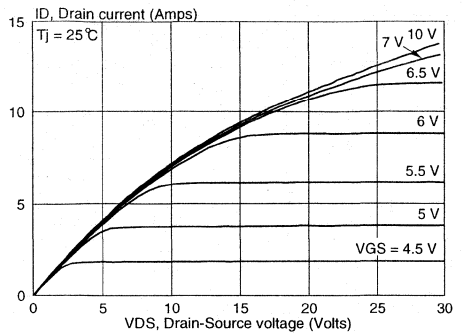


Fig.5. Typical output characteristics.
$I_D = f(V_{DS})$; parameter V_{GS}

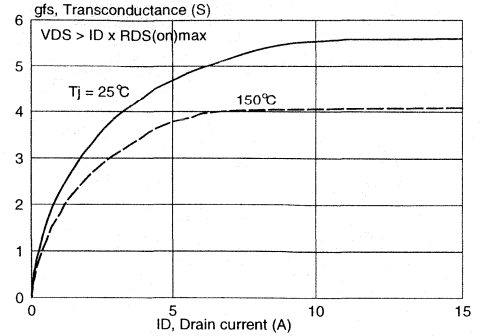


Fig.8. Typical transconductance.
$g_{fs} = f(I_D)$; parameter T_j

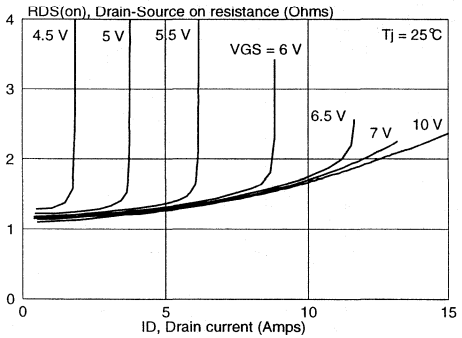


Fig.6. Typical on-state resistance.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

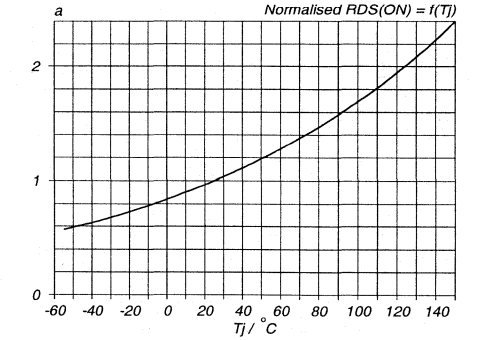


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 3 A; V_{GS} = 10 V

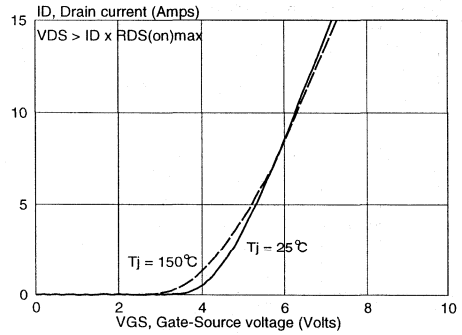


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

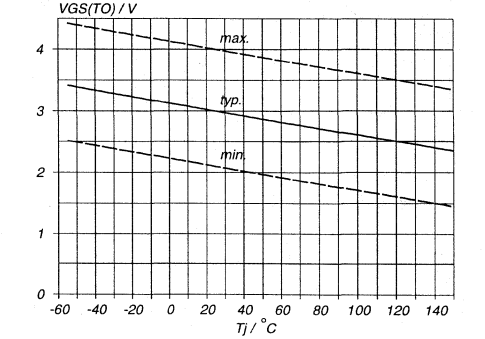


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

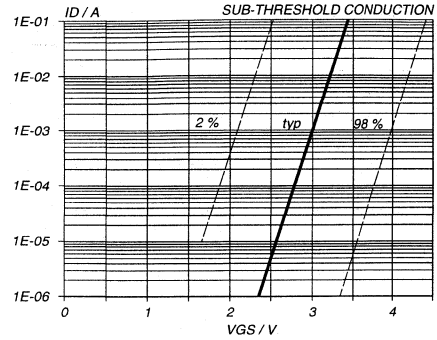


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

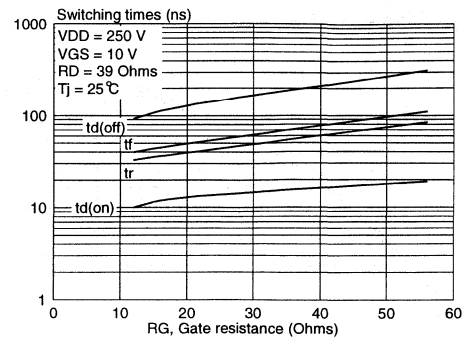


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

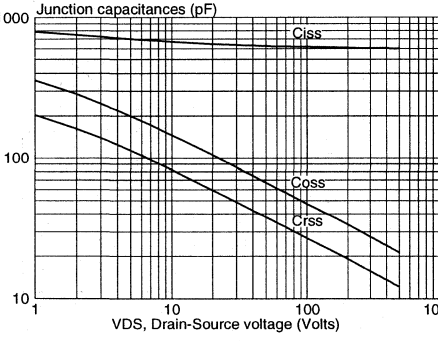


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

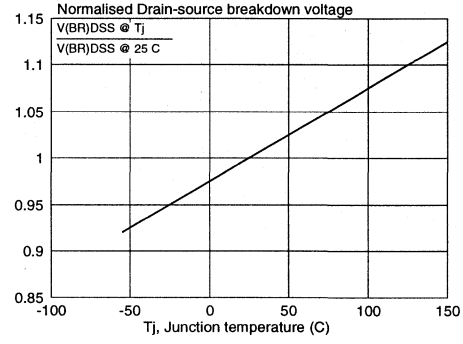


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

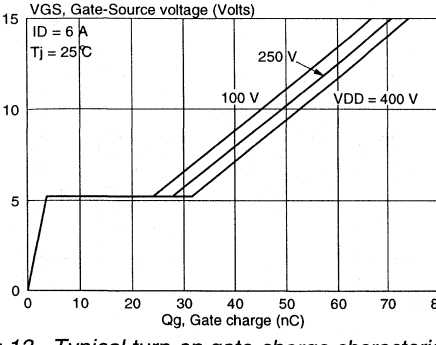


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

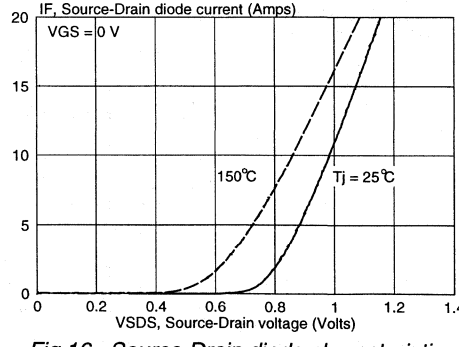


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

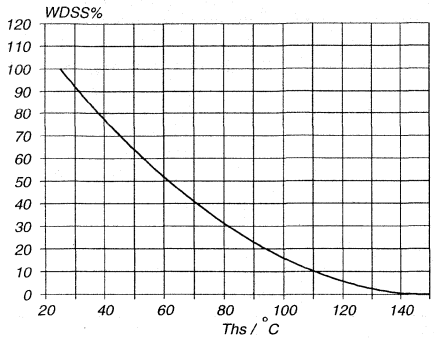


Fig.17. Normalised non-repetitive avalanche energy rating.
$E_{AS}\% = f(T_{hs})$

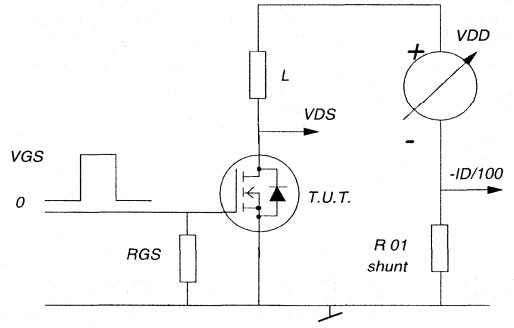


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot \frac{V_{(BR)DSS}}{(V_{(BR)DSS} - V_{DD})}$$

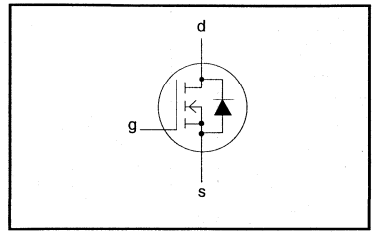
PowerMOS transistors Avalanche energy rated

PHX7N40E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Isolated package

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 400 V

I_D = 3.8 A

$R_{DS(ON)} \leq 1\ \Omega$

GENERAL DESCRIPTION

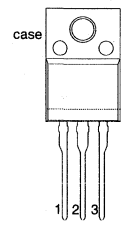
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHX7N40E is supplied in the SOT186A full pack, isolated package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

SOT186A



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	400	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	400	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{hs} = 25 °C; V_{GS} = 10 V	-	3.8	A
		T_{hs} = 100 °C; V_{GS} = 10 V	-	2.4	A
I_{DM}	Pulsed drain current	T_{hs} = 25 °C	-	29	A
P_D	Total dissipation	T_{hs} = 25 °C	-	35	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 5.5 A; $V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	290	mJ
E_{AR}	Repetitive avalanche energy[1]		-	7.4	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	5.5	A

1 pulse width and repetition rate limited by T_j max.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	3.6	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	400	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 3.6 A	-	0.7	1	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 3.6 A	2	4	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 400 V; V_{GS} = 0 V	-	1	25	µA
		V_{DS} = 320 V; V_{GS} = 0 V; T_j = 125 °C	-	30	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 7.2 A; V_{DD} = 320 V; V_{GS} = 10 V	-	52	62	nC
Q_{gs}	Gate-source charge		-	3	5	nC
Q_{gd}	Gate-drain (Miller) charge		-	26	30	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 200 V; R_D = 27 Ω;	-	12	-	ns
t_r	Turn-on rise time	R_G = 12 Ω	-	33	-	ns
$t_{d(off)}$	Turn-off delay time		-	93	-	ns
t_f	Turn-off fall time		-	42	-	ns
L_d	Internal drain inductance	Measured from drain lead to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	620	-	pF
C_{oss}	Output capacitance		-	108	-	pF
C_{rss}	Feedback capacitance		-	63	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{hs} = 25°C	-	-	7.2	A
I_{SM}	Pulsed source current (body diode)	T_{hs} = 25°C	-	-	29	A
V_{SD}	Diode forward voltage	I_S = 7.2 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 7.2 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	270	-	ns
Q_{rr}	Reverse recovery charge		-	3.3	-	µC

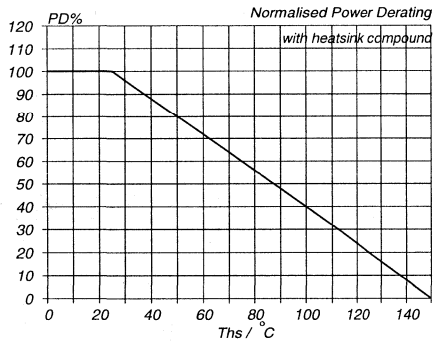


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{hs})

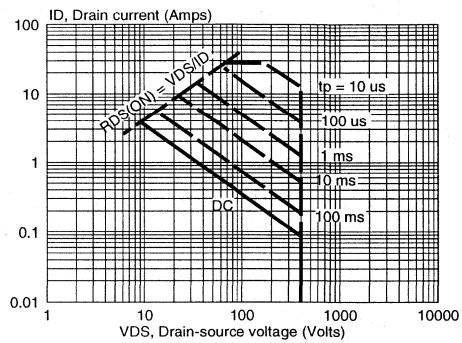


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

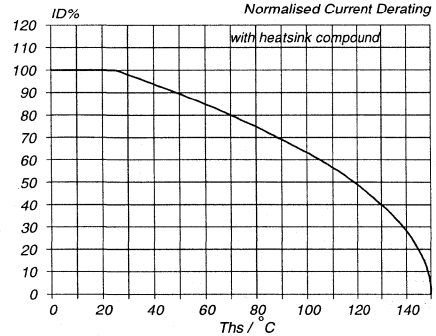


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{hs}); conditions: V_{GS} ≥ 10 V

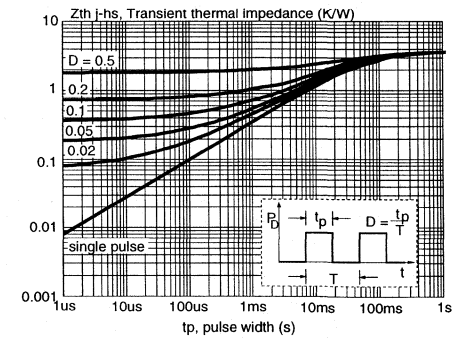


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}hs}$ = f(t); parameter D = t_p/T

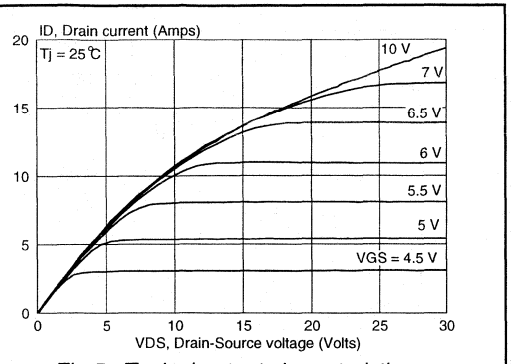


Fig.5. Typical output characteristics.
$I_D = f(V_{DS})$; parameter V_{GS}

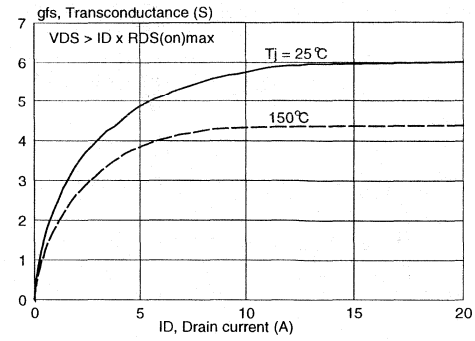


Fig.8. Typical transconductance.
$g_{fs} = f(I_D)$; parameter T_j

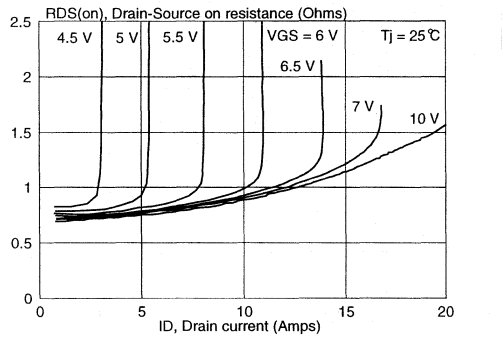


Fig.6. Typical on-state resistance.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

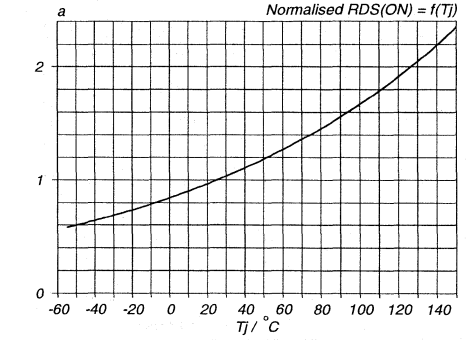


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 3.6 A; V_{GS} = 10 V

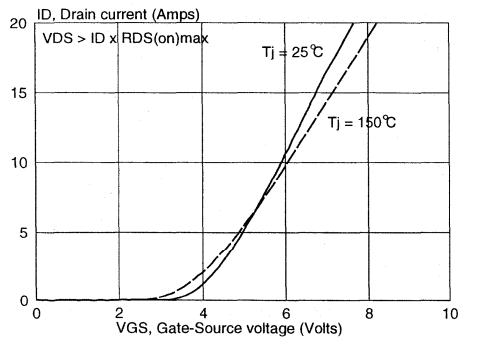


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

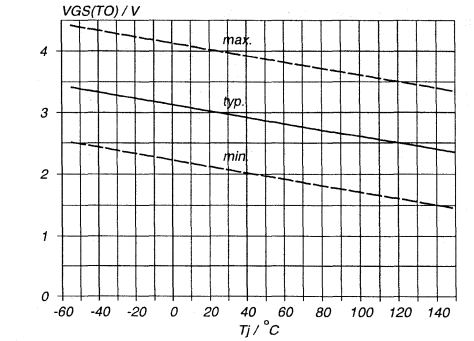


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

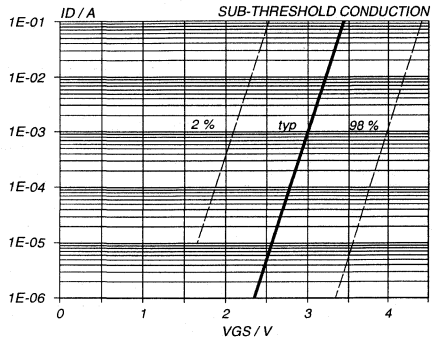


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

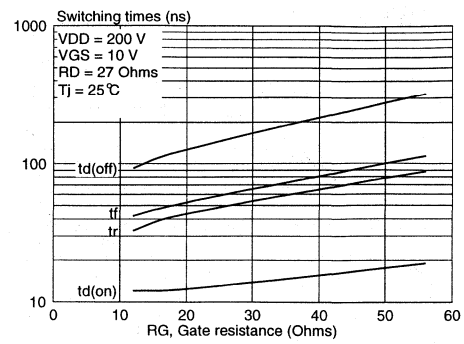


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

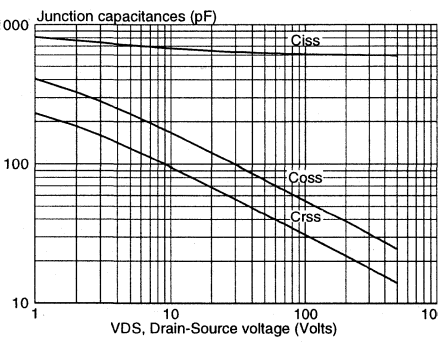


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

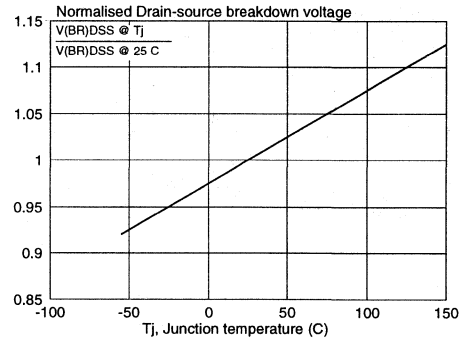


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

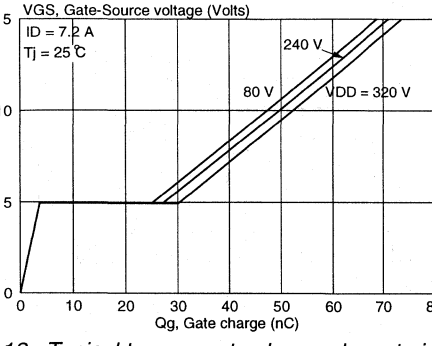


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

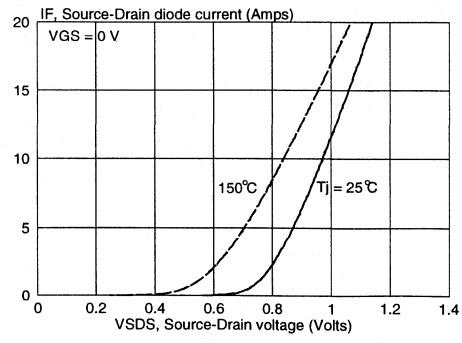


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

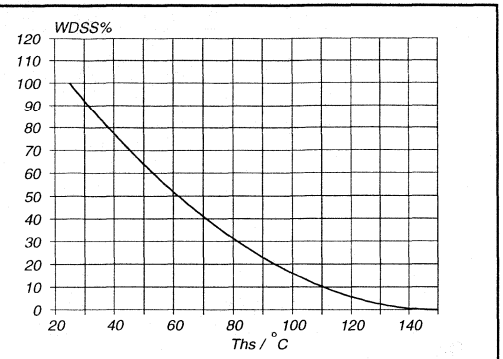


Fig.17. Normalised non-repetitive avalanche energy rating.
$E_{AS}\% = f(T_{hs})$

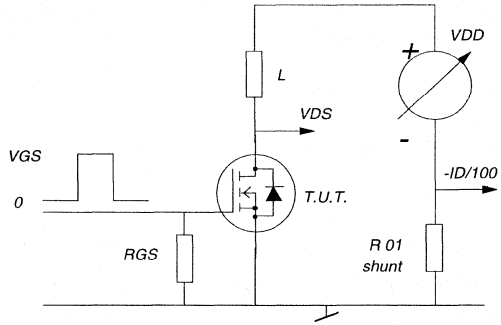


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot \frac{V_{(BR)DSS}}{(V_{(BR)DSS} - V_{DD})}$$

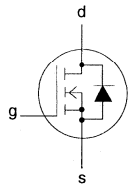
PowerMOS transistors Avalanche energy rated

PHX7N60E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Isolated package

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 600 V

I_D = 3.6 A

$R_{DS(ON)} \leq 1.2\ \Omega$

GENERAL DESCRIPTION

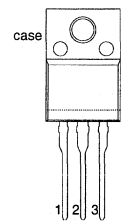
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHX7N60E is supplied in the SOT186A full pack, isolated package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

SOT186A



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	600	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	600	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{hs} = 25 °C; V_{GS} = 10 V	-	3.6	A
		T_{hs} = 100 °C; V_{GS} = 10 V	-	2.3	A
I_{DM}	Pulsed drain current	T_{hs} = 25 °C	-	28	A
P_D	Total dissipation	T_{hs} = 25 °C	-	37	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 6.2 A; $V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	570	mJ
E_{AR}	Repetitive avalanche energy[1]		-	13	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	6.2	A

1 pulse width and repetition rate limited by T_j max.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	3.4	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	600	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 3.5 A	-	0.9	1.2	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 3.5 A	3	4.5	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 600 V; V_{GS} = 0 V	-	2	100	µA
		V_{DS} = 480 V; V_{GS} = 0 V; T_j = 125 °C	-	50	500	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 7 A; V_{DD} = 480 V; V_{GS} = 10 V	-	90	110	nC
Q_{gs}	Gate-source charge		-	6	7	nC
Q_{gd}	Gate-drain (Miller) charge		-	44	60	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V; R_D = 39 Ω;	-	17	-	ns
t_r	Turn-on rise time	R_G = 9.1 Ω	-	43	-	ns
$t_{d(off)}$	Turn-off delay time		-	118	-	ns
t_f	Turn-off fall time		-	50	-	ns
L_d	Internal drain inductance	Measured from drain lead to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1100	-	pF
C_{oss}	Output capacitance		-	140	-	pF
C_{rss}	Feedback capacitance		-	80	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{hs} = 25˚C	-	-	7	A
I_{SM}	Pulsed source current (body diode)	T_{hs} = 25˚C	-	-	28	A
V_{SD}	Diode forward voltage	I_S = 7 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 7 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	530	-	ns
Q_{rr}	Reverse recovery charge		-	6.7	-	µC

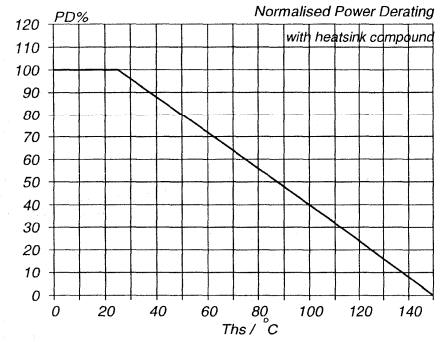


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ ˚C}$ = f(T_{hs})

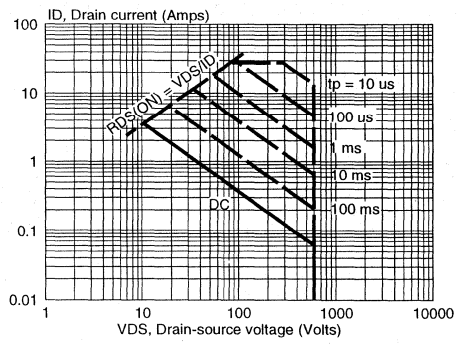


Fig.3. Safe operating area. T_{hs} = 25 ˚C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

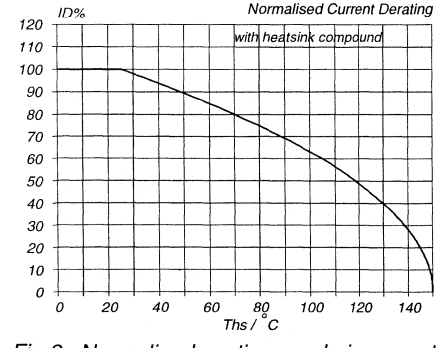


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ ˚C}$ = f(T_{hs}); conditions: V_{GS} ≥ 10 V

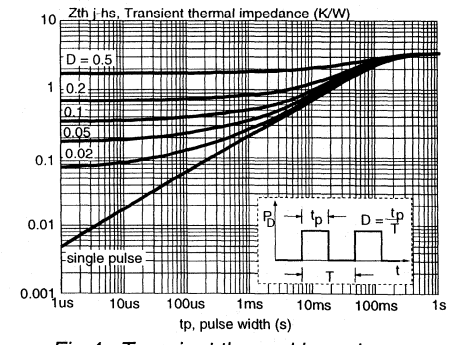


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}hs}$ = f(t); parameter D = t_p/T

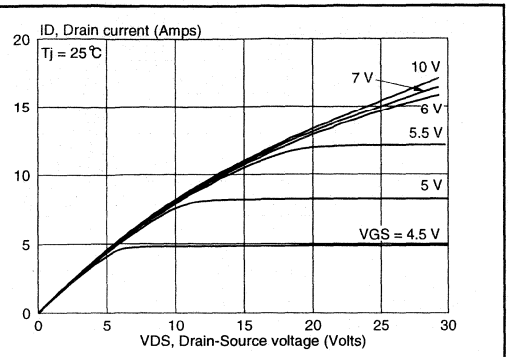


Fig.5. Typical output characteristics. $I_D = f(V_{DS})$; parameter V_{GS}

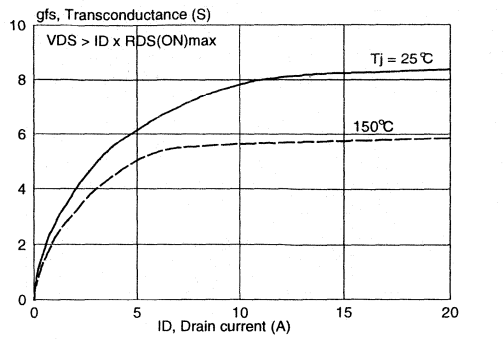


Fig.8. Typical transconductance. $g_{fs} = f(I_D)$; parameter T_j

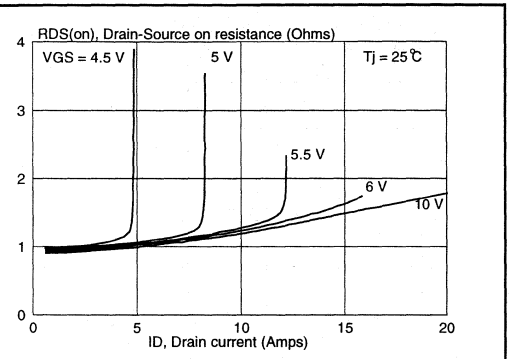


Fig.6. Typical on-state resistance. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

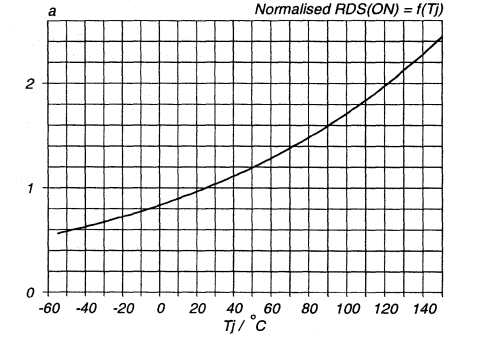


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 3.5$ A; $V_{GS} = 10$ V

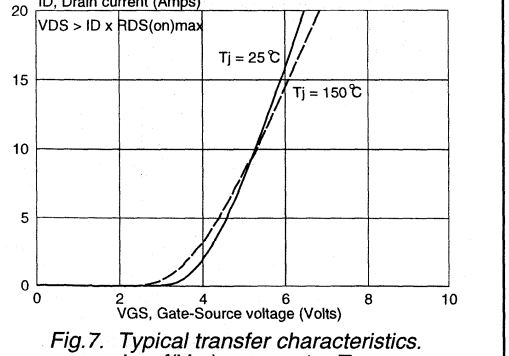


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; parameter T_j

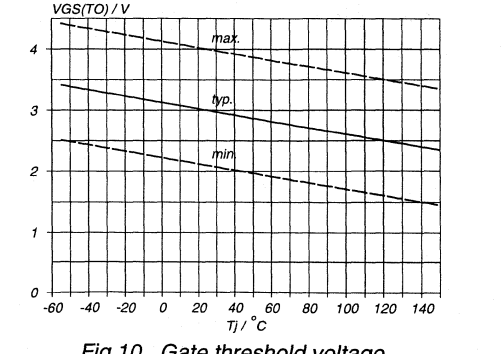


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: $I_D = 0.25$ mA; $V_{DS} = V_{GS}$

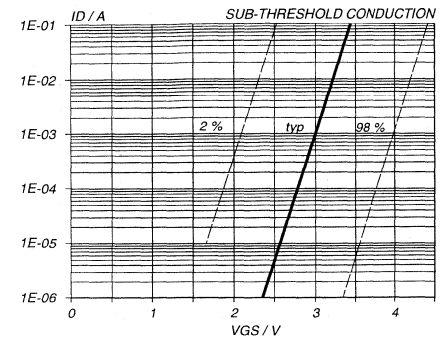


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

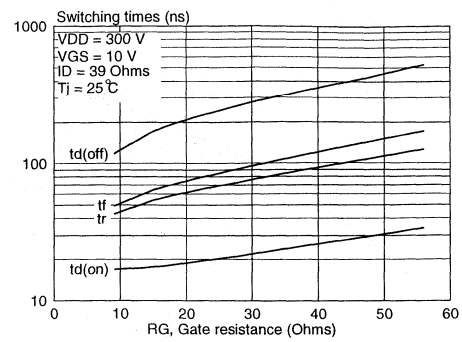


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

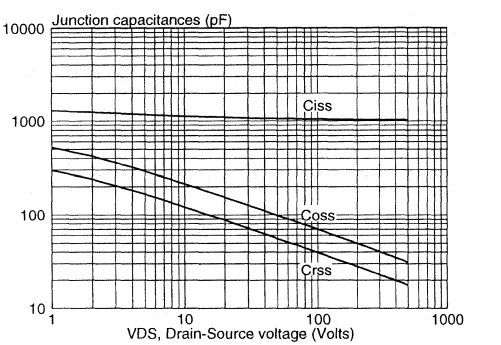


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

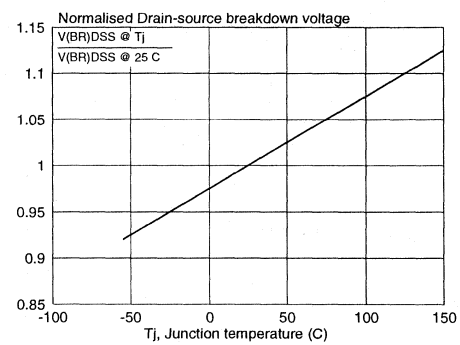


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

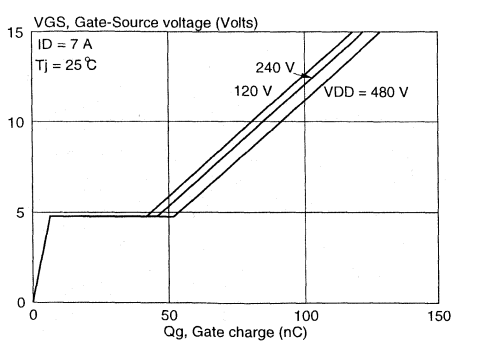


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

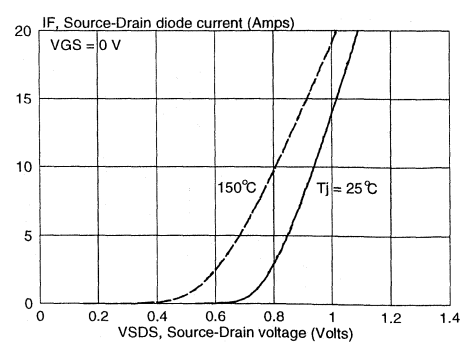


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

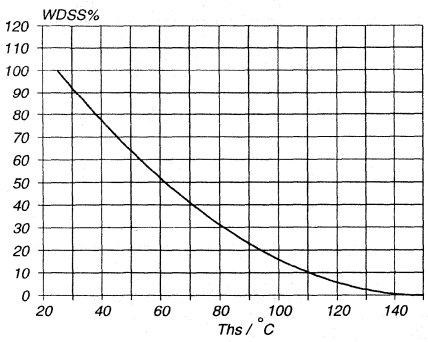


Fig.17. Normalised non-repetitive avalanche energy rating.
$E_{AS}\% = f(T_{hs})$

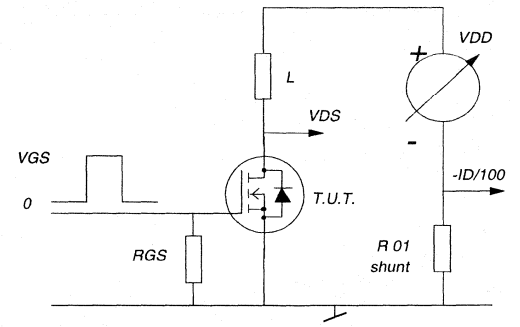


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot \frac{V_{(BR)DSS}}{(V_{(BR)DSS} - V_{DD})}$$

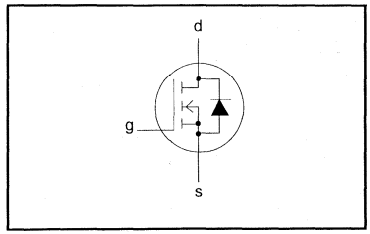
PowerMOS transistors Avalanche energy rated

PHX8N50E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Isolated package

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 500 V

I_D = 4.2 A

$R_{DS(ON)} \leq 0.85\ \Omega$

GENERAL DESCRIPTION

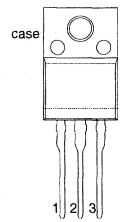
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHX8N50E is supplied in the SOT186A full pack, isolated package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

SOT186A



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	500	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	500	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{hs} = 25 °C; V_{GS} = 10 V	-	4.2	A
		T_{hs} = 100 °C; V_{GS} = 10 V	-	2.7	A
I_{DM}	Pulsed drain current	T_{hs} = 25 °C	-	34	A
P_D	Total dissipation	T_{hs} = 25 °C	-	37	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 8 A; $V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	510	mJ
E_{AR}	Repetitive avalanche energy[1]		-	13	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	8	A

1 pulse width and repetition rate limited by T_j max.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	3.4	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	500	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 4.8 A	-	0.7	0.85	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 4.8 A	3.5	6	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 500 V; V_{GS} = 0 V	-	1	25	µA
		V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 °C	-	40	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 8.5 A; V_{DD} = 400 V; V_{GS} = 10 V	-	88	110	nC
Q_{gs}	Gate-source charge		-	6	7	nC
Q_{gd}	Gate-drain (Miller) charge		-	47	60	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 250 V; R_D = 30 Ω;	-	18	-	ns
t_r	Turn-on rise time	R_G = 9.1 Ω	-	50	-	ns
$t_{d(off)}$	Turn-off delay time		-	104	-	ns
t_f	Turn-off fall time		-	60	-	ns
L_d	Internal drain inductance	Measured from drain lead to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1060	-	pF
C_{oss}	Output capacitance		-	160	-	pF
C_{rss}	Feedback capacitance		-	90	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{hs} = 25˚C	-	-	8.5	A
I_{SM}	Pulsed source current (body diode)	T_{hs} = 25˚C	-	-	34	A
V_{SD}	Diode forward voltage	I_S = 8.5 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 8.5 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	440	-	ns
Q_{rr}	Reverse recovery charge		-	6.4	-	µC

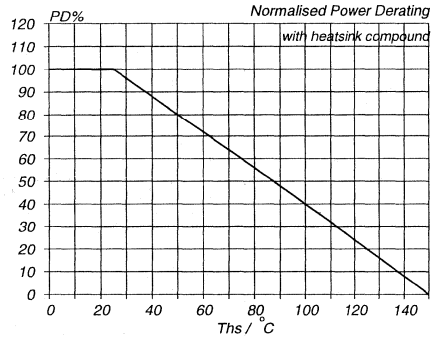


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ ˚C}$ = f(T_{hs})

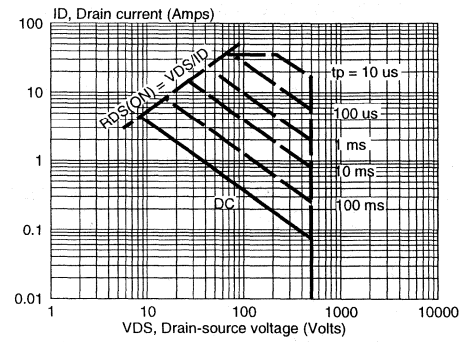


Fig.3. Safe operating area. T_{hs} = 25 ˚C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

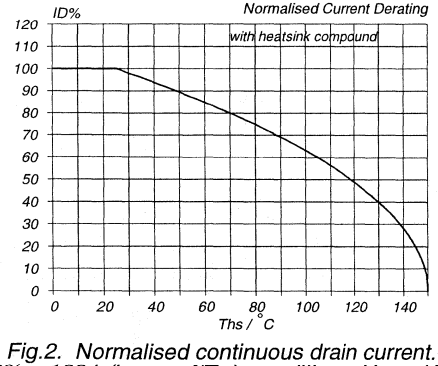


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ ˚C}$ = f(T_{hs}); conditions: V_{GS} ≥ 10 V

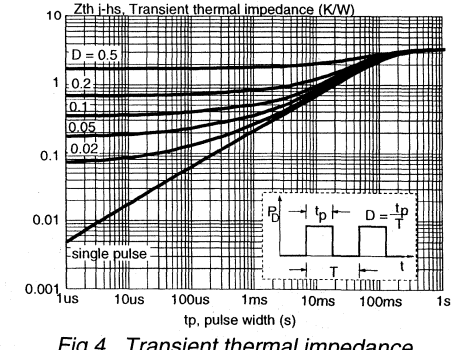


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}hs}$ = f(t); parameter D = t_p/T

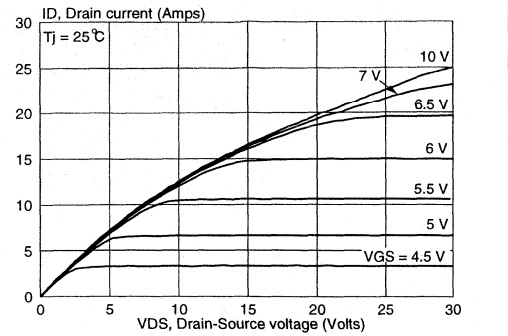


Fig.5. Typical output characteristics.
$I_D = f(V_{DS})$; parameter V_{GS}

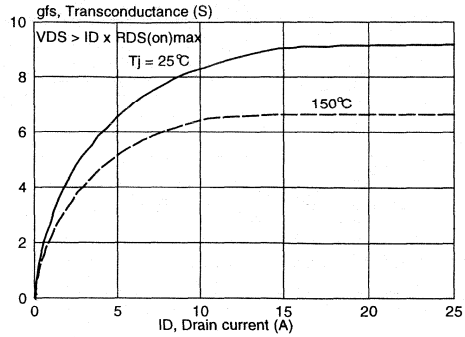


Fig.8. Typical transconductance.
$g_{fs} = f(I_D)$; parameter T_j

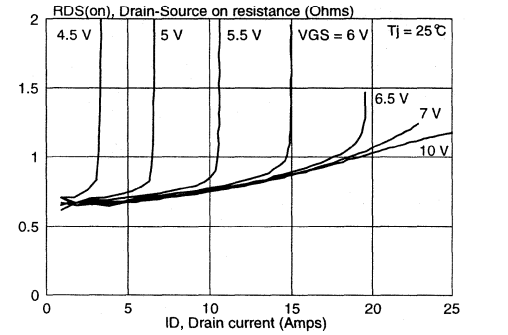


Fig.6. Typical on-state resistance.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

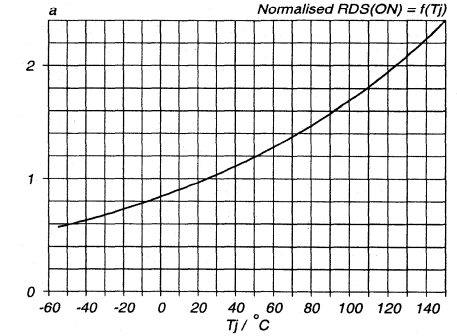


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 4.25 A; V_{GS} = 10 V

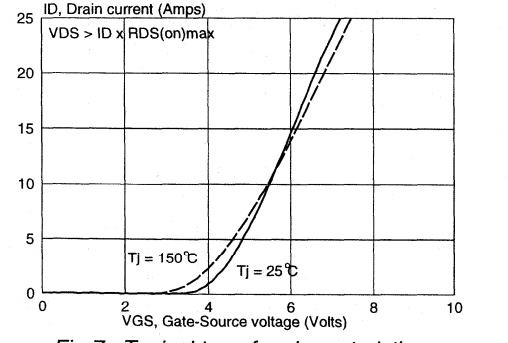


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

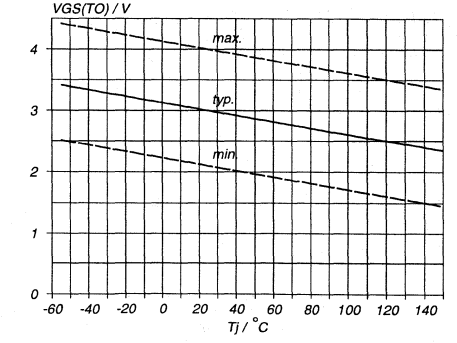


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

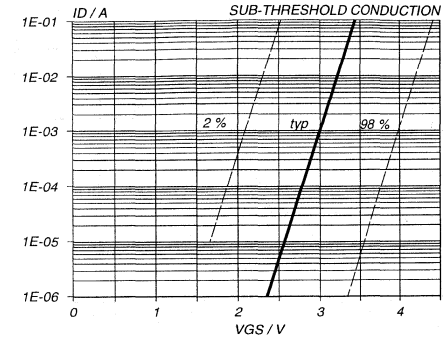


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

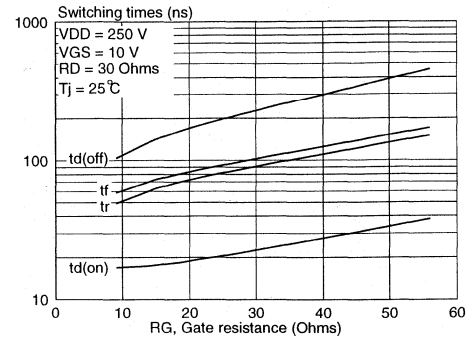


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

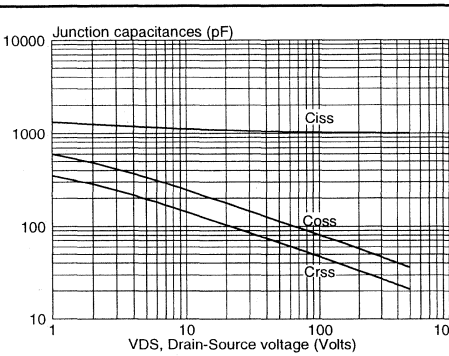


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

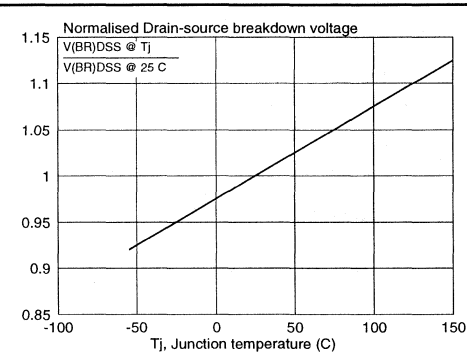


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

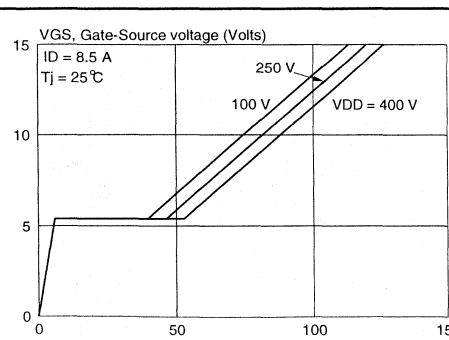


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

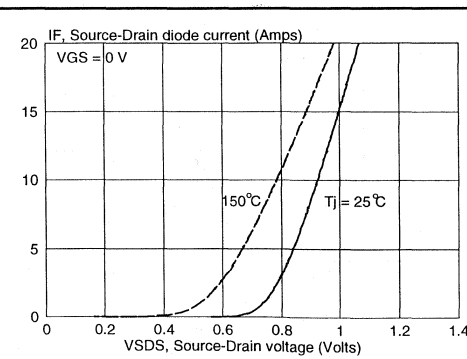


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

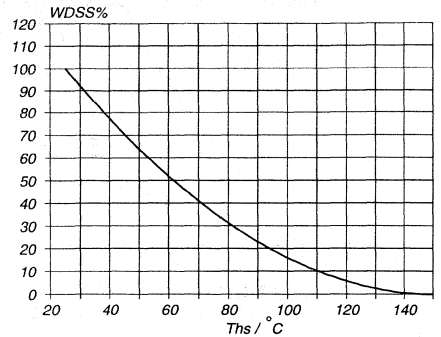


Fig.17. Normalised non-repetitive avalanche energy rating.
$E_{AS}\% = f(T_{hs})$

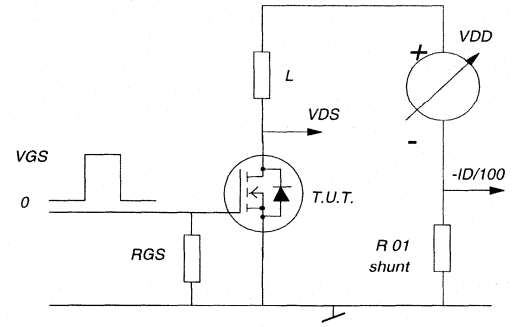


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot \frac{V_{(BR)DSS}}{(V_{(BR)DSS} - V_{DD})}$$

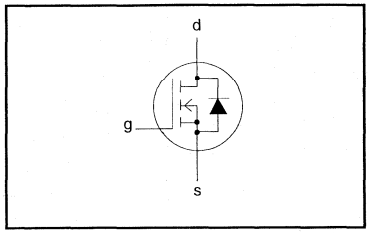
PowerMOS transistors FREDFET, Avalanche energy rated

PHX8ND50E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Isolated package
- Fast reverse recovery diode

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 500 V

I_D = 4.2 A

$R_{DS(ON)} \leq 0.85\ \Omega$

t_{rr} = 180 ns

GENERAL DESCRIPTION

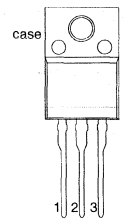
N-channel, enhancement mode field-effect power transistor, incorporating a **F**ast **R**ecovery **E**pitaxial **D**iode (FRED). This gives improved switching performance in half bridge and full bridge converters making this device particularly suitable for inverters, lighting ballasts and motor control circuits.

The PHX8ND50E is supplied in the SOT186A full pack, isolated package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

SOT186A



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	500	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	500	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{hs} = 25 °C; V_{GS} = 10 V	-	4.2	A
		T_{hs} = 100 °C; V_{GS} = 10 V	-	2.7	A
I_{DM}	Pulsed drain current[1]	T_{hs} = 25 °C	-	34	A
P_D	Total dissipation	T_{hs} = 25 °C	-	37	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 8 A; $V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	510	mJ
E_{AR}	Repetitive avalanche energy[1]		-	13	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	8	A

1 pulse width and repetition rate limited by T_j max.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	3.4	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	500	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 4.8 A	-	0.7	0.85	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 4.8 A	3.5	6	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 500 V; V_{GS} = 0 V	-	1	25	µA
		V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 °C	-	40	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 8.5 A; V_{DD} = 400 V; V_{GS} = 10 V	-	88	110	nC
Q_{gs}	Gate-source charge		-	6	7	nC
Q_{gd}	Gate-drain (Miller) charge		-	47	60	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 250 V; R_D = 30 Ω;	-	18	-	ns
t_r	Turn-on rise time	R_G = 9.1 Ω	-	50	-	ns
$t_{d(off)}$	Turn-off delay time		-	104	-	ns
t_f	Turn-off fall time		-	60	-	ns
L_d	Internal drain inductance	Measured from drain lead to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1060	-	pF
C_{oss}	Output capacitance		-	160	-	pF
C_{rss}	Feedback capacitance		-	90	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{hs} = 25°C	-	-	8.5	A
I_{SM}	Pulsed source current (body diode)	T_{hs} = 25°C	-	-	34	A
V_{SD}	Diode forward voltage	I_S = 8.5 A; V_{GS} = 0 V	-	-	1.5	V
t_{rr}	Reverse recovery time	I_S = 8.5 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	180	-	ns
		I_S = 8.5 A; V_{GS} = 0 V; dI/dt = 100 A/µs; 125°C	-	220	-	ns
Q_{rr}	Reverse recovery charge	I_S = 8.5 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	0.65	-	µC
		I_S = 8.5 A; V_{GS} = 0 V; dI/dt = 100 A/µs; 125°C	-	2.6	-	µC
I_{rrm}	Peak reverse recovery current	I_S = 8.5 A; V_{GS} = 0 V; dI/dt = 100 A/µs; 125°C	-	15	-	A

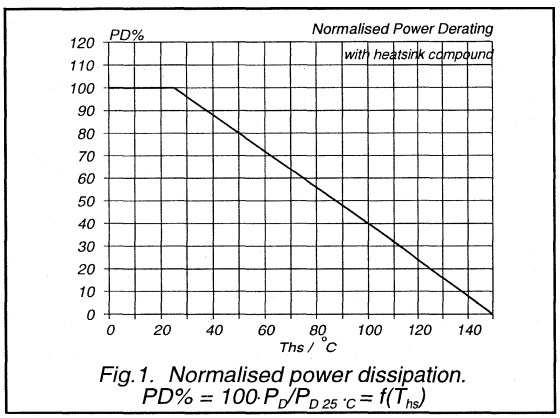


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{hs})

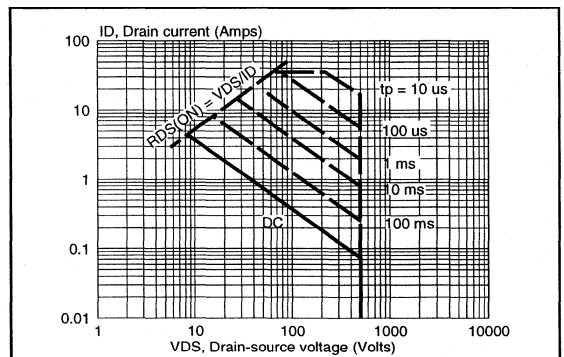


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

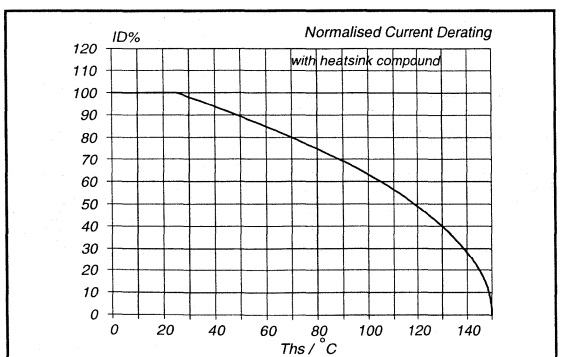


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{hs}); conditions: V_{GS} ≥ 10 V

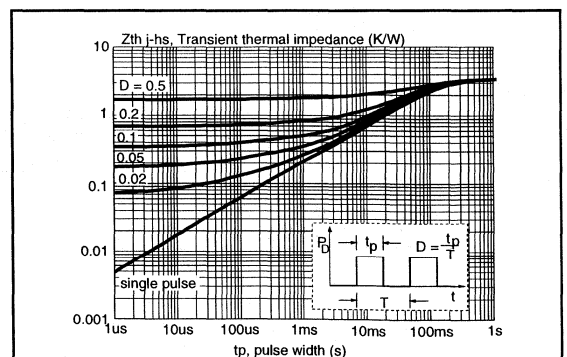


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}hs}$ = f(t); parameter D = t_p/T

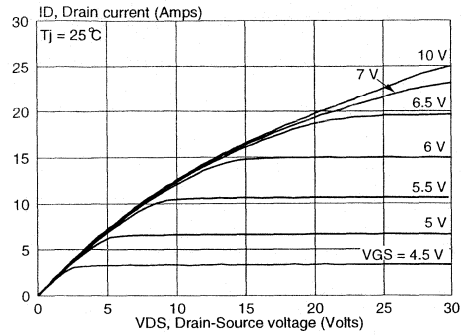


Fig.5. Typical output characteristics. $I_D = f(V_{DS})$; parameter V_{GS}

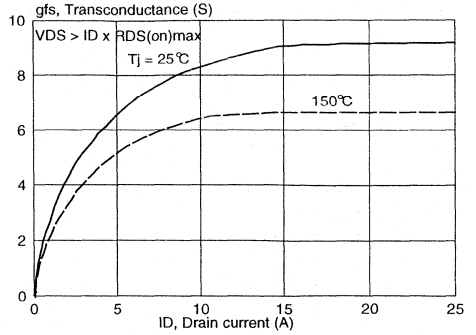


Fig.8. Typical transconductance. $g_{fs} = f(I_D)$; parameter T_j

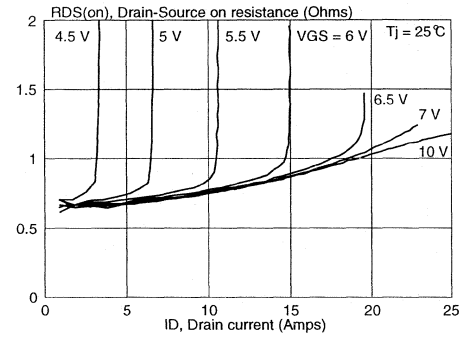


Fig.6. Typical on-state resistance. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

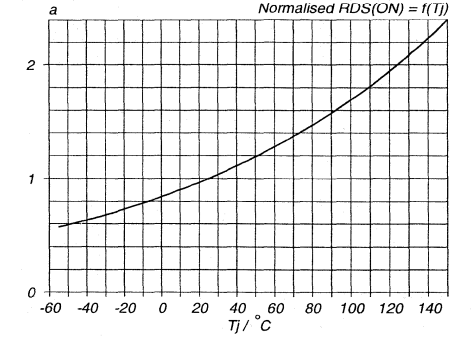


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 4.25 A; V_{GS} = 10 V

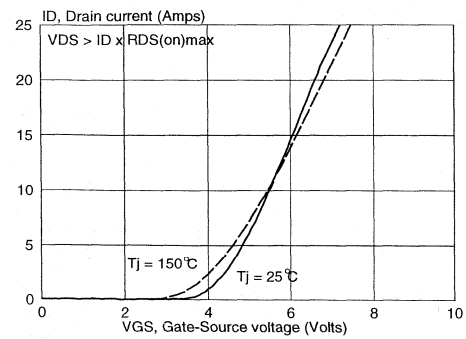


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; parameter T_j

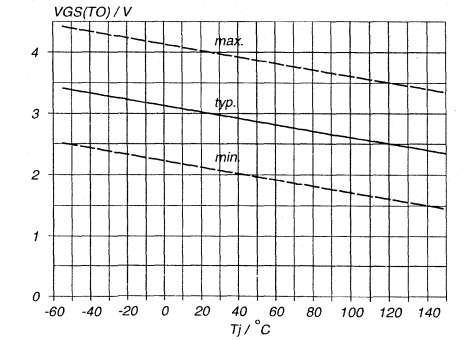


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

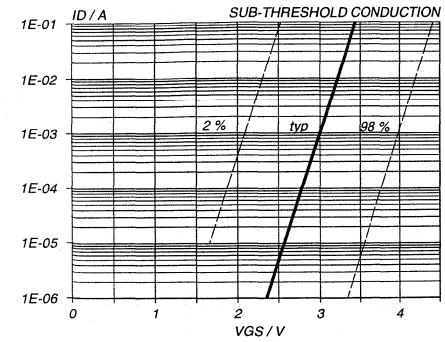


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

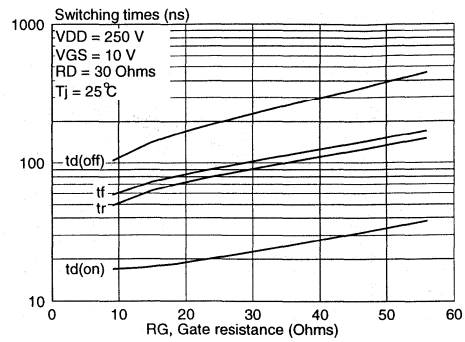


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

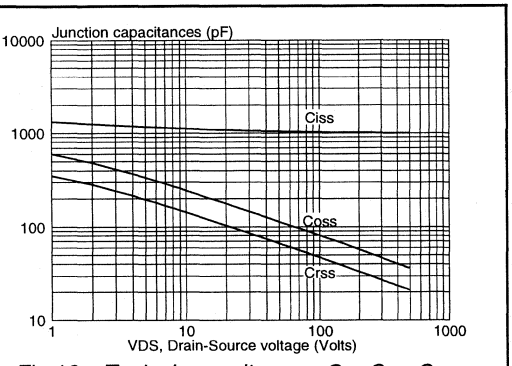


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

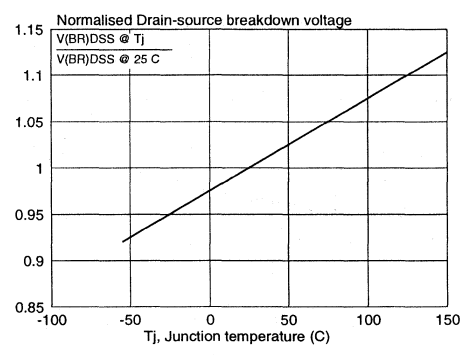


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

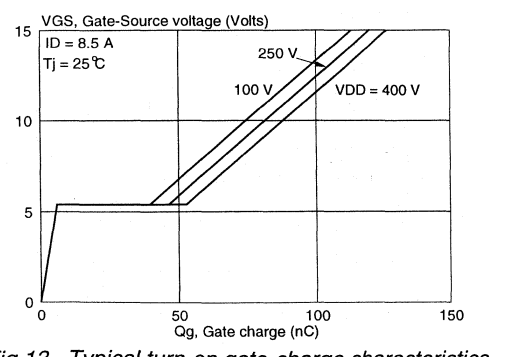


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

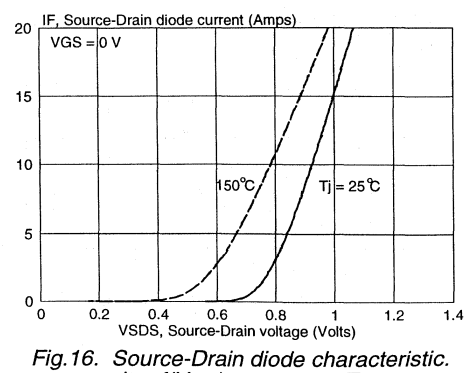


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

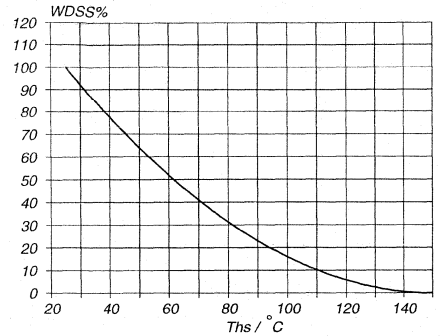


Fig.17. Normalised non-repetitive avalanche energy rating.
$E_{AS}\% = f(T_{hs})$

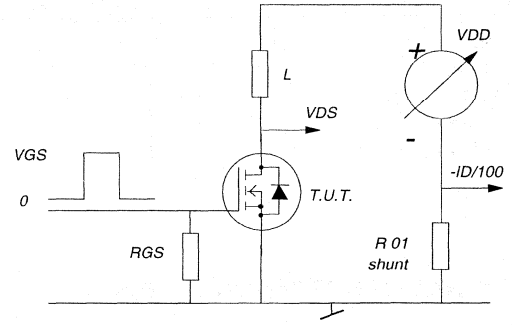


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot \frac{V_{(BR)DSS}}{(V_{(BR)DSS} - V_{DD})}$$

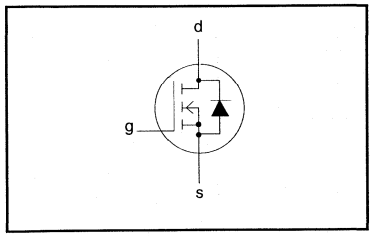
PowerMOS transistors Avalanche energy rated

PHX10N40E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Isolated package

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 400 V

I_D = 5.3 A

$R_{DS(ON)} \leq 0.55\ \Omega$

GENERAL DESCRIPTION

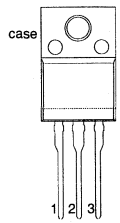
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHX10N40E is supplied in the SOT186A full pack, isolated package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

SOT186A



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	400	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	400	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{hs} = 25 °C; V_{GS} = 10 V	-	5.3	A
		T_{hs} = 100 °C; V_{GS} = 10 V	-	3.4	A
I_{DM}	Pulsed drain current	T_{hs} = 25 °C	-	42	A
P_D	Total dissipation	T_{hs} = 25 °C	-	37	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 10 A; $V_{DD} \leq$ 50 V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	520	mJ
E_{AR}	Repetitive avalanche energy[1]		-	13	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	10	A

1 pulse width and repetition rate limited by T_j max.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	3.4	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	400	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 5.3 A	-	0.42	0.55	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 5.3 A	3.5	6	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 400 V; V_{GS} = 0 V	-	1	25	μA
		V_{DS} = 320 V; V_{GS} = 0 V; T_j = 125 °C	-	30	250	μA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 10.6 A; V_{DD} = 320 V; V_{GS} = 10 V	-	90	110	nC
Q_{gs}	Gate-source charge		-	7	9	nC
Q_{gd}	Gate-drain (Miller) charge		-	49	60	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 200 V; R_D = 18 Ω;	-	13	-	ns
t_r	Turn-on rise time	R_G = 9.1 Ω	-	65	-	ns
$t_{d(off)}$	Turn-off delay time		-	108	-	ns
t_f	Turn-off fall time		-	70	-	ns
L_d	Internal drain inductance	Measured from drain lead to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1080	-	pF
C_{oss}	Output capacitance		-	190	-	pF
C_{rss}	Feedback capacitance		-	110	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{hs} = 25°C	-	-	10.6	A
I_{SM}	Pulsed source current (body diode)	T_{hs} = 25°C	-	-	42	A
V_{SD}	Diode forward voltage	I_S = 10.6 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 10.6 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	330	-	ns
Q_{rr}	Reverse recovery charge		-	4.8	-	µC

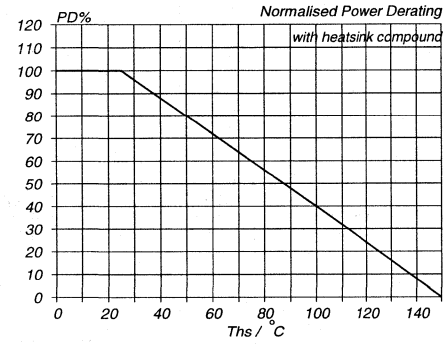


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{hs})

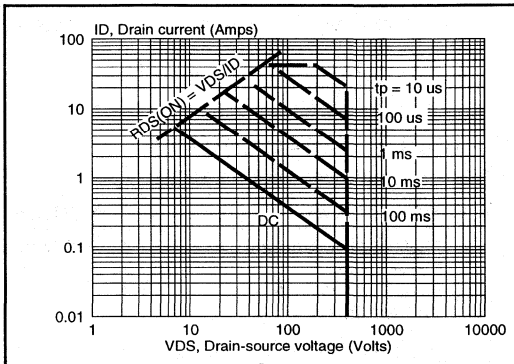


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

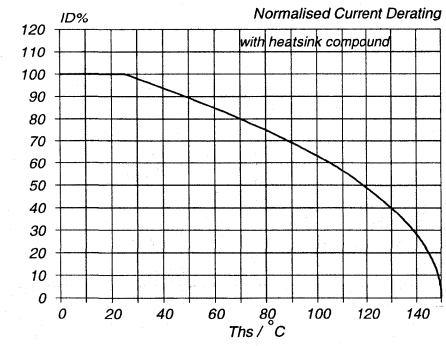


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{hs}); conditions: V_{GS} ≥ 10 V

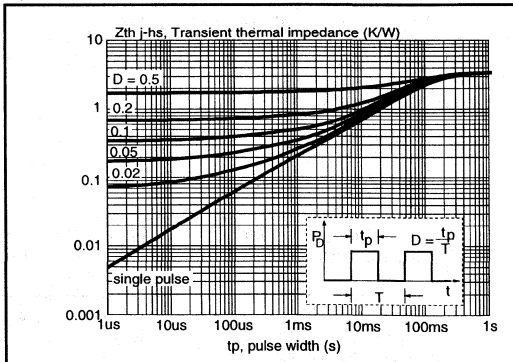


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}hs}$ = f(t); parameter D = t_p/T

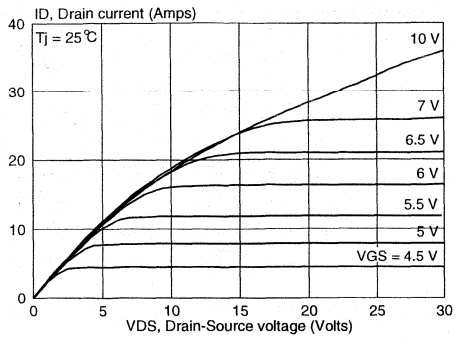


Fig.5. Typical output characteristics.
$I_D = f(V_{DS})$; parameter V_{GS}

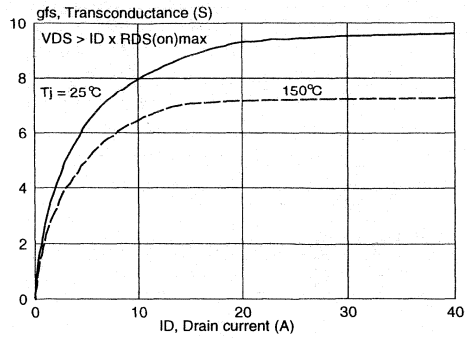


Fig.8. Typical transconductance.
$g_{fs} = f(I_D)$; parameter T_j

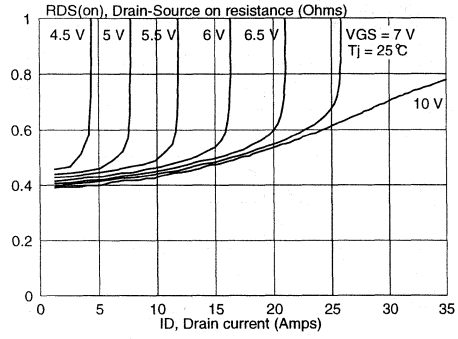


Fig.6. Typical on-state resistance.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

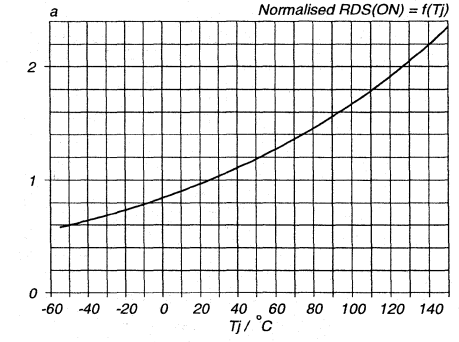


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 5.3 A; V_{GS} = 10 V

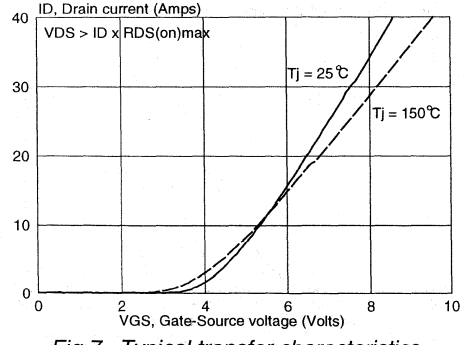


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

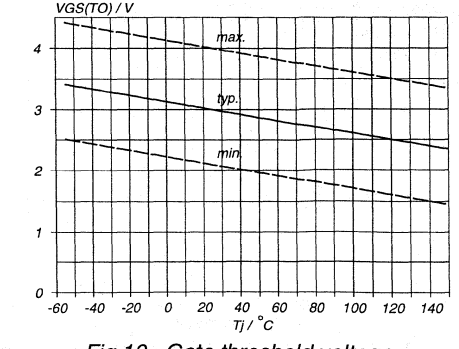


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

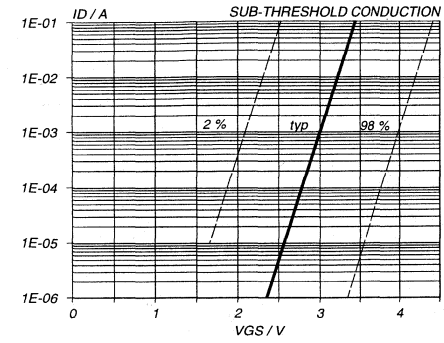


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

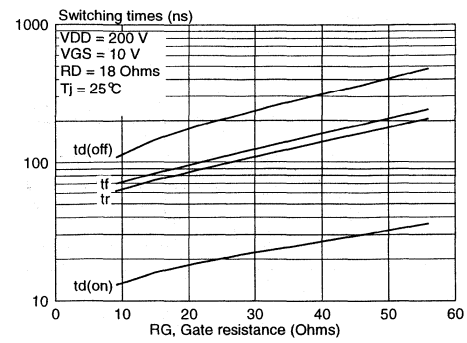


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

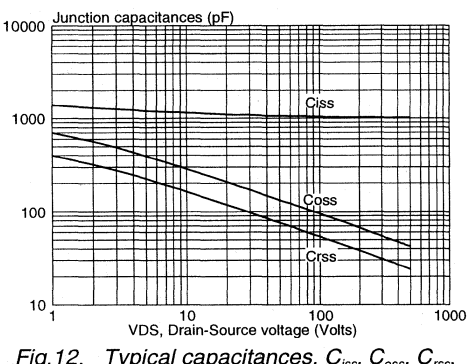


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

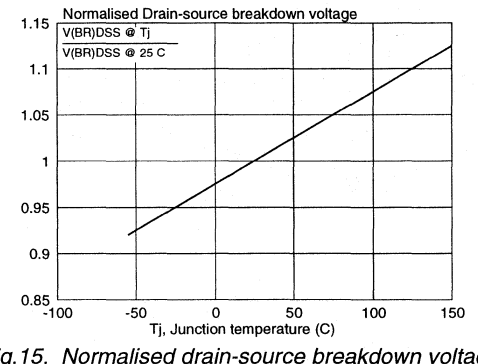


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

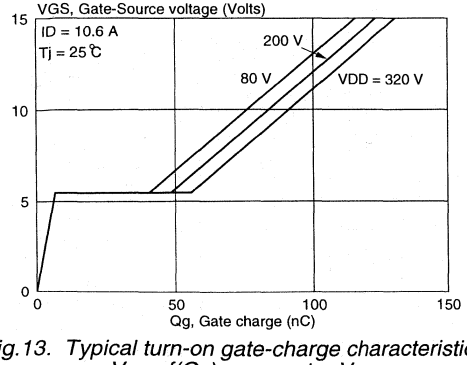


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

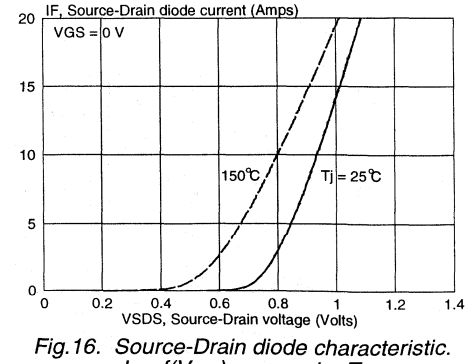


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

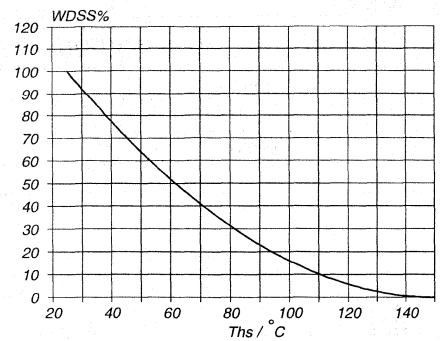


Fig.17. Normalised non-repetitive avalanche energy rating.
$E_{AS}\% = f(T_{hs})$

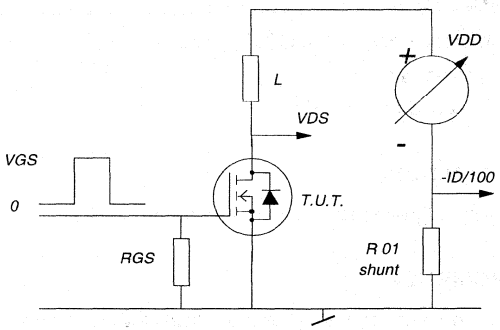


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot \frac{V_{(BR)DSS}}{(V_{(BR)DSS} - V_{DD})}$$

N-channel enhancement mode vertical D-MOS transistor

PMBF107

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

APPLICATIONS

- Relay, high-speed and line transformer drivers.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT23 package, intended for use as a line current interruptor in telephone sets.

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain

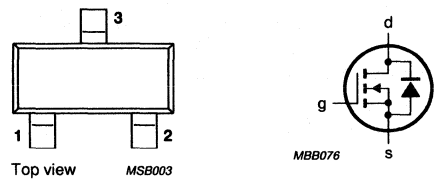


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		200	V
I_D	drain current (DC)		100	mA
R_{DSon}	drain-source on-resistance	I_D = 20 mA; V_{GS} = 2.6 V	28	Ω
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	2.4	V

N-channel enhancement mode vertical D-MOS transistor

PMBF107

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
V_{GSO}	gate-source voltage	open drain	–	±20	V
I_D	drain current (DC)		–	100	mA
I_{DM}	drain current	peak value	–	250	mA
P_{tot}	total power dissipation	T_{amb} = 25 °C; note 1	–	250	mW
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		–	150	°C

Note

1. Device mounted on an FR4 printed-circuit board.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient; note 1	500	K/W

Note

1. Device mounted on an FR4 printed-circuit board.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	200	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 130 V	–	–	30	nA
I_{DSX}	drain cut-off current	V_{GS} = 0.2 V; V_{DS} = 70 V	–	–	1	μA
I_{GSS}	gate-source leakage current	V_{GS} = ±15 V; V_{DS} = 0;	–	–	±10	nA
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	0.8	–	2.4	V
R_{DSon}	drain-source on-state resistance	V_{GS} = 2.6 V; I_D = 20 mA	–	20	28	Ω
		V_{GS} = 10 V; I_D = 150 mA	–	14	–	Ω
$\lvert y_{fs} \rvert$	transfer admittance	V_{DS} = 15 V; I_D = 250 mA	75	170	–	mS
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 10 V; f = 1 MHz	–	50	65	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 10 V; f = 1 MHz	–	16	25	pF
C_{rss}	feedback capacitance	V_{GS} = 0; V_{DS} = 10 V; f = 1 MHz	–	4	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	V_{GS} = 0 to 10 V; V_{DD} = 50 V; I_D = 250 mA	–	2	10	ns
t_{off}	turn-off time	V_{GS} = 0 to 10 V; V_{DD} = 50 V; I_D = 200 mA	–	5	20	ns

N-channel enhancement mode vertical D-MOS transistor

PMBF107

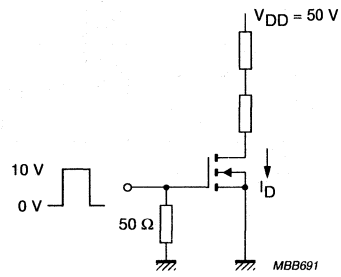


Fig.2 Switching time test circuit.

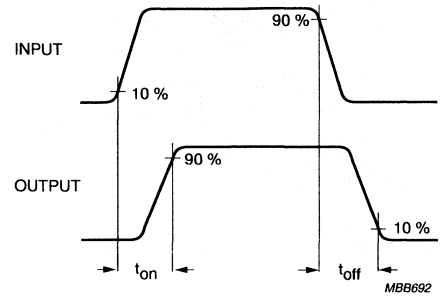


Fig.3 Input and output waveforms.

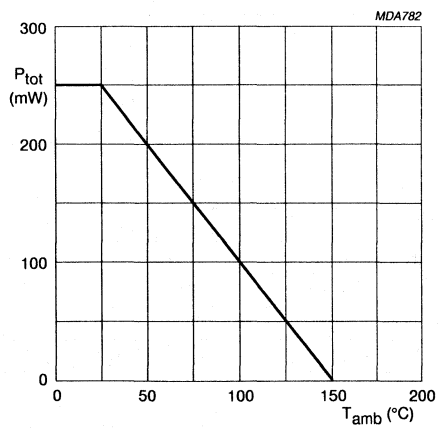


Fig.4 Power derating curve.

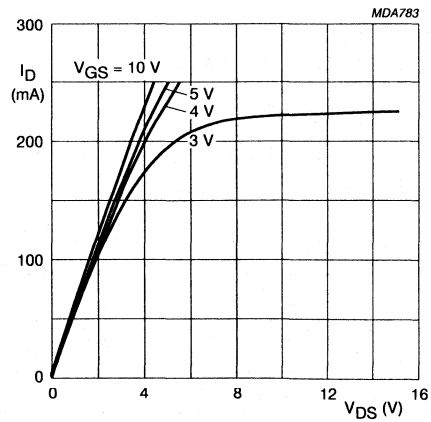


Fig.5 Typical output characteristics; T_j = 25 °C.

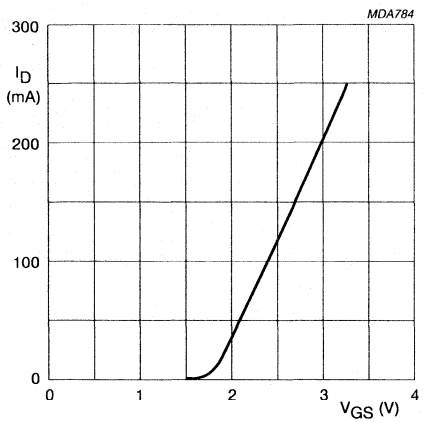


Fig.6 Typical transfer characteristic; V_{DS} = 10 V; T_j = 25 °C.

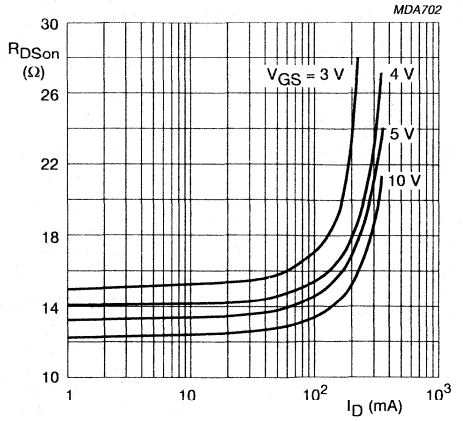


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

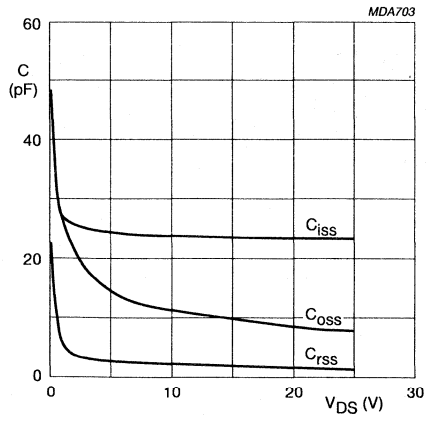


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

N-channel enhancement mode vertical D-MOS transistor

PMBF170

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope. Designed for use as a Surface Mounted Device (SMD) in thin and thick-film circuits with applications in relay, high-speed and line transformer drivers.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	60	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	250	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Drain-source on-resistance I_D = 200 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	2.5	Ω
		max.	5.0	Ω
Transfer admittance I_D = 200 mA; V_{DS} = 10 V	$\lvert Y_{fs} \rvert$	min.	100	mS
		typ.	200	mS

PINNING - SOT23

1 = gate
2 = source
3 = drain

Marking code:

PMBF170 = PKX

PIN CONFIGURATION

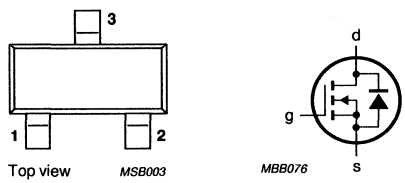


Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

PMBF170

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)				
Drain-source voltage	V_{DS}	max.	60	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	250	mA
Drain current (peak)	I_{DM}	max.	500	mA
Total power dissipation up to		max.	300	mW (note 1)
T_{amb} = 25 °C (note 1)	P_{tot}	max.	250	mW (note 2)
Storage temperature range	T_{stg}		−65 to +150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	430	K/W
From junction to ambient (note 2)	$R_{th\ j\text{-}a}$	=	500	K/W

Notes

1. Mounted on ceramic substrate measuring 10 mm × 8 mm × 0.7 mm.
2. Mounted on printed-circuit board.

N-channel enhancement mode vertical D-MOS transistor

PMBF170

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage			
I_D = 10 μA; V_{GS} = 0	$V_{(BR)\ DSS}$	min.	60 V
		typ.	90 V
Drain-source leakage current			
V_{DS} = 25 V; V_{GS} = 0	I_{DSS}	max.	500 nA
V_{DS} = 48 V; V_{GS} = 0	I_{DSS}	max.	1 μA
Gate-source leakage current			
V_{GS} = 15 V; V_{DS} = 0	I_{GSS}	max.	10 nA
Gate-source cut-off voltage			
I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min.	0.8 V
		max.	3.0 V
Drain-source on-resistance			
I_D = 200 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	2.5 Ω
		max.	5.0 Ω
Transfer admittance			
I_D = 200 mA; V_{DS} = 10 V	$\lvert Y_{fs} \rvert$	min.	100 mS
		typ.	200 mS
Input capacitance			
V_{DS} = 10 V; V_{GS} = 0 V; f = 1 MHz	C_{iss}	typ.	25 pF
		max.	40 pF
Output capacitance			
V_{DS} = 10 V; V_{GS} = 0 V; f = 1 MHz	C_{oss}	typ.	22 pF
		max.	30 pF
Feedback capacitance			
V_{DS} = 10 V; V_{GS} = 0 V; f = 1 MHz	C_{rss}	typ.	6 pF
		max.	10 pF
Switching times			
V_{GS} = 0 to 10 V; I_D = 200 mA ; V_{DD} = 50 V	t_{on}	max.	10 ns
	t_{off}	max.	15 ns

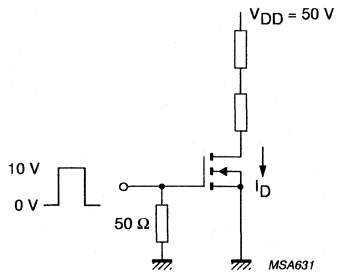


Fig.2 Switching times test circuit.

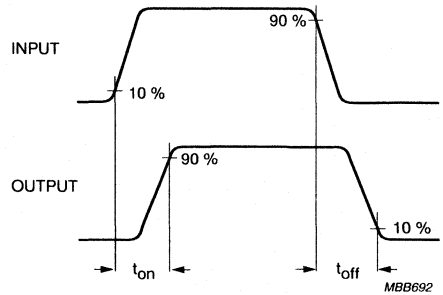
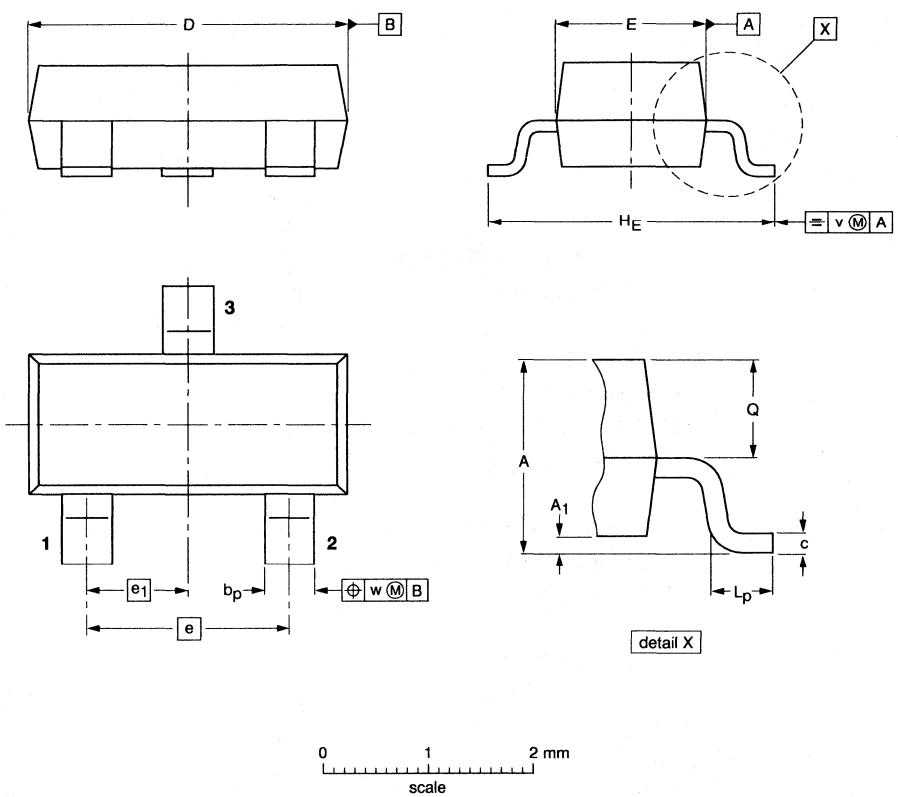


Fig.3 Input and output waveforms.

PACKAGE OUTLINES

Package	Surface-mount	Page
SOT23	yes	1870
SOT54 (TO-92)	no	1871
SOT54variant (TO-92variant)	no	1872
SOT78 (TO-220AB)	no	1873
SOT89	yes	1874
SOT96-1 (SO8)	yes	1875
SOT137-1 (SO24)	yes	1876
SOT186 (TO-220 exposed tabs)	no	1877
SOT186A (TO-220)	no	1878
SOT223	yes	1879
SOT226 (low-profile TO-220)	no	1880
SOT263 (5-lead TO-220)	no	1881
SOT263-01 (lead option TO-220)	no	1882
SOT323	yes	1883
SOT338-1 (SSOP16)	yes	1884
SOT340-1 (SSOP24)	yes	1885
SOT363	yes	1886
SOT404	yes	1887
SOT426	yes	1888
SOT428	yes	1889
SOT429 (TO-247)	no	1890
SOT457 (TSOP6)	yes	1891

Plastic surface mounted package; 3 leads **SOT23**

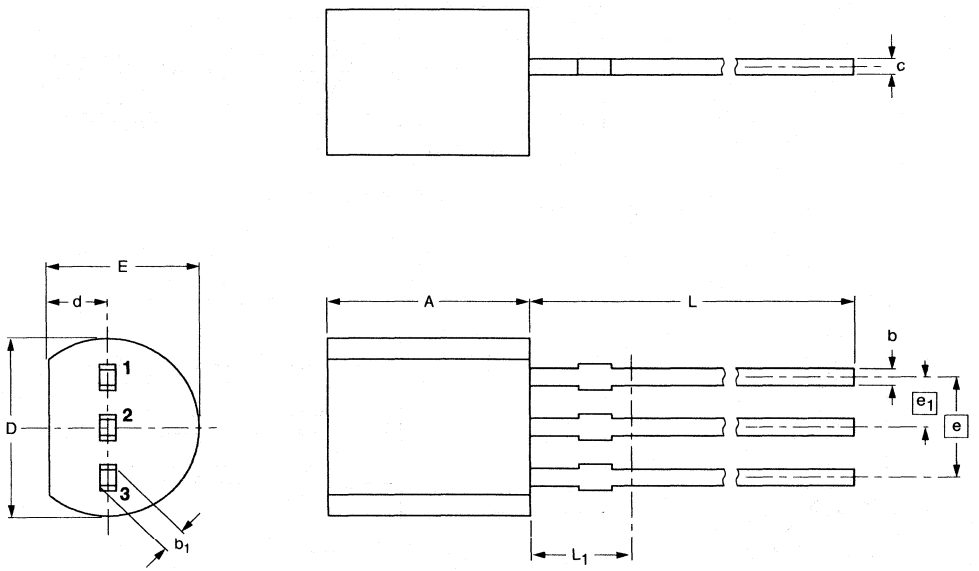


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max.	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT23						97-02-28

Plastic single-ended leaded (through hole) package; 3 leads **SOT54**



DIMENSIONS (mm are the original dimensions)

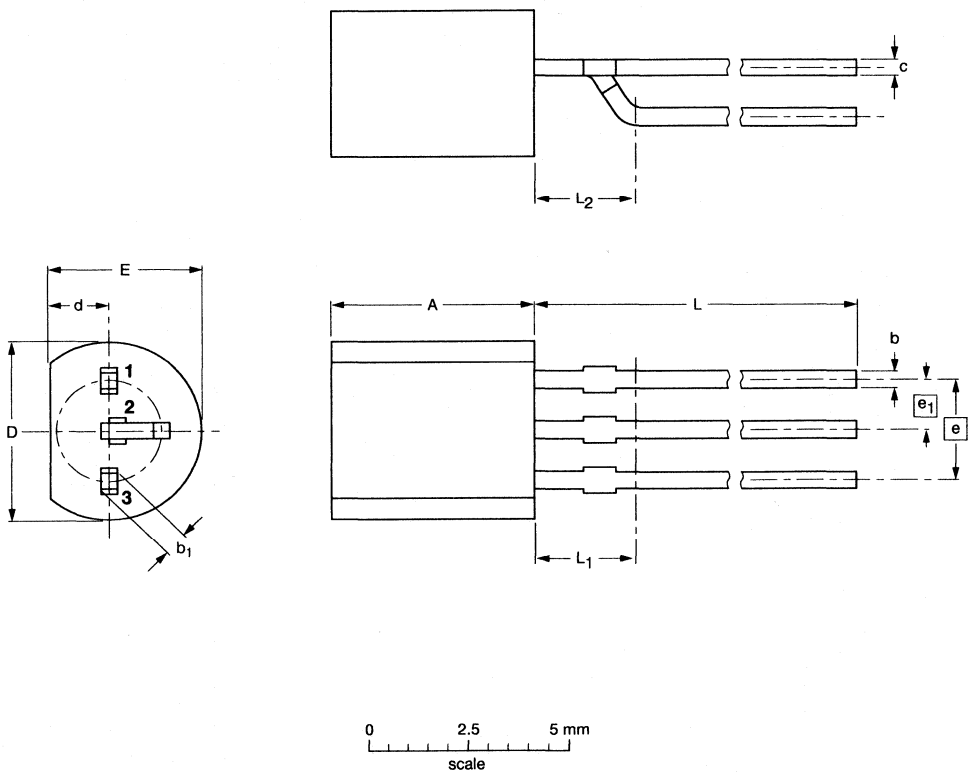
UNIT	A	b	b_1	c	D	d	E	e	e_1	L	L_1(1)
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT54		TO-92	SC-43			97-02-28

Plastic single-ended leaded (through hole) package; 3 leads (on-circle) **SOT54 variant**



DIMENSIONS (mm are the original dimensions)

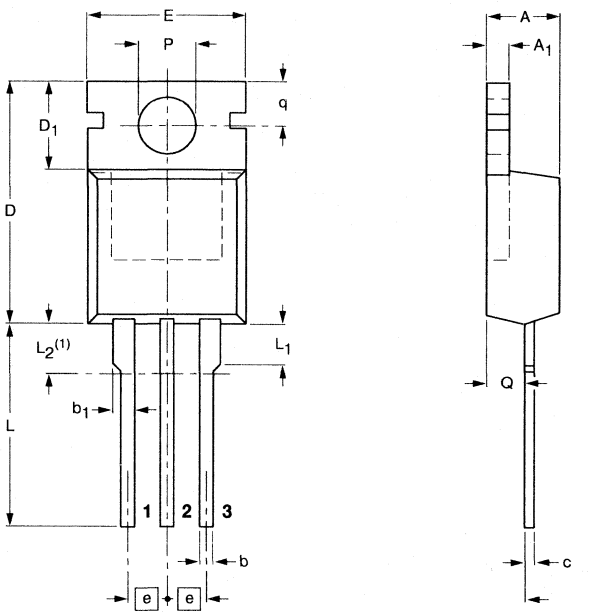
UNIT	A	b	b_1	c	D	d	E	e	e_1	L	L_1(1) max	L_2 max
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5	2.5

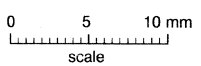
Notes

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT54 variant		TO-92 variant	SC-43			98-03-26

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB **SOT78**





DIMENSIONS (mm are the original dimensions)

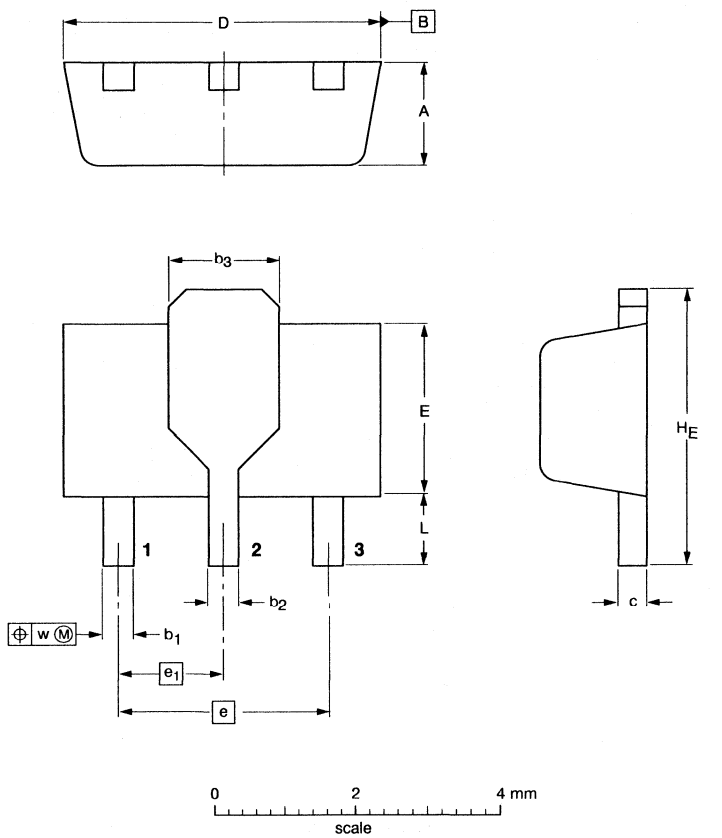
UNIT	A	A_1	b	b_1	c	D	D_1	E	e	L	L_1	$L_2^{(1)}$ max.	P	q	Q
mm	4.5 4.1	1.39 1.27	0.9 0.7	1.3 1.0	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	2.54	15.0 13.5	3.30 2.79	3.0	3.8 3.6	3.0 2.7	2.6 2.2

Note

1. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT78		TO-220AB				97-06-11

Plastic surface mounted package; drain pad for good heat transfer; 3 leads **SOT89**



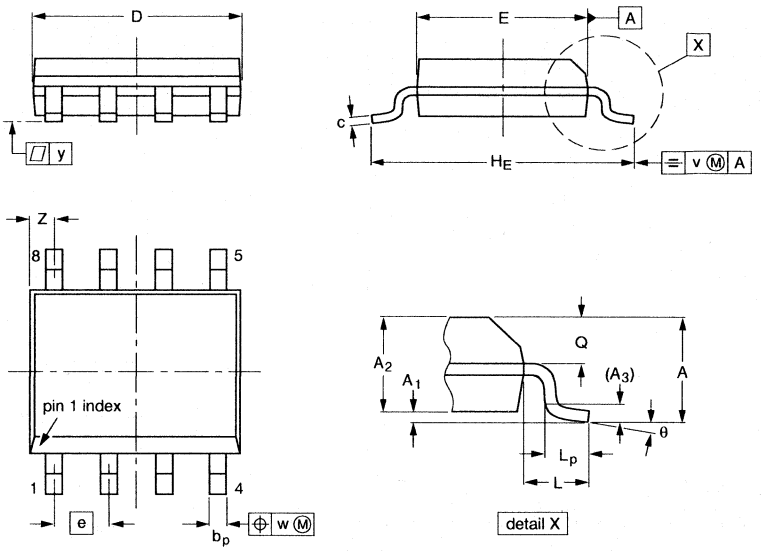
DIMENSIONS (mm are the original dimensions)

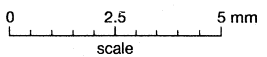
UNIT	A	b_1	b_2	b_3	c	D	E	e	e_1	H_E	L min.	w
mm	1.6 1.4	0.48 0.35	0.53 0.40	1.8 1.4	0.44 0.37	4.6 4.4	2.6 2.4	3.0	1.5	4.25 3.75	0.8	0.13

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT89						97-02-28

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

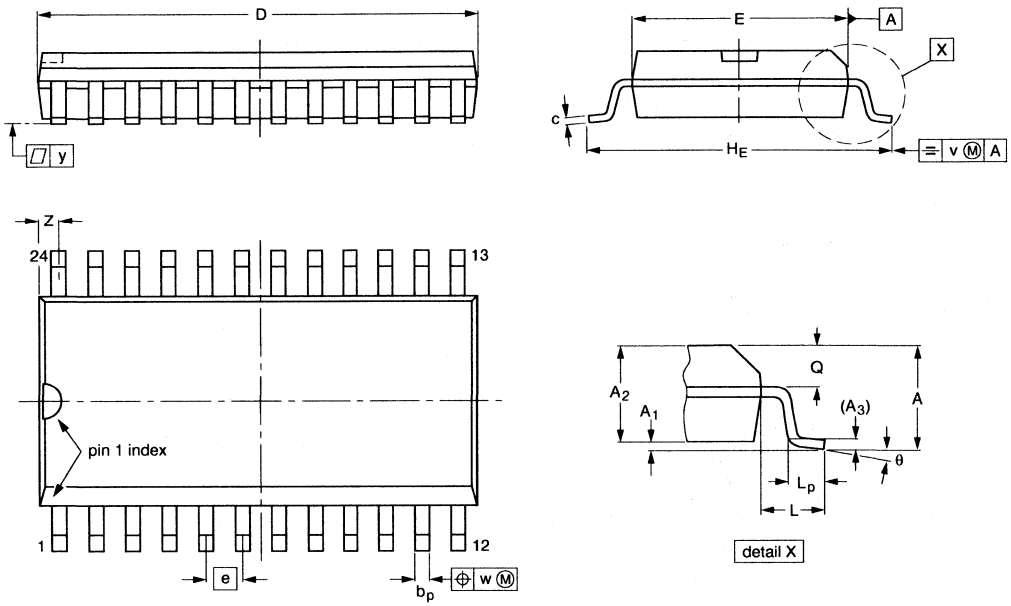
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT96-1	076E03S	MS-012AA			~~95-02-04~~ 97-05-22

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

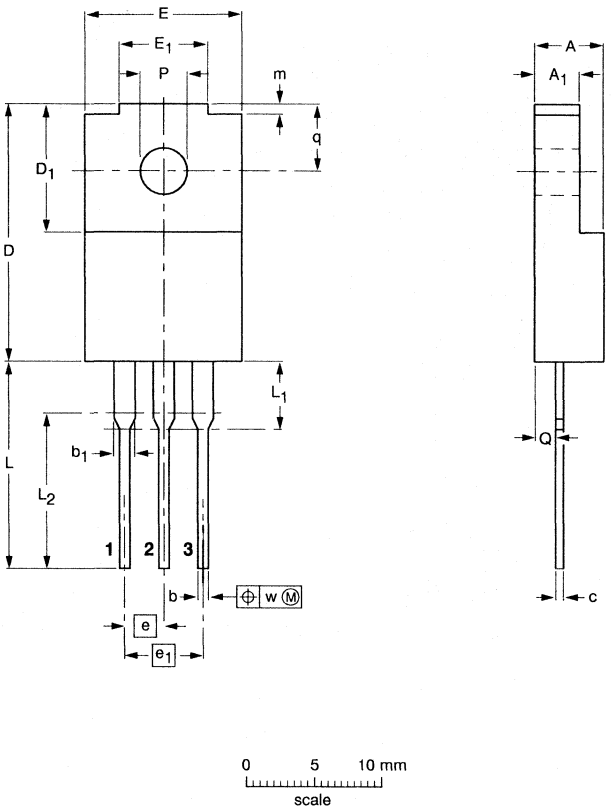
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3 lead TO-220 exposed tabs **SOT186**



DIMENSIONS (mm are the original dimensions)

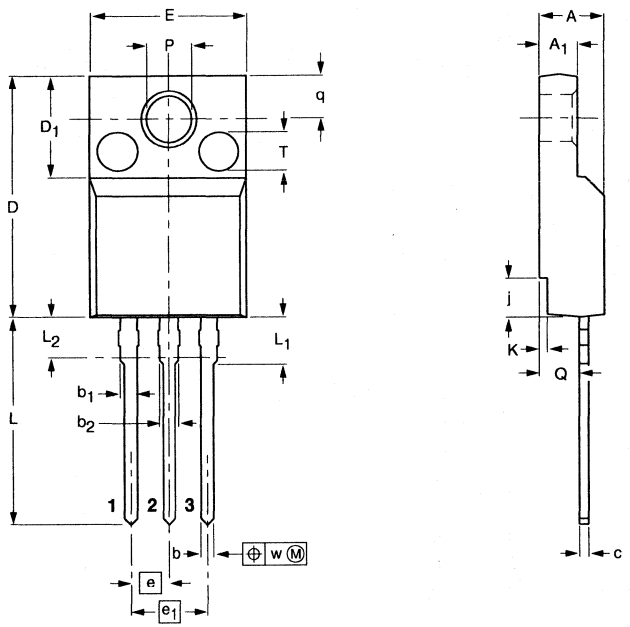
UNIT	A	A_1	b	b_1	c	D	D_1	E	E_1	e	e_1	L	L_1(1)	L_2	m	P	Q	q	w
mm	4.4 4.0	2.9 2.5	0.9 0.7	1.5 1.3	0.55 0.38	17.0 16.4	7.9 7.5	10.2 9.6	5.7 5.3	2.54	5.08	14.3 13.5	4.8 4.0	10	0.9 0.5	3.2 3.0	1.4 1.2	4.4 4.0	0.4

Note

1. Terminal dimensions within this zone are uncontrolled. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT186		TO-220				97-06-11

Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3 lead TO-220 **SOT186A**



0 5 10 mm
scale

DIMENSIONS (mm are the original dimensions)

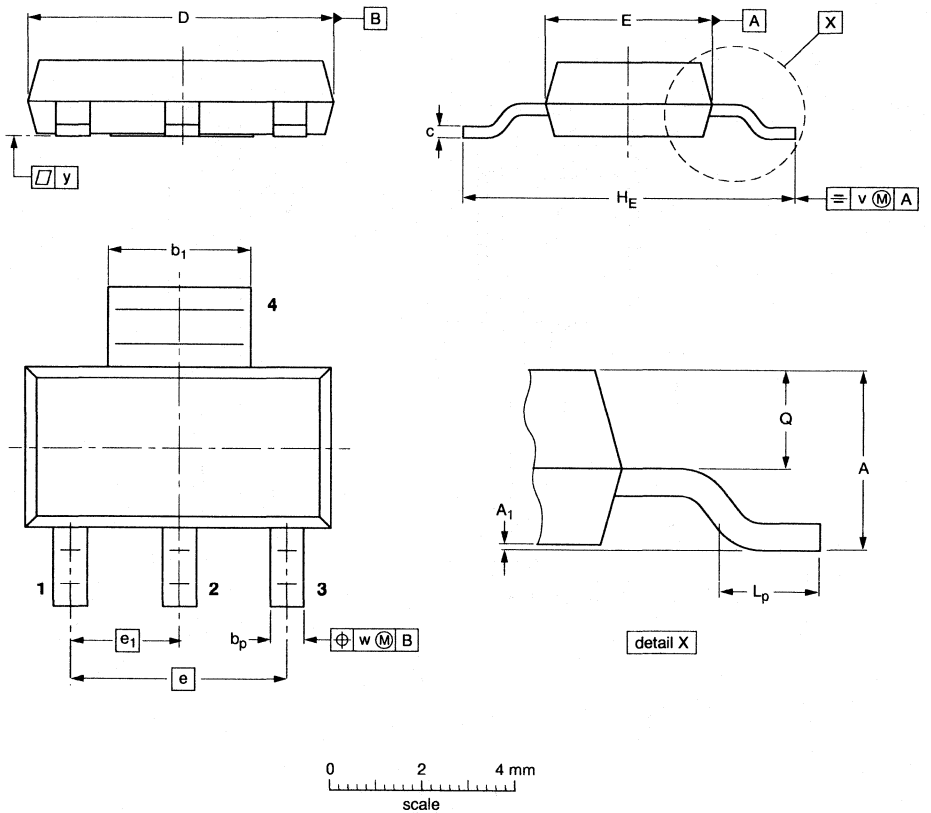
UNIT	A	A_1	b	b_1	b_2	c	D	D_1	E	e	e_1	j	K	L	L_1	L_2 (1) max.	P	Q	q	T (2)	w
mm	4.6 4.0	2.9 2.5	0.9 0.7	1.1 0.9	1.4 1.2	0.7 0.4	15.8 15.2	6.5 6.3	10.3 9.7	2.54	5.08	2.7 2.3	0.6 0.4	14.4 13.5	3.30 2.79	3	3.2 3.0	2.6 2.3	3.0 2.6	2.5	0.4

Notes

1. Terminal dimensions within this zone are uncontrolled. Terminals in this zone are not tinned.
2. Both recesses are ∅ 2.5 × 0.8 max. depth

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT186A		TO-220				97-06-11

Plastic surface mounted package; drain pad for good heat transfer; 4 leads **SOT223**

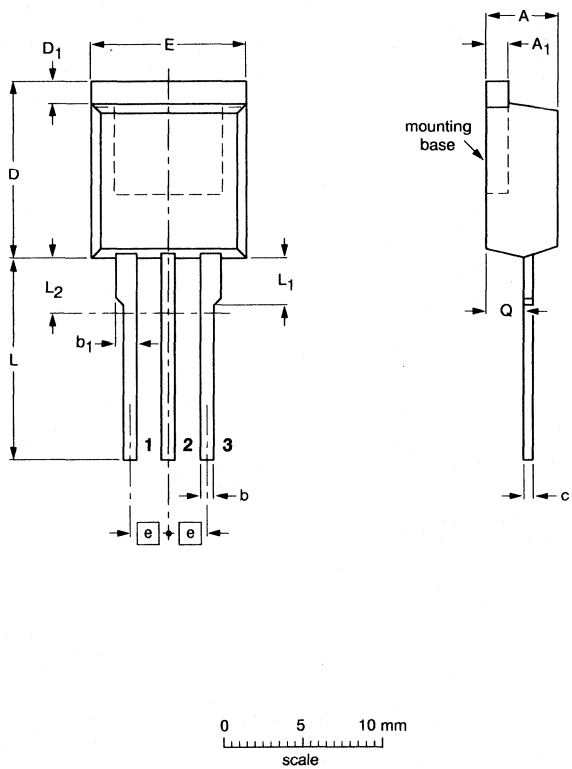


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT223						~~96-11-11~~ 97-02-28

Plastic single-ended package; 3 lead low-profile TO-220 **SOT226**



DIMENSIONS (mm are the original dimensions)

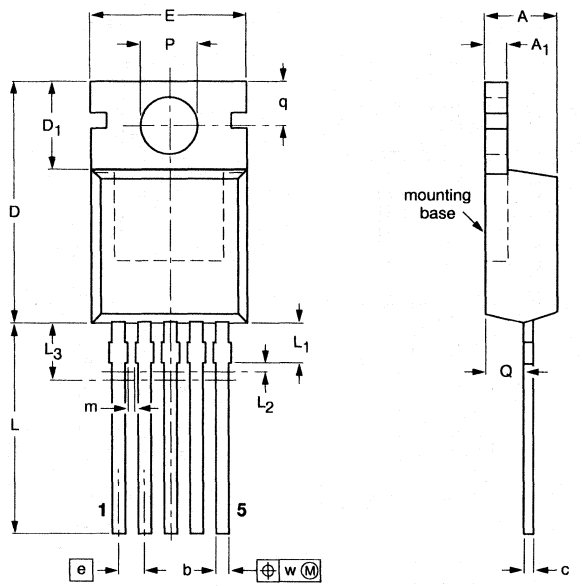
UNIT	A	A_1	b	b_1	c	D	D_1	E	e	L	L_1	$L_2^{(1)}$ max	Q
mm	4.5 4.1	1.39 1.27	0.9 0.7	1.3 1.0	0.7 0.4	11.0 10.0	1.5 1.1	10.3 9.7	2.54	15.0 13.5	3.30 2.79	3.0	2.6 2.2

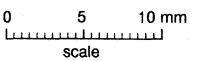
Note

1. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT226		low-profile TO-220				97-06-11

Plastic single-ended package; heatsink mounted; 1 moumting hole; 5-lead TO-220 **SOT263**





DIMENSIONS (mm are the original dimensions)

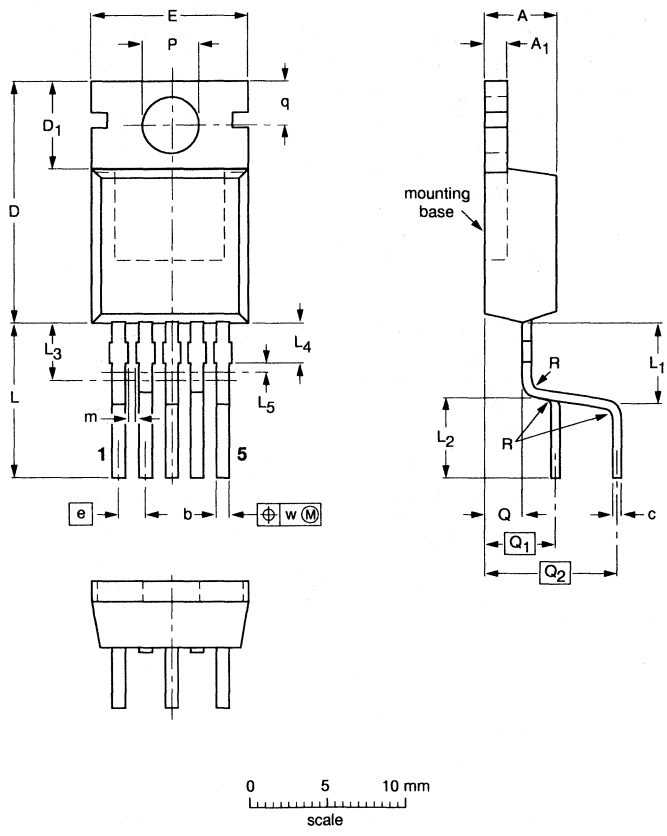
UNIT	A	A_1	b	c	D	D_1	E	e	L	L_1 (1)	L_2 (2)	L_3 (3) max.	m	P	q	Q	w
mm	4.5 4.1	1.39 1.27	0.9 0.7	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	1.7	15.0 13.5	2.4 1.6	0.5	3.5	0.8 0.6	3.8 3.6	3.0 2.7	2.6 2.2	0.4

Notes

1. Terminal dimensions are uncontrolled in this zone.
2. Positional accuracy of the terminals is controlled in this zone.
3. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT263		5-lead TO-220				97-06-11

Plastic single-ended package; heatsink mounted; 1 mounting hole; 5-lead TO-220 lead form option **SOT263-01**



DIMENSIONS (mm are the original dimensions)

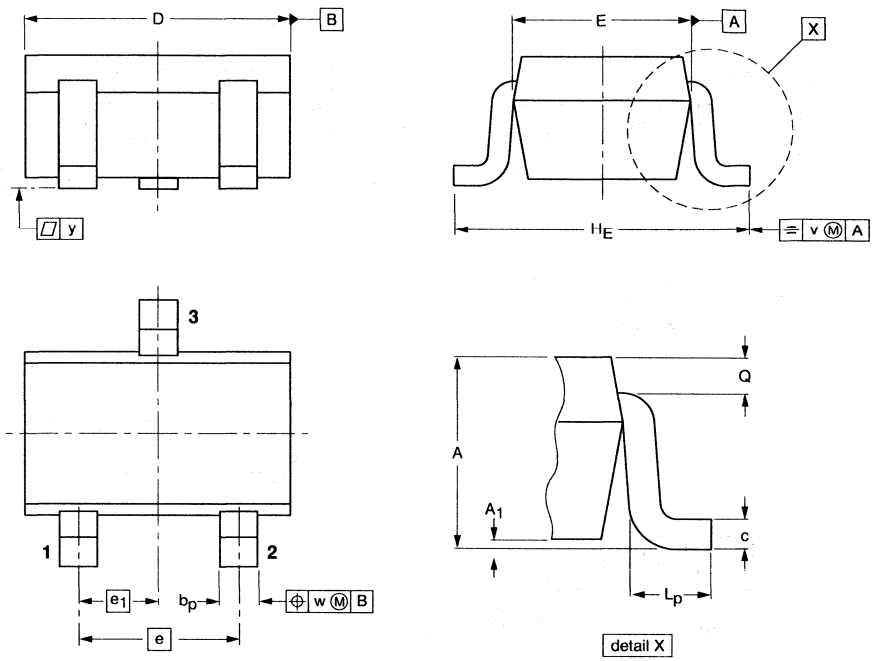
UNIT	A	A_1	b	c	D	D_1	E	e	L	L_1	L_2	L_3(1) max.	L_4(2)	L_5(3) max.	m	P	q	Q	Q_1	Q_2	R	w
mm	4.5 4.1	1.39 1.27	0.90 0.75	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	1.7	9.8 9.7	5.9 5.3	5.2 5.0	3.5	2.4 1.6	0.5	0.8 0.6	3.8 3.6	3.0 2.7	2.0	4.5	8.2	0.5	0.4

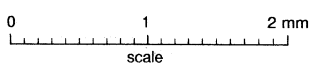
Notes

1. Terminals in this zone are not tinned.
2. Positional accuracy of the terminals is controlled in this zone.
3. Terminal dimensions are uncontrolled in this zone.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT263-01		5-lead (option) TO-220				97-06-11

Plastic surface mounted package; 3 leads **SOT323**



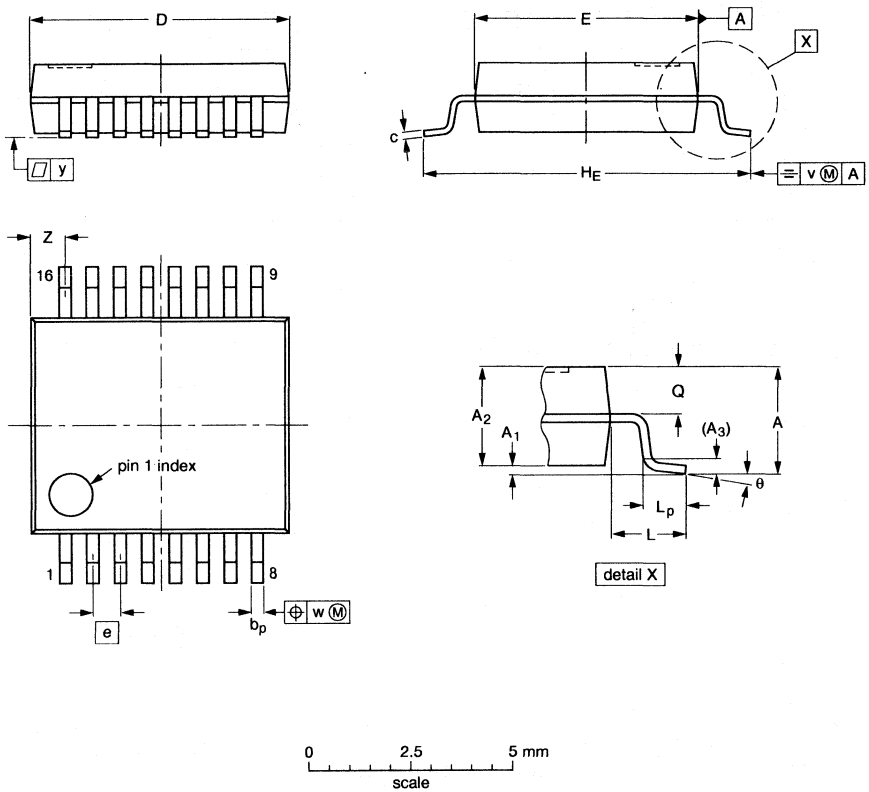


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.8	0.1	0.4 0.3	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT323			SC-70			97-02-28

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

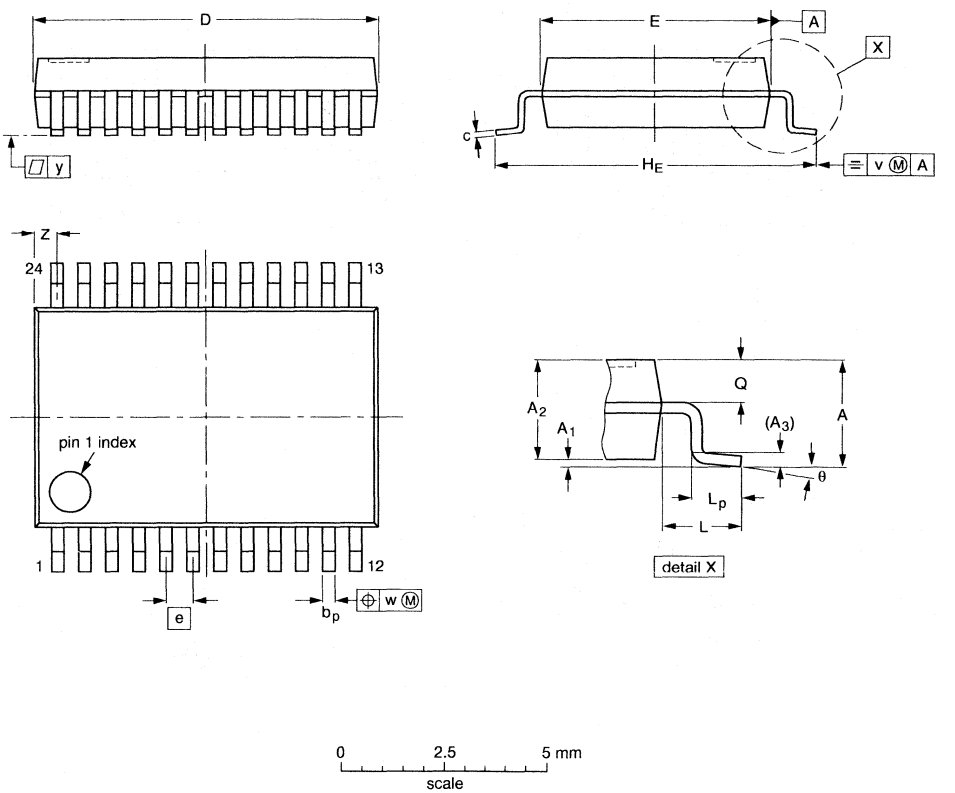
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150AC				~~94-01-14~~ 95-02-04

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

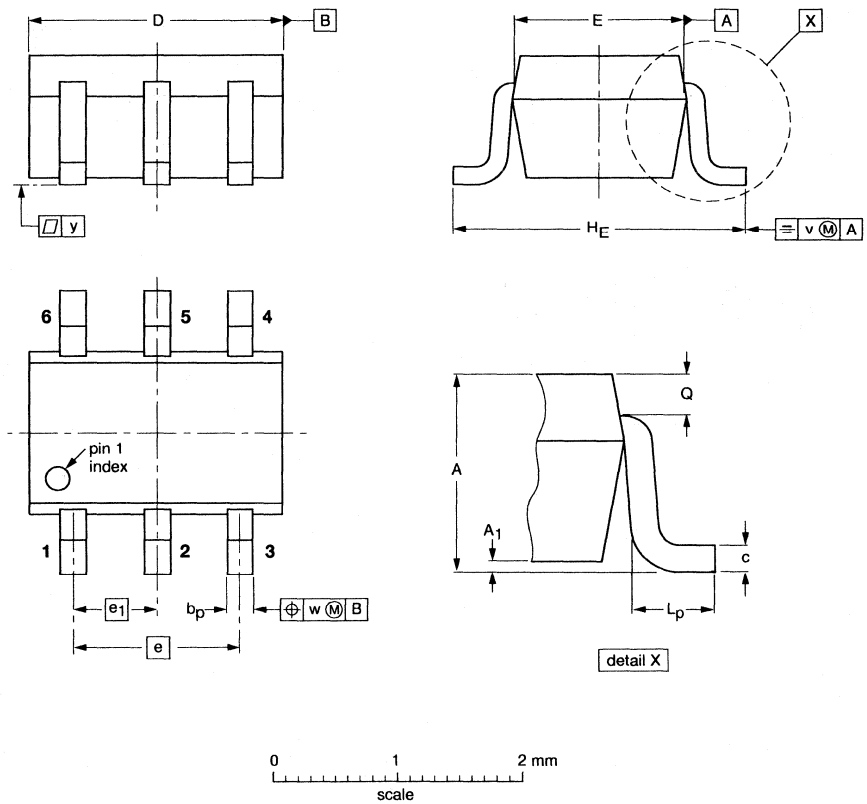
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				~~93-09-08~~ 95-02-04

Plastic surface mounted package; 6 leads **SOT363**

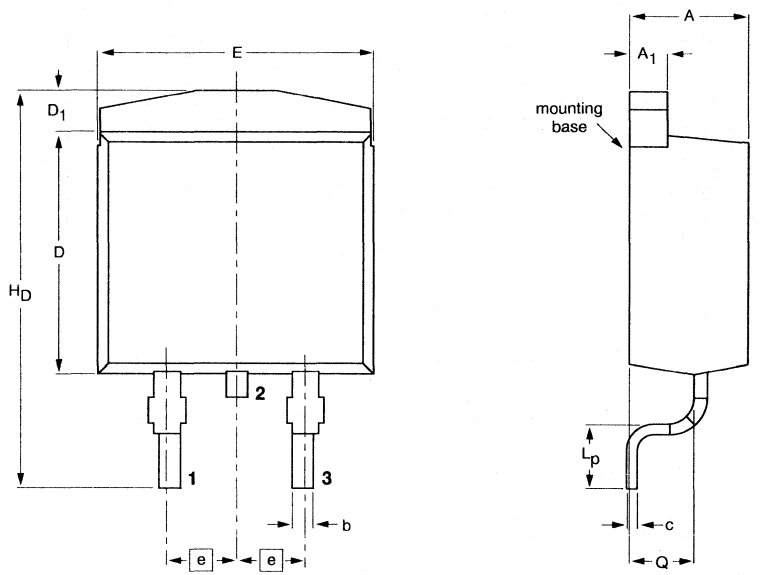


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT363			SC-88			97-02-28

Plastic single-ended surface mounted package (Philips version of D2-PAK); 3 leads (one lead cropped) **SOT404**

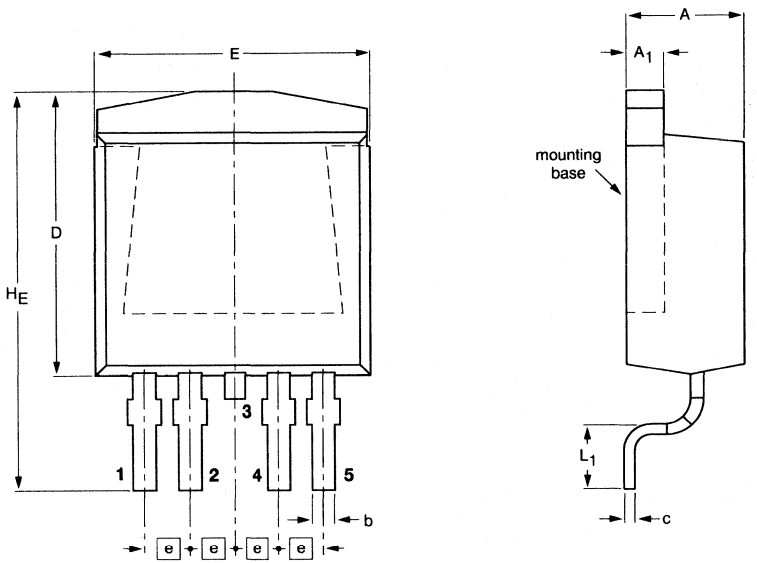


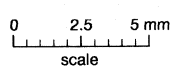
DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	c	D	D_1	E	e	L_p	H_D	Q
mm	4.5 4.1	1.40 1.27	0.85 0.60	0.64 0.46	9.65 8.65	1.6 1.2	10.3 9.7	2.54	2.9 2.1	15.4 14.8	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT404						98-04-07

Plastic single-ended surface mounted package (Philips version of D2-PAK); 5 leads (one lead cropped) **SOT426**



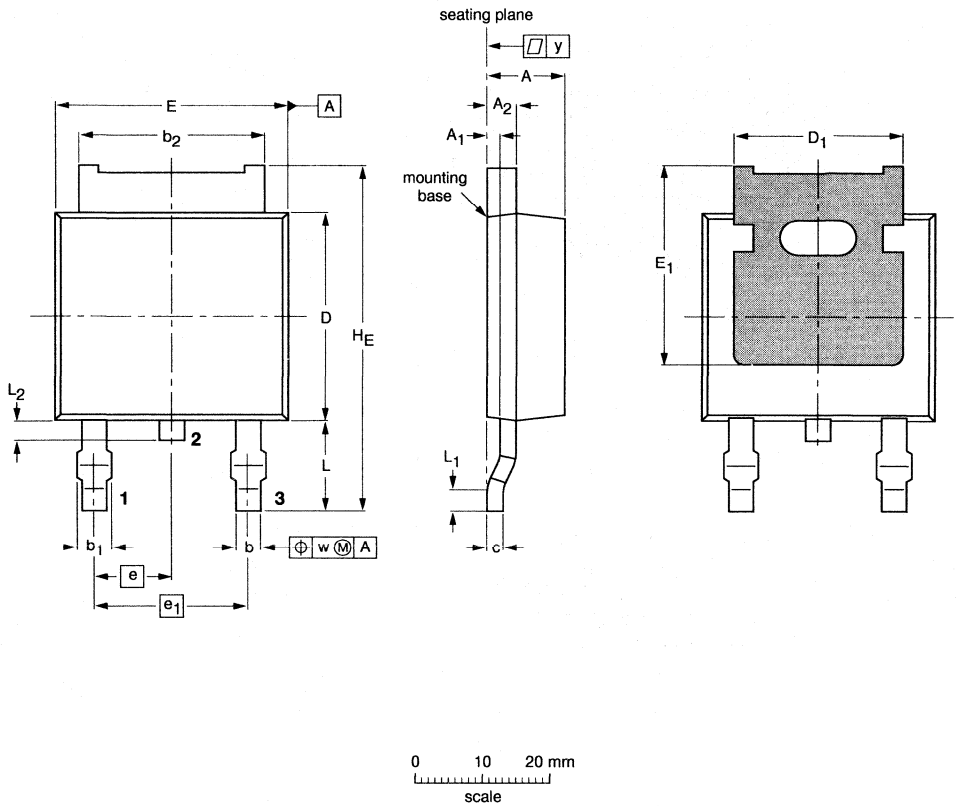


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	c	D max.	E	e	L_1	H_E
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	10.30 9.70	1.70	2.90 2.10	15.80 14.80

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT426						98-04-07

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads (one lead cropped) **SOT428**



DIMENSIONS (mm are the original dimensions)

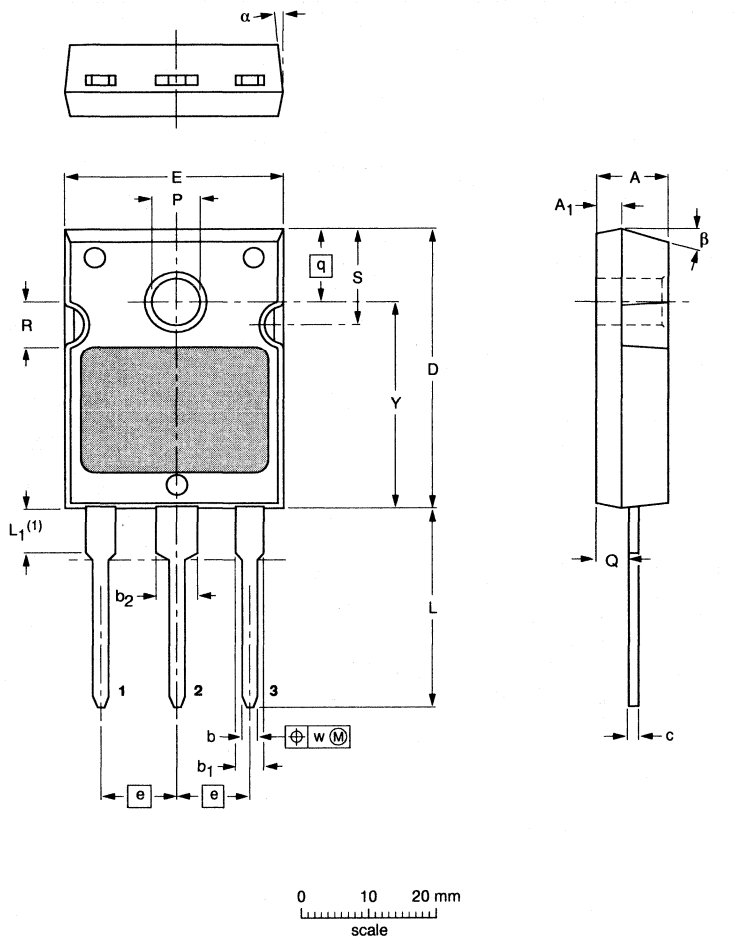
UNIT	A max.	A_1 (1)	A_2	b	b_1 max.	b_2	c	D max.	D_1 max.	E max.	E_1 min.	e	e_1	H_E max.	L	L_1 min.	L_2	w	y max.
mm	2.38 2.22	0.65 0.45	0.89 0.71	0.89 0.71	1.1 0.9	5.36 5.26	0.4 0.2	6.22 5.98	4.81 4.45	6.73 6.47	4.0	2.285	4.57	10.4 9.6	2.95 2.55	0.5	0.7 0.5	0.2	0.2

Note

1. Measured from heatsink back to lead.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT428						98-04-07

Plastic single-ended through-hole package; heatsink mounted; 1 mounting hole; 3-lead TO-247 **SOT429**



DIMENSIONS (mm are the original dimensions)

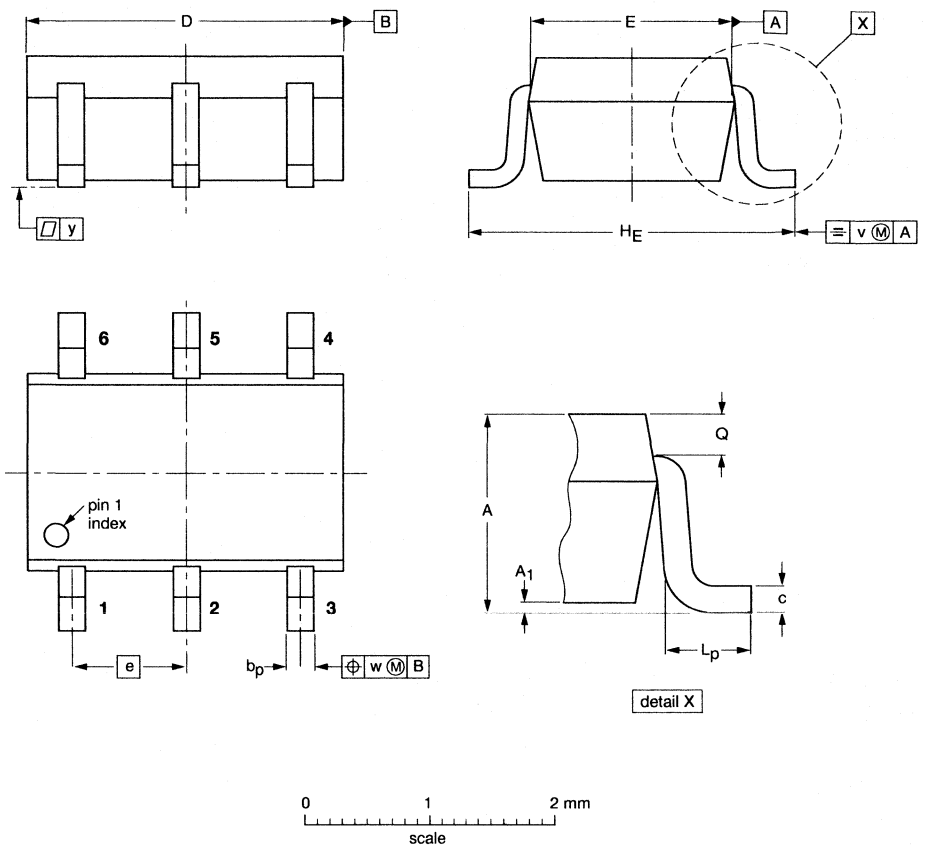
UNIT	A	A_1	b	b_1	b_2	c	D	E	e	L	L_1(1)	P	Q	q	R	S	w	Y	α	β
mm	5.3 4.7	1.9 1.7	1.2 0.9	2.2 1.8	3.2 2.8	0.9 0.6	21 20	16 15	5.45	16 15	4.0 3.6	3.7 3.3	2.6 2.4	5.3	3.5 3.3	7.5 7.1	0.4	15.7 15.3	6° 4°	17° 13°

Note

1. Tinning of terminals are uncontrolled within zone L_1.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT429		TO-247				98-04-07

Plastic surface mounted package; 6 leads **SOT457**



DIMENSIONS (mm are the original dimensions)

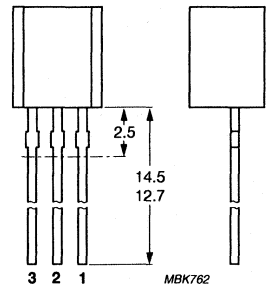
UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT457			SC-74			97-02-28

LEADFORM OPTIONS

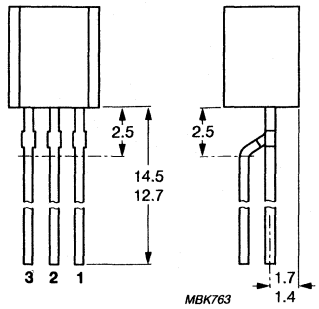
LEADFORM OPTIONS

- These options require a special part number before ordering.
- Contact your local Philips Semiconductors representative for pricing, minimum order quantities and part number.



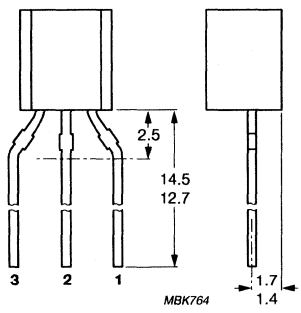
SOT54 (TO-92)

Fig.1 Leadform 54.



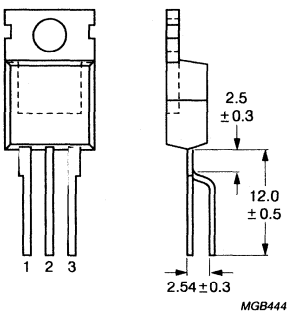
SOT54var (TO-92)

Fig.2 Leadform 54V.



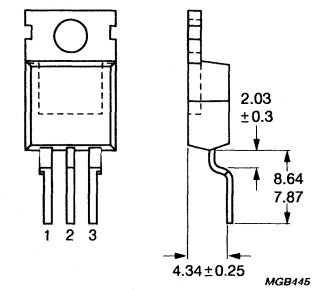
SOT54A (TO-92)

Fig.3 Leadform 54A.



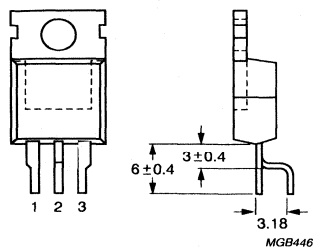
SOT78 (TO-220)

Fig.4 Leadform 78-02.



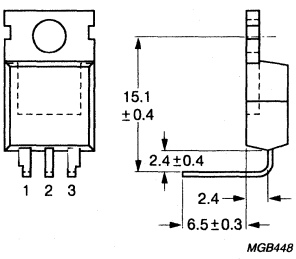
SOT78 (TO-220)

Fig.5 Leadform 78-05W.



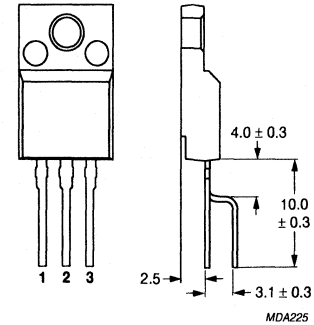
SOT78 (TO-220)

Fig.6 Leadform 78-13.



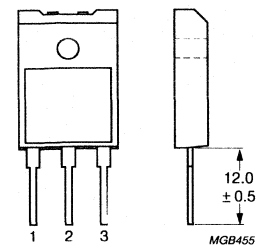
SOT78 (TO-220)

Fig.7 Leadform 78-15.



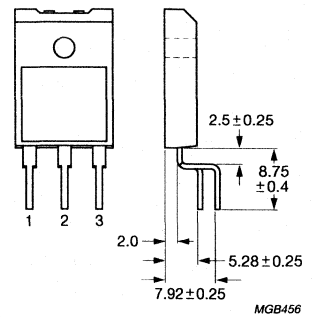
SOT186

Fig.8 Leadform 186A-02



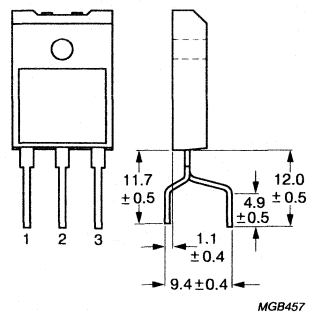
SOT199

Fig.9 Leadform 199-01.



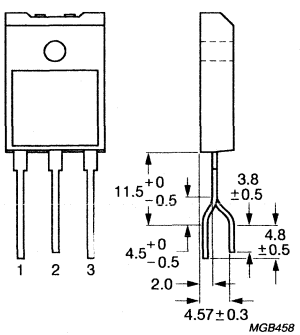
SOT199

Fig.10 Leadform 199-02.



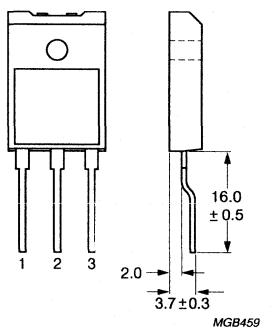
SOT199

Fig.11 Leadform 199-04.



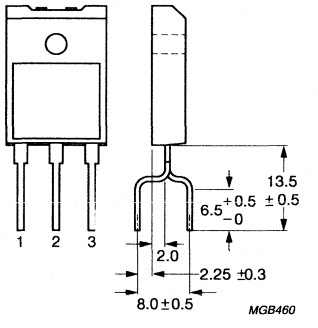
SOT199

Fig.12 Leadform 199-05.



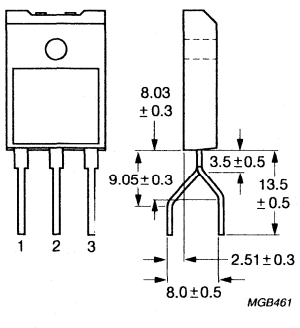
SOT199

Fig.13 Leadform 199-06.



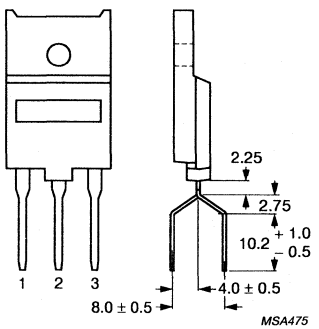
SOT199

Fig.14 Leadform 199-08.



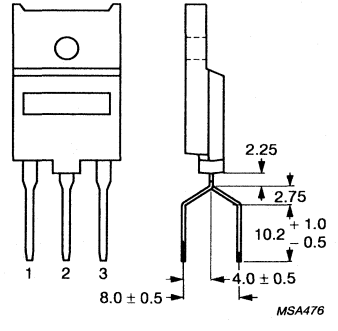
SOT199

Fig.15 Leadform 199-09.



SOT399

Fig.16 Leadform 399-01



SOT399

Fig.17 Leadform 399-02.

MOUNTING AND SOLDERING

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INTRODUCTION

There are two basic forms of electronic component construction, those with leads for through-hole mounting and (micro)miniature types for surface mounting. Through-hole mounting gives a very rugged construction and uses well established soldering methods. Surface mounting has the advantages of high packing density plus high-speed automated assembly.

LEADED DEVICES

The following general rules are for the save handling and soldering of leaded devices. Special rules for particular types may apply and, for these, instructions are given in the individual data sheets. With all components, excessive forces or heat can cause serious damage and should always be avoided.

Handling

- Avoid perpendicular forces on the body of the device
- Avoid sudden forces on the leads or body. These forces are often much greater than allowed
- Avoid high acceleration as a result of any shock, e.g. dropping the device on a hard surface
- During bending, support the leads between body or stud and the bending point
- During the bending process, axial forces on the body must not exceed 20 N
- Bending the leads through 90° is allowed at any distance from the body when it is possible to support the leads during bending without contacting the body or weldings
- Bending close to the body or stud without supporting the leads is only allowed if the bend radius is greater than 0.5 mm
- Twisting the leads is allowed at any distance from the body or stud only if the lead is properly clamped between body or stud and the twisting point
- Without clamping, twisting the leads is allowed only at a distance of greater than 3 mm from the body; the torque angle must not exceed 30°
- Straightening bent leads is allowed only if the applied pulling force in the axial direction does not exceed 20 N and the total pull duration is not longer than 5 s.

Soldering

- Avoid any force on the body or leads during or immediately after soldering
- Do not correct the position of an already soldered device by pushing, pulling or twisting the body
- Avoid fast cooling after soldering.

The maximum allowable soldering time is determined by:

- Package type
- Mounting environment
- Soldering method
- Soldering temperature
- Distance between the point of soldering and the seal of the device's body.

GENERAL DATA AND INSTRUCTIONS FOR THE SOT186A; SOT263; TO 220AB

General rules

1. Fasten the device to the heatsink before soldering the leads.
2. Avoid stress to the leads.
3. Keep mounting tool (e.g. screwdriver) clear of the plastic body.
4. The rectangular washer may only touch the plastic part of the body; it should not exert any force on that part (screw mounting).

Mounting methods

CLIP MOUNTING

Mounting with a spring clip gives:

1. A good thermal contact under the crystal area, and slightly lower thermal resistance than screw mounting.
2. Safe insulation for mains operation.

Minimum force for good heat transfer is 10 N.

Maximum force to avoid damaging the device is 80 N.

M3 SCREW MOUNTING

It is recommended that the rectangular spacing washer is inserted between screw head and mounting tab.

Do not use self-tapping screws.

Mounting torque for screw mounting:

For thread-forming screws these are final values.

Minimum torque for good heat transfer is 0.55 Nm.

Maximum torque to avoid damaging the device is 0.80 Nm.

When a nut or screw is driven directly against the tab, the torques are as follows:

Minimum torque for good heat transfer is 0.40 Nm.

Maximum torque to avoid damaging the device is 0.60 Nm.

RIVET MOUNTING NON-INSULATED

The device should not be pop-rivetted to the heatsink. It is permissible to press-rivet the metal tab providing that eyelet rivets of soft material are used, and the press forces are slowly and carefully controlled.

This method is not permitted for full-pack envelopes because it will damage the plastic encapsulation.

Heatsink requirements

Flatness in the mounting area: 0.02 mm maximum per 10 mm.
Mounting holes must be deburred, for further information see clip and screw mounting instructions.

Heatsink compound

The thermal resistance from mounting base to heatsink ($R_{th\ mb\text{-}h}$) can be reduces by applying a metallic oxide compound between the contact surfaces. Values given are of thermal resistance using this type of compound. Dow Corning 340 Heat sink compound is recommended. For insulated mounting, the compound should be applied to the bottom of both device and insulator.

Thermal data for heatsink mounting methods (TO220 only)

Typical figures, for exact figures see data for each device type.

$R_{th\ mb\text{-}h}$	Thermal resistance from mounting base to heatsink	K/W	
	Mounting method	**Clip**	**Screw**
direct with heatsink compound		0.3	0.5
direct without heatsink compound		1.4	1.4
with heatsink compound and 0.1 mm maximum mica insulator		2.2	–
with heatsink compound and 0.25 mm maximum alumina insulator		0.8	–
with heatsink compound and 0.05 mm mica insulator			
	insulated up to 500 V	–	1.4
	insulated up to 800 V/1 000 V	–	1.6
without heatsink compound and 0.05 mm mica insulator			
	insulated up to 500 V	–	3.0
	insulated up to 800 V/1 000 V	–	4.5

Additional insulators are generally not required when mounting the full-pack outlines.

Soldering

Recommendation for devices with a maximum junction temperature rating <175 °C:

DIP OR WAVE SOLDERING

Maximum permissible solder temperature is 260 °C at a distance from the body of >5 mm and for a total contact time with soldering bath or waves of <7 s.

HAND SOLDERING

Maximum permissible solder temperature is 275 °C at a distance from the body of >3 mm and for a total contact time with the soldering iron of <5 s.

The body of the device must not touch anything with a temperature >200 °C.

It is not permitted to solder the metal tab of the device to a heatsink, otherwise the junction temperature rating will be exceeded.

Avoid any force on body and leads during or after soldering; do not correct the position of the device or of its leads after soldering.

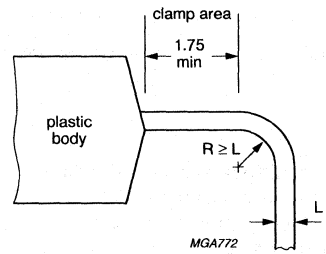
Lead bending

Maximum permissible tensile force on the body for 5 seconds is 20 N. The leads can be bent, twisted or straightened.

To keep forces within the above mentioned limits the leads should always be clamped rigidly near the body during bending. This is also to prevent damage to the seal of the leads within the plastic body.

Leads can be bent as near to the body as required, but adequate length should always be allowed for clamping. This is a minimum of 1.75 mm from the body to the start of a bend radius.

The internal radius of bend should never be less than the thickness of the lead. A minimum radius of at least 1.5 × lead thickness is preferred. See Fig.1. Surface cracks in the dip tin coating on the lead are common when a radius less than 1.5 × lead thickness is used. Although exposing the copper material, these cracks do not affect the mechanical strength of the lead. Lead forming by Philips is available as an option on all products supplied in these outlines.



Dimensions in mm.

Fig.1 Minimum lead bend radius.

Additional guide-lines

It is recommended that where a device is rigidly secured to a heatsink which is in turn rigidly secured to a PCB, that a bend is put in the leads to act as an expansion loop. This will prevent differential expansion of the mounting parts transferring stress to the soldering joint, as shown in Fig.2. This is only necessary where the device is mounted so rigidly that expansion forces are transmitted through the assembly.

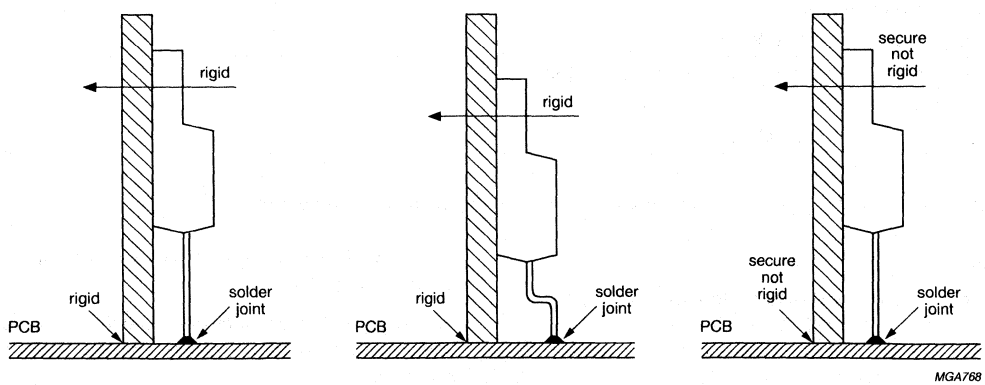
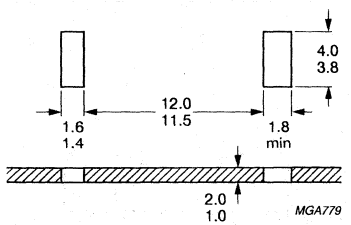


Fig.2 Printed circuit board and heatsink mounting.

INSTRUCTIONS FOR CLIP MOUNTING

Direct mounting with clip

1. Apply heatsink compound to the mounting base, then place the device on the heatsink.
2. Push the short end of the clip into the narrow slot in the heatsink with the clip at an angle of 10° to 30° to the vertical. See Figs.3 and 4.
3. Push down the clip over the device until the long end of the clip snaps into the wide slot in the heatsink. The clip should bear on the plastic body, not on the tab. See Fig.5.



Dimensions in mm.

Fig.3 Heatsink requirements.

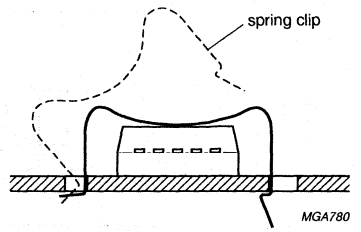


Fig.4 Mounting.

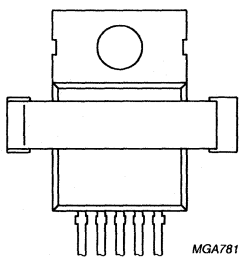
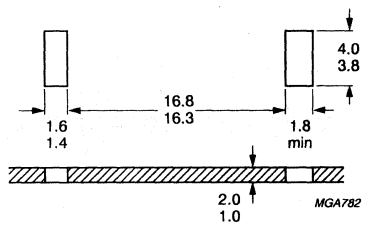


Fig.5 Position of device (top view).

Insulated mounting with clip

With the insulators up to 2 kV insulation is obtained.

1. Apply heatsink compound to the bottom of both device and insulator, then place the device with the insulator on the heatsink.
2. Push the short end of the clip into the narrow slot in the heatsink with the clip at an angle of 10° to 30° to the vertical. See Figs 6, 7 and 8.
3. Push down the clip over the device until the long end of the clip snaps into the wide slot in the heatsink. The clip should bear on the plastic body, not on the tab. Ensure that the device is centred on the mica insulator to prevent unwanted movement.



Dimensions in mm.

Fig.6 Heatsink requirements.

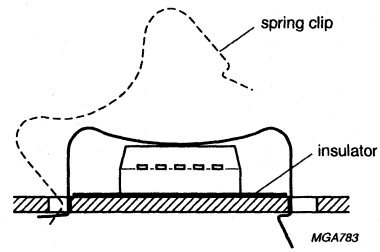


Fig.7 Mounting.

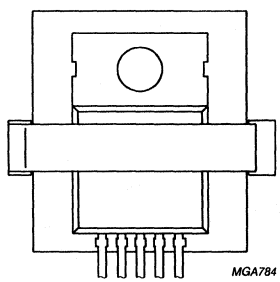


Fig.8 Position of device (top view).

INSTRUCTIONS FOR SCREW MOUNTING

Direct mounting with screw and spacing washer

THROUGH HEATSINK WITH NUT

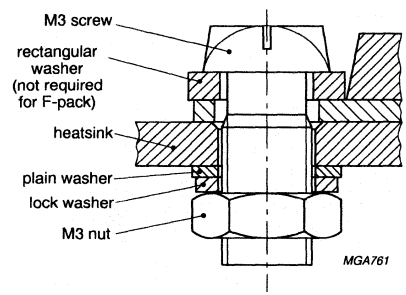


Fig.9 Assembly.

INTO TAPPED HEATSINK

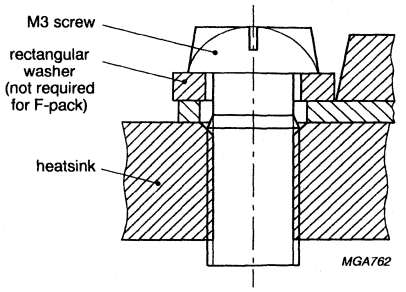
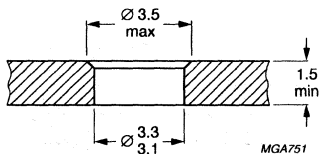
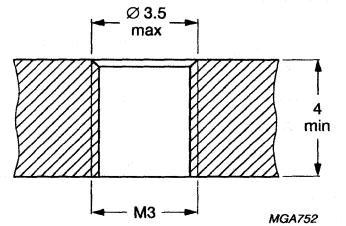


Fig.11 Assembly.



Dimensions in mm.

Fig.10 Heatsink requirements.



Dimensions in mm.

Fig.12 Heatsink requirements.

Insulated mounting with screw and spacing washer

Not recommended where mounting tab is on mains voltage. Not applicable for F-pack.

THROUGH HEATSINK WITH NUT

Known as a 'bottom mounting'.

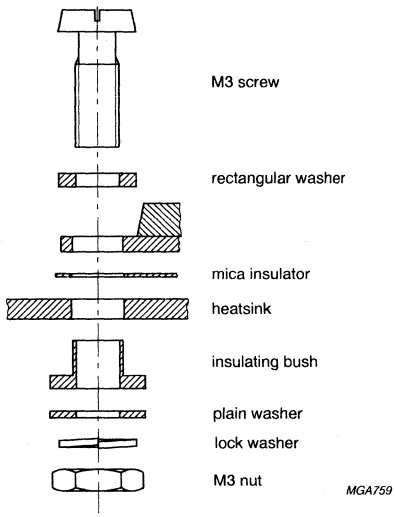
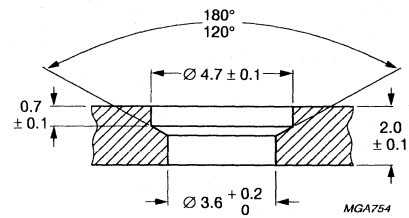


Fig.13 Insulated screw mounting with rectangular washer.



Dimension in mm.

Fig.14 Heatsink requirements for 500 V insulation.

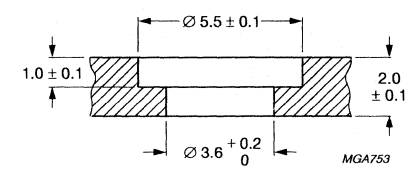


Fig.15 Heatsink requirements for 800 V insulation.

INTO TAPPED HEATSINK

Known as a 'top mounting'.

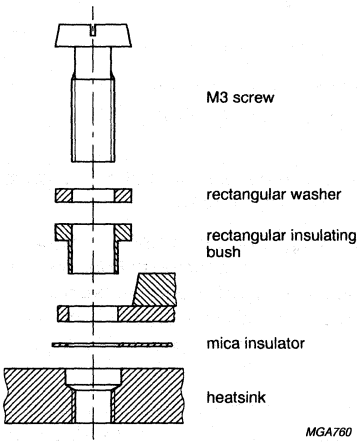
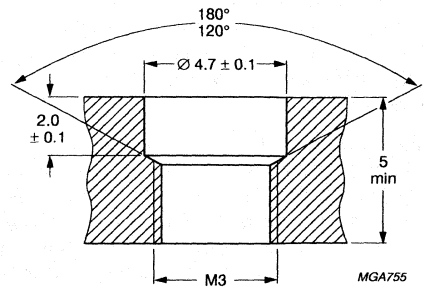
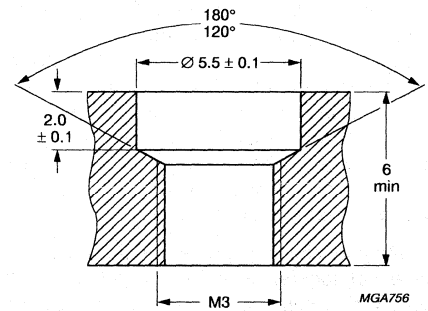


Fig.16 Insulated screw mounting with rectangular washer into tapped heatsink.



Dimension in mm.

Fig.17 Heatsink requirements for 500 V insulation.



Dimension in mm.

Fig.18 Heatsink requirements for 1000 V insulation.

SURFACE-MOUNT DEVICES

Since the introduction of Surface Mount Devices (SMDs), component design and manufacturing techniques have changed almost beyond recognition. Smaller pitch, minimum footprint area and reduced component volume all contribute to a more compact circuit assembly. As a consequence, when designing printed circuit boards (PCBs), the dimensions of the footprints are perhaps more crucial than ever before.

One of the first steps in this design process is to consider which soldering method, either wave or reflow, will be used during production. This determines not only the solder footprint dimensions, but also the minimum spacing between components, the available area underneath the component where tracks may be laid, and possibly the required component orientation during soldering.

Although reflow soldering is recommended for SMDs, many manufacturers use, and will continue to use for some time to come, a mixture of surface-mount and through-hole components on one substrate (a mixed print).

The mix of components affects the soldering methods that can be applied. A substrate having SMDs mounted on one or both sides but no through-hole components is likely to be suitable for reflow or wave soldering. A double sided mixed print that has through-hole components and some SMDs on one side and densely packed SMDs on the other normally undergoes a sequential combination of reflow and wave soldering. When the mixed print has only through-hole components on one side and all SMDs on the other, wave soldering is usually applied.

To help with your circuit board design, this guideline gives an overview of both reflow and wave soldering methods, and is followed by some useful hints on hand soldering for repair purposes, and the recommended footprints for our SMD discrete semiconductor packages.

Reflow soldering process

There are three basic process steps for single-sided PCB reflow soldering, these are:

1. Applying solder paste to the PCB
2. Component placement
3. Reflow soldering.

APPLYING SOLDER PASTE TO THE PCB

Solder paste can be applied to the PCBs solder lands by one of either three methods: dispensing, screen or stencil printing.

Dispensing is flexible but is slow, and only suitable for pitches of 0.65 mm and above.

With screen printing, a fine-mesh screen is placed over the PCB and the solder paste is forced through the mesh onto the solder lands of the PCB. However, because of mesh aperture limitations (emulsion resolution), this method is only suitable for solder paste deposits of 300 μm and wider.

Stencil printing is similar to screen printing, except that a metal stencil is used instead of a fine-mesh screen. The stencil is usually made of stainless steel or bronze and should be 150 to 200 μm thick. A squeegee is passed across the stencil to force solder paste through the apertures in the stencil and onto the solder lands on the PCB (see Fig.19). It does not suffer from the same limitations as the other two printing methods and so is the preferred method currently available.

It is recommended that for solder paste printing, the equipment is located in a controlled environment maintained at a temperature of 23 ±2 °C, and a relative humidity between 45% and 75%.

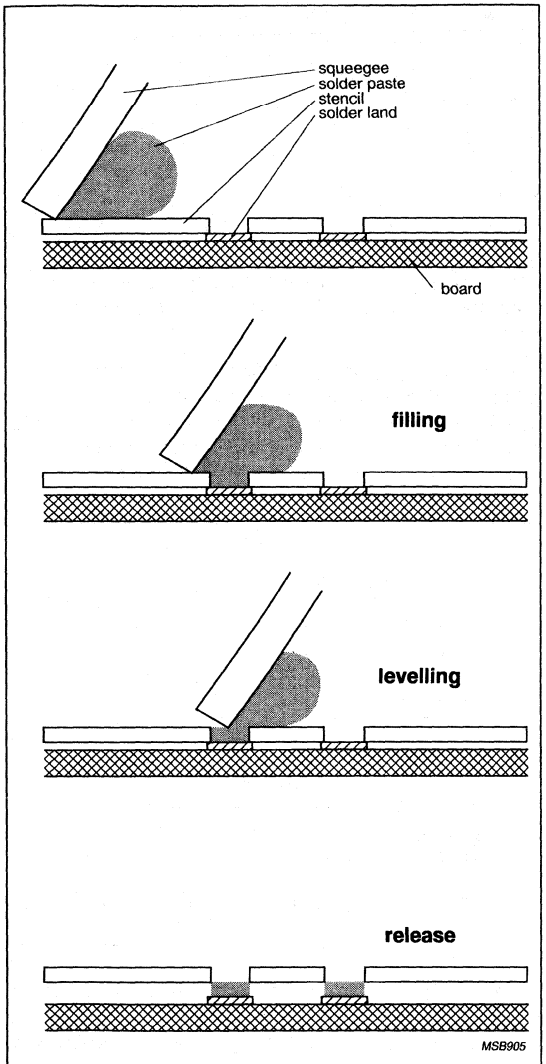


Fig.19 Applying solder paste by stencilling.

Stencil printing

The printing process must be able to apply the solder paste deposits to the PCB:

- In the correct amounts
- At the correct position on the lands
- With an acceptable height and shape.

The amount of solder paste used must be sufficient to give reliable soldered joints. This amount is controlled by the stencil thickness, aperture dimensions, process settings, and the volume of paste pressed through the apertures by the squeegee.

The downward force of the squeegee is counteracted by the hydrodynamic pressure of the paste, and so the machine should be set to ensure that the stencil is just 'cleaned' by the squeegee.

Suitable aperture dimensions depend on the stencil thickness. The solder paste deposits must have a flat part on the top (Fig.20, examples 4 and 5), which can be achieved by correct process settings. The footprints given in this book were designed for these correct deposit types. Stencil apertures that are too small result in irregular dots on the lands (Fig.20, examples 1 to 3). If the apertures are too large, solder paste can be scooped out, particularly if a rubber squeegee is used (Fig.20, example 6).

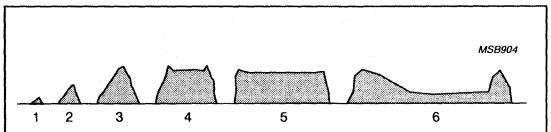


Fig.20 Shapes of solder deposits for increasing stencil apertures (left to right).

Ideally, the deposited solder paste should sit entirely on the solder land. The tolerated misplacement of solder paste with respect to the solder land is determined by the most critical component. The solder paste deposit must be deposited within 100 µm with respect to the solder land.

Furthermore, the tackiness (tack strength) of the solder paste must be sufficient to hold surface-mount devices on the PCB during assembly and during transport to the reflow oven. Tack strength depends on factors such as paste composition, drying conditions, placement pressure, dwell time and contact area. As a general rule, component placement should be within four hours after the paste printing process.

Squeegee

The squeegee can be either metal or rubber. A metal squeegee gives better overall results and so is recommended, however with step stencils, a rubber squeegee has to be used. The footprints given in this chapter were designed for application by both types of squeegee.

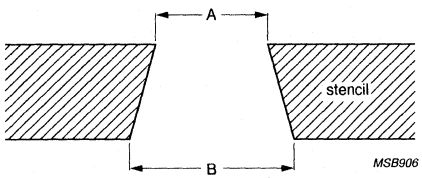
Stencil apertures

Stencil apertures can be made by either:

- Etching
- Laser cutting
- Electroforming.

Of the three methods, etching is less accurate as the deviation in aperture dimensions with respect to the target is relatively large (target is +50 μm at squeegee side and 0 μm at PCB side).

Laser-cut and electroformed stencils have smaller deviations in dimensions and are therefore more suitable for small and fine-pitch components (see Fig.21).



A = B +0/–30 (μm); B= X 30 (μm); X = nominal apertures size.

Fig.21 Specifications of laser-cut stencil apertures for discrete and passive components.

A useful method of controlling the stencil printing process during production is by monitoring the weight of solder paste on the board which may vary between 80% and 110% of the theoretical amount according to the target (designed) apertures. Smearing and clogging of a small aperture cannot be detected with this method.

Solder paste

Reflow soldering uses a paste consisting of small nodules of solder and a flux with binder, solvents and additives to control rheological properties. The flux in the solder paste can be rosin mildly activated or rosin activated.

The requirements of the solder paste are:

- Good rolling behaviour
- No slump during heat-up
- Low viscosity during printing
- High viscosity after printing
- Sufficient tackiness to hold the components
- Removal of oxides during reflow soldering.

Suitable solder paste types have the following compositions:

- Sn62Pb36Ag2
- Sn63Pb37
- Sn60Pb40.

COMPONENT PLACEMENT

The position of the component with respect to the solder lands is an important factor in the final result of the assembly process. A misaligned component can lead to unreliable joints, open circuits and/or bridges between leads.

The placement accuracy is defined as the maximum permissible deviation of the component outline or component leads, with respect to the actual position of the solder land pattern belonging to that component or component leads on the circuit board (see Fig.22).

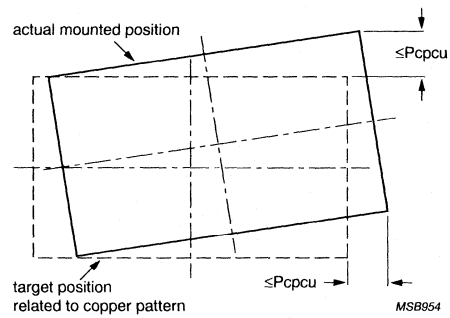


Fig.22 Component placement tolerances.

A maximum placement deviation (P) of 0.25 mm is used in these guidelines, which relates to the accuracy of a low-end placement machine. A higher placement accuracy is required for components with a fine pitch. This is given in the footprint description for the components concerned.

Besides the position in x- and y-directions, the z-position with respect to the solder paste, which is determined by the placement force, is also important. If the placement force is too high, solder paste will be squeezed out and solder balls or bridges will be formed. If the force is too low, physical contact will be insufficient, leads will not be soldered properly and the component may shift.

REFLOW SOLDERING

There are several methods available to provide the heat to reflow the solder paste, such as convection, hot belt, hot gas, vapour phase and resistance soldering. The preferred method is, however, convection reflow.

Convection reflow

With this method, the PCBs passes through an oven where it is preheated, reflow soldered and cooled (see Fig.23). If the heating rate of the board and components are similar, however, preheating is not necessary.

During the reflow soldering process, all parts of the board must be subjected to an accurate temperature/ time profile. Figure 23 shows a suitable profile framework for single-sided reflow soldering and the first side of double-sided print boards. It's important to note that this profile is for discrete semiconductor packages. The actual framework for the entire PCB could be smaller than the one shown, as other components on the board may have different process requirements.

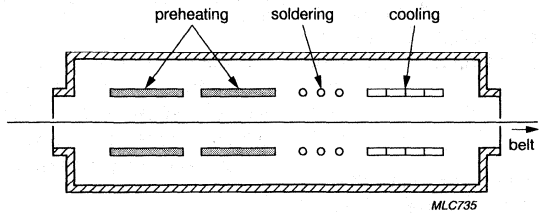
Reflow soldering can be done in either air or a nitrogen atmosphere. If soldering in air, the temperature (T_p) must not exceed 240 °C on the first side of a double-sided print board with organic coated solder lands. This is because peak temperatures greater than 240 °C reduce the solderability of the lands on the second side to be soldered. This peak temperature can rise to 280 °C when soldering the second side with organic coated solder lands in air.

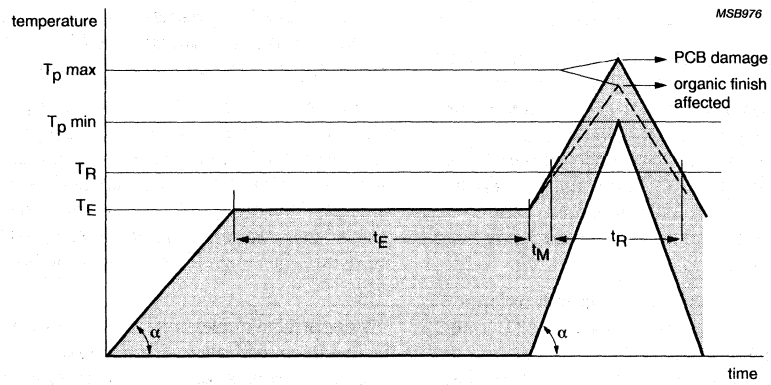
If soldering in a nitrogen atmosphere, a peak temperature of 280 °C is allowed for double-sided print boards or single-sided reflow soldering. Soldering in a nitrogen atmosphere results in smoother joint meniscus, smaller contact angles, and better wetting of the copper solder lands.

The profile can be achieved by correct combinations of conveyor speed and heater temperature. To check whether the profile is within specification, the coldest and hottest spots on the board have to be located.

To do this, you should dispense solder paste deposits regularly over the surface of a test board and on the component leads. Set the oven to a moderate temperature with maximum conveyor velocity and pass the test board through. If too many solder paste dots melt, lower the oven's temperature. Continue passing test boards through the oven, while lowering the speed of the belt in small steps.

The deposit that melts first indicates the warmest location, the one that melts last indicates the coldest location. Paste dots not reflowed after two runs must be replaced by fresh dots. Thermocouples have to be mounted at the coldest and warmest location and temperature profiles measured.





α	≤ 10 °C/s.	t_E	≤ 1 min, if possible (else ≤ 5 min).
T_E	≤ 160 °C.	t_M	= 2 to 30 s.
T_R	= 180 °C.	t_R	≤ 70 s.
$T_P$min	= 205 °C.		
$T_P$max	= 240 °C	for soldering the first side of a double-sided board with organic finish.	
$T_P$max	= 280 °C	for all other cases.	

Fig.23 Convection reflow soldering method (top), process requirements for reflow soldering (bottom).

Double-wave soldering process

There are four basic process steps for double-wave soldering, these are:

1. Applying adhesive
2. Component placement
3. Curing adhesive
4. Wave soldering process.

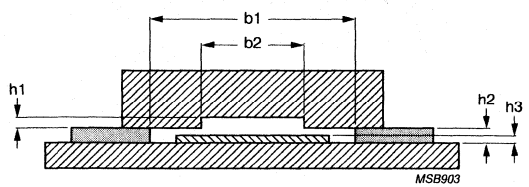
APPLYING ADHESIVE

To hold SMDs on the board during wave soldering, it is necessary to bond the component to the PCB with one or more adhesive dots. This is done either by dispensing, stencilling or pin transfer. Dispensing is currently the most popular technique. It is flexible and allows a controlled amount of adhesive to be applied at each position. Stencil printing and pin transfer are less flexible and are mainly used for mass production. The component-specific requirements for an adhesive dot are:

- Shape (volume) of the adhesive dot
- Number of dots per component
- Position of the dots.

Volume of adhesive

There must be enough adhesive to keep components in their correct positions while being transported to the curing oven. This means that the deposited adhesive must be higher than the gap between the component and the board surface. Nevertheless, there should not be too much deposit as it may smear onto the solder lands, where it can affect their solderability. The gap between a component and printed board depends on the geometry of the board and component (see Fig.24).



h1 = component stand-off height.
h2 = solder resist (and track) height on PCB.
h3 = copper height on PCB.
b1 = gap between solder lands on the PCB.
b2 = gap between metallization of the component.

Fig.24 Available space for adhesive between component and PCB (unmarked area).

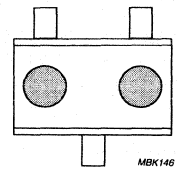
Table 1 gives guidelines for volumes of adhesive dots per package. The spreading in volumes should be within ±15%.

Table 1 Guidelines for volumes of adhesive dots

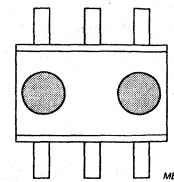
COMPONENT	NUMBER OF DOTS	VOLUME PER DOT (mm^3)
SC-70 (SOT323)	2	0.045
SC-88 (SOT363)	2	0.045
SOT23	2	0.06
SOT89	2	0.3
SOT223	2	0.70

Number, position and volume of dots per component

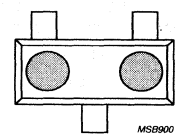
Figure 25 shows the recommended positions and numbers of adhesive dots for a variety of packages. SOT89 and SOT223 packages require much larger adhesive dots compared with those for other components.



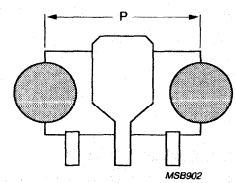
a. SC-70 (SOT323).



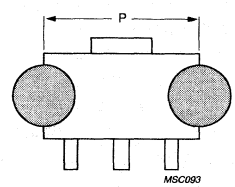
b. SC-88 (SOT363).



c. SOT23.



d. SOT89 (P = 4.4 mm).



e. SOT223 (P = 6.0 mm).

For optimum power dissipation, the SOT89 requires a good thermal contact (i.e. good solder joint) between the package and the solder land. During wave-soldering, however, flux may not always reach the total soldering area beneath the component body, which in turn can lead to an incomplete solder joint. If the SOT89 is double-wave soldered, therefore, power derating must be applied.

Fig.25 Position of adhesive dots. Pitch between two small dots is 1.0 mm.

Nozzle outlet diameter

Depending on adhesive type and component size, the nozzle outlet diameter of the dispenser can vary between 0.6 and 0.7 mm for the larger dots, and between 0.3 and 0.5 mm for the smaller dots.

As the rheology of the adhesive is temperature dependent, the temperature in the nozzle must be carefully controlled before dispensing. The required temperature depends on the adhesive type, but is usually between 26 °C and 32 °C to maintain the adhesive's rheology within specification during dispensing. Thermally curing epoxy adhesives are normally used.

Adhesives

Beside the nozzle diameters, different adhesive types are also used for different component sizes.
Small components can be secured during assembly and wave soldering with a thin (low green strength) adhesive, which can be dispensed at high speeds. For larger components (such as QFP and SO packages), a higher green strength adhesive is required.

COMPONENT PLACEMENT

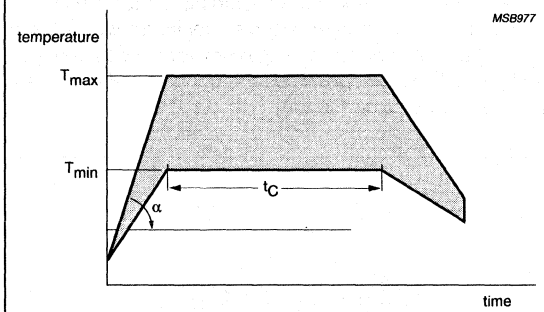
Positioning components on the PCB is similar in practice to that of reflow soldering. To prevent component shift and smearing of the adhesive, board support is important while placing components.

CURING THE ADHESIVE

To provide sufficient bonding strength between component and board, the adhesive must be properly cured. Figure 26 gives general process requirements for curing most thermosetting epoxy adhesives with latent hardeners. The temperature profile of all adhesive dots on the PCB must be within this framework. It's important to note that this profile is for discrete semiconductor packages. The actual framework for the entire PCB could be smaller than the one shown, as other components on the board may have different process requirements.

To check whether the profile is within specification, the temperature of coldest and hottest spots must be measured. The coldest spot is usually under the largest package: the hottest spot is usually under the smallest package.

The adhesive can be cured either by infrared or hot-air convection.



$T_{max} \leq 160$ °C.
$T_{min} \geq 110$ °C.
$t_C \geq 3$ minutes.
$\alpha \leq 100$ °C/min (some adhesives allow higher heating rates).
If $T_{min} > 125$ °C, t_C may be <3 min, depending on adhesive specification.

Fig.26 Process requirements for curing thermosetting adhesives.

Bonding strength

The bonding strength of glued components on the board can be checked by measuring the torque force. For small components the requirements are given in Table 2.
No values are specified for larger packages.

Table 2 Bonding strength requirements

COMPONENT	MINIMUM BONDING STRENGTH (cNcm)	TARGET BONDING STRENGTH (cNcm)
SC-70 (SOT323) SC-88 (SOT363)	110	250
SOT23	150	250

WAVE SOLDERING PROCESS

After applying adhesive, placing the component on the PCB and curing, the PCB can be wave soldered. The wave soldering process is basically built up from three sub-processes. These are:

1. Fluxing
2. Preheating
3. (Double) wave soldering.

Although listed here as sub-process they are in practice combined in one machine. All are served by one transport mechanism, which guides the PCBs at an incline through the soldering machine. It's important to note that the PCB must be loaded into the machine so that the SMDs on the board come into direct contact with the solder wave (see Fig.27).

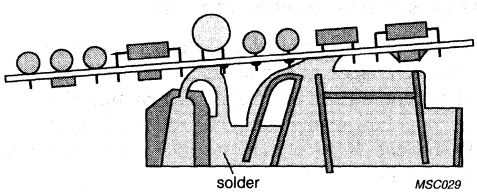


Fig.27 Double-wave soldering.

In principle, two different systems of PCB transports are available for wave soldering:

- Carrier transport

  PCBs are mounted on a soldering carrier, which moves through the soldering machine, taking it from one sub-process to the next. The advantage of carrier mounting is that the board is fixed and warpage during soldering is reduced.

- Carrierless transport

  PCBs are guided through the soldering machine by a chain with grips. This method is more convenient for mass production.

Fluxing

Fluxing is necessary to promote wetting both of the PCB and the mounted components. This ensures a good and even solder joint.

During the fluxing process, the solder side of the PCB (including the components) are covered with a thin layer of solder flux, which can be applied to the PCB either by spraying or as a foam. Although several types of solder flux are available for this purpose, they can be categorized into three main groups:

- Non-activated flux (e.g. rosin-based fluxes)
- Mildly activated flux (e.g. rosin-based or synthetic fluxes)
- Highly activated flux (e.g. water-soluble fluxes).

The choice for a particular flux type depends mainly on the products to be soldered.

Although there is always some flux residue left on the PCB after soldering, it's not always necessary to wash the boards to remove it. Whether to clean the board can depend on:

- The type of flux used (highly activated fluxes are corrosive and so should always be removed).
- The required appearance of the board after soldering.
- Customer requirements.

Preheating

After the flux is applied, the PCB needs to be preheated. This serves several purposes: it evaporates the flux solvents, it accelerates the activity of the flux and it heats the PCB and components to reduce thermal shock.

The required pre-heat temperature depends on the type of flux used. For example, the more common low-residue fluxes require a pre-heat temperature of 120 °C (measured on the wave solder side of the PCB).

(Double) wave soldering

The PCB first passes over a highly intensive (jet) solder wave with a carefully controlled constant height. This ensures good contact with the PCB, the edges of SMDs and the leads of components near to high non-wetted bodies. The greater the board's immersion depth into this first wave, the fewer joints will be missed.

If the PCB is carrier mounted, the first wave's height, and thus the board's immersion depth, can be greater. Carrierless soldering is more convenient for mass production, but the height of the wave must be lower to avoid solder overflowing to the top side of the board. The height of the jet wave is given in Table 3 along with an indication of soldering process window. This information is based on a 1.6 mm thick PCB.

Table 3 Process ranges for carrierless and carrier double wave soldering

	CARRIERLESS	CARRIER
Preheat temperature of board at wave solder side (°C)	120 ±10	
Heating rate preheating (°C/s)	$\Delta T/\Delta t \leq 3$	
First (jet) wave:		
wave height with respect to bottom side of board (mm)	1.6 +0.5/–0	3.0 +0.5/–0
Second (laminar) wave (double sided overflow):		
height with respect to underside of the board (mm)	0.8 +0.5/–0	
relative stream velocity with respect to the board	0	
Solder temperature (°C)	250 ±3	
Contact times (s):		
first (jet) wave	0.5 +0.5/–0	
second (laminar) wave	2.0 ±0.2 (plain holes); 2.5 ±0.2 (plated holes)	
PCB transport angle (°)	7 ±0.5	
Solder alloys	Sn60Pb40; Sn60Pb38Bi2	

The second, smoother laminar solder wave completes formation of the solder fillet, giving an optimal soldered connection between component and PCB. It also reduces the possibility of solder bridging by taking up excessive solder.

To reduce lead/tin oxides and possibly other solder imperfection forming during soldering, the complete wave configuration can be encapsulated by an inert atmosphere such as nitrogen.

Hand soldering microminiature components

It is possible to solder microminiature components with a light-weight hand-held soldering iron, but this method has obvious drawbacks and should be restricted to laboratory use and/or incidental repairs on production circuits:

- Hand-soldering is time-consuming and therefore expensive
- The component cannot be positioned accurately and the connecting tags may come into contact with the substrate and damage it
- There is a risk of breaking the substrate and internal connections in the component could be damaged
- The component package could be damaged by the iron.

Assessment of soldered joint quality

The quality of a soldered joint is assessed by inspecting the shape and appearance of the joint. This inspection is normally done with either a low-powered magnifier or microscope, however where ultra-high reliability is required, video, X-ray or laser inspection equipment may be considered.

Both sides of the PCB should be carefully examined: there should be no misaligned, missing or damaged components, soldered joints should be clean and have a similar appearance, there should be no solder bridging or residue, and the PCB should be assessed for general cleanliness.

Unlike leaded component joints where the lead also provides added mechanical strength, the SMD relies on the quality of the soldering for both electrical and mechanical integrity. It is therefore necessary that the inspector is trained to make a visual assessment with regard to long-term reliability.

Criteria used to assess the quality of an SMD solder joint include:

- Correct position of the component on the solder lands
- Good wetting of the surfaces
- Correct amount of solder
- A sound, smooth joint surface.

POSITIONING

If a lead projects over the solder land too far an unreliable joint is obtained. Figures 28 to 30 show the maximum shift allowed for various components. The dimensions of these solder lands guarantee that, in the statistically extreme situation, a reliable soldered joint can be made.

GOOD WETTING

This produces an even flow of solder over the surface land and component lead, and thinning towards the edges of the joint. The metallic interaction that takes place during soldering should give a smooth, unbroken, adherent layer of solder on the joint.

CORRECT AMOUNT OF SOLDER

A good soldered joint should have neither too much nor too little solder: there should be enough solder to ensure electrical and mechanical integrity, but not so much that it causes solder bridging.

SOUND, SMOOTH JOINT SURFACE

The surface of the solder should be smooth and continuous. Small irregularities on the solder surface are acceptable, but cracks are unacceptable.

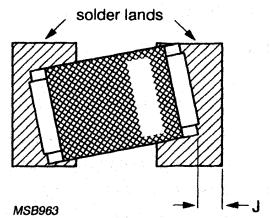


Fig.28 $J \geq 0.3$ mm.

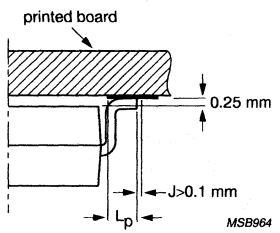


Fig.29 $J \geq 0.1$ mm; solder land > L_p.

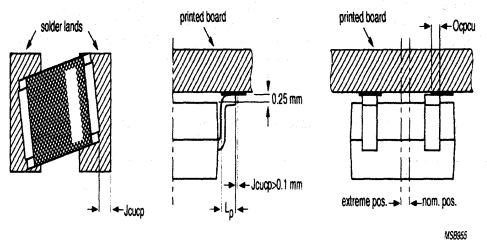


Fig.30 Oc > half lead width.

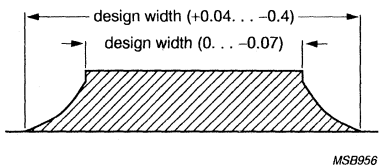
Footprint definitions

A typical SMD footprint, is composed of:

- Solder lands (conductive pattern)
- Solder resist pattern
- Occupied area of the component
- Solder paste pattern (for reflow soldering only)
- Area underneath the SMD available for tracks
- Component orientation during wave soldering.

SOLDER LANDS (CONDUCTIVE PATTERN)

The dimensions of the solder lands given in these guidelines are the actual dimensions of the conductive pattern on the printed board (see Fig.31). These dimensions are more crucial for fine-pitch components.



solder land width

The solder land dimensions are designed to give optimum soldering results. They do not take into account the copper area for optimum power dissipation. If an extra area is required to improve power dissipation, it should be coated with solder resist. This is especially important for power packages such as SOT89 and SOT223.

Fig.31 Requirements of solder land dimensions.

SOLDER RESIST PATTERN

The solder resist on the circuit board prevents short circuits during soldering, increases the insulation resistance between adjacent circuit details and stops solder flowing away from solder lands during reflow soldering.

In contrast to the tracks, which must be entirely covered, solder lands must be free of solder resist. Because of this, the cut-outs in the solder resist pattern should be at least 0.15 mm or 0.3 mm larger than the relevant solder lands (for a photo-defined and screen printed solder resist pattern respectively). The solder resist cut-outs given with the footprints in these guidelines are sketched and their dimensions can be calculated by using the above rule. Consult your printed board supplier for agreement with these solder resist cut-outs.

OCCUPIED AREA OF THE COMPONENT

A minimum spacing between components is necessary to avoid component placement problems, short circuits during wave or reflow soldering and dry solder joints during wave soldering caused by non-wettable component bodies. These problems can be avoided by placing the components so the occupied areas do not overlap (see Fig.32).

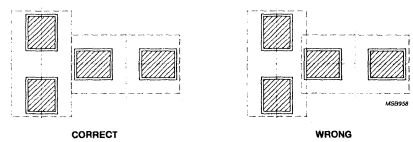


Fig.32 Minimum spacing required (bottom) between components.

SOLDER PASTE PATTERN

It is important to use a solder paste printer which is optical aligned with the PCBs copper pattern for the reflow footprints presented here. This is because, for these footprints, the solder paste deposit must be within a 0.1 mm tolerance with respect to the copper pattern.

To ensure the right amount of solder for each solder joint, the stencil apertures must be equal to the solder paste areas given by the footprints.

AREA AVAILABLE FOR TRACKS (CONDUCTIVE PATTERN)

Tracks underneath leadless SMDs must be covered with solder resist. However, as solder resist can sometimes be thin or have pin holes at the edges of tracks (especially when applied by screen printing), an additional clearance for tracks with respect to the actual metallization position of the mounted component should be taken into account (see Fig.33).

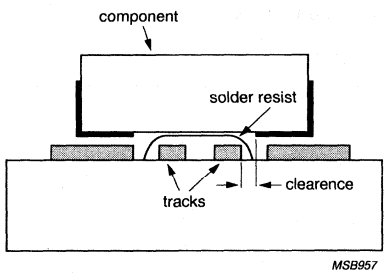


Fig.33 Clearance required underneath component between metallization and tracks.

For components that need the additional clearance, the footprints on the following pages give the maximum space for tracks not connected to the solder lands (clearance ≥ 0.1 mm), for low-voltage applications. The number of tracks in this space is determined by the specified line resolution of the printed board.

COMPONENT ORIENTATION DURING WAVE SOLDERING

Where applicable, footprints for wave soldering are given with the transport direction of the PCB. This is given as either a 'preferred transport direction during soldering' or 'transport direction during soldering'.

Components with small terminals and non-wettable bodies, have a smaller risk of dry joints, especially when using carrierless soldering as the components are placed according to the 'preferred orientation'.

Components have no orientation preference for reflow soldering.

Recommended footprints

The recommended footprints for our discrete semiconductor packages are given on the following pages. For their dimensional outline drawings, see the 'Package outlines' section in this book.

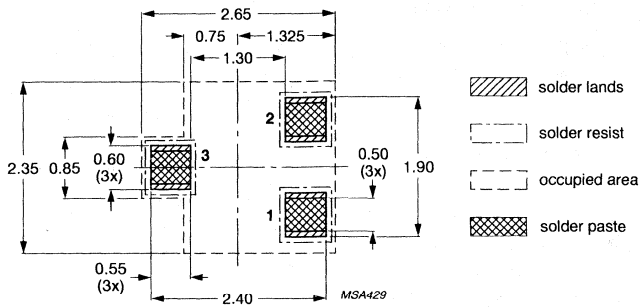


Fig.34 Reflow soldering footprint for SC-70 (SOT323).

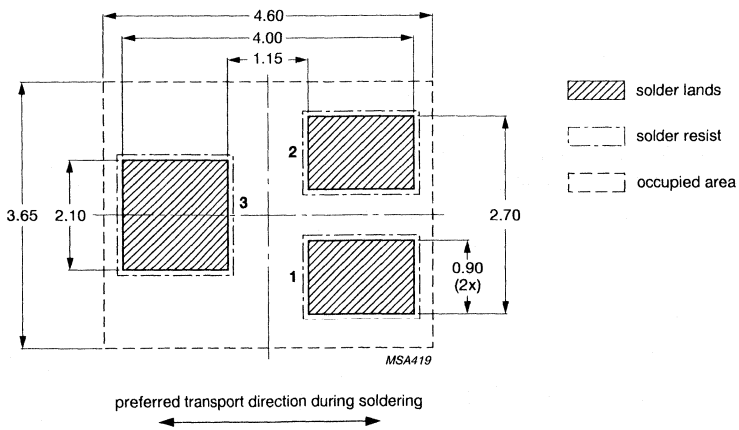


Fig.35 Wave soldering footprint for SC-70 (SOT323).

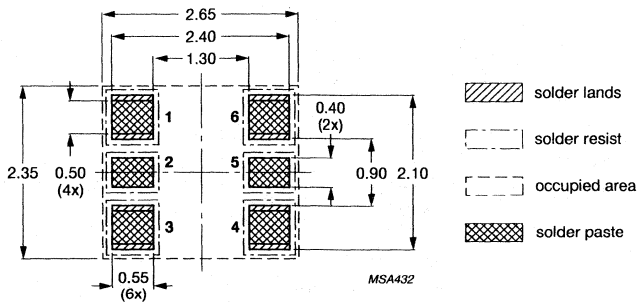


Fig.36 Reflow soldering footprint for SC-88 (SOT363).

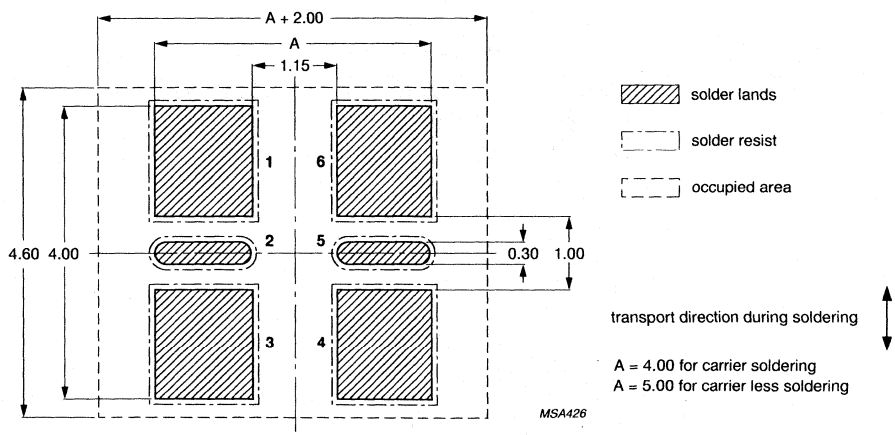


Fig.37 Wave soldering footprint for SC-88 (SOT363).

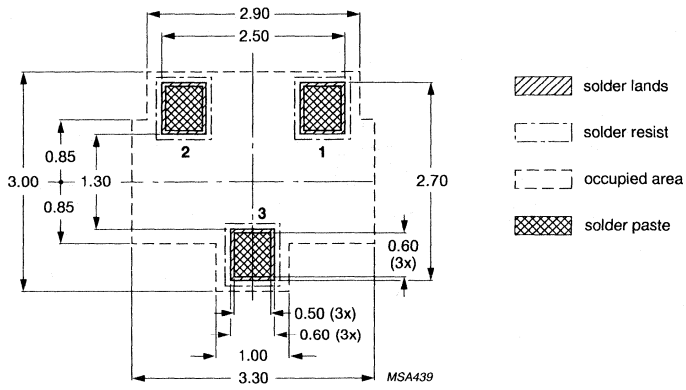


Fig.38 Reflow soldering footprint for SOT23.

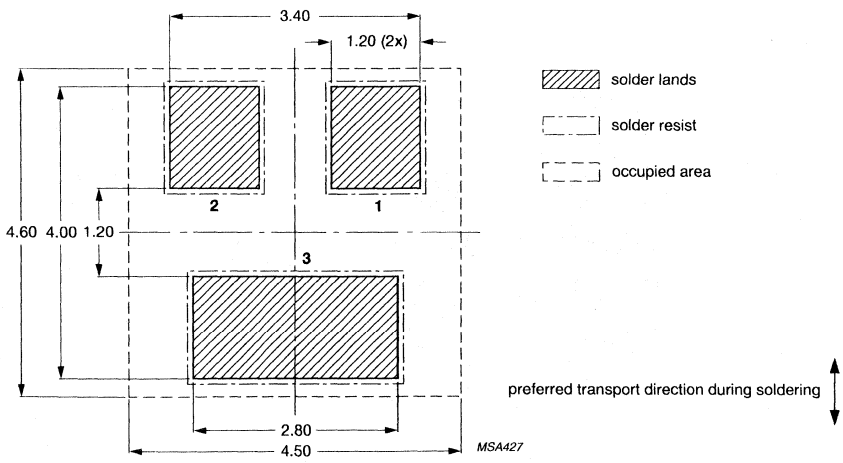


Fig.39 Wave soldering footprint for SOT23.

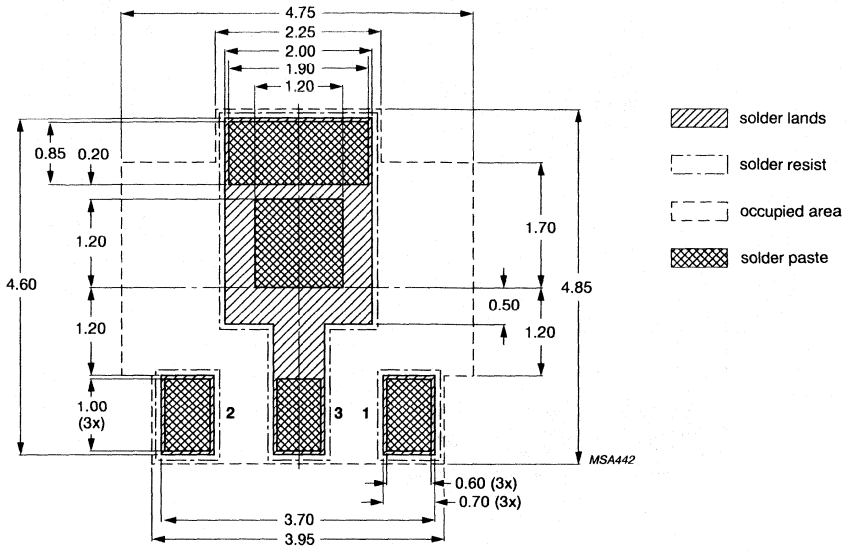
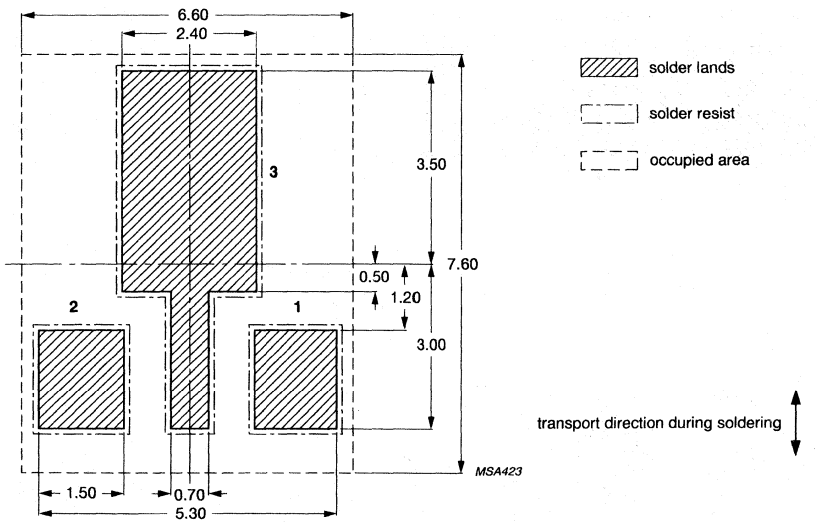


Fig.40 Reflow soldering footprint for SOT89.



Not recommended for wave soldering (see Fig.25).

Fig.41 Wave soldering footprint for SOT89.

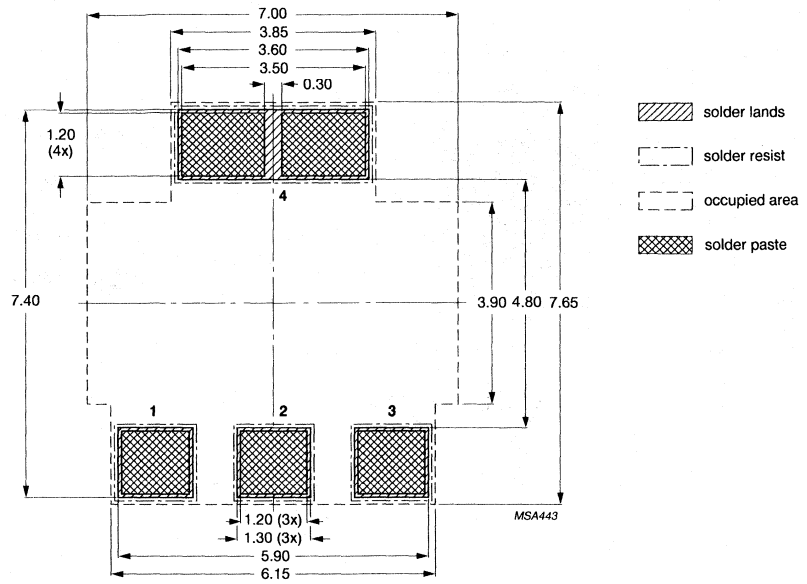


Fig.42 Reflow soldering footprint for SOT223.

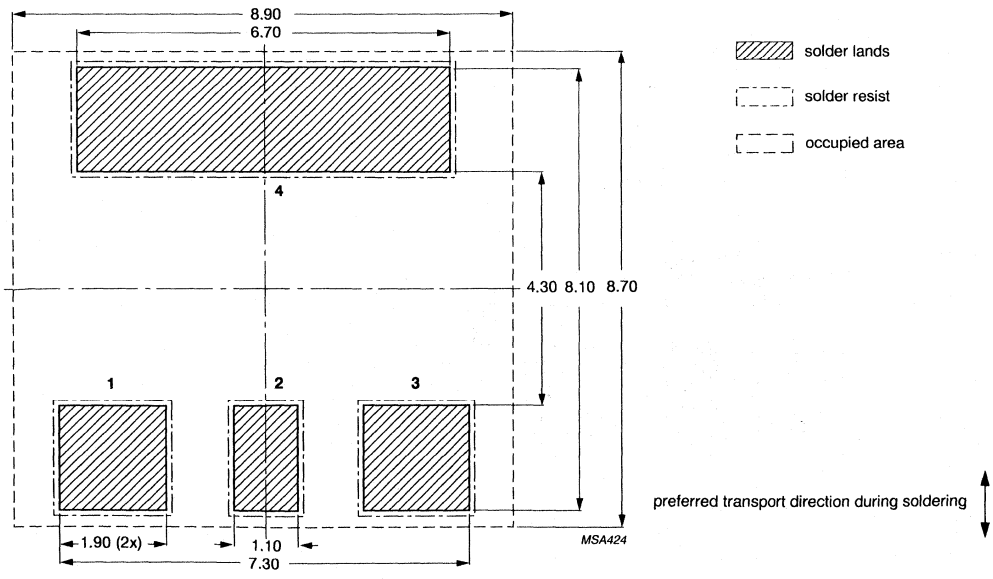
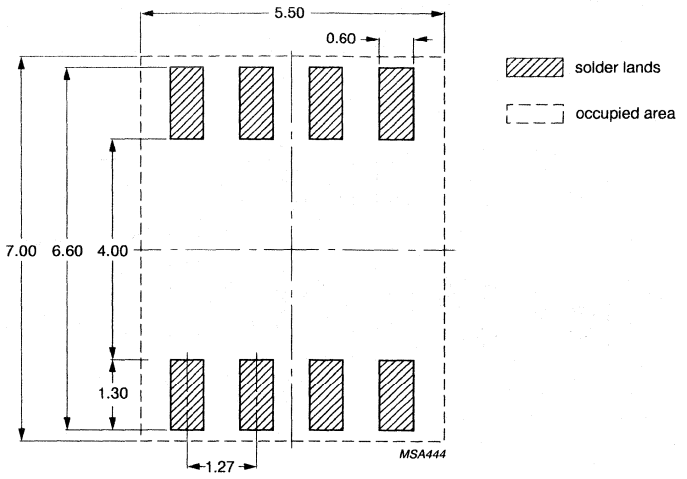
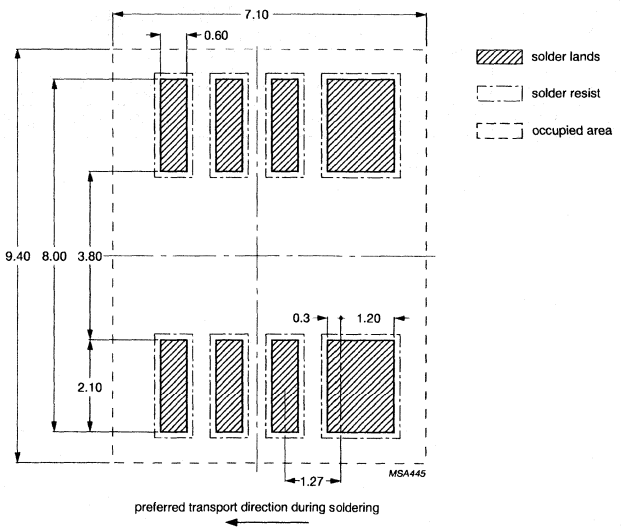


Fig.43 Wave soldering footprint for SOT223.



Placement accuracy: ±0.25 mm.

Fig.44 Reflow soldering footprint for SO8 (SOT96-1)



Placement accuracy: ±0.25 mm.

Fig.45 Wave soldering footprint for SO8 (SOT96-1)

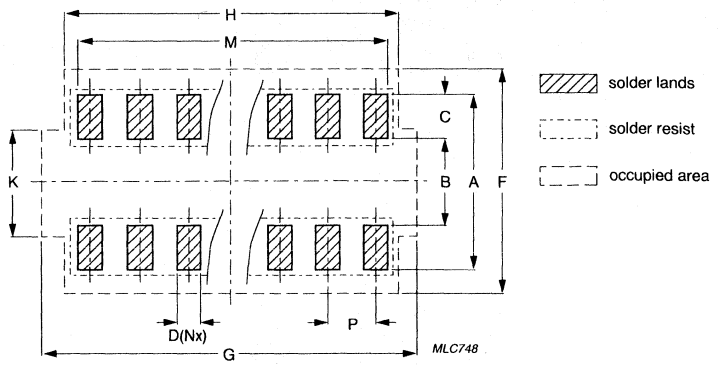


Fig.46 Reflow soldering footprint for SSOP16 (SOT338-1) and SSOP24 (SOT340-1).

Footprint dimensions for reflow soldering

PACKAGE NAME	PHILIPS CODE	N	FOOTPRINT DIMENSIONS IN mm										PLACEMENT ACCURACY
			P	A	B	C	D	F	G	H	K	M	
SSOP16	SOT338-1	16	0.65	8.10	5.70	1.20	0.40	8.35	6.50	5.20	5.55	4.95	±0.15
SSOP24	SOT340-1	24	0.65	8.10	5.90	1.10	0.40	8.35	8.50	7.80	5.55	7.55	±0.15

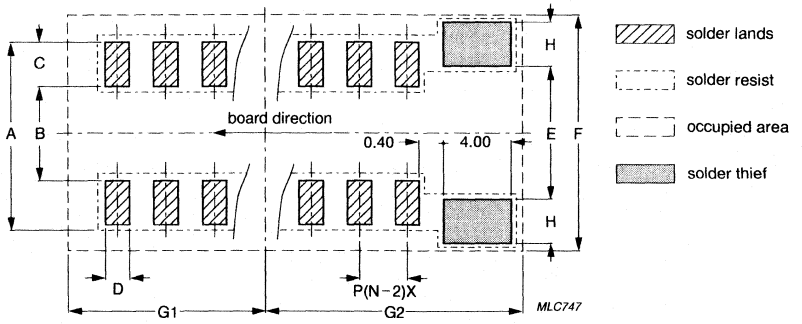


Fig.47 Wave soldering footprint for SSOP16 (SOT338-1) and SSOP24 (SOT340-1).

Footprint dimensions for wave soldering

PACKAGE NAME	PHILIPS CODE	N	FOOTPRINT DIMENSIONS IN mm										PLACEMENT ACCURACY
			P	A	B	C	D	E	F	G1	G2	H	
SSOP16	SOT338-1	16	0.65	9.15	5.35	1.90	0.30	6.15	10.65	4.25	7.075	2.00	±0.10
SSOP24	SOT340-1	24	0.65	9.15	5.55	1.80	0.30	6.30	10.80	5.25	8.375	2.00	±0.10

PACKING AND PACKING QUANTITIES

	Page
SCOPE	1928
SURFACE-MOUNT DEVICES	1928
Tape specification	
Reel specification	
Tube specification	
Packing quantities	
LEADED DEVICES	1934
Tape and reel packing of TO-92 devices	
Bulk packing of TO-92 devices	

SCOPE

This chapter covers packing and packing quantity details for surface-mount and leaded devices in the following packages:

Table 1 Survey of packages

PACKAGE	
SURFACE-MOUNT	**THROUGH-HOLE**
SOT23	TO-92 (SOT54)
SOT89	TO-92 var. (SOT54 var.)
SO8 (SOT96-1)	SOT78
SOT223	SOT186
SC-70 (SOT323)	SOT186A
SSOP16 (SOT338-1)	SOT226
SSOP24 (SOT340-1)	SOT263
SC-88 (SOT363)	SOT263-1
SOT404	SOT429
SOT426	
SOT428	
SO24 (SOT137-1)	
TSOP6 (SOT457)	

SURFACE-MOUNT DEVICES

Tape and reel packing for surface-mount devices meets the feed requirements for automatic pick and place equipment (packing conforms to IEC publication 286-3). Tape is an ideal shipping container making handling easy and providing secure blister cavities in which the devices are sealed with peel-off cover tape.

Tape specification

Tape dimensions are specified in Tables 2, 3 and 4 and in Figures 1 through 5 for 8, 12, 16 and 24 mm tape.

Table 2 Carrier tape widths

8 mm	12 mm	16 mm	24 mm
SC-70 (SOT323)	SOT89	SSOP16 (SOT338-1)	SOT404
SC-88 (SOT363)	SOT223	SSOP24 (SOT340-1)	SOT426
SOT23	SO8 (SOT96-1)		SO24 (SOT137-1)
TSOP6 (SOT457)			

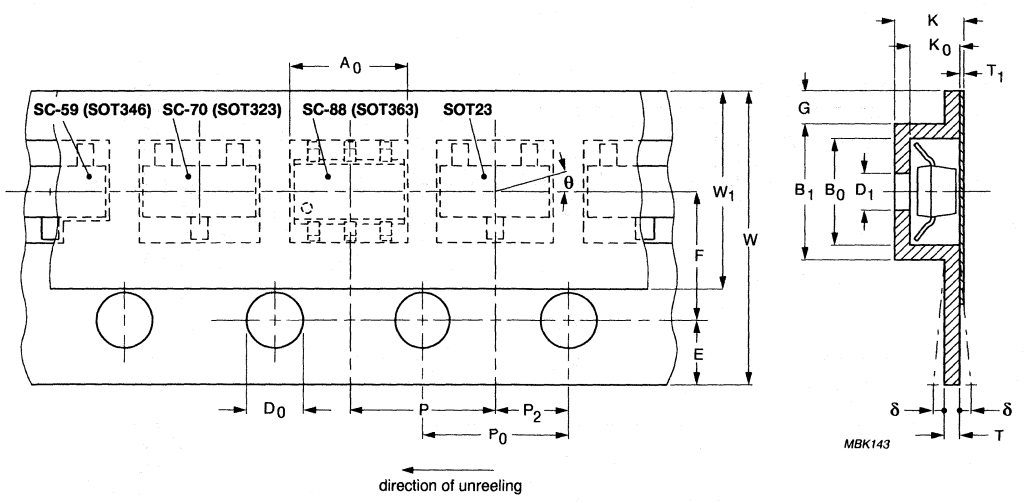
Table 3 Variable tape dimensions

PACKAGE	SYMBOL						
	W (mm)	F (mm)	P (mm)	D_1 (mm)	A_0 (mm)	B_0 (mm)	K_0 (mm)
SC-70 (SOT323)	8.0	3.5	4.0	1.0	2.4	2.4	1.2
SC-88 (SOT363)	8.0	3.5	4.0	1.0	2.4	2.4	1.2
SOT23	8.0	3.5	4.0	1.0	3.1	2.6	1.3
TSOP6 (SOT457)	8.0	3.5	4.0	1.0	3.2	3.1	1.3
SOT89	12.0	5.5	8.0	1.5	4.3	4.6	1.6
SO8 (SOT96-1)	12.0	5.5	8.0	1.5	6.7	5.4	1.8
SOT223	12.0	5.5	8.0	1.5	7.0	7.4	1.9
Tolerance	±0.2	±0.05	±0.1	min.	±0.1	±0.1	±0.1
SSOP16 (SOT338-1)	16.0	7.5	12.0	1.5	8.2	6.6	2.5
SSOP24 (SOT340-1)	16.0	7.5	12.0	1.5	8.2	8.8	2.5
SOT428	16.0	7.5	8.0	1.5	6.9	10.5	2.65
Tolerance	±0.3	±0.1	±0.1	min.	±0.1	±0.1	±0.1
SO24 (SOT137-1)	24.0	12.0	12.0	1.5	11.1	16.1	2.7

PACKAGE	SYMBOL						
	W (mm)	F (mm)	P (mm)	D_1 (mm)	A_0 (mm)	B_0 (mm)	K_0 (mm)
SOT404	24.0	12.0	16.0	1.5	10.6	16.7	4.9
SOT426	24.0	12.0	16.0	1.5	10.6	16.7	4.9
Tolerance	±0.5	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1

Table 4 Fixed tape dimensions

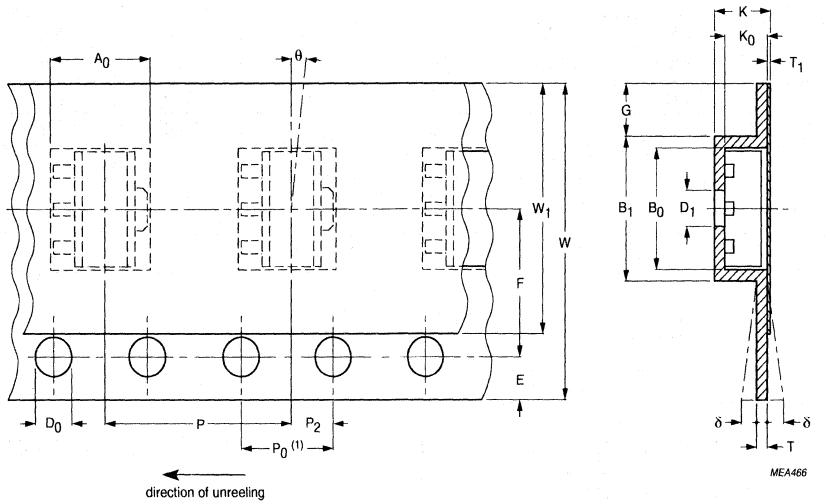
TAPE WIDTH	SYMBOL							
	E (mm)	D_0 (mm)	P_0 (mm)	P_2 (mm)	G (mm)	T (mm)	δ (mm)	θ (deg)
8 and 12 mm	1.75	1.5	4.0	2.0	0.75	0.4	0.3	15
Tolerance	±0.1	−0/+0.1	±0.1	±0.05	min.	max.	max.	max.
16 mm	1.75	1.5	4.0	2.0	0.75	0.4	0.3	10
Tolerance	±0.1	−0/+0.1	±0.1	±0.1	min.	max.	max.	max.
24 mm	1.75	1.5	4.0	2.0	0.75	0.4	0.3	10
Tolerance	±0.1	−0/+0.1	±0.1	±0.1	min.	max.	max.	max.



For dimensions see Tables 3 and 4.

(1) Tolerance over any 10 pitches is ±0.2 mm.

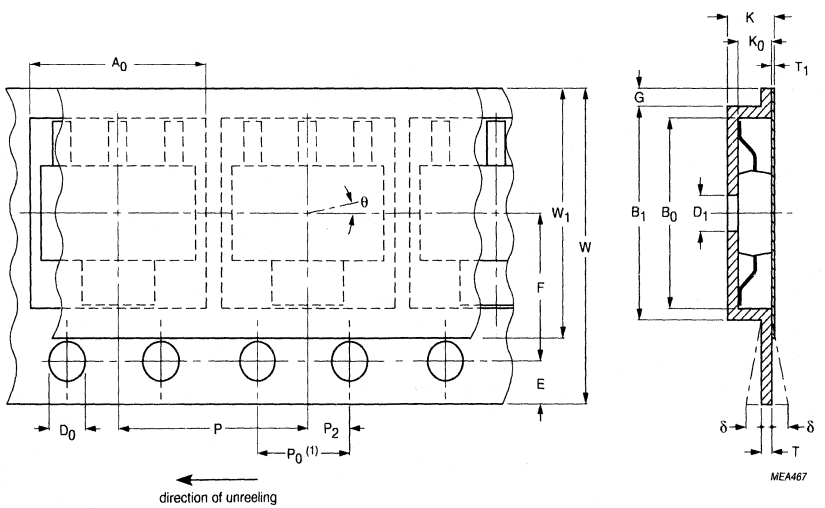
Fig.1 Specification for 8 mm tape (SC-70 (SOT323), SC-88 (SOT363) and SOT23).



For dimensions see Tables 3 and 4.

(1) Tolerance over any 10 pitches is 0.2 mm.

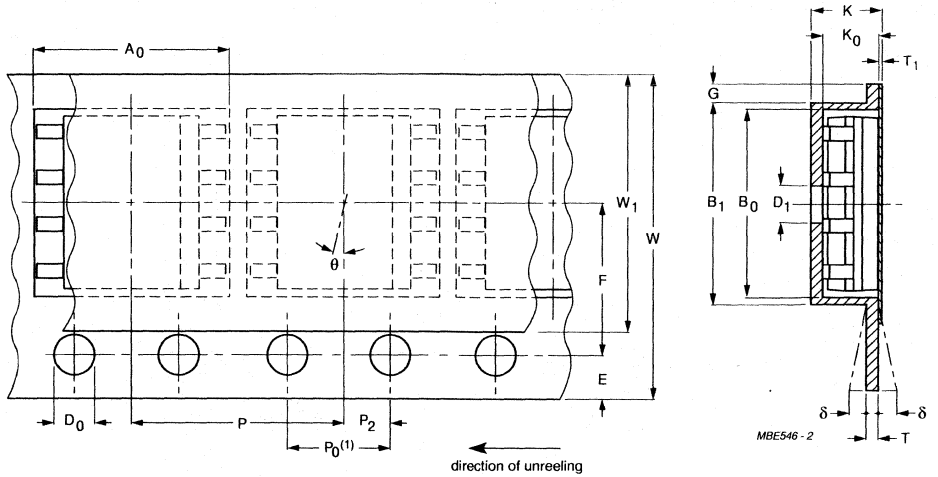
Fig.2 Specification for 12 mm tape (SOT89).



For dimensions see Tables 3 and 4.

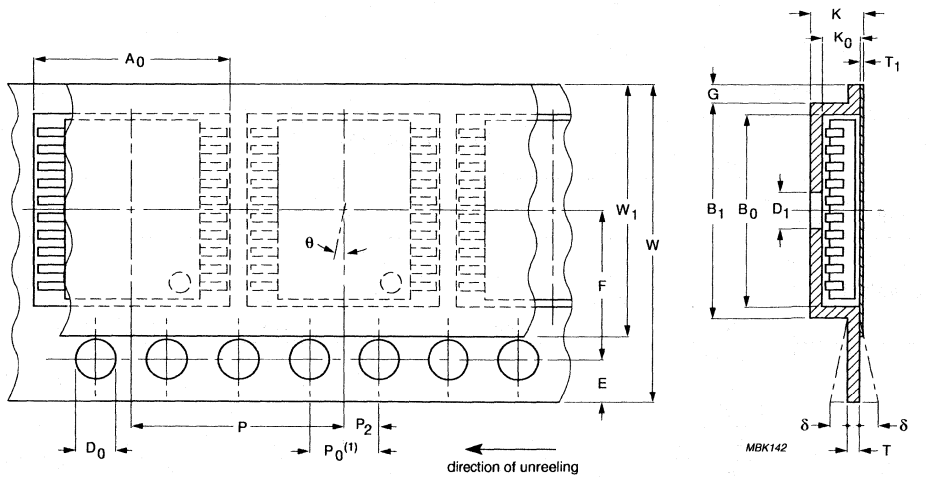
(1) Tolerance over any 10 pitches is 0.2 mm.

Fig.3 Specification for 12 mm tape (SOT223).



For dimensions see Tables 3 and 4.
(1) Tolerance over any 10 pitches is 0.2 mm.

Fig.4 Specification for 12 mm tape (SO8 (SOT96-1)).

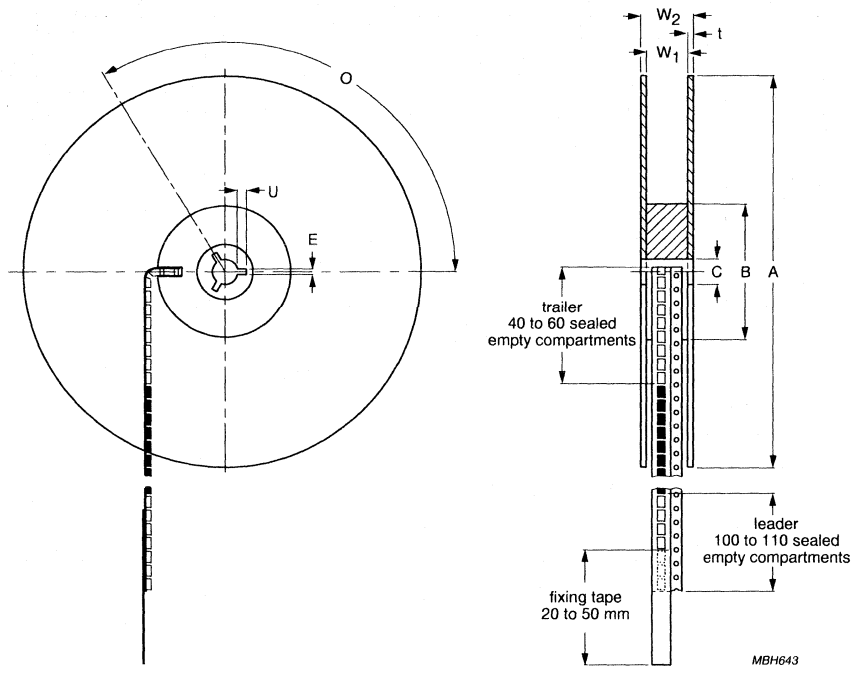


For dimensions see Tables 3 and 4.
(1) Tolerance over any 10 pitches is 0.2 mm.

Fig.5 Specification for 16 mm tape SSOP16 (SOT338-1) and SSOP24 (SOT340-1)).

Reel specification

Reel dimensions are specified in Fig.6 and Table 5 for 8, 12, 16 and 24 mm tape.



For dimensions see Table 5.

Fig.6 Reel specification.

Table 5 Reel dimensions

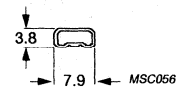
TAPE WIDTH	SYMBOL							
	A (mm)	**B (mm)**	**C (mm)**	**W_1 (mm)**	**W_2 (mm)**	**E (mm)**	**U (mm)**	**O (deg)**
8 mm	180/286 or 180/330	62	12.75	8.4	14.4	1.5	3.6	120
12 mm	180/330	62	12.75	12.4	18.4	1.5	3.6	120
16 mm	330	62	12.75	16.4	22.4	1.5	3.6	120
24 mm	180/330	62	12.75	24.4	30.4	1.5	3.6	120
Tolerance	±0.5	±1.5	−0/+0.15	−0/+1.5	max.	min.	min.	–

Tube specification

Devices in SO8 packages are also available in tubes. The tube dimensions are specified in Fig.7.

Packing quantities

Table 6 shows the packing quantities for a single box for each package style, and Table 7 shows the smallest packing quantity (SPQ) for a single tube and the packing quantity (PQ) for a single box for SO and SSOP packages.



Dimensions in mm; Tube length: 515 mm.

Fig.7 SO8 tube dimensions.

Table 6 Packing quantities by package with relevant ordering code ending

PACKAGE	PACKING QUANTITY	ORDERING CODE ENDING	KIND OF PACKING	REEL DIAMETER (mm/inch)
SC-70 (SOT323)	3000	115	8 mm tape and reel	180/7
	10000	135	8 mm tape and reel	286/11¼
SC-88 (SOT363)	3000	115	8 mm tape and reel	180/7
	10000	135	8 mm tape and reel	286/11¼
SOT23	3000	215	8 mm tape and reel	180/7
	10000	235	8 mm tape and reel	286/11¼
SOT89	1000	115	12 mm tape and reel	180/7
	4000	135	12 mm tape and reel	330/13
SOT223	1000	115	12 mm tape and reel	180/7
	4000	135	12 mm tape and reel	330/13
SO24 (SOT137-1)	500	115	24 mm tape and reel	180/7
	1000	118	24 mm tape and reel	330/13
SO8 (SOT96-1)	2500	118	8 mm tape and reel	330/13
SSOP16 (SOT338-1)	2000	118	16 mm tape and reel	330/13
SSOP24 (SOT340-1)	1000	118	16 mm tape and reel	330/13
SOT404	800	118	24 mm tape and reel	330/13
SOT426	800	118	24 mm tape and reel	330/13
SOT428	2500	118	16 mm tape and reel	330/13
TSOP6 (SOT457)	3000	115	8 mm tape and reel	180/7

Table 7 Packing quantities by package in tubes

PACKAGE	PACKING QUANTITY	ORDERING CODE ENDING	KIND OF PACKING
TO-220AB (SOT78)	50	–	520 mm tube (turn-lock)
	1000	127	20 tubes in a box
SO8 (SOT96-1)	100	–	515 mm tube (turn-lock)
	2000	112	20 tubes in a box
SOT186	50	–	520 mm tube (turn-lock)
	1000	127	20 tubes in a box

PACKAGE	PACKING QUANTITY	ORDERING CODE ENDING	KIND OF PACKING
SOT186A	50	–	520 mm tube (turn-lock)
	1000	127	20 tubes in a box
SOT226	50	–	520 mm tube (turn-lock)
	1000	127	20 tubes in a box
SOT263	50	–	413 mm tube (turn-lock)
	1000	127	20 tubes in a box
SOT263-01	50	–	413 mm tube (turn-lock)
	600	127	12 tubes in a box
SOT429	25	–	413 mm tube (turn-lock)
	500	127	20 tubes in a box

LEADED DEVICES

Tape and reel packing of TO-92 devices

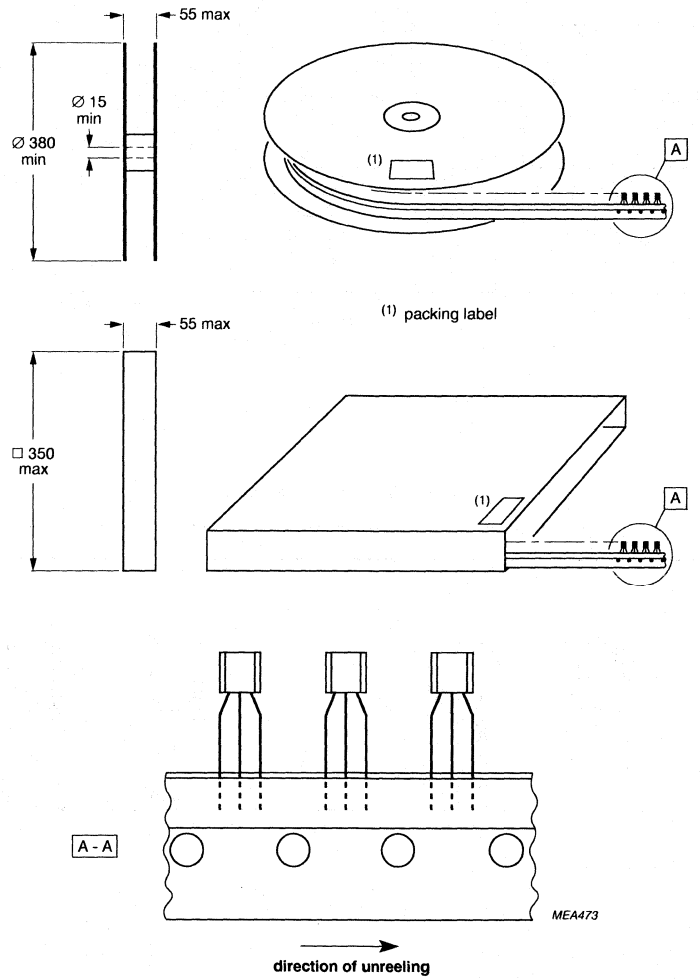
Tape and reel packing meets the feed requirements of automatic pick and place equipment (packing conforms to IEC publication 286-2 and 286-3). Additionally, the tape is an ideal shipping container.
The transistors are supplied on tape in boxes (ammopack) or on reels. The number per reel and per ammopack is 2000. The ammopack has 80 layers of 25 transistors each. Each layer contains 25 transistors, plus one empty position in order to fold the layer correctly.The ammopack is accessible from both sides, enabling the user to choose between 'normal' (see Fig.8) and 'reverse' tape. 'Normal' is indicated by a plus sign (+) on the ammopack and 'reverse' by a minus sign (–). In the European version, the leading pin is the source.

DROPOUTS

A maximum of 0.5% of the specified number of transistors in each packing may be missing. Up to 3 consecutive components may be missing provided the gap is followed by 6 consecutive components.

TAPE SPLICING

Splice the carrier tape on the back and/or front so that the feed hole pitch (P_0) is maintained (see Figs 9 and 10).



Dimensions in mm.

Fig.8 Dimensions of reel and box.

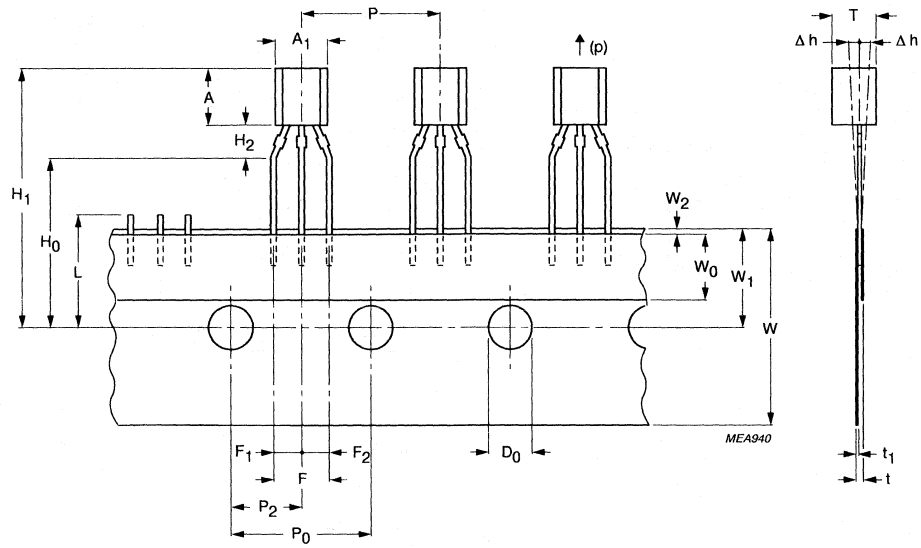


Fig.9 TO-92 transistors on tape.

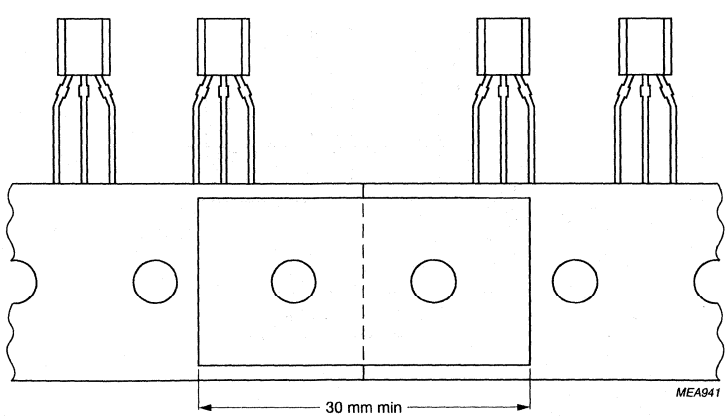


Fig.10 Joining tape with splicing patch.

Table 8 Tape specification (TO-92 leaded types)

SYMBOL	DIMENSION	SPECIFICATIONS					REMARKS
		MIN.	NOM.	MAX.	TOL.	UNIT	
A_1	body width	4	–	4.8	–	mm	
A	body height	4.8	–	5.2	–	mm	
T	body thickness	3.5	–	3.9	–	mm	
P	pitch of component	–	12.7	–	±1	mm	
P_0	feed hole pitch	–	12.7	–	±0.3	mm	
	cumulative pitch error	–	–	–	±0.1		note 1
P_2	feed hole centre to component centre	–	6.35	–	±0.4	mm	to be measured at bottom of clinch
F	distance between outer leads	–	5.08	–	+0.6/–0.2	mm	
Δh	component alignment	–	0	1	–	mm	at top of body
W	tape width	–	18	–	±0.5	mm	
W_0	hold-down tape width	–	6	–	±0.2	mm	
W_1	hole position	–	9	–	+0.7/–0.5	mm	
W_2	hold-down tape position	–	0.5	–	±0.2	mm	
H_0	lead wire clinch height	–	16.5	–	±0.5	mm	
H_1	component height	–	–	23.25	–	mm	
L	length of snipped leads	–	–	11	–	mm	
D_0	feed hole diameter	–	4	–	±0.2	mm	
t	total tape thickness	–	–	1.2	–	mm	t_1 = 0.3 to 0.6
F_1, F_2	lead-to-lead distance	–	–	–	+0.4/–0.2	mm	
H_2	clinch height	–	–	–	–	mm	
(p)	pull-out force	6	–	–	–	N	

Note

1. Measured over 20 devices.

Bulk packing of TO-92 devices

In addition to TO-92 on tape, TO-92 can also be delivered in bulk. Products are packed in boxes and plastic bags with 1000 pieces to a bag and 5 bags to a box.

As well as the standard TO-92 with straight leads, leads with delta pinning are available in bulk on request (see package outline chapter).

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Data handbook system

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Printed in USA

135107/26M/04/pp1944

Date of release: November 1998

Document order number: 9397 750 03246